### CRV FEB FPGA Register Map (word addresses)

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There are four FPGAs on the FEB. The address space for each FPGA is offset by 0x400 from its neighbor. The region 0x300 to 0x3FF broadcasts to all FPFAs simultaneously.

0x000..0x2FF – FPGA1. CMB Inputs 1..4 *connected to HDMI inputs* 1..4

0x400..0x6FF – FPGA2. CMB Inputs 1..4 *connected to HDMI inputs* 5..8

0x800..0xAFF – FPGA3. CMB Inputs 1..4 *connected to HDMI inputs* 9..12

0xC00..0xEFF – FPGA4. CMB Inputs 1..4 *connected to HDMI inputs13*..16

### **0x022: Read/Write test Counter Bits 31...16**

A write to this address defines the upper 16 bits of the 32 bit test counter.   
A read returns the present value of the upper bits.

### **0x023: Read/Write test Counter Bits 15...0**

A write to this address defines the lower 16 bits of the 32 bit test counter.   
A read from this address displays the value of the lower bits and increments all 32 bits of the counter after the read.