### CRV FEB FPGA Register Map (word addresses)

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There are four FPGAs on the FEB (part number xc7s50fgga484-2). The address space for each FPGA is offset by 0x400 from its neighbor. The region 0x300 to 0x3FF broadcasts to all FPFAs simultaneously.

0x000..0x2FF – FPGA1. CMB Inputs 1..4 *connected to HDMI inputs* 1..4

0x400..0x6FF – FPGA2. CMB Inputs 1..4 *connected to HDMI inputs* 5..8

0x800..0xAFF – FPGA3. CMB Inputs 1..4 *connected to HDMI inputs* 9..12

0xC00..0xEFF – FPGA4. CMB Inputs 1..4 *connected to HDMI inputs13*..16

### **0x000: Control and status register**

Bit 0: Power Down AFE 0. 0: Run. 1: Power down.

Bit 1: Power Down AFE 1. 0: Run. 1: Power down.

Bit 2: Issue a reset to the AFE deserializer logic in the FPGA

Bit 3: Issue a MIG DDR interface reset

Bit 4: Reset readout sequencer 1: Reset, 0: No action

Bit 5: Issue a general reset. The AFE FIFOs, Trigger counter, Spill counter and Readout sequencer are reset.

Bit 6: Reset the serial controller in the AFE chips.

Bit 7: Clear FM receive parity error.

Bit8: Trigger pedestal averager

Bits15:9: Not presently defined.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 15..9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Not Used | Start Ped averager | Clear FM Rx Parity Error | AFE Reset | General Reset | Force MIG DDR Write Command | Reset MIG DDR Interface | Reset AFE de-serializers | AFE 1 Power Down | AFE 0 Power Down |

### **0x00A: LVDS Transmit FIFO**

A write to this location will send a 16 bit FM word on the LVDS FEB to controller link.

### **0x00B: LVDS Transmit FIFO Empty Flag**

A read of this address will return the state of the transmit FIFO empty flag on bit 0.

**0x020: I/V ADC Input Multiplexer control register**

Selects which of 16 DAC trim resistors is connected to the lower level 16:1multiplexer. Set Mux enable to 0 before taking SiPM pulsed data. The top level 4:1 mux is controlled by the microprocessor. That mux has no disconnect option. The command Mux n where n is 0..3 chooses which lower level mux is connected to the PGA and 24 bit ADC. The microprocessor command A0 n will display n conversions of the 24 bit ADC.

|  |  |  |
| --- | --- | --- |
| 15..5 | 4 | 3..0 |
| Not Used | Mux Enable | Channel Select |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **REGISTER 0x020** | | | | | |  |  |  |
| **BIT 15…5** | **4** | **3** | **2** | **1** | **0** |  | **HEX** |  |
| Not Used | 0 | X | X | X | X |  | 0x0 | All multiplexers are disabled |
| Not Used | 1 | 0 | 0 | 0 | 0 |  | 0x10 | First mux enabled: A0 H, A1 H |
| Not Used | 1 | 0 | 0 | 0 | 1 |  | 0x11 | First mux enabled: A0 L, A1 L |
| Not Used | 1 | 0 | 0 | 1 | 0 |  | 0x12 | First mux enabled: A0 L, A1 H |
| Not Used | 1 | 0 | 0 | 1 | 1 |  | 0x13 | First mux enabled: A0 L, A1 H |
| Not Used | 1 | 0 | 1 | 0 | 0 |  | 0x14 | Second mux enabled: A0 H, A1 H |
| Not Used | 1 | 0 | 1 | 0 | 1 |  | 0x15 | Second mux enabled: A0 L, A1 L |
| Not Used | 1 | 0 | 1 | 1 | 0 |  | 0x16 | Second mux enabled: A0 L, A1 H |
| Not Used | 1 | 0 | 1 | 1 | 1 |  | 0x17 | Second mux enabled: A0 L, A1 H |
| Not Used | 1 | 1 | 0 | 0 | 0 |  | 0x18 | Third mux enabled: A0 H, A1 H |
| Not Used | 1 | 1 | 0 | 0 | 1 |  | 0x19 | Third mux enabled: A0 L, A1 L |
| Not Used | 1 | 1 | 0 | 1 | 0 |  | 0x1A | Third mux enabled: A0 L, A1 H |
| Not Used | 1 | 1 | 0 | 1 | 1 |  | 0x1B | Third mux enabled: A0 L, A1 H |
| Not Used | 1 | 1 | 1 | 0 | 0 |  | 0x1C | Fourth mux enabled: A0 H, A1 H |
| Not Used | 1 | 1 | 1 | 0 | 1 |  | 0x1D | Fourth mux enabled: A0 L, A1 L |
| Not Used | 1 | 1 | 1 | 1 | 0 |  | 0x1E | Fourth mux enabled: A0 L, A1 H |
| Not Used | 1 | 1 | 1 | 1 | 1 |  | 0x1F | Fourth mux enabled: A0 L, A1 H |

**0x021: Channel Mask Register**

A 16 bit register to select which channels to read out. Bits 0..15 enable channels 0..15

### **0x022: Read/Write test Counter Bits 31...16**

A write to this address defines the upper 16 bits of the 32 bit test counter.   
A read returns the present value of the upper bits.

### **0x023: Read/Write test Counter Bits 15...0**

A write to this address defines the lower 16 bits of the 32 bit test counter.   
A read to this address displays the value of the lower bits and increments all 32 bits of the counter after the read.

### **0x024: One wire command register**

Bits 0..7: If an individual write transaction is requested, the lower eight bits of this register are sent to the one wire interface.

Bit 8: Start the read temperature sequencer. A complete read temperature sequence will execute when this bit is set. The read value of this bit will return a 0 until the sequence is complete.

Bit 9: Start the read ROM sequencer. A complete ROM read sequence will execute when this bit is set. The read value of this bit will return a 0 until the sequence is complete.

|  |  |  |  |
| --- | --- | --- | --- |
| 15..10 | 9 | 8 | 7..0 |
| Not Used | Read ROM | Read Temperature | Command Byte |

### **0x025: One wire control register**

Bit 0..3: Selects which CMB read data is stored in the register file

Bit 4: Request a write transaction

Bit 5: Request a read transaction

Bit 6: Request a reset transaction

Bit 7: Transaction status. Returns a ‘1’ when transaction is in progress

Bit 15..8: Transaction bitcount (N-1). For a write set to seven. For a 72 bit read set to 71.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 15..8 | 7 | 6 | 5 | 4 | 3..0 |
| Transaction bit count | Busy | Rst | Read | Write | CMB Sel |

**0x026..0x2A: One wire returned data register file**

The contents depend on the specifics of the one wire transaction

**0x030..0x3F: Bias trim DAC voltage setting**

There are 16 12 bit DACs with a span of ±4.096V. The coding is offset binary, 0x000 is -4.096V, 0xFFF is +4.096V.

**0x040..0x43: LED flasher intensity DACs**

Four 12 bit DACs with a span of 0..14V. The coding is straight binary, 0x000 is 0V and 0xFFF is 14V. Addresses 0x40..0x43 Apply to CMB 1..4.

**0x044..0x45: Bias bus DACs**

Two 12 bits DACs with a possible span of 0..80V. The coding is straight binary, 0x000 is 0V, 0xFFF corresponds to 80V. Address 0x44 applies to CMB1..2, Address 0x45 applies to CMB 3..4. The maximum voltage is in fact set by the bias generator jumper setting on the board. At the highest position the maximum bias voltage is about 76V.

**0x046..0x47: AFE VGA DACs**

Two 12 bits DACs with a span of 0..1.54V. The coding is straight binary, 0x000 is 0V, 0xFFF is 1.54V. Address 0x46 applies to AFE 1, Address 0x47 applies to AFE 2.

**0x048..0x5F: DAC setup registers**

These normally don’t require modifying. For details see the AD5328 data sheet

**0x064: uBunch High**

Read the uBunch high value.

**0x065: uBunch Low**

Read the uBunch low value.

### **0x06C: Uptime Counter bits 31...16**

### **0x06D: Uptime Counter bits 15...0**

A counter showing the number of seconds since the last FPGA reset

### **0x080..0x8F: Pedestal registers**

These define the pedestal subtracted from the ADC values before the trigger threshold is applied. These values are also subtracted from the ADC values before being histogrammed.

### **0x090..0x9F: Threshold registers**

These define the threshold.

### **0x0FF: AFE setup data read register**

### Data returned from an AFE in response to a read request is stored here.

### **0x100..0x13B: AFE 1 register file**

### This space is mapped onto to the AFE5807 register map.

### **0x200..0x23B: AFE 2 register file**

### **Broadcast Addresses**

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A write to these addresses will set the corresponding registers in all four FPGAs at once. Reads are still individual to each FPGA. This is a way of checking that the broadcast did actually occur.

### **0x300: Flash gate control register**

Bit 0: Enable the flash gate

Bit 1: Select the CMB pulse routing. 1: Flash Gate, 0: LED flasher.

Bit 2: LED Flasher signal source. 0: Test pulser, 1: DCO frequency.

|  |  |  |  |
| --- | --- | --- | --- |
| 15..3 | 2 | 1 | 0 |
| Not Used | LED Source | CMB Pulse Select | Flash Gate Enable |

### **0x301: Flash Gate Turn on time**

A write to this address defines the time in the microbunch in steps of 6.28ns that the flash gate is asserted, that is when the SiPM voltage is lowered. The microbunch duration is 270 steps.

### **0x302: Flash Gate Turn off time**

A write to this address defines the time in the microbunch in steps of 6.28ns that the flash gate is de-asserted, that is when the SiPM voltage is raised.

**0x303: Trigger Control Register**

Bit 1: Selects the trigger input type as a pulse or an FM data stream

The assumption is that a trigger pulse comes from the LEMO connector, the FM encoded trigger message comes from the RJ-45 connector. The microprocessor controls the multiplexer that routes either the LEMO or the RJ-45 signal to the trigger input on the FPGAs.

**0x304: Read/Write Hit Pipeline Delay Register**

Specifies the number of pipeline stages the hit data traverses before being presented to the first level FIFO. This is used to compensate for trigger delays. The least count is 12.56 ns and the span is eight bits. The minimum delay setting is one and increases monotonically up to a setting of 255. A setting of zero corresponds to a delay of 256 or 3.22μs.

**0x305: Read/Write Beam On Sample length register**

Specifies the number ADC samples per microbunch

**0x306: Read/Write Beam Off Sample length register**

Specifies the number ADC samples per bunch marker

**0x30C: Read/Write ADC samples per hit**

A four bit value that speSpecifies the number ADC samples per microbunch

### **0x30E: Self Trigger Control Register**

A write to this address can select between two types of self trigger.

Bit 0: Self trigger qualified by an external trigger and the spill gate. If a hit occurs during the gate interval, the data is recorded, otherwise no data is written.

Bit 1: Self trigger qualified by the spill gate.

### **0x316: Broadcast write the four CSR registers**

A write to this address is equivalent to writing to 0x000,0x400,0x800,0xC00 simultaneously.

### **0x318: LED Time**