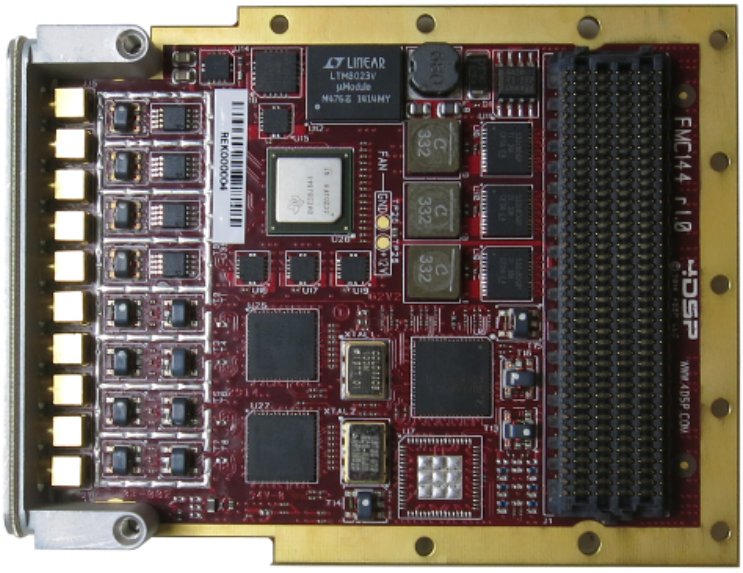
FMC144/FMC142/FMC140 User Manual



Abaco Systems, USA

Support Portal

Revision History

Date	Revision	Revision
2014-10-22	Release	r1.0
2014-11-21	Corrected clock and external trigger input labels in block diagram	r1.1
2015-01-21	Updated information for FMC142 and FMC140.	r1.2
2015-03-11	Added chapter Usage on an FMC site with only 4 high speed Lanes	r1.3
2015-10-06	Added Appendix B: Errata	r1.4

Table of Contents

1 Acronyms and related documents

1.1 Acronyms

ADC	Analog-to-Digital Converter
DDR	Double Data Rate
DDS	Direct Digital Synthesis
DSP	Digital Signal Processing
EEPROM	Electrically Erasable Programmable ROM
FBGA	Fineline Ball Grid Array
FMC	FPGA Mezzanine Card
FPGA	Field-Programmable Gate Array
JTAG	Join Test Action Group
LED	Light-Emitting Diode
LSB	Least Significant Bit(s)
LVDS	Low Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor Logic level
MGT	Multi-Gigabit Transceiver
MSB	Most Significant Bit(s)
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PLL	Phase-Locked Loop
PMC	PCI Mezzanine Card
PSRR	Power Supply Rejection Ratio
QDR	Quadruple Data rate
SDRAM	Synchronous Dynamic Random Access memory
SRAM	Synchronous Random Access memory
TTL	Transistor Logic level
XMC	PCIe Mezzanine card

Table 1: Glossary

1.2 Related Documents

- FPGA Mezzanine Card (FMC) standard ANSI/VITA 57.1-2010
- Datasheet ADC16DX370, TI - Analog-to-Digital Converter
- Datasheet DAC38J84, TI - Digital-to-Analog Converter
- Datasheet LMK048xB, TI - PLL and Clock Generator

2 General description

The FMC144 is an eight-channel ADC/DAC FMC daughter card. It provides four 16-bit A/D channels and four 16-bit D/A channels which can be clocked by an internal clock source (optionally locked to an external reference) or an externally-supplied sample clock. In addition, there is one trigger input for customized sampling control. The FMC144 daughter card is mechanically and electrically compliant to FMC standard (ANSI/VITA 57.1-2010).

The FMC142 offers half of the channels: two A/D and two D/A channels. The FMC140 has four A/D channels and no D/A channels. Also refer to Table 2: Ordering Information for the different configuration options.

The FMC14X can be configured as a stackable module with high-pin count connectors on both the top and bottom sides. The factory default configuration is as a regular non-stackable FMC module with a high-pin count connector on the bottom side of the card. The FMC14X also has front panel I/O and can be used in a conduction-cooled environment.

The design is based on TI's ADC16DX370 dual-channel 16-bit 370Msps ADC and TI's DAC38J84 quad-channel 16-bit 2.5Gsps DAC. The analog signal inputs are either AC- or DC-coupled and connected to MMCX/SSMC coax connectors on the front panel.

The FMC14X allows flexible control of sampling frequency and offset correction through serial communication busses. The card is also equipped with power supply and temperature monitoring and offers several power-down modes to switch off unused functions.

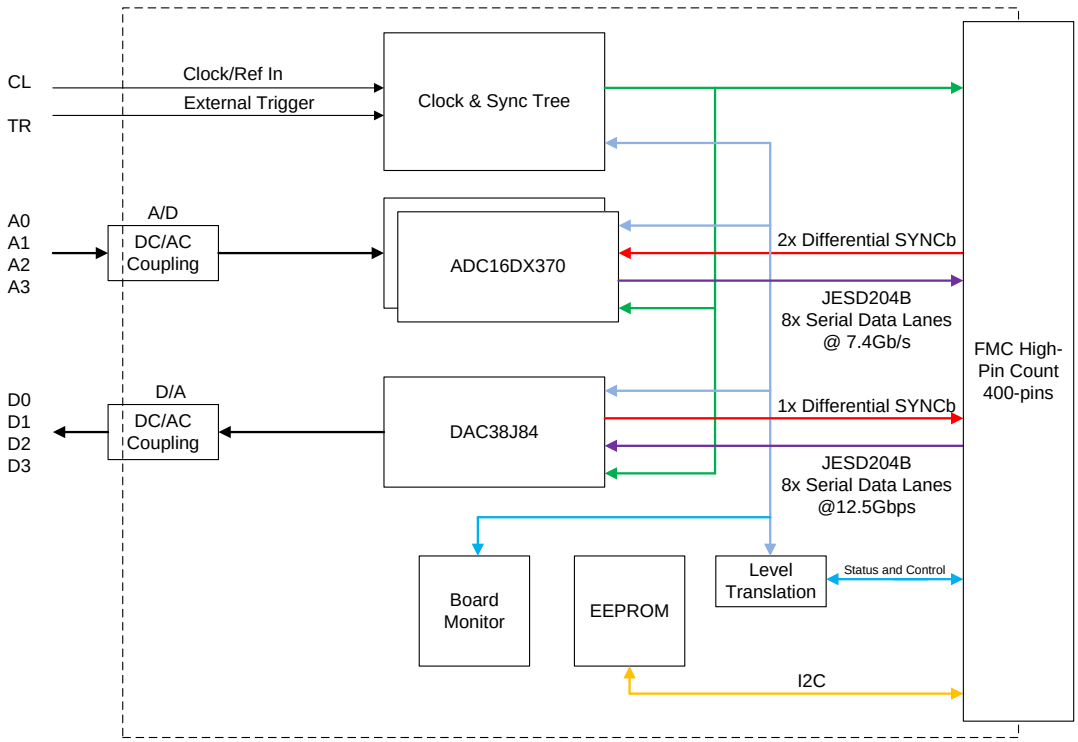


Figure 1: FMC144 block diagram

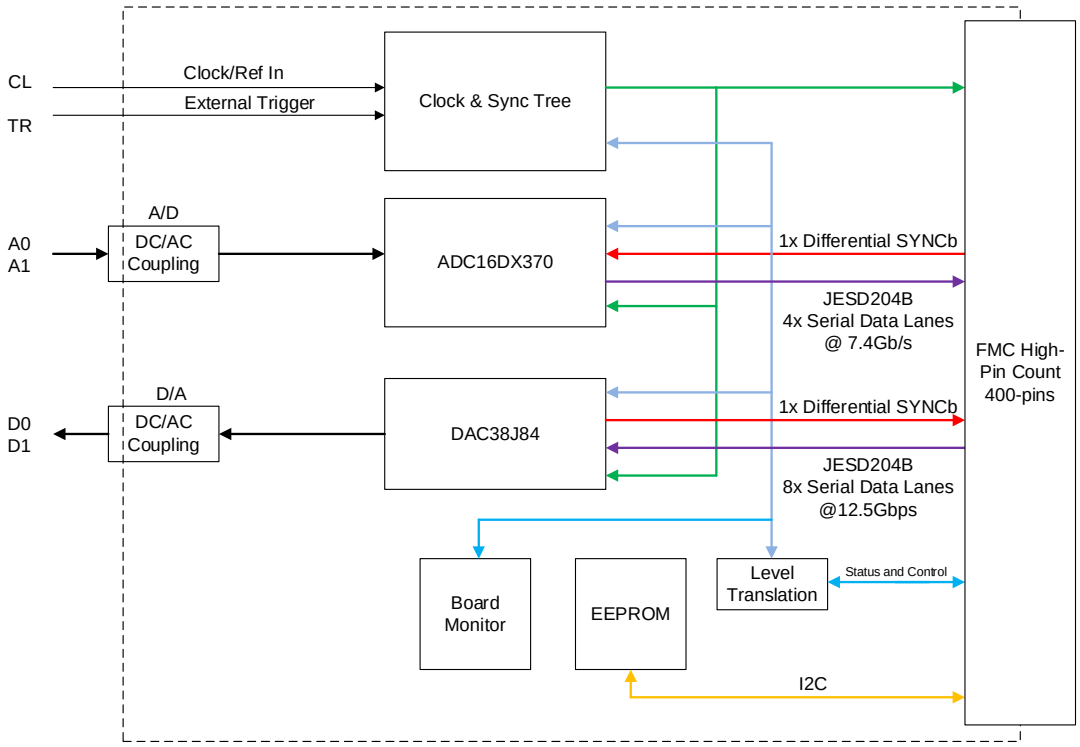


Figure 2: FMC142 block diagram

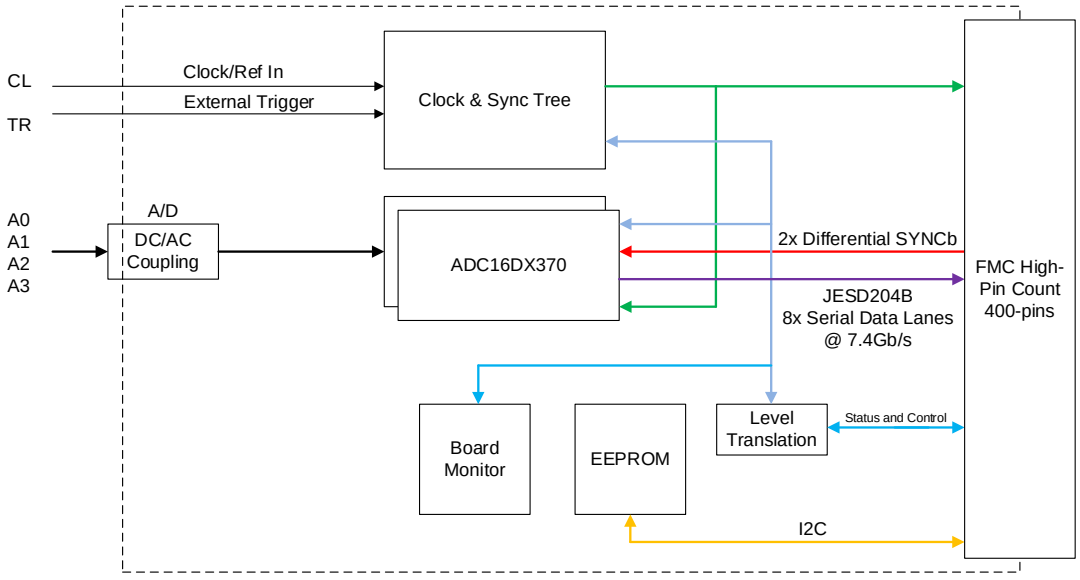


Figure 3: FMC140 block diagram

2.1 Ordering Information

The design defines different build options resulting in different part numbers. AC- or DC-coupling is a part number option.

Card Type	Connector	# ADC Channels	# DAC Channels
FMC144	HPC	4	4
FMC142	HPC	2	2
FMC140	HPC	4	0

Table 2: Ordering Information

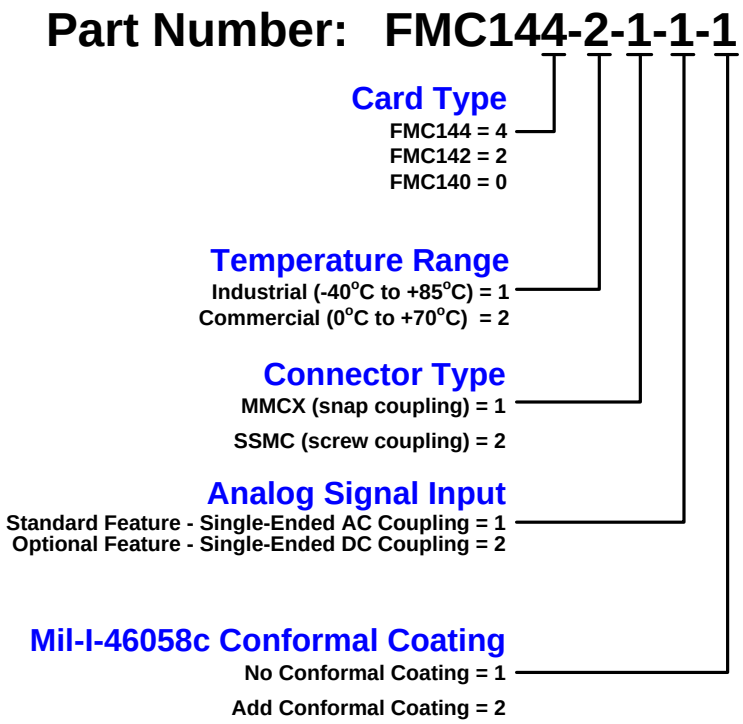


Figure 4: Ordering Information

2.2 Installation and handling instructions

- Prevent electrostatic discharges by observing ESD precautions when handling the card.
- Do not flex the card and do not exceed the maximum torque specification on the coax connectors.
- The FMC14X daughter card must be installed on a carrier card compliant to the FMC standard.
- The carrier card must support the high-pin count connector (400-pins).
- The carrier card can support a VADJ/VIO_B voltage range of 1.65V to 3.3V, but typically VADJ will be 1.8V or 2.5V for LVDS operation.

3 Design

3.1 Physical specifications

3.1.1 Board Dimensions

The FMC14X card complies with the FMC standard known as ANSI/VITA 57.1. The card is a single-width, conduction-cooled mezzanine module (with region 1 and front panel I/O). The front area holds 10 MMCX or 10 SSMC connectors. The stacking height is 10mm.

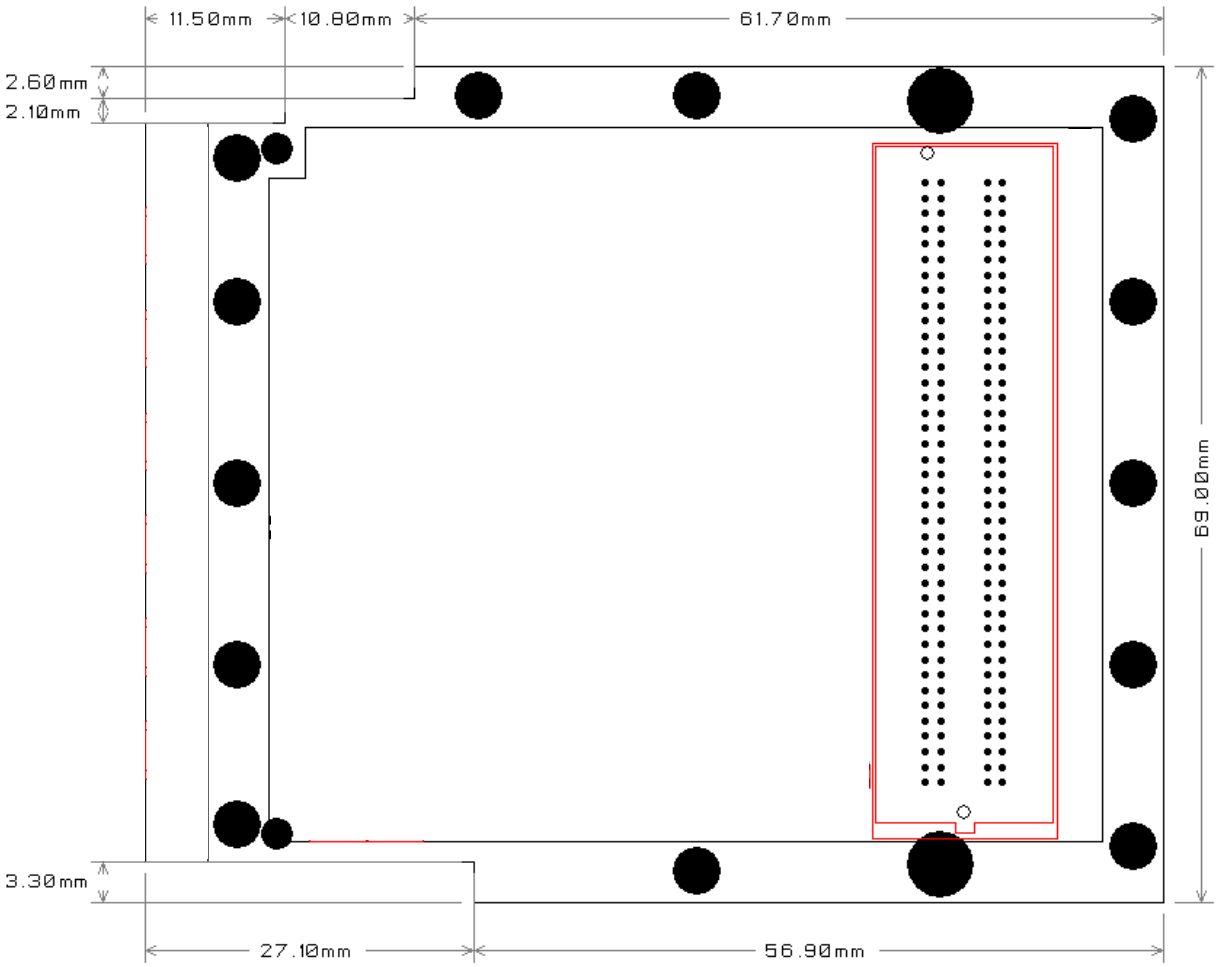


Figure 5 : FMC14X dimensions

3.1.2 Front panel

There are 10 SSMC/MMCX connectors available from the front panel. From top to bottom; analog in A3 to A0, clock in/out (CL), trigger in (TR), and analog out D0 toD3.

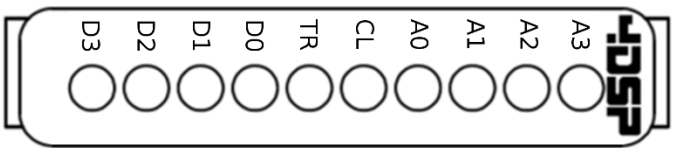


Figure 6: FMC144 Bezel design

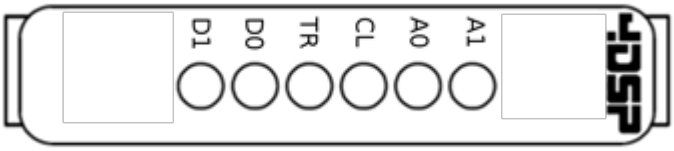


Figure 7: FMC142 Bezel design

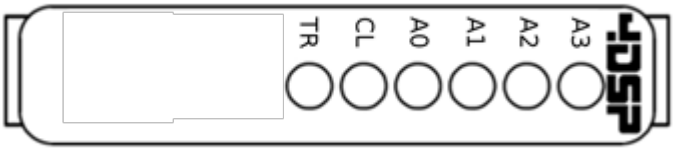


Figure 8: FMC140 Bezel design

3.2 Electrical specifications

The main ADC sample data is transferred using JESD204B subclass 1-coded differential pairs connected to the GBT pins on the FMC connector. There are two lanes available per ADC channel.

The DAC devices use JESD204B subclass 1-coded differential pairs connected to the GBT pins on the FMC connector to transfer sample data. There are two lanes available per DAC channel.

Control signals operate in LVCMOS mode. A VADJ range of 1.65V to 3.3V is supported. The voltage on the VIO_B pins will follow the voltage on VADJ.

The CLK0 and CLK1 pins are LVDS by the FMC standard. CLK0 is connected to a spare clock output of the clock tree. CLK1 is connected to a spare SYSREF output of the clock tree. CLK2 and CLK3 are not used.

3.2.1 EEPROM

The FMC14X card carries a 2kbit EEPROM (M24C02-WDW) which is accessible from the carrier card through the I^2C bus. The EEPROM is powered by 3P3VAUX. The standby current is only 0.01µA when SCL and SDA are kept at 3P3VAUX level. These signals may also be left floating since pull-up resistors are present on the FMC14X. The EEPROM is write-protected.

3.2.2 FMC Top Connector

The recommendations from AV57.1 Table 14 have been taken into account resulting in the following arrangement:

- The JESD204B ADC data pairs are mapped to DP[0..7]_M2C_[P/N].
- The JESD204B DAC data pairs are mapped to DP[0..7]_C2M_[P/N].
- The reference clocks for the gigabit lanes are mapped to GBTCLK[0..1]_M2C_[P/N].
- The reference clock for the FPGA logic is mapped to CLK0_M2C_[P/N].
- The sysref clock for the FPGA logic is mapped to CLK1_M2C_[P/N].
- Other signals are mapped to LA bank starting at index 0.

The high-pin count connector has four dedicated LVDS clock pairs and two gigabit reference clocks. It can host up to 80 LVDS (data) pairs and 20 gigabit (data) pairs. There are 10 carrier-to-module gigabit data pairs and 10 module-to-carrier gigabit data pairs. Refer to appendix A for a detailed control/status signal list.

	# Single-Ended	# LVDS Clock Pairs	# LVDS Data Pairs	# GBT Clock Pairs	# GBT Data Pairs C2M	# GBT Data Pairs M2C
CLK0 – **LVDS Clock**		1				
CLK1 – **LVDS Sysref**		1				
CLK2 **– N/C**						
CLK3 **– N/C**						
GBTCLK0 – **REF CLK**				1		
GBTCLK1 – **REF CLK**				1		
Trigger/Sync		2				
ADC0						
SA[0..1]						2
SB[0..1]						2
SYNCb			1			
OVR[A/B]	2					
ADC1						
SA[0..1]						2
SB[0..1]						2
SYNCb			1			
OVR[A/B]	2					
DAC0						
RX[0..7][P/N]					8	
SYNCB[P/N]			1			
Alarm	1					
Other	23					
# Total Pairs	28	4	3	2	8	8

Table 3: HPC Signal Utilization

3.2.1 Usage on an FMC site with only 4 high speed Lanes

It is possible to use the FMC144, FMC142 and FMC140 on an FMC site that only offers four high speed serial lanes. For the FMC142 and FMC1140 this does not affect the performance at all. On the FMC140 and FMC144 it does mean that the serial lanes to the ADC have to be operated at the double speed compared to the 8 lane solution.

For the FMC144 there is a performance impact on the DAC. The maximum bit rate per lane of the DAC38J84 is 12.5 Gbps. This implies that if only 4 transceiver lanes are available each of the four DACs can only receive 12.5/10 =1.25 bytes/sec (you need to divide by 10 because the 10b/8b encoding). With 2 bytes per sample the maximum sample rate of each DAC without interpolation is 625 MSPS. With interpolation the full rate of 2.5GSPS can be realized. More details on the working of the DAC device can be found in the DAC38J84 datasheet.

3.2.2 FMC Bottom Connector

The high-pin count connector enables FMC card stacking. The following connections are available between the top and bottom FMC connector:

- RES0
- 3P3VAUX, 3P3V, 12P0V, VADJ
- JTAG (see section 3.2.3)
- DP[8..9]_M2C[P/N]
- DP[8..9]_C2M[P/N]
- GBTCLK[1]_M2C_[P/N] (build option)
- Five LVDS signal LA bank

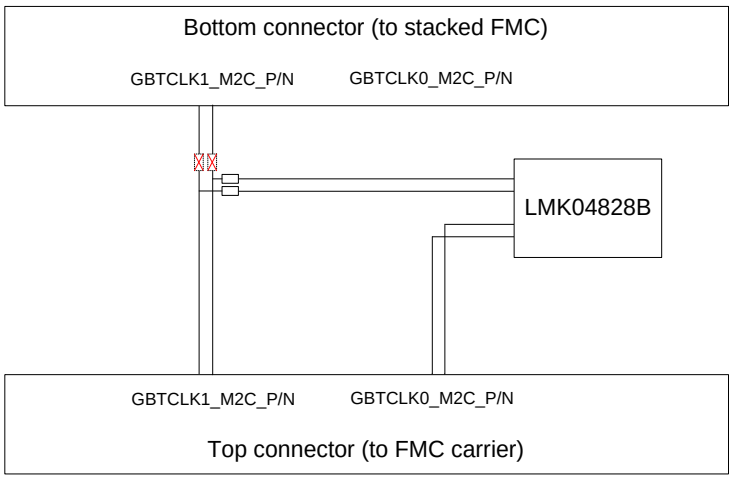


Figure 9: GBTCLK[1]_M2C_[P/N] build option

3.2.3 JTAG Chain

In a stacked environment, the TDI pin is decoupled from the TDO pin by the PRST_M2C_L signal coming from the bottom connector. TRST#, TCK, TMS, TDI, and TDO are directly connected between top to bottom connector on the FMC14X.

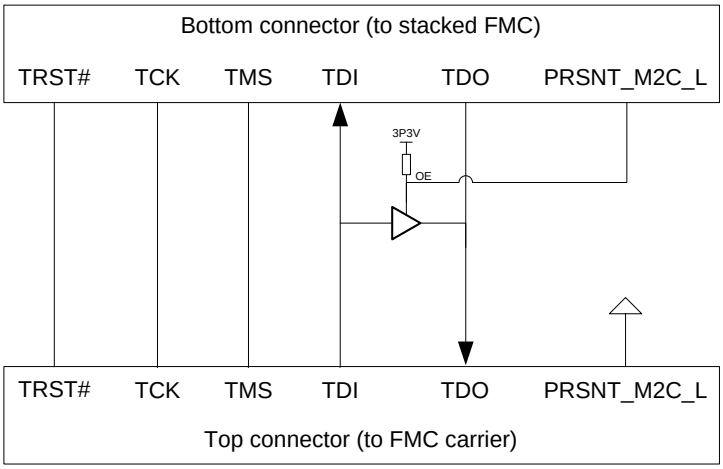


Figure 10: JTAG Connection

3.3 Main characteristics

Analog Inputs	
Number of channels	FMC144: 4 (A0-A3) FMC142: 2 (A0-A1) FMC140: 4 (A0-A3)
Channel resolution	16-bit
Input voltage range	1.7Vp-p (8.6 dBm)
Input impedance	50Ω (AC-coupled)
Analog input bandwidth	200kHz to 800MHz (AC-coupled version)
SNR	Max 68dBFS
SFDR	Max 80dBc
Analog Outputs	
Number of channels	FMC144: 4 (D0-D3) FMC142: 2 (D0-D1) FMC140: 0
Channel resolution	16-bit
Output voltage range	1Vpp in AC Coupling 1.7Vpp in DC Coupling
Output impedance	50Ω (AC-coupled)
Analog output bandwidth	3-800MHz (AC-coupled version)
SFDR	Max 75dBc
External Clock/Reference Input	
Input Level	0.35Vpp (-5dBm) to 4.5Vpp (17dBm)
Input impedance	50Ω (AC-coupled)
External Trigger input	
Format	LVTLL/LVCMOS Logic '0' → max 0.8V / Logic '1' → min 2.0V
Frequency range	Up to 185 MHz
ADC Output	
Data width	FMC144: JESD204B 8-pairs FMC142: JESD204B 4-pairs FMC140: JESD204B 8-pairs
Data Format	Offset binary or two's complement
Sampling Frequency Range	Up to 370MHz
DAC Input	
Data width	FMC144: JESD204B 8-pairs FMC142: JESD204B 8-pairs FMC140: N/A
Data Format	Offset binary or two's complement
Sampling Frequency Range	Up to 1.25GHz

Table 4 : FMC14X daughter card main characteristics

3.4 Analog input channels

3.4.1 AC Coupling

The AC-coupled input uses wideband RF baluns (TC1-1-13M). The input bandwidth is 4.5 to 800MHz. Two baluns are used to compensate for imbalance and reduce harmonic distortion. A capacitor in between the baluns blocks the DC path to ground which protects the signal source if a DC-coupled signal with offset is accidentally connected to the FMC14X.

The input impedance is matched to 50Ω behind the transformers by terminating each node to the common mode voltage of the ADC. The topology is shown in Figure 11.

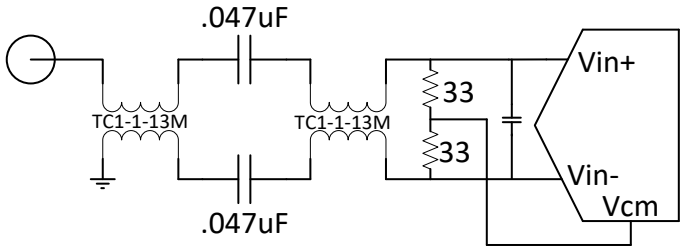


Figure 11 : AC-coupled input assembly

3.4.2 DC Coupling

The DC-coupled input utilizes the LMH6552 current feedback differential amplifier. The Op-amp is set up for a gain of two, yielding an overall gain of one in the conversion from single-ended to differential. Larger gain can be realized as a build option, reducing the bandwidth accordingly. Series 100 ohm resistors diminish the peaking caused by bond wire inductance and isolate the LMH6552 from the input capacitance of the ADC.

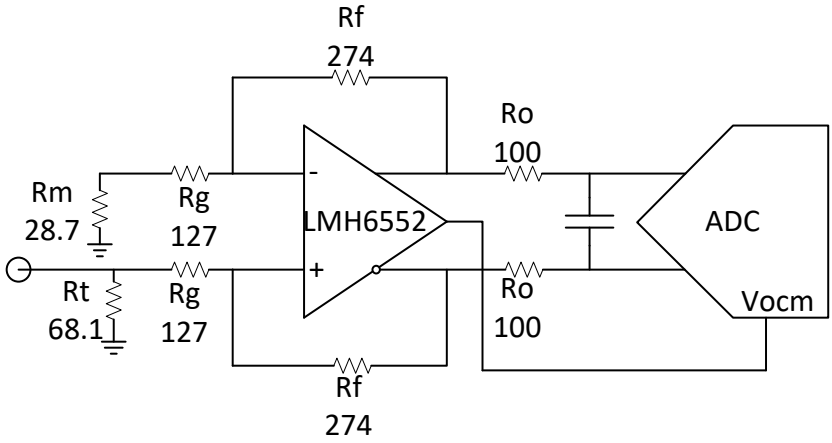


Figure 12 : DC-coupled input assembly

3.5 Analog output channels

3.5.1 AC Coupling

The AC-coupled output topology utilizes a transformer configuration. The bandwidth of the default transformer is 3 to 800MHz. The transformer has a 4:1 impedance ratio. Applying a 20mA full-scale output current leads to a 1Vpp output. The low DC impedance between IOUTP or IOUTN and the transformer center tap sets the center of the AC signal to ground, so the 1Vpp output for the 4:1 transformer results in an output between -0.5V and +0.5V. The transformer must be of this configuration to allow current flow through the center tap. Available options for the transformer are as follows (contact Abaco):

Manufacturer P/N	Manufacturer	Impedance Ratio	Bandwidth
TC1-1TG2+	Mini-circuits	1	.4 to 500MHz
TC1.5-52TG2+	Mini-circuits	1.5	0.5 to 550MHz
TC2-1TG2+	Mini-circuits	2	3 to 300MHz
TC3-1TG2+	Mini-circuits	3	5 to 300MHz
TC4-1WG2+	Mini-circuits	4	3 to 800MHz
TC4-6TG2+	Mini-circuits	4	1.5 to 600MHz
TC4-14G2+	Mini-circuits	4	200 to 1400MHz
TC8-1G2+	Mini-circuits	8	2 to 500MHz

Table 5 : Pin Compatible Transformers

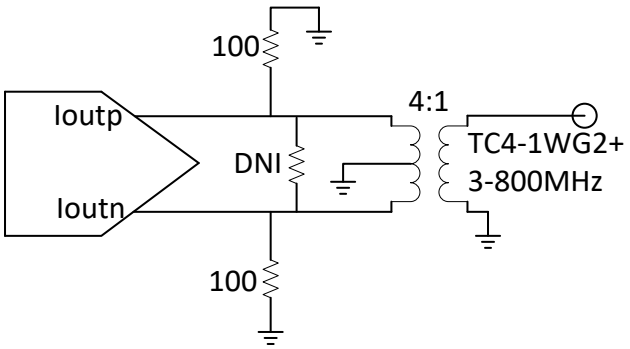


Figure 13 : AC-coupled output assembly

3.5.2 DC Coupling

The DC-coupled output uses the THS3201 current feedback operational amplifier for the current-to-voltage conversion.

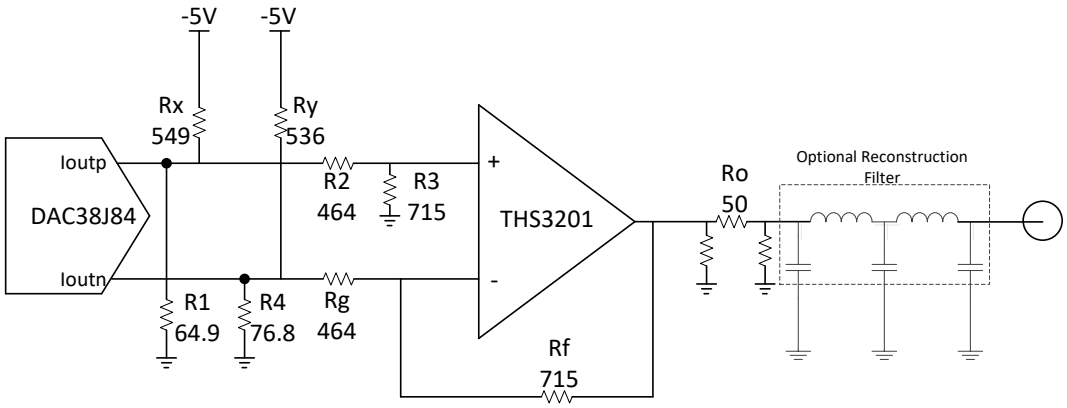


Figure 14 : DC-coupled output assembly

The values listed in Figure 14 were chosen to allow each side of the DAC current output to swing close to the positive limits of the compliance voltage. The DAC compliance voltage range is -0.5V to 0.6V. With the values chosen, each side of the DAC output swings approximately from -0.5V to 0.6V. This gives an output voltage of approximately 1.7Vpp.

3.6 External trigger/synchronization input

The external trigger input can be configured in different ways through build options. The trigger input can be 50Ω terminated, accepting most common high-speed signaling standards like single-ended LVPECL. By default, the 50Ω termination is not mounted in order to support LVTTL/LVCMOS and similar input standards. The input is single-ended and DC-coupled by default, with an input impedance of approximately 2.5kΩ. A resistor divider on the inverted input determines the threshold. The input threshold is approximately 1.25V. One output is routed to the FMC connector the other output to the synchronization circuit.

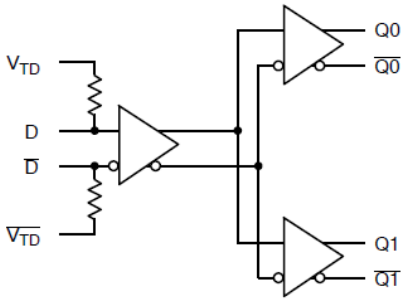


Figure 15: Level translation AnyLevel to LVDS

The trigger input can be used as a sync input to synchronize local converters or multiple cards. See section 3.7.

3.7 Multi-channel synchronization

Since the converters are subclass 1 JESD204B devices, they support synchronization across the channels. Frame and LMFC clocks are generated inside the devices and are used to properly align the phase of the serial data. The phases of the frame and multi-frame clocks are determined by the frame alignment step for JESD204B link initialization. Frame alignment takes place on the rising edge of the SYSREF signal. The LMK04828B is used to generate

device clocks and SYSREF signals, while also guaranteeing proper setup and hold time between them.

The external trigger input can also be utilized to generate synchronous SYSREF events across multiple FMC144 boards. The synchronization pulse is additionally routed to the FPGA.

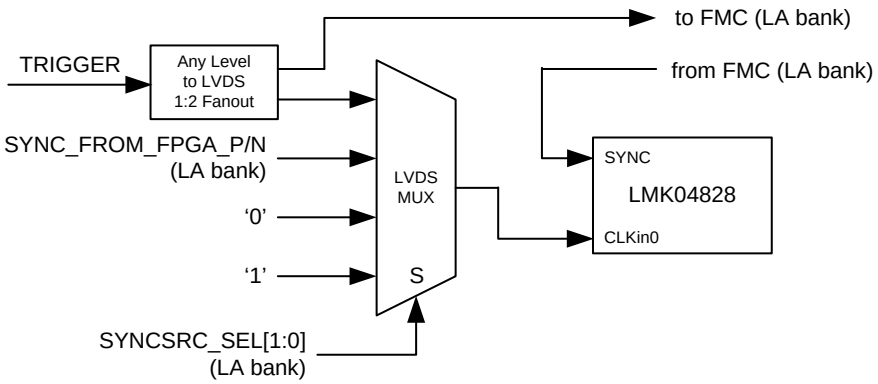


Figure 16: Synchronization topology

For synchronization to work across multiple cards, the cards must be supplied with synchronized clock or reference signals. An external synchronization signal is also required. Match the cable length between the clock/sync generator and each FMC14X. The clock generator must be able to tune the phase relationship between the clock and sync signal to satisfy the setup/hold timing requirements.

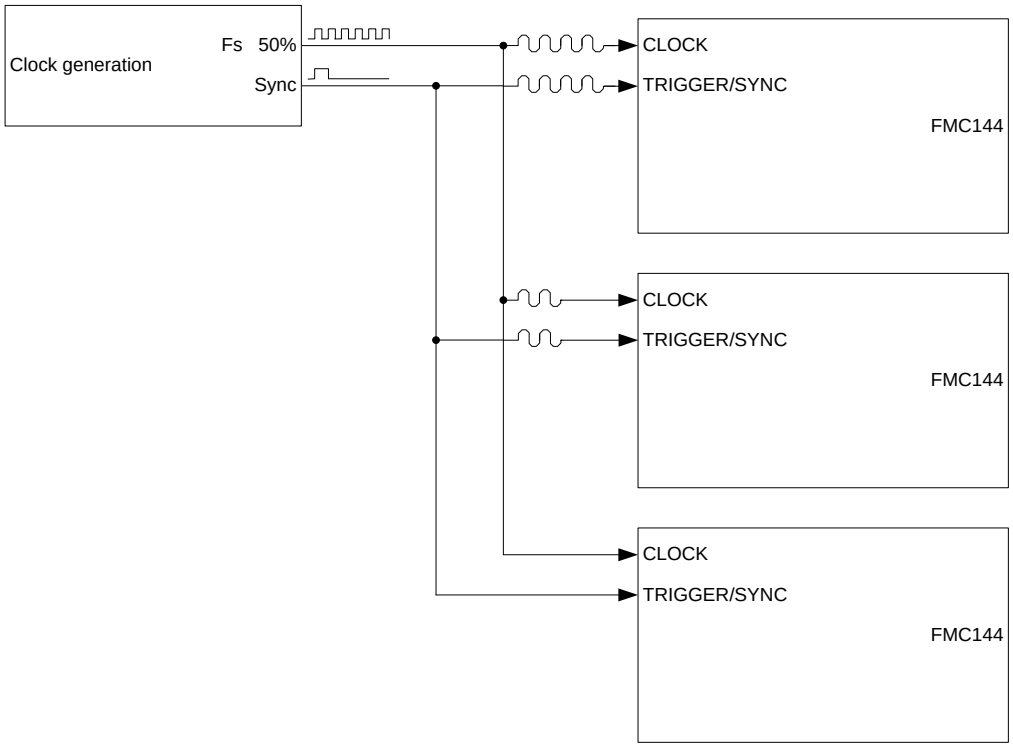


Figure 17 : Synchronizing Multiple Cards

3.8 Clock tree

3.8.1 External clock input

There is one clock input on the front panel that can serve as a sampling clock input or as a reference clock input if the internal clock is desired. There is a build option for clock output.

Note: When internal clock is enabled and there is no need for an external reference, it is highly recommended to leave the external clock input unconnected to prevent interference with the internal clock.

3.8.2 Architecture

The clock architecture of the FMC14X combines flexibility and high performance. Components have been chosen to minimize jitter and phase noise and improve the data conversion performance. The user may choose either an external or internal sampling clock.

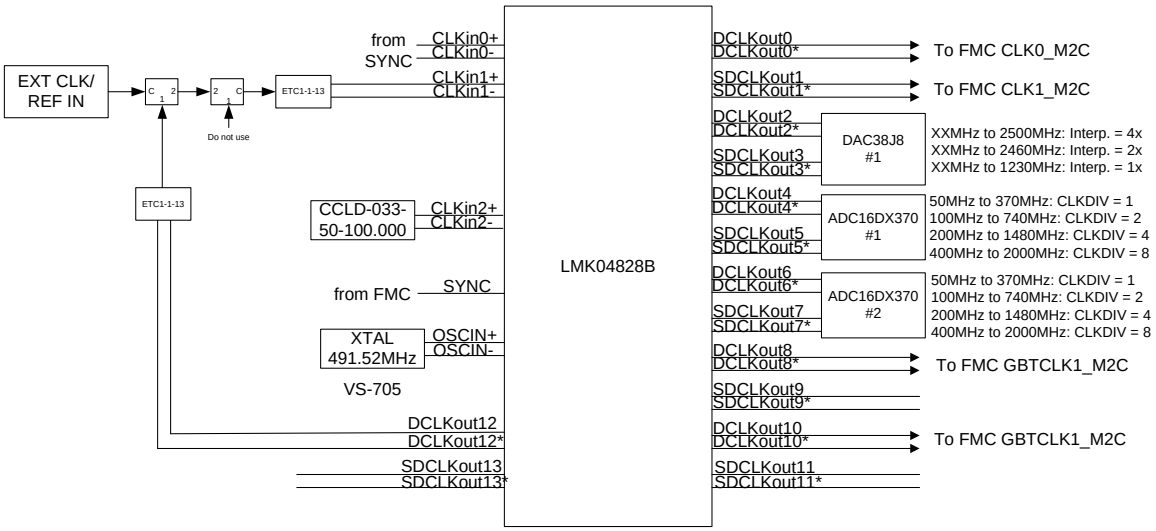


Figure 18 : Clock Tree Architecture

TI's LMK04828B Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner is the base of the clock tree. There are two integer-N PLLs in the LMK04828B. There are three different configurations of the clocking architecture:

1. Internal clock with internal reference:
   The onboard reference is locked and used as reference for PLL2.
2. Internal clock with external reference:
   PLL1 is used to lock the onboard reference to an external clock source. The onboard reference is used as reference for PLL2.
3. External clock:
   None of the PLLs are used. The external input signal is used directly as a source for the clock distribution section.

The PLLs ensure locking of the internal clock to either an internal or externally supplied reference. Only the second PLL is used when in internal reference mode. In this case, when no external reference is present, an onboard 491.52MHz tunable crystal oscillator is used.

When utilizing the internal reference, the high-impedance output from the first PLL must be enabled so the reference settles to a stable frequency.

The internal VCOs of the PLL serve as the clock source when using the internal or external reference. The PLL has multiple outputs, each with its own clock divider.

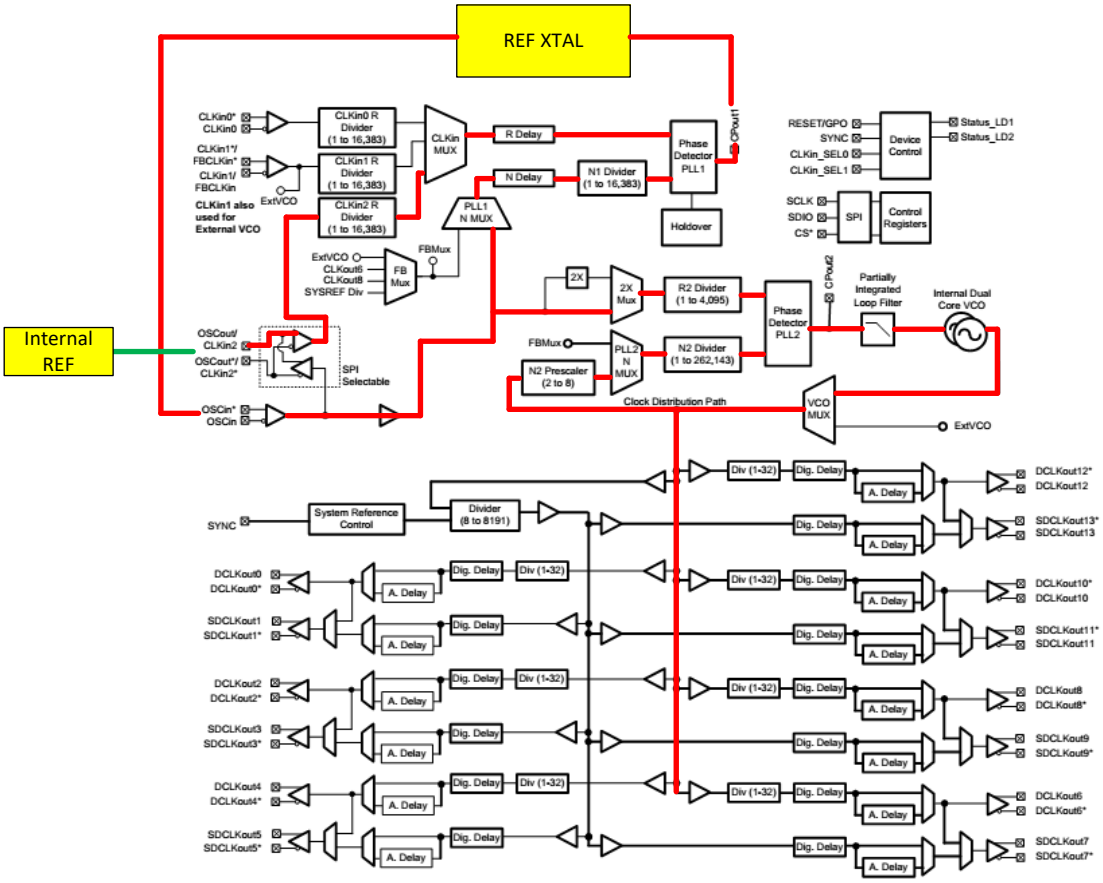


Figure 19: Internal clock with internal reference (REF XTAL locked)

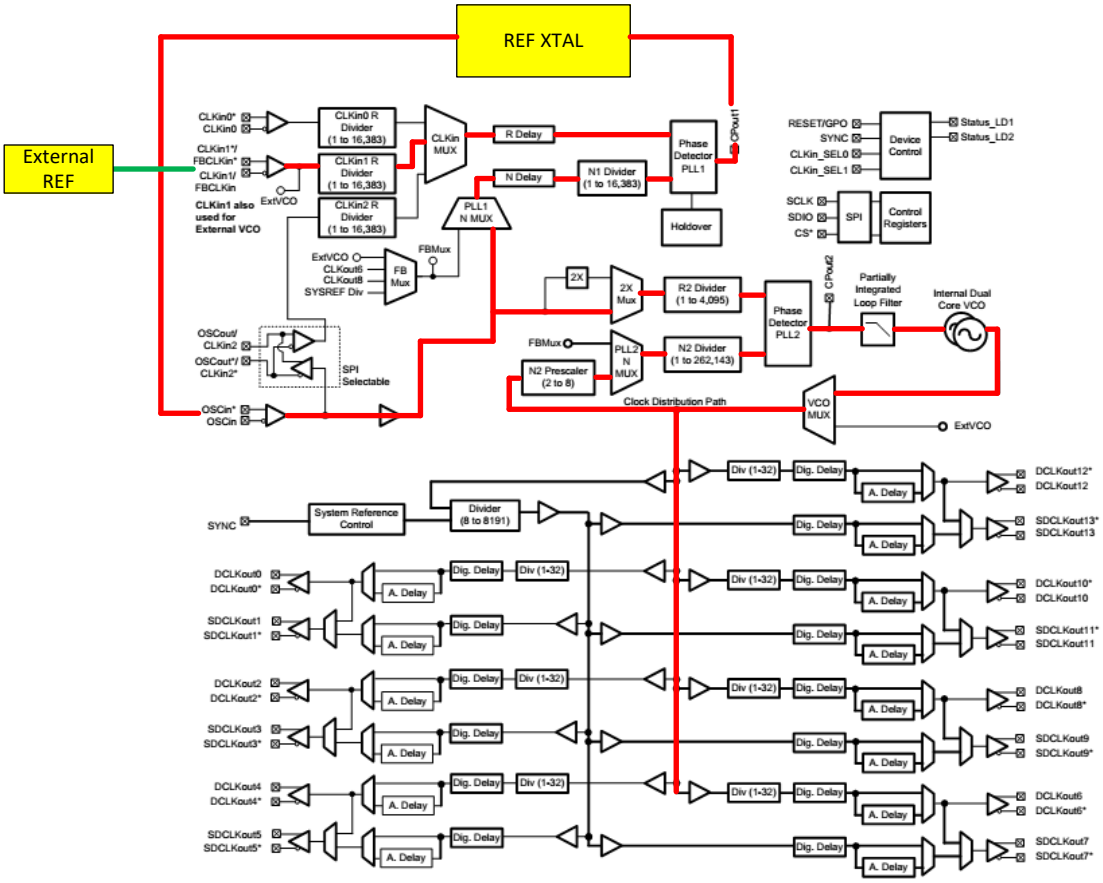


Figure 20: Internal clock with external reference (REF XTAL locked)

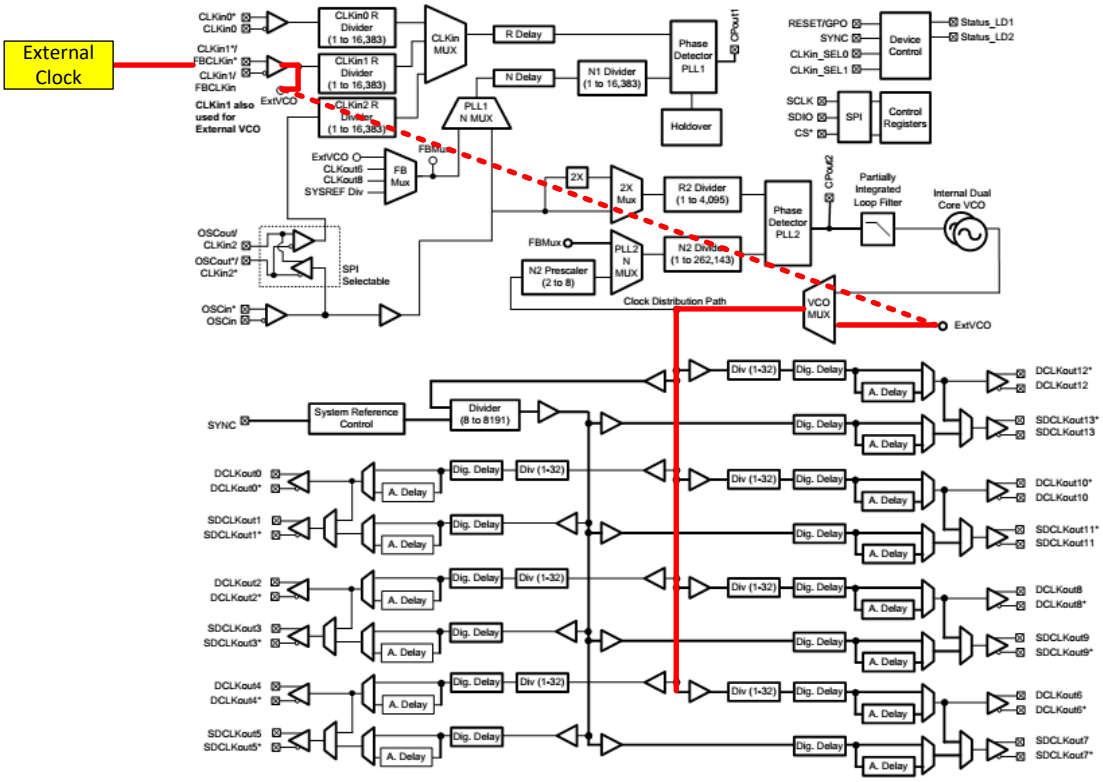


Figure 21: External clock

3.8.3 PLL design

The PLL functionality of the LMK04828B is used when sampling from an internal sampling clock. This enables flexibility in frequency selection while maintaining high performance.

The default loop filter for PLL1 is designed for a phase detector frequency of 80kHz. This is chosen so the default external reference input frequency can be 10MHz.

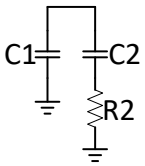


Figure 22 : PLL1 loop filter design

Reference	Value	Device Size
C1	120nF	0402
C2	4700nF	0402
R2	10k	0402

Table 6: PLL1 loop filter component values

The default loop filter for PLL2 is designed for a phase detector frequency of 160kHz.

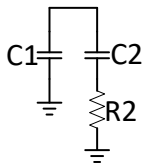


Figure 23: PLL2 loop filter design

Reference	Value	Device Size
C1	0.027nF	0402
C2	2.7nF	0402
R2	14.7k	0402

Table 7: PLL 2 loop filter component values

3.8.4 Clock Ranges

The available clock ranges with the above architecture and phase detector frequencies are as follows:

Range	ADC Clock Range	DAC Clock Range
ADC Maximum Range	50 to **370MHz**	103.09MHz to 1480MHz
DAC Maximum Range	50 to 357.14MHz	103.09MHz to **2500MHz**

Table 8: ADC and DAC Clock Ranges

Please note that it is only possible to use either the DAC or the ADC at its full sample rate. For the ADC range, it is possible to generate frequencies from 50 to 370MHz in a maximum step size of 500kHz.

3.9 Power supply

Power is supplied to the FMC14X card through the FMC connector. The pin current rating is 2.7A, but the overall maximum is limited according to Table 9.

Voltage	# Pins	Max Amps	Max Watt
+3.3V	4	3 A	10 W
+12V	2	1 A	12 W
VADJ (+1.8V / +2.5V)	4	4 A	10 W
VIO_B (VADJ)	2	1.15 A	2.3 W

Table 9: FMC standard power specification

The power provided by the carrier card can be very noisy. Special care is taken with the power supply generation on the FMC144 card to minimize the effect of power supply noise on clock

generation and data conversion. Regulators have sufficient copper area to dissipate the heat in combination with proper airflow (see section 5.3 Cooling).

Power plane	Typical	Maximum
VADJ	1 mA	1 mA
3P3V	2.1 A	2.2 A
12P0V	330 mA	330 mA
3P3VAUX (Operating) 3P3VAUX (Standby)	0.1 mA 0.01 µA	3 mA 1 µA

Table 10: Typical / Maximum current drawn from FMC144 AC-Coupled Version

Power plane	Typical	Maximum
VADJ	1 mA	1 mA
3P3V	2.1 A	2.2 A
12P0V	950 mA	1000 mA
3P3VAUX (Operating) 3P3VAUX (Standby)	0.1 mA 0.01 µA	3 mA 1 µA

Table 11: Typical / Maximum current drawn from FMC144 DC-Coupled Version

4 Controlling the FMC14X

The FMC14X is designed to be fully controlled through the SPI interfaces and other control signals on the FMC connector. Good knowledge of the internal structure and communication protocol of relevant onboard devices is required for controlling the FMC14X. Refer to the datasheets mentioned in the Related Documents section of this manual for detailed information. Abaco may also be contacted for support (www.abaco.com).

4.1 Guidelines for controlling the clock tree

Apart from enabling the onboard reference, the whole clock tree is controlled by programming the LMK04828B device through a serial communication bus. The following guidelines should be taken into account:

1. Only the second PLL is used in the LMK04828B when there is no external reference. The charge pump output needs to be set to midscale.
2. The internal reference is enabled by driving REF_EN high. The internal reference should only be enabled if the internal clock is used and no external reference is applied.
3. It is recommended to disable the unused clock outputs on the LMK04828B.
4. It is recommended to disable PLL functions and VCO input on the LMK04828B when an external sampling clock is applied.
5. When the internal clock is used, the PLL functions need to be enabled. The recommended phase detector frequency is 100MHz and the recommended VCO frequency is 2500MHz. If the internal reference is used, the reference divider should be set to 1 and the VCO divider is set to 25.
6. Other phase detector frequencies may be used, but stability of the PLL is not guaranteed in all cases.

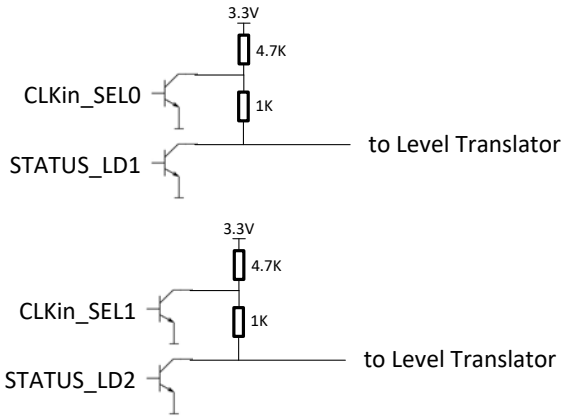


Figure 24: SELECT/STATUS architecture

4.2 Guidelines for controlling the ADCs

Controlling the ADC enables advanced control of the digitizing process. The ADC16DX370 can be programmed through a serial communication interface to change the output format or use advanced settings including offset correction, amplitude and phase imbalance, over-range detection, signal processing, input clock divider setting, and sampling instant phase adjustment.

1) The ADC cores require calibration after power-up to achieve full performance. After power-up, each ADC detects that the power supplies and clock are valid, waits for a power-up delay, and then performs a calibration of the ADC core. The power-up delay is 8.4e6 sampling clock cycles or 22.7ms at a 370MSPs sampling rate. The calibration requires approximately 2.0e6 sampling clock cycles. Re-calibration is recommended for large changes in ambient temperature to maintain optimal dynamic performance. If the system requires that the input clock divider is set to 2, 4, or 8, then ADC calibration must be performed manually after the divider has been set to the desired value. Changing the clock divider setting initiates a JESD204B link reinitialization.
2) The DC offset correction is bypassed by default but may be enabled and configured via the SPI interface. When DC offset correction is enabled, any signal in the stop band of the high-pass filter is attenuated.
3) Separate over-range detection output signals for channels A0, A1, A2, and A3 are dedicated to pins. The OVER[A/B/C/D] pin asserts (high) when an over-range signal is detected at the input of channel A0/A1/A2/A3 respectively. The short delay from when an over-range signal is incident at the input until the OVER[A(x)] is asserted allows for almost immediate detection of over-range signals without delay from the internal ADC pipeline latency or data serialization latency. The input power threshold to indicate an over-range event is programmable via the SPI interface from full-scale code range down to a +/-128 LSB code range in steps of 128 codes relative to the 16-bit code range of the data at the output of the ADC core. After an over-range event occurs and the signal at the channel input reduces to a level below full-scale, an internal counter begins counting to provide a hold function. When the counter reaches a programmable counter threshold, the OVER[A(x)] signal is de-asserted. The duration of the hold

counter is programmable via the SPI interface to hold for 0, 3, 7, or 15 frame clock cycles.

4) The differential drivers of the ADC device that output the serial JESD204B data are voltage-mode drivers with amplitude control and de-emphasis features which may be configured via the SPI for a variety of different channel applications. Eight amplitude control (VOD) and eight de-emphasis control (DEM) settings are available. Both VOD and DEM must be configured to optimize the noise performance of the serial interface for a particular lossy channel. The output common-mode of the driver varies with the configuration of the output swing.
5) Power down and sleep modes are provided to allow the user to reduce the power consumption of the device. Both modes reduce power consumption by the same amount, but they differ in the amount of time required to return to normal operation. Upon changing from power down back to normal operation, an ADC calibration routine is performed. Awaking from sleep mode does not perform an ADC calibration. Neither power-down mode nor sleep mode resets the configuration registers.
6) Data may be output in the serial stream as two's complement format by default or optionally as offset binary. This formatting is configured via the SPI interface and is performed in the data path prior to JESD204B data framing and 8b/10b encoding.

The ADC16DX370 utilizes a JESD204B subclass 1 interface to transfer data from the ADC to the FPGA on the carrier card. It supports the following features:

Feature	**Supported**
Subclass	Subclass 1. The ADC16DX370 supports most subclass 0 requirements but is not strictly subclass compliant.
SYSREF	Periodic, Pulsed Periodic, and One-Shot.
Latency	Deterministic latency supported for subclass 1 implementations using standard SYSREF signal.
Transport layer features and configuration	L=1 or 2 for each channel. K configuration Scrambling
Data link layer features	8b/10b encoding Lane synchronization D21.5, K28.5, ILA PRBS7, PRBS23, Ramp test sequences

Table 12: ADC16DX370 Supported Features

4.3 Guidelines for controlling the DACs

Controlling the DAC enables advanced control of the conversion process. The DAC38J84 can be programmed through a serial communication interface to change the input format or use advanced settings including gain control, offset correction, and several power-down modes.

1) The DAC38J84 has an on-chip, low-jitter phase-locked loop (PLL). The PLL external loop filter is not currently supported.

2) The DAC38J84 includes an output multiplexer before the digital-to-analog converters that allows any signal channel D0-D3 to be routed to any DAC A-D. See pathx_out_sel in the datasheet for details on how to configure the cross-bar switches.
3) The DAC38J84 provides an optional mechanism to protect the power amplifier (PA) in cases where the signal power shows some abnormality. In the PA protection mechanism, the signal power is monitored by maintaining a sliding window accumulation of the last N samples. N is selectable to be 64 or 128. The average amplitude of the input signal is computed by dividing the accumulated value by the number of samples in the delay-line (N). The result is then compared against a programmable threshold value. If the threshold is violated, the delayed input signal is divided by a programmable value to form a scaled down version of the input signal.
4) All receive channels include a 12-bit counter for accumulating pattern verification errors. The counter increments once for every cycle that the TESTFAIL bit is detected. The counter will not increment when it is at its maximum value. This can be used to get a measure of the bit error rate.
5) All receive channels provide features that facilitate mapping the received data eye or extracting a symbol response. The process of transforming this data into a map of the eye or a symbol response must be performed externally, typically in software.
6) The DAC incorporates a temperature sensor block which monitors the temperature by measuring the voltage across two transistors. The voltage is converted to an 8-bit digital word using a successive approximation register (SAR) analog-to-digital conversion process. The result is scaled, limited, and formatted as a two's complement value representing the temperature in degrees Celsius. The sampling is controlled by the serial interface signals SDENB and SCLK. If the temperature sensor is enabled, a conversion takes place each time the serial port is written or read. The temperature sensor is enabled even when the device is in sleep mode.
7) The DAC offers flexible alarm monitoring which can be used to alert of a possible malfunction scenario. All of the alarm events can be accessed either through the SPI register and/or the ALARM pin. Once an alarm is set, the corresponding alarm bit must be reset through the serial interface to allow further testing.

4.4 Guidelines for controlling onboard monitoring

The FMC14X holds an AMC7823 for monitoring several power supply voltages on the board as well as the temperature. The device can be programmed and read out through its SPI bus.

1) The measured values must be multiplied by a constant to get the actual analog level (see Table 13). The measured value on channel five (-5.0V) must use the formula 10*(ADC5/4095-1) to decode the correct supply level. The monitor reference voltage is 1.25V, giving an effective input range 0-2.5V.
2) Continuously operating the SPI bus might interfere with the A/D or D/A conversion process and cause signal distortion. It is recommended to program the minimum and maximum thresholds in the monitoring devices and only read from the devices when the interrupt line is asserted (GALARMn). Only the first four channels can be monitored with thresholds. These are the main supplies derived from the other voltages on channel four to seven.
3) It is recommended to power down the unused features: DAC operation, precision current source, and reference buffer amplifier.
4) Internal reference must be selected. Since the AMC7823 is powered from 3.3V, only internal reference of +1.25V is allowed.

5) Only internal trigger mode is supported. Auto mode is recommended to continuously monitor channel 0 to channel 3 and verify against the programmed thresholds.
6) GPIO #5 controls the EEPROM Write Protect signal.

Parameter:	Voltage	Formula
Channel 0	3.0V_ANALOG	2.0 * ADC0
Channel 1	0.9V_ANALOG	1.0 * ADC1
Channel 2	1.2V_ANALOG	1.0 * ADC2
Channel 3	1.8V_ANALOG	1.0 * ADC3
Channel 4	+5V_ANALOG	3.0 * ADC4
Channel 5	-5V_ANALOG	10 * (ADC5/4095-1)
Channel 6	3.3V_ANALOG	2.0 * ADC6
Channel 7	VADJ	2.0 * ADC7
Temperature (Ch.8)	(internally generated)	1.6C / LSB

Table 13: Temperature and voltage parameters

5 Environment

5.1 Temperature

Operating temperature

- 0˚C to +70˚C (Commercial)
- -40˚C to +85˚C (Industrial)

Storage temperature:

- -40˚C to +120˚C

5.2 Monitoring

The AMC7823 device may be used to monitor the voltage on the different power rails as well as the temperature. It is recommended that the carrier card and/or host software use the power-down features in the devices in case the temperature is too high. Normal operations can resume once the temperature is within the operating conditions boundaries.

5.3 Cooling

Two different types of cooling are available for the FMC14X.

5.3.1 Convection cooling

The air flow provided by the fans of the chassis the FMC14X is enclosed in will dissipate the heat generated by the onboard components. A minimum airflow of 300 LFM is recommended.

Optionally, low profile FANs can be glued on top of the devices. The card has a 12V fan power connection. For standalone operations (such as on a Xilinx development kit), it is highly recommended to blow air across the FMC to ensure that the temperature of the devices is

within the allowed range. Abaco's warranty does not cover boards on which the maximum allowed temperature has been exceeded.

5.3.2 Conduction cooling

In demanding environments, the ambient temperature inside a chassis could be close to the operating temperature defined in this document. It is very likely that in these conditions the junction temperature of power-consuming devices will exceed the operating conditions recommended by the device manufacturers (mostly +85°C). While a low profile heat sink coupled with sufficient air flow might be sufficient to maintain the temperature within operating boundaries, some active cooling would yield better results and would certainly help with resuming operations much faster if the devices are disabled because of a temperature "over range".

6 Safety

This module presents no hazard to the user.

7 EMC

This module is designed to operate from within an enclosed host system built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

8 Warranty

	Hardware	*Software/Firmware*
Basic Warranty (included)	1 Year from Date of Shipment	90 Days from Date of Shipment
Extended Warranty (optional)	2 Years from Date of Shipment	1 Year from Date of Shipment

Appendix A: HPC control/status signals

Signal Name	Group	FMC Pin	Direction	Description
SCLK	LMK04828 ADC16DX370 DAC38J84 AMC7823	G12	C2M	SPI interface serial clock pin (shared)
SDI	LMK04828 ADC16DX370 DAC38J84 AMC7823	G13	C2M	SPI interface data input pin (shared)
SDO	ADC16DX370 AMC7823	G19	M2C	SPI interface data output pin (shared)
RESET/GPO	LMK04828	H14	C2M	Device reset or GPO
CS*	LMK04828	H22	C2M	SPI Chip select
SYNCIN	LMK04828	G22	C2M	
Status_LD1 / CLKin_SEL0	LMK04828	C18	M2C	Programmable Status Pin (MISO)
Status_LD2 / CLKin_SEL1	LMK04828	C19	M2C	Programmable Status Pin
CLK0	LMK04828	H4/H5	M2C	DCLKOUT0 from LMK04828
CLK1	LMK04828	G2/G3	M2C	SDCLKOUT1 from LMK04828
CSB_1	ADC16DX370	D21	C2M	SPI interface chip select pin (ADC1)
CSB_2	ADC16DX370	C22	C2M	SPI interface chip select pin (ADC2)
ADC_SYNCB_1	ADC16DX370	G9/G10	C2M	SYNCB input (ADC1, A&B)
ADC_SYNCB_2	ADC16DX370	H7/H8	C2M	SYNCB input (ADC2, C&D)
ADC_OVRA	ADC16DX370	D15	M2C	Over-Range (ADC-A)
ADC_OVRB	ADC16DX370	C14	M2C	Over-Range (ADC-B)
ADC_OVRC	ADC16DX370	C15	M2C	Over-Range (ADC-C)
ADC_OVRD	ADC16DX370	H16	M2C	Over-Range (ADC-D)
DAC_SYNCB	DAC38J84	H10/H11	M2C	DAC sync request
DAC_SYNCN_AB	DAC38J84	H19	M2C	CH-AB Sync Req
DAC_SYNCN_CD	DAC38J84	H20	M2C	CH-CD Sync Req
ALARM	DAC38J84	D14	M2C	CMOS output for ALARM condition
RESETB	DAC38J84	G25	C2M	Active low input for chip RESET, which resets all the programming registers to their default state
SDENB	DAC38J84	D20	C2M	Active low serial data enable (CS)
SDO	DAC38J84	G18	M2C	Unidirectional serial interface data
SLEEP	DAC38J84	G24	C2M	Active high asynchronous hardware power-down input
TXENABLE	DAC38J84	H26	C2M	Transmit enable active high input
Ref_En	VS-705	G21	C2M	Enable the TCXO power supply
OSC100_EN	CCLD-033-50-100	H13	C2M	Enable 100MHz Osc
Clock Sel1	PE4257	C10	C2M	External reference
Clock Sel2	PE4257	C11	C2M	External reference/Clock output

I2C_SDA	FMC Connector	C31	BiDir	I2C serial data
I2C_SCL	FMC Connector	C30	C2M	I2C serial clock
CLKBUF_TRIGGER	External	G6/G7	M2C	External Trigger Signal
FPGA_TRIGGER	External	D8/D9	C2M	FPGA trigger source
SYNCSRC_SEL0	SY89547LMG	D11	C2M	Trigger SRC Select (0)
SYNCSRC_SEL1	SY89547LMG	D12	C2M	Trigger SRC Select (1)
GALARM#	AMC7823	D18	M2C	Global Alarm
MON_RESET#	AMC7823	D23	C2M	Reset for Monitor
SS#	AMC7823	C23	C2M	SPI Chip Select
ALARM0	AMC7823	D17	M2C	Monitor Alarm 0
ALARM1	AMC7823	H17	M2C	Monitor Alarm 1
ALARM2	AMC7823	G15	M2C	Monitor Alarm 2
ALARM3	AMC7823	G16	M2C	Monitor Alarm 3

Table 14 FMC control/status

Signal Name	Group	FMC Pin	Direction	Description
GBTCLK0	LMK04828	D4/D5	M2C	DCLKOUT8 from LMK04828
GBTCLK1	LMK04828	B20/B21	M2C	DCLKOUT10 from LMK04828
ADC1_SA0	ADC16DX370	C6/C7	M2C	Channel A0, lane 1 of 2
ADC1_SB0	ADC16DX370	A2/A3	M2C	Channel A1, lane 1 of 2
ADC2_SA0	ADC16DX370	A6/A7	M2C	Channel A2, lane 1 of 2
ADC2_SB0	ADC16DX370	A10/A11	M2C	Channel A3, lane 1 of 2
ADC1_SA1	ADC16DX370	A14/A15	M2C	Channel A0, lane 2 of 2
ADC1_SB1	ADC16DX370	A18/A19	M2C	Channel A1, lane 2 of 2
ADC2_SA1	ADC16DX370	B16/B17	M2C	Channel A2, lane 2 of 2
ADC2_SB1	ADC16DX370	B12/B13	M2C	Channel A3, lane 2 of 2
DAC_RX0	DAC38J84	C2/C3	C2M	DAC lane 1 of 8
DAC_RX1	DAC38J84	A22/A23	C2M	DAC lane 2 of 8
DAC_RX2	DAC38J84	A26/A27	C2M	DAC lane 3 of 8
DAC_RX3	DAC38J84	A30/A31	C2M	DAC lane 4 of 8
DAC_RX4	DAC38J84	A34/A35	C2M	DAC lane 5 of 8
DAC_RX5	DAC38J84	A38/A39	C2M	DAC lane 6 of 8
DAC_RX6	DAC38J84	B36/B37	C2M	DAC lane 7 of 8
DAC_RX7	DAC38J84	B32/B33	C2M	DAC lane 8 of 8

Table 15 JESD204B reference clocks and data lanes

Appendix B: Errata

Errata Status Summary			
Errata #	Title	Impact	Revisions
1	PLL1 Lock Indication False	Minor	FMC140 r1.1 and earlier FMC142 r1.1 and earlier FMC144 r1.1 and earlier

1. **Description**:

   On some boards, when PLL1 is used to lock the internal 491.52MHz Voltage Controlled Saw Oscillator (VCSO) to either the on-board 100MHz reference oscillator, or an external reference, the LMK04828 clock chips RB_PLL1_LD Lock status bit may indicate an unlocked state. This problem is oscillator dependent and is caused by a relatively low impedance voltage divider (123K ohms at ½ VDD, ~1.65V) internal to the 491.52MHz VCSO which loads the PLL1 loop filter. This problem is exacerbated at lower phase detector frequencies where there is a longer time between phase detector pulses. This effect is minimal when the tuning voltage of the 'locked' oscillator is at or near ½ VDD. As the tuning voltage diverges from ½ VDD the divider will increasingly pull the tuning voltage back toward ½ VDD. At tuning voltages (approximately) above 2.1V, or below 1.1V, the LMK04828 PLL1 Digital Lock Detector circuitry detects this condition and indicates that the PLL1 is unlocked.

   Impact:

   There is the potential for PLL1 to be unlocked resulting in reduced performance.

   Workaround:

   Program the LMK04828 PLL1_N divider registers at 0x159:0x15A for an output frequency slightly above (or below) 491.520MHz, this will bring the VCSOs tuning voltage closer to the mid-supply and remove the problem. When this issue was observed on the reference design, increasing the PLL1_N register value from 0xA000 to 0xA001 for an output of 491.600MHz resolved the problem.

   Resolution:

   None planned.