2023 超大型積體電路電腦輔助設計概論

2023 Introduction to VLSI CAD Lab 11

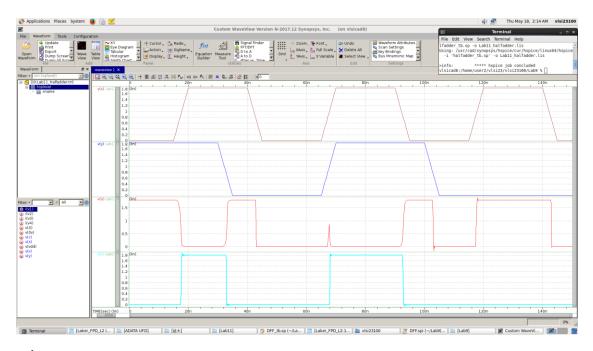
學號: E94096097 姓名: 陳慕永

※作業要求的圖請使用**電腦截圖程式**截取,請勿用手機拍照的方式繳交 ※Report 檔請以 pdf 的格式繳交

- HA
 - Presim
 - 請截取 terminal 顯示 job concluded 的圖

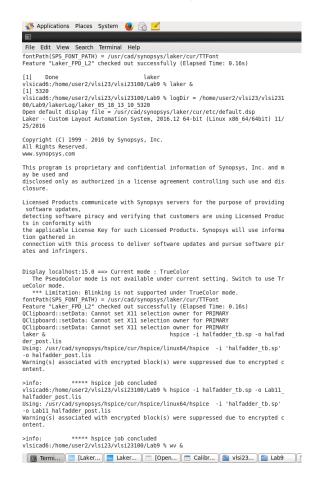
```
Applications Places System
                               File Edit View Search Terminal Help
  **error** (halfadder tb.sp:8) unable to open file "cic018.l" .Either file does
n't exists or path is wrong. Please enter the correct file location.
               ***** job aborted
 lic: Release hspice token(s)
lic: total license checkout elapse time:
                                               10.35(s)
vlsicad6:/home/user2/vlsi23/vlsi23100/Lab9 % cat Lab11 halfadder.lis
 ***** HSPICE -- N-2017.12 linux64 (Nov 21 2017) ******
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  to Synopsys, Inc. This software may only be used in accordance
 with the terms and conditions of a written license agreement with
 Synopsys, Inc. All other use, reproduction, or distribution of
  this software is strictly prohibited.
 Input File: halfadder_tb.sp
  Command line options: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice -i ha
lfadder tb.sp -o Lab11 halfadder.lis
 lic:
 lic: FLEXlm: SDK 11.6.8.3
 lic: USER: vlsi23100
                                  HOSTNAME: vlsicad6
 lic: HOSTID: "5cf3fcba2b50"
                                  PID:
                                            23535
 lic: Using FLEXlm license file:
 lic: 26585@lstc
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 31-mar-2024/2023.03
 lic: 320(in use)/450(total) FLOATING license(s) on SERVER 26585@lstc
 lic:
  **error** (halfadder_tb.sp:8) unable to open file "cic018.l" .Either file does
n't exists or path is wrong. Please enter the correct file location.
               ***** job aborted
lic: Release hspice token(s)
lic: total license checkout elapse time:
                                               10.35(s)
vlsicad6:/home/user2/vlsi23/vlsi23100/Lab9 % hspice -i halfadder tb.sp -o Lab11
halfadder.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice -i 'halfadder_tb.sp'
-o Lab11 halfadder.lis
               ***** hspice job concluded
vlsicad6:/home/user2/vlsi23/vlsi23100/Lab9 %
```

• 請截取 WaveView 中的波形

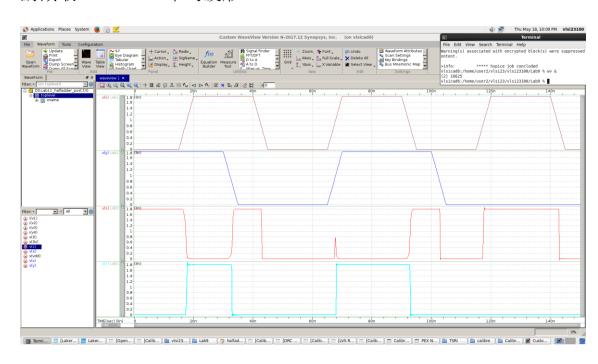


• Post-sim

• 請截取 terminal 顯示 job concluded 的圖

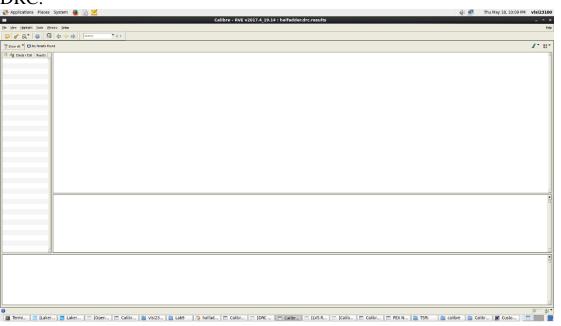


· 請截取 WaveView 中的波形

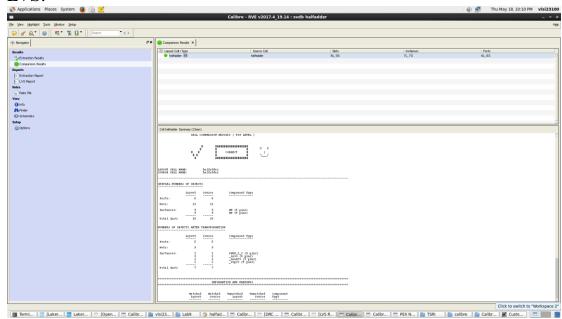


• DRC/LVS 結果

DRC:



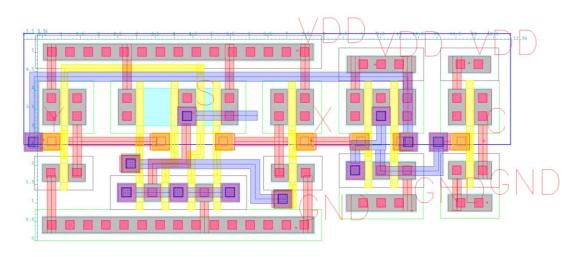
LVS:



• Layout 截圖(顯示長寬)

長:12.96

寬:5.51



• 嘗試簡單說明 Presim 與 Post-sim 結果比較

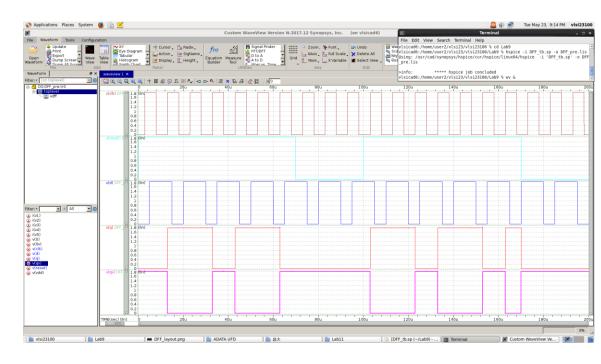
Presim 和 Post-sim 的波形幾乎一樣,只差在 Presim 的 output 波形的直角轉角處震盪較 Post-sim 的劇烈一點點。

DFF

- Presim
 - 請截取 terminal 顯示 job concluded 的圖

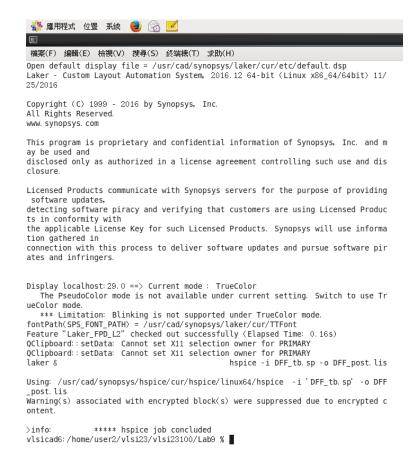


• 請截取 WaveView 中的波形

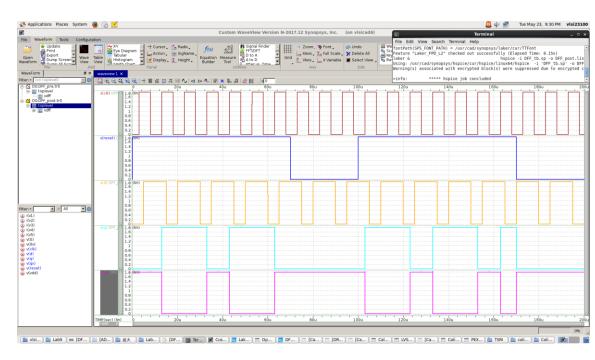


Post-sim

• 請截取 terminal 顯示 job concluded 的圖

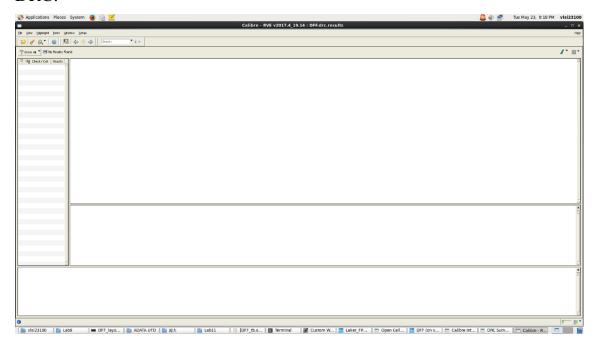


• 請截取 WaveView 中的波形

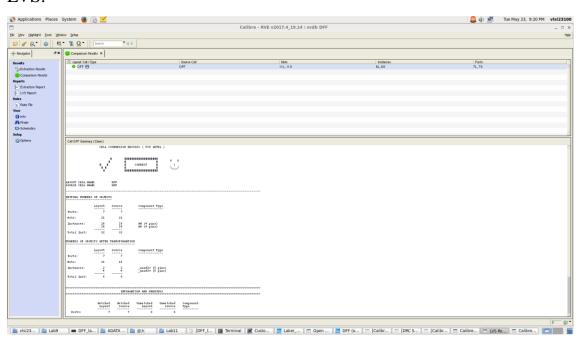


• DRC/LVS 結果

DRC:



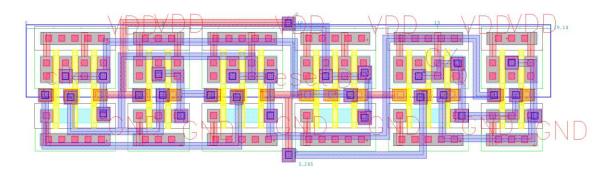
LVS:



• Layout 截圖(顯示長寬)

長:19.14

寬:5.285



• 嘗試簡單說明 Presim 與 Post-sim 結果比較
Presim 和 Post-sim 的波形幾乎一樣,只差在 Post-sim 的
output 波形的雜訊較 Presim 的多一點點。

• 心得討論

畫 layout 時若是由多個小元件組成一個大元件可以先畫出小元件 再兜出大元件會比較省時並且比較容易縮面積。我也學到原來 gate 和 body 可以安排在相鄰的空間與 VDD 和 GND 可以分割成 多段不用連接在一起。