## 2023 超大型積體電路電腦輔助設計概論

## 2023 Introduction to VLSI CAD Lab 12

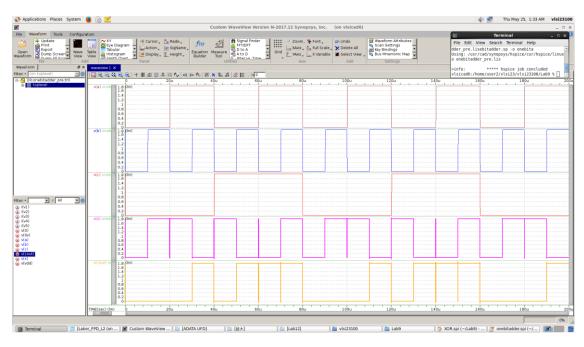
學號: E94096097 姓名: 陳慕永

※作業要求的圖請使用**電腦截圖程式**截取,請勿用手機拍照的方式繳交 ※Report 檔請以 pdf 的格式繳交

- Full Adder
  - Presim
    - 請截取 terminal 顯示 job concluded 的圖

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               ***** hspice job concluded
vlsicad6:/home/user2/vlsi23/vlsi23100/Lab9 %
```

• 請截取 WaveView 中的波形

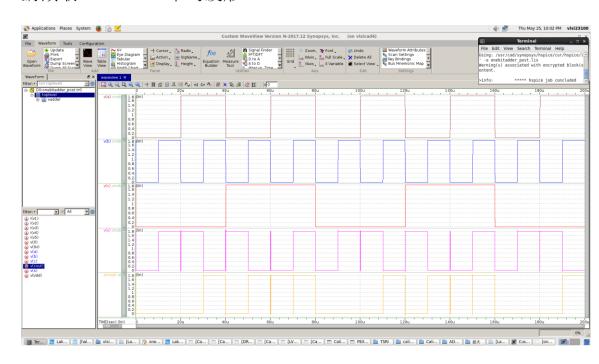


#### Post-sim

• 請截取 terminal 顯示 job concluded 的圖

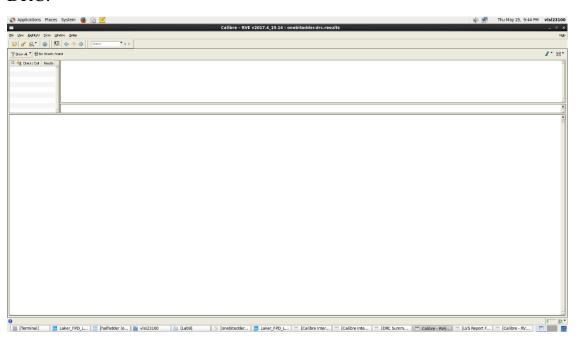


• 請截取 WaveView 中的波形

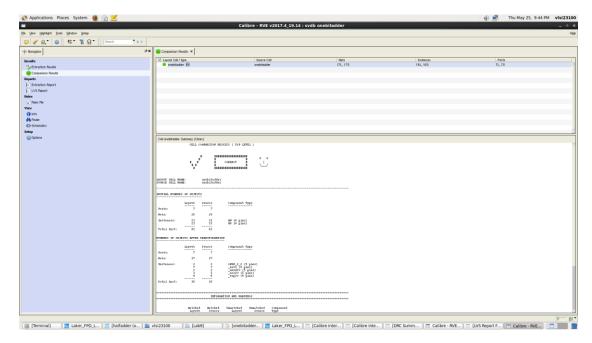


• DRC/LVS 結果

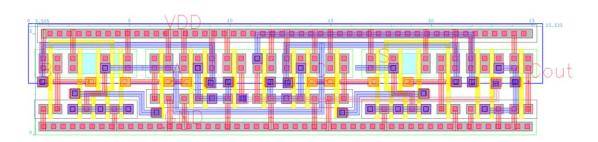
### DRC:



## LVS:



• Layout 截圖



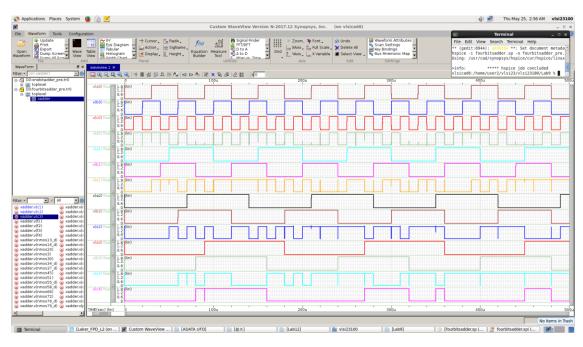
• 嘗試簡單說明 Presim 與 Post-sim 結果比較

幾乎一樣,只有細微的波形震盪不一樣。

- 4-bit Ripple Carry Adder
  - Presim
    - 請截取 terminal 顯示 job concluded 的圖

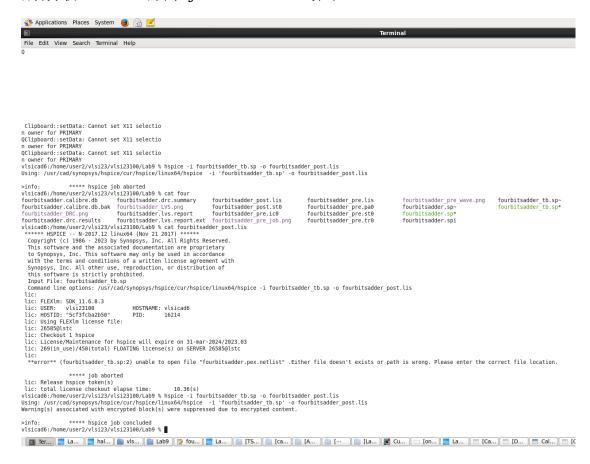


· 請截取 WaveView 中的波形

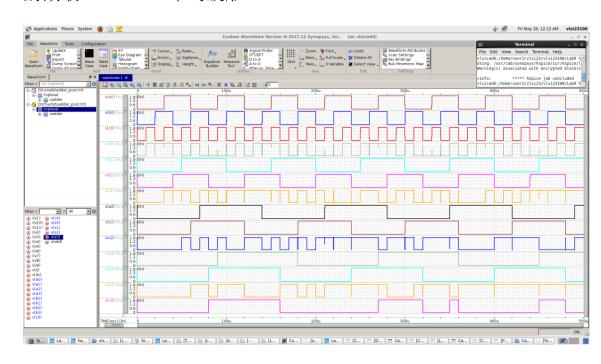


#### Post-sim

• 請截取 terminal 顯示 job concluded 的圖

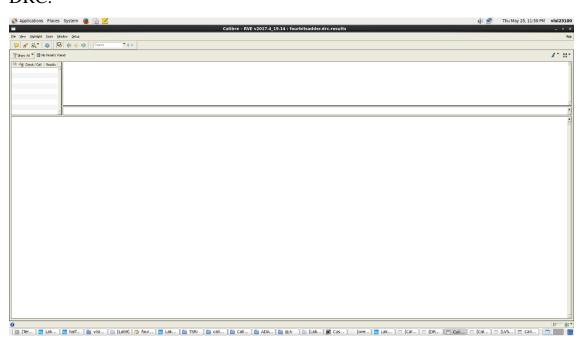


· 請截取 WaveView 中的波形

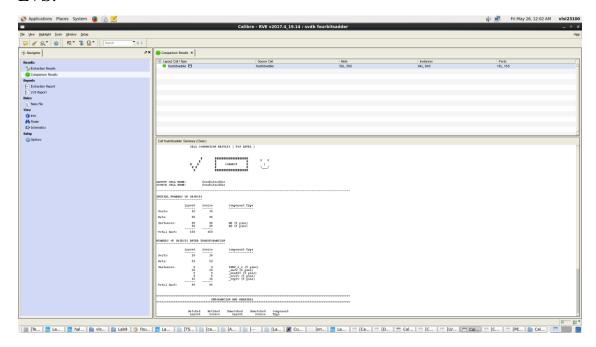


• DRC/LVS 結果

### DRC:



## LVS:



• Layout 截圖(顯示長寬)

長:100.07

寬:5.505

面積:550.88535



• 嘗試簡單說明 Presim 與 Post-sim 結果比較

Output 的波形在 input 的值變化時有時會突然有突波出現,

且 Presim 和 Post-sim 出現的位置不盡相同,突然變化的值也都不一樣,但最後都會回到正確的值。

# • 心得討論

在做此 Lab 時發現不同 gate 的 PIMP 和 NIMP 其實可以共用,

這可以省下非常多面積,也發現若是小的元件畫的好,大的元件可以非常有效率的接完線就完成了,更發現 and 和 or 的佈局非常像。