

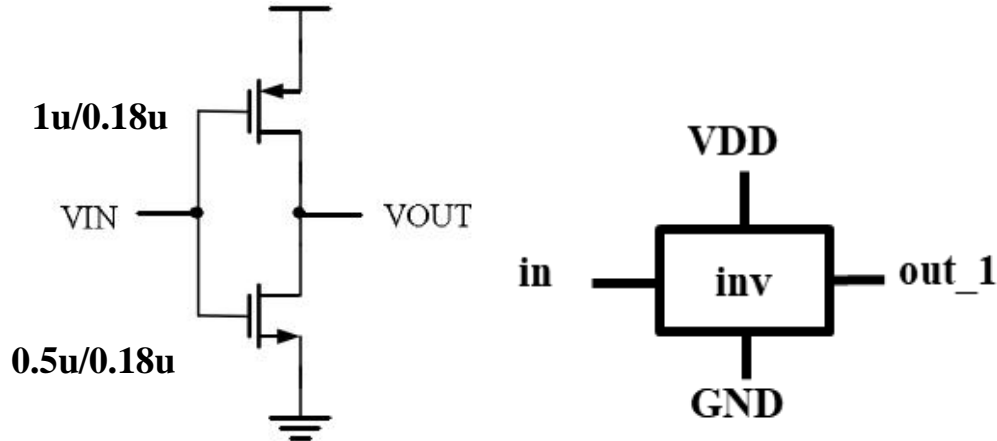
## LAB8 Homework

學號：E94096097

姓名：陳慕丞

檔案名稱為 Lab8\_學號.pdf，若檔名格式錯誤或非.pdf 檔會扣分！！

1-1. 設計一個 inverter，電晶體長寬比如下



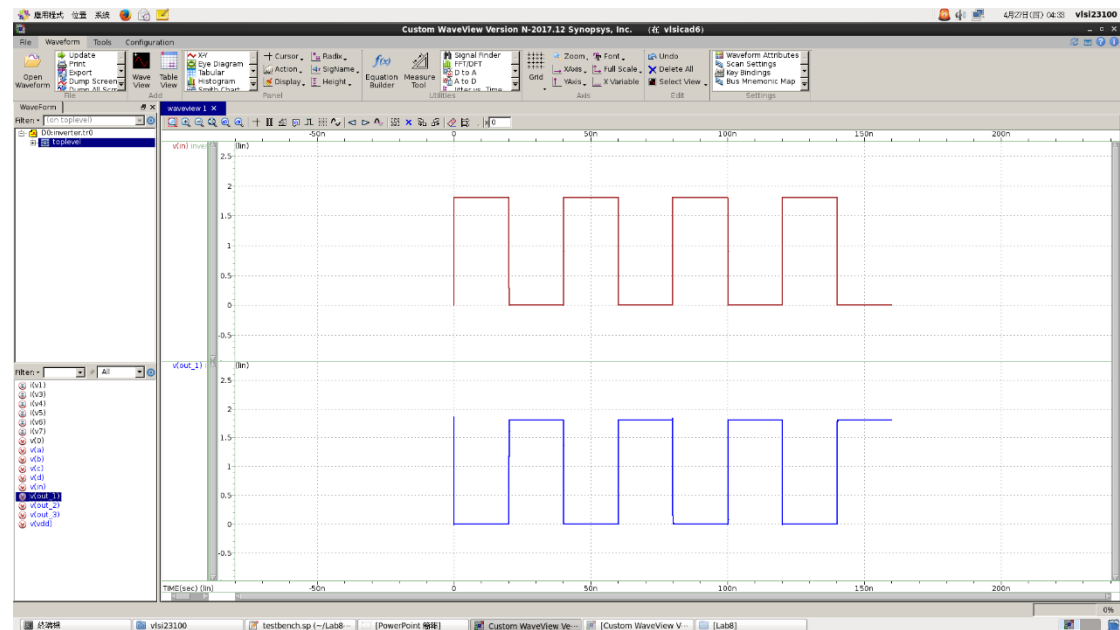
1-2. 請截取 terminal 顯示 job concluded 的圖

```
lic: FLEXlm: SDK.11.6.8.3
lic: USER: vlsi23100 HOSTNAME: vlsica06
lic: HOSTID: "5c7cfcb42460" PID: 28950
lic: Using FLEXlm license file
lic: 26585@ltn
lic: Checkout: 1 hspice
lic: License/Maintenance for hspice will expire on 31-mar-2024/2023.03
lic: S13(in_use)/450(total) FLOATING license(s) on SERVER 26585@ltn
lic:
init: begin read circuit files, cpu clock= 1.54E+00
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/ad
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/behave
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/bjt
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/burr_b
init: rm
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/comlin
init: ear
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/dio
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/fet
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/lin_te
init: ch
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/pci
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/signet
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/tl
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/tline
init: option search = /usr/cad/synopsys/hspice/cur/hspice/parts/xilinx
init: option run/vl
init: end read circuit files, cpu clock= 1.54E+00 peak memory= 262 mb
init: begin check errors, cpu clock= 1.54E+00
error: ***** hspice job aborted
lic: Release hspice token(s)
vlsica06:/home/user2/vlsi23/vlsi23100/Lab8 % hspice testbench.sp -o inverter.lis
Using /usr/cad/synopsys/hspice/cur/hspice/linu64/hspice 'testbench.sp' -o inverter.lis

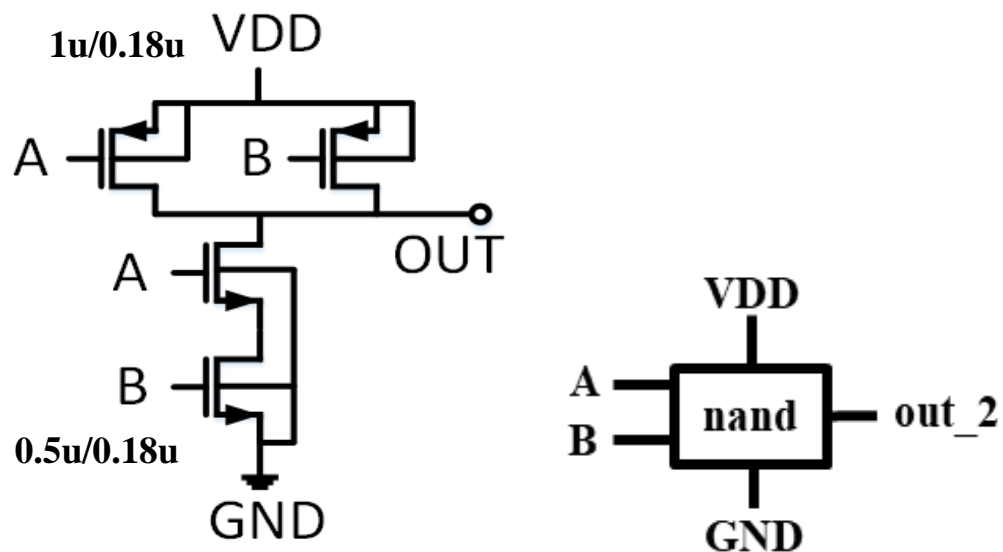
>info ***** hspice job concluded
vlsica06:/home/user2/vlsi23/vlsi23100/Lab8 %
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata::gedit-spell-language not supported
vv &
[2] 32121
vlsica06:/home/user2/vlsi23/vlsi23100/Lab8 % vv &
[3] 32345
vlsica06:/home/user2/vlsi23/vlsi23100/Lab8 %
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata::gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata::gedit-encoding not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata::gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata::gedit-encoding not supported
hspice testbench.sp -o inverter.lis
Using /usr/cad/synopsys/hspice/cur/hspice/linu64/hspice 'testbench.sp' -o inverter.lis

>info ***** hspice job concluded
vlsica06:/home/user2/vlsi23/vlsi23100/Lab8 %
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata::gedit-spell-language not supported
```

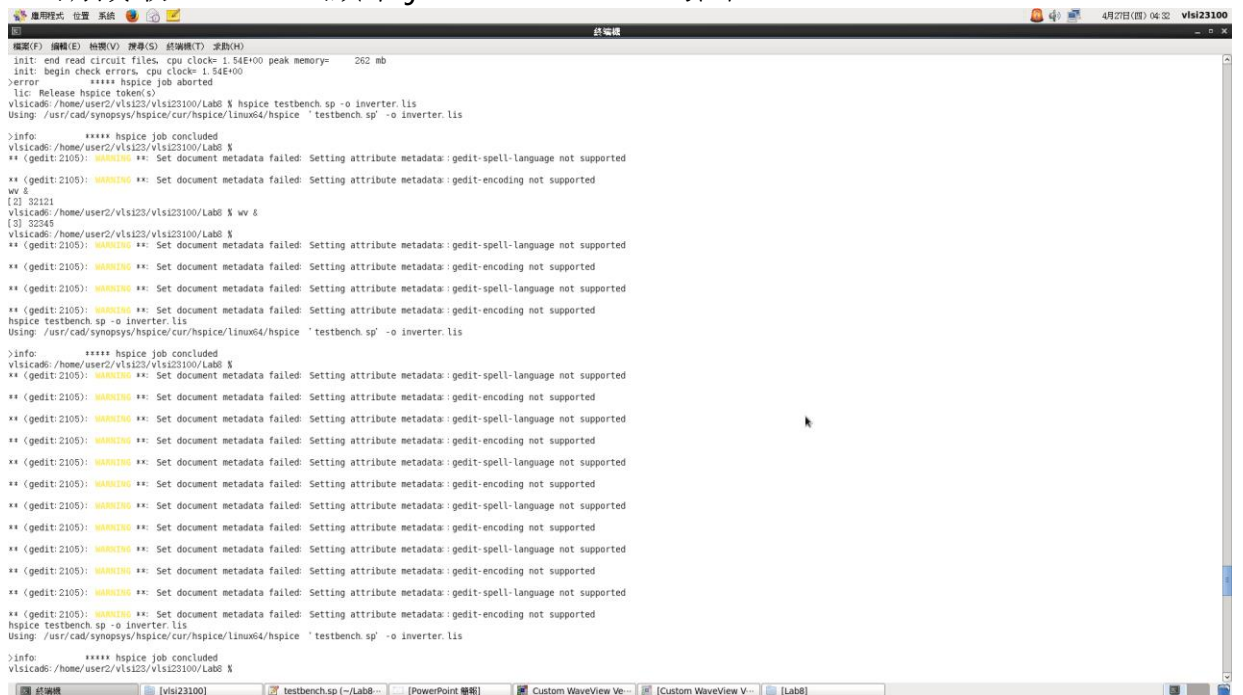
1-3. 請截取 WaveView 中 in 及 out\_1 的波形



2-1. 設計一個 NAND，電晶體長寬比如下



## 2-2. 請截取 terminal 顯示 job concluded 的圖



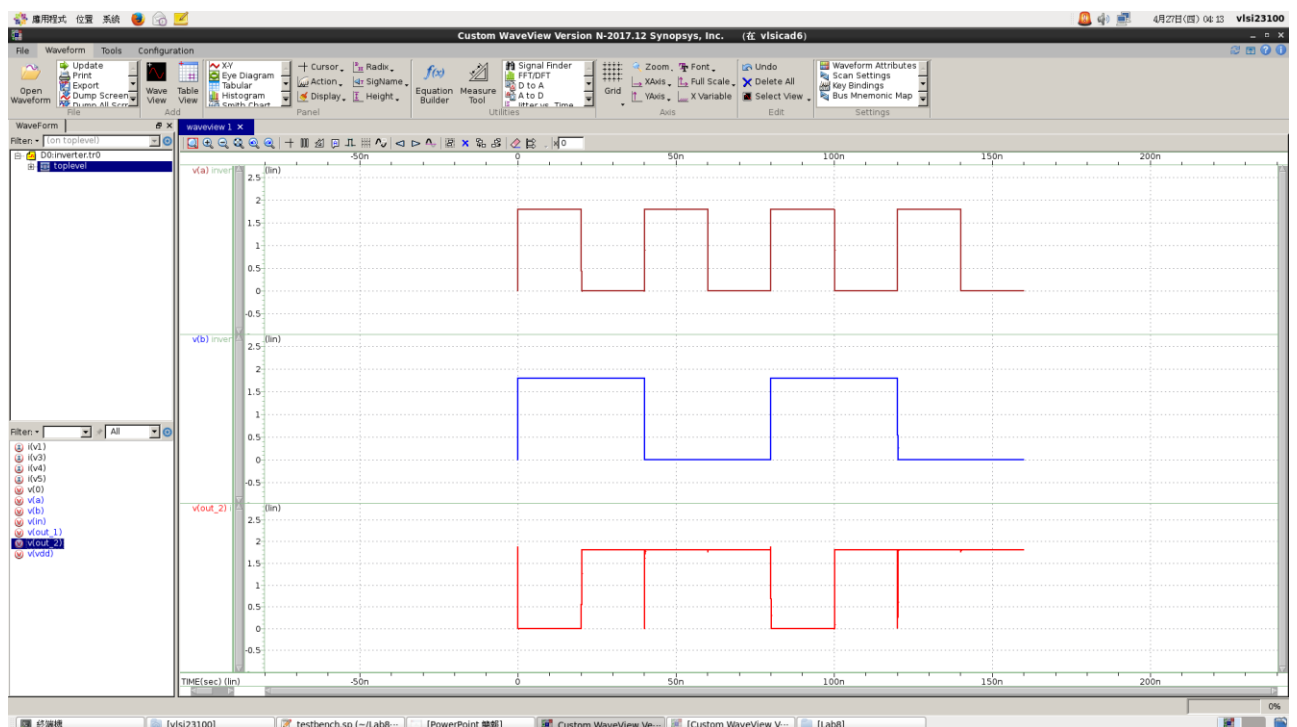
```
init: end read circuit files, cpu clock= 1.54E+00 peak memory= 262 mb
init: begin check errors, cpu clock= 1.54E+00
error: ***** hspice job aborted
lic: Release hspice token(s)
visicad6: /home/user2/vls123/vls123100/Lab8 % hspice testbench.sp -o inverter.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice `testbench.sp' -o inverter.lis

>info: ***** hspice job concluded
visicad6: /home/user2/vls123/vls123100/Lab8 %
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
vv 6
[2] 32121
visicad6: /home/user2/vls123/vls123100/Lab8 % vv 6
[3] 32345
visicad6: /home/user2/vls123/vls123100/Lab8 %
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
hspice testbench.sp -o inverter.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice `testbench.sp' -o inverter.lis

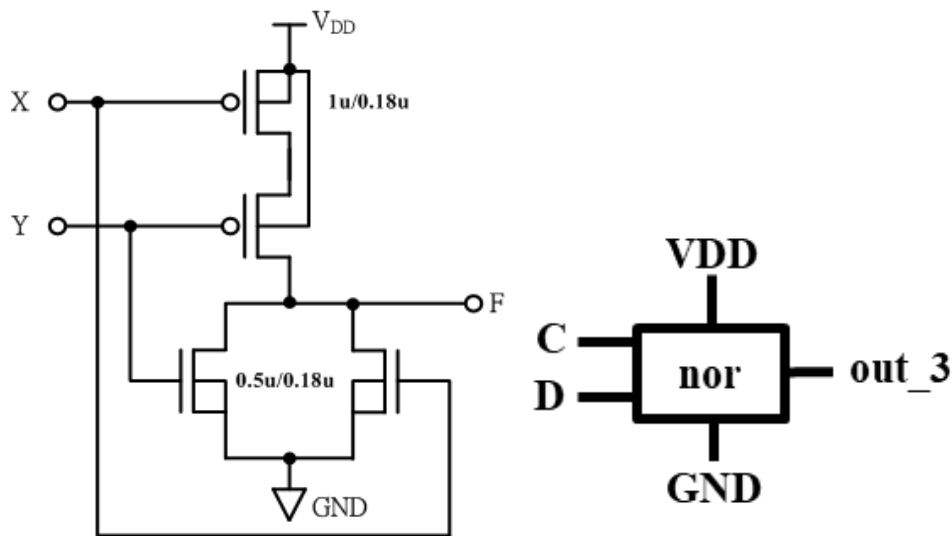
>info: ***** hspice job concluded
visicad6: /home/user2/vls123/vls123100/Lab8 %
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-spell-language not supported
** (gedit:2105): WARNING **: Set document metadata failed: Setting attribute metadata: gedit-encoding not supported
hspice testbench.sp -o inverter.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice `testbench.sp' -o inverter.lis

>info: ***** hspice job concluded
visicad6: /home/user2/vls123/vls123100/Lab8 %
```

## 2-3. 請截取 WaveView 中 A、B 及 out\_2 的波形



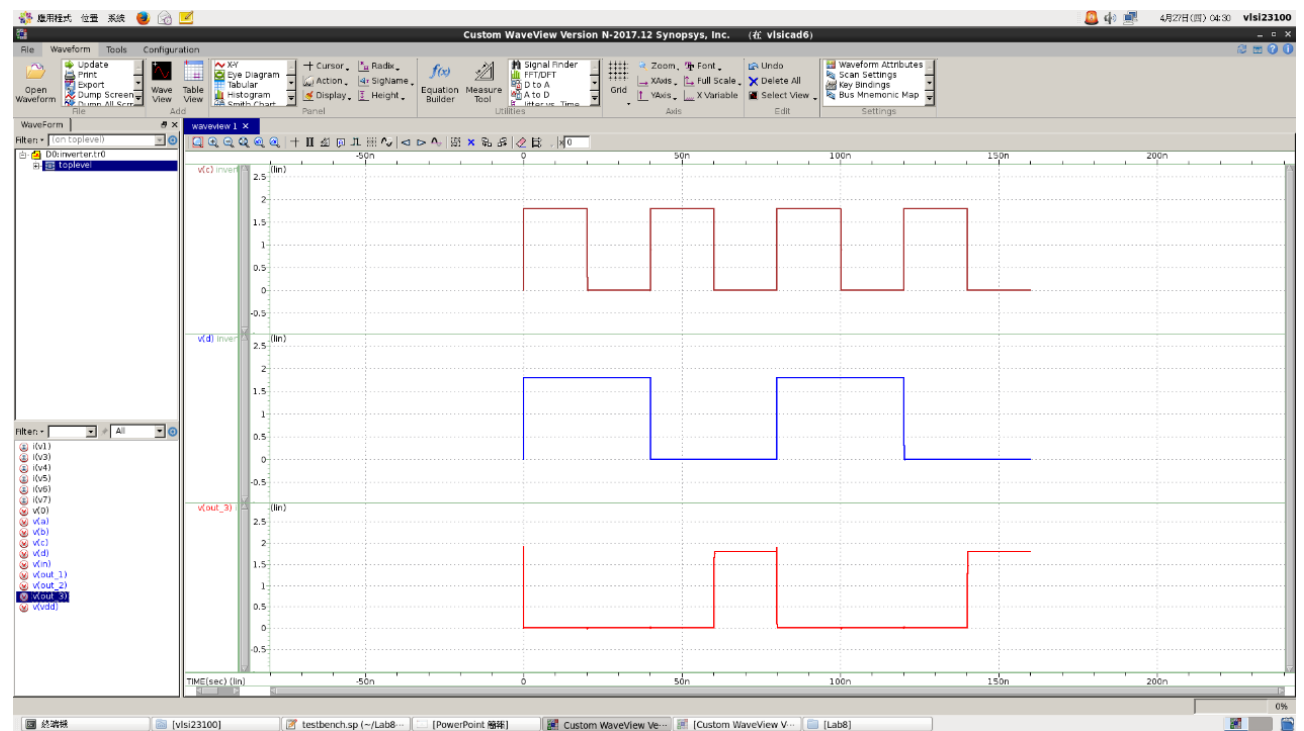
3-1. 設計一個 NOR，電晶體長寬比如下



### 3-2. 請截取 terminal 顯示 job concluded 的圖

A screenshot of a Windows terminal window. The title bar at the top reads "终端" (Terminal). The menu bar includes "檔案(F)", "編輯(E)", "檢視(V)", "搜尋(S)", "終端機(T)", and "工具(O)". The terminal content shows a script running with many error messages: "Set document metadata failed: Setting attribute metadata: git-spell-language not supported" and "Set document metadata failed: Setting attribute metadata: git-encoding not supported". These messages are repeated for each line of the script. At the bottom, the script concludes with "\*\*\*\* hspice job concluded" and "Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'testbench.sp' -o inverter.lis". The status bar at the very bottom displays the file path "C:\Users\user2\vs123\vs123100\Lab6 %" and the file name "testbench.sp (-) - Lab6 %".

### 3-3. 請截取 WaveView 中 C、D 及 out\_3 的波形



### 4. 結論/建議 (可寫可不寫，不影響作業評分，僅做為下次上課方式的參考)