

National Cheng Kung University

Department of Electrical Engineering

Introduction to VLSI CAD (Spring 2023)

Lab Session 7

SOM

Name	Student ID	Contribution ratio
曲致駿	E94096306	30%
陳慕丞	E94096097	70%
Check list		
Part	Points	Marks(Y/N)
Lab7_1 RTL pass	10	Y
Lab7_1 SYN pass	15	Y
Lab7_2 RTL pass	10	Y
Lab7_2 SYN pass	15	Y
Superlint >= 90%	5	Y
Simple baseline	10	Y
Strong baseline	5	Y
Boss baseline	5	Y

DEADLINE 4/26(三) 23:59

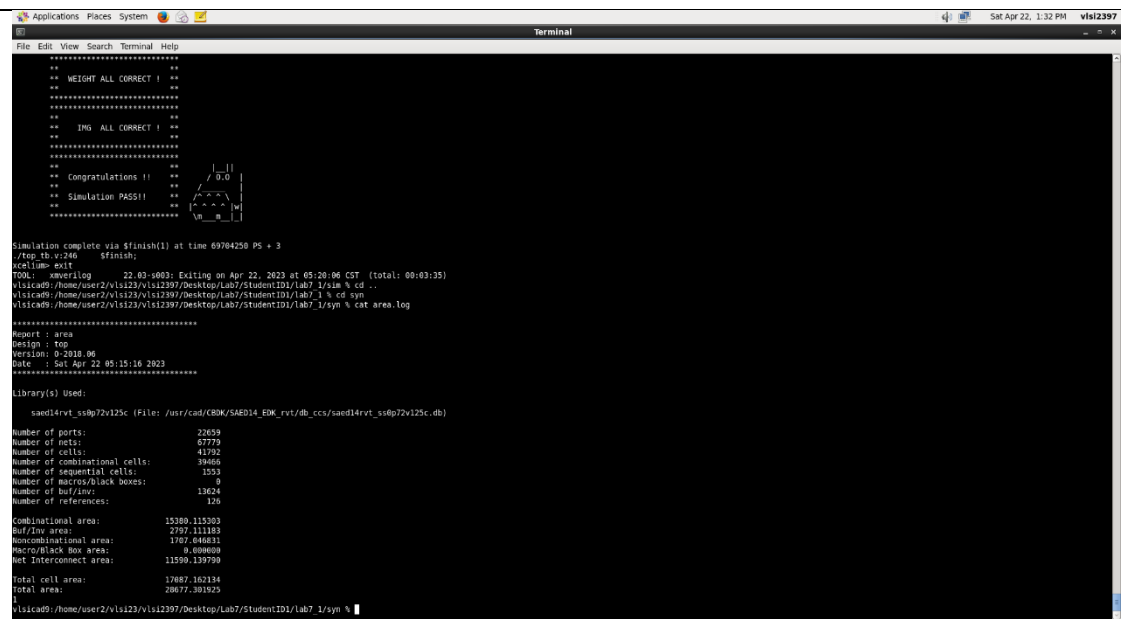
(1) Lab7_1 PA result : (must fill your PA, otherwise PA will get 0 grade)

Lab7_1					
CYCLE(ns)	Tb0(ns)	Tb1(ns)	Tb2(ns)	Tb3(ns)	Area(um^2)
8.5	69704.25	69704.25	69704.25	69704.25	17087
PA = (tb0+tb1+tb2+tb3)*area			4764146079		

(2) Show area.log screenshot, need to reveal total cell area.

Lab7_1

area.log



```

*****
** WEIGHT ALL CORRECT ! **
**                               **
*****
** IMG ALL CORRECT ! **
**                               **
*****
**                               **
** Congratulations !! **
**                               **
** Simulation PASS!! **
**                               **
*****
Simulation complete via $finish(1) at time 69704250 P5 + 3
./top_tb.v:240 $finish;
xcltmm exit
TOOL: xmerilog 22.03-s003; Exiting on Apr 22, 2023 at 05:20:06 CST (total: 00:03:35)
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/Lab7_1/vim % cd ..
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/Lab7_1 % cd syn
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/Lab7_1/syn % cat area.log
*****
Report = area
Design = top
Version: 0-2018.06
Date = Sat Apr 22 05:15:16 2023
*****
Library(s) Used:
    saed14rvt_ss0p72v125c (File: /usr/cad/CEM/SAB014_EIM_rvt/db_ccs/saed14rvt_ss0p72v125c.db)
Number of ports: 22838
Number of nets: 67779
Number of cells: 41792
Number of combinational cells: 39466
Number of sequential cells: 1553
Number of macros/black boxes: 0
Number of buffers: 13624
Number of references: 126
Combinational area: 15380.115303
Buf/Inv area: 2797.111183
Noncombinational area: 1707.646831
Macro/Black box area: 0.609060
Net Interconnect area: 11590.139799
Total cell area: 17887.162134
Total area: 26877.301925
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/Lab7_1/syn %

```

RTL tb0

```
Applications Places System
Terminal
File Edit View Search Terminal Help
xcelab: %MEMMODR (/top tb.v,165|36): $readmem default memory order incompatible with IEEE1364.
$readmemh('GOLDEN WEIGHT, golden_weight);
xcelab: %MEMMODR (/top tb.v,166|42): $readmem default memory order incompatible with IEEE1364.
Building instance overlay tables: ..... Done
Generating native compiled code:
worklib.controller.v <@x3486659>
streams: 9, words: 4522
worklib.top.tb.v <@x7c8e96d>
streams: 10, words: 24480
worklib.W5C.v <@x3486659>
streams: 7, words: 5143
worklib.top.v <@x7b4c25d>
streams: 14, words: 3971
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 71 6
Registers: 288 28
Scalar wires: 16 -
Expanded wires: 640 64
Vectored wires: 1677 -
Always blocks: 273 15
Initial blocks: 5 5
Cont. assignments: 905 45
Pseudo assignments: 68 5
Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.top.tb.v
Loading snapshot worklib.top.tb.v ..... Done
%Verdi* Loading libscore lvs122.so
xcelium- source /usr/cad/cadence/XCELIUM/XCELIUM 22.03.003/tools/xcelium/files/xmsinc
xcelium- run
*****
** WEIGHT ALL CORRECT ! **
**
*****
** IMG ALL CORRECT ! **
**
*****
**
**
** Congratulations !! **
**
** Simulation PASS!! **
**
*****
Simulation complete via $finish(1) at time 69712750 PS + 2
/top.tb.v:246 $finish;
xcelium- exit
TOOL: xmvcrlog 22.03-s003: Exiting on Apr 22, 2023 at 05:41:26 CST (total: 00:00:02)
vlsicad9:/home/user2/vls123/vls12397/Desktop/Lab7/StudentID1/Lab7_1/sim %
Terminal [lab7_1] [area_syn_00.png]
```

RTL tb1

```
Applications Places System
Terminal
File Edit View Search Terminal Help
module worklib.top.tb.v
errors: 0, warnings: 0
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
$readmemh('GOLDEN PIC, golden_pic);
xcelab: %MEMMODR (/top tb.v,165|36): $readmem default memory order incompatible with IEEE1364.
$readmemh('GOLDEN WEIGHT, golden_weight);
xcelab: %MEMMODR (/top tb.v,166|42): $readmem default memory order incompatible with IEEE1364.
Building instance overlay tables: ..... Done
Generating native compiled code:
worklib.top.tb.v <@x7c8e96d>
streams: 10, words: 24483
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 71 6
Registers: 288 28
Scalar wires: 16 -
Expanded wires: 640 64
Vectored wires: 1677 -
Always blocks: 273 15
Initial blocks: 5 5
Cont. assignments: 905 45
Pseudo assignments: 68 5
Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.top.tb.v
Loading snapshot worklib.top.tb.v ..... Done
%Verdi* Loading libscore lvs122.so
xcelium- source /usr/cad/cadence/XCELIUM/XCELIUM 22.03.003/tools/xcelium/files/xmsinc
xcelium- run
*****
** WEIGHT ALL CORRECT ! **
**
*****
** IMG ALL CORRECT ! **
**
*****
**
**
** Congratulations !! **
**
** Simulation PASS!! **
**
*****
Simulation complete via $finish(1) at time 69704250 PS + 2
/top.tb.v:246 $finish;
xcelium- exit
TOOL: xmvcrlog 22.03-s003: Exiting on Apr 22, 2023 at 05:41:37 CST (total: 00:00:02)
vlsicad9:/home/user2/vls123/vls12397/Desktop/Lab7/StudentID1/Lab7_1/sim %
Terminal [lab7_1] [area_syn_00.png] Save Screenshot
```

RTL tb1

RTL tb2

```

Applications Places System
Terminal
File Edit View Search Terminal Help
module worklib_top tb_v
  errors: 0, warnings: 0
  Caching library 'worklib' ..... Done
  Elaborating the design hierarchy:
  $readmemh("GOLDEN_PIC", golden_pic);
  |
xmelab: "W_MEMODR (/top tb.v,165|36): $readmem default memory order incompatible with IEEE1364.
  $readmemh("GOLDEN_WEIGHT", golden_weight);
  |
xmelab: "W_MEMODR (/top tb.v,166|42): $readmem default memory order incompatible with IEEE1364.
  Building instance overlay tables: ..... Done
  Generating native compiled code:
  worklib_top.tb_v <=768c96d>
  streams: 10, words: 24486
  Building instance specific data structures.
  Loading native compiled code: ..... Done
  Design hierarchy summary:
  Instances Unique
  Modules: 71 6
  Registers: 288 28
  Scalar wires: 16 -
  Expanded wires: 640 64
  Vectored wires: 1677 -
  Always blocks: 273 15
  Initial blocks: 5 5
  Cont. assignments: 905 45
  Pseudo assignments: 68 5
  Simulation timescale: 10ps
  Writing initial simulation snapshot: worklib_top.tb_v
Loading snapshot worklib_top.tb_v ..... Done
*Verdi* Loading libsscore lib152.so
xcelium> source /usr/cad/cadence/XCELIUM/XCELIUM_22.03.003/tools/xcelium/files/xmsimrc
xcelium> run
*****
** **
** WEIGHT ALL CORRECT ! **
** **
*****
** **
** IMG ALL CORRECT ! **
** **
*****
** **
** Congratulations !! **
** **
** Simulation PASS!! **
** [ ^ ^ ^ ^ ] **
** \ m m / **
*****
Simulation complete via $finish(1) at time 69704250 PS + 2
./top.tb.v:246 $finish;
xcelium> exit
T00L: xmvcrlog 22.03-s003: Exiting on Apr 22, 2023 at 05:43:13 CST (total: 00:00:02)
vlsicad9:/home/user2/Vlsi23/Vlsi2397/Desktop/Lab7/StudentID/Lab7_1/sim %
Terminal [lab7_1] [area syn 0d.png] Save Screenshots

```

RTL tb3

```

Applications Places System
Terminal
Sat Apr 22, 1:52 PM vlsi2397

File Edit View Search Terminal Help

module worklib.top tbv
  errors: 0, warnings: 0
  Caching library 'worklib' ..... Done
  Elaborating the design hierarchy:
  $readmemh('GOLDEN_PIC', golden_pic);
  $readmemh('GOLDEN_WEIGHT', golden_weight);
  |
  |
xmelab: 'W_MEMMODR (/top.tb.v,165|36): $readmem default memory order incompatible with IEEE1364.
  $readmemh('GOLDEN_WEIGHT', golden_weight);
  |
  |
xmelab: 'W_MEMMODR (/top.tb.v,166|42): $readmem default memory order incompatible with IEEE1364.
  Building instance overlay tables: ..... Done
  Generating native compiled code: ..... Done
  worklib.top.tb.v: <0x7c8c96d>
  streams: 10, words: 24486
  Building instance specific data structures.
  Loading native compiled code: ..... Done
  Design hierarchy summary:
  Modules:          Instances  Unique
  Registers:        288        28
  Scalar wires:     16         -
  Expanded wires:   640        64
  Vectors wires:    1677       -
  Always blocks:    273        15
  Initial blocks:   5          5
  Cont. assignments: 985        45
  Pseudo assignments: 68        5
  Simulation timescale: 10ps
  Writing initial simulation snapshot: worklib.top.tb.v
  Loading snapshot worklib.top.tb.v ..... Done
*Verdi* Loading Libscore Jns152.so
xcelium: source /usr/cad/cadence/XCELIUM/XCELIUM_22.03.003/tools/xcelium/files/xmsinrc
xcelium: run
*****
**                               **
**  WEIGHT ALL CORRECT !  **
**                               **
*****
**                               **
**  IMG ALL CORRECT !  **
**                               **
*****
**                               **
**                               **
**  Congratulations !!  **
**                               **
**  Simulation PASS!!  **
**                               **
*****
          | |
          / 0.0 |
          / ^ ^ ^ |
          \ ^ ^ ^ |w|
          \a  a |
*****

Simulation complete via $finish(1) at time 69704250 PS + 2
./top.tb.v:246 $finish;
xcelium: exit
TOOL: xmvcrilog 22.03-s003: Exiting on Apr 22, 2023 at 05:43:29 CST (total: 00:00:02)
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/Lab7_1/sim %

Terminal [lab7_1] [area_syn_00.png] [Save Screenshot]

```

SYN tb0

```
Applications Places System Terminal
File Edit View Search Terminal Help
xmelab: *W.UDPRTD (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15624|2): UDP table entry is redundant.
f ? ? ? ? : ? : - :
xmelab: *W.UDPRTD (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15643|2): UDP table entry is redundant.
f ? ? ? ? : ? : - :
xmelab: *W.UDPRTD (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15662|2): UDP table entry is redundant.
buf MCM_B6_0(QN, ION);
xmelab: *W.CSINF1 (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.13767|23): implicit wire has no fanin (SAEDRVTI4_LDPRSQB_1.SAEDRVTI4_LDPRSQB_1_inst.IQN).
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 84497 2043
UDPs: 1958 38
Primitives: 203969 4
Timing outputs: 46232 835
Registers: 26 56
Scalar wires: 53517 -
Expanded wires: 26 2
Vectored wires: 2 -
Always blocks: 11 5
Initial blocks: 6 6
Cont. assignments: 96 7188
Pseudo assignments: 2 2
Timing checks: 35678 4813
Interconnect: 100836 47869
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.SAEDRVTI4_F5DM_V2_0P5_func.v
Loading snapshot worklib.SAEDRVTI4_F5DM_V2_0P5_func.v ..... Done
*Verdi* Loading libscore ius152.sp
xcelium> source /usr/cad/cadence/XCELIUM/XCELIUM_22.03.003/tools/xcelium/files/xsimrc
xcelium> run
*****
** **
** WEIGHT ALL CORRECT ! **
** **
*****
** **
** IMG ALL CORRECT ! **
** **
*****
** **
** Congratulations !! **
** **
** Simulation PASS!! **
** **
*****
Simulation complete via $finish(1) at time 69712750 PS + 3
./top.tb.v:246 $finish;
xcelium> exit
TOOL: xmvverilog 22.03-s003: Exiting on Apr 22, 2023 at 05:40:24 CST (total: 00:03:58)
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/lab7_1/sim %
```

SYN tb1

```
Applications Places System Terminal
File Edit View Search Terminal Help
xmelab: *W.UDPRTD (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15624|2): UDP table entry is redundant.
f ? ? ? ? ? : ? : - :
xmelab: *W.UDPRTD (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15643|2): UDP table entry is redundant.
f ? ? ? ? ? : ? : - :
xmelab: *W.UDPRTD (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15662|2): UDP table entry is redundant.
buf MCM_B6_0(QN, ION);
xmelab: *W.CSINF1 (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.13767|23): implicit wire has no fanin (SAEDRVTI4_LDPRSQB_1.SAEDRVTI4_LDPRSQB_1_inst.IQN).
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 84497 2043
UDPs: 1958 38
Primitives: 203969 4
Timing outputs: 46232 835
Registers: 26 56
Scalar wires: 53518 -
Expanded wires: 26 2
Vectored wires: 2 -
Always blocks: 11 5
Initial blocks: 6 6
Cont. assignments: 96 7188
Pseudo assignments: 2 2
Timing checks: 35678 4813
Interconnect: 100836 47869
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.SAEDRVTI4_F5DM_V2_0P5_func.v
Loading snapshot worklib.SAEDRVTI4_F5DM_V2_0P5_func.v ..... Done
*Verdi* Loading libscore ius152.sp
xcelium> source /usr/cad/cadence/XCELIUM/XCELIUM_22.03.003/tools/xcelium/files/xsimrc
xcelium> run
*****
** **
** WEIGHT ALL CORRECT ! **
** **
*****
** **
** IMG ALL CORRECT ! **
** **
*****
** **
** Congratulations !! **
** **
** Simulation PASS!! **
** **
*****
Simulation complete via $finish(1) at time 69704250 PS + 3
./top.tb.v:246 $finish;
xcelium> exit
TOOL: xmvverilog 22.03-s003: Exiting on Apr 22, 2023 at 05:35:47 CST (total: 00:03:56)
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/lab7_1/sim %
```

SYN tb2

Applications Places System

Terminal

Sat Apr 22, 1:40 PM visl2397

File Edit View Search Terminal Help

xmelab: *W_UDPRDT (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,15624[2]): UDP table entry is redundant.
f ? ? ? ? : ? : - ;
|
xmelab: *W_UDPRDT (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,15643[2]): UDP table entry is redundant.
f ? ? ? ? : ? : - ;
|
xmelab: *W_UDPRDT (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,15662[2]): UDP table entry is redundant.
buf MGH BG 0(ON, IQN);
|
xmelab: *W_CSINF1 (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,13767[23]): implicit wire has no fanin (SAEDRVIT14_LDPRSQB_1.SAEDRVIT14_LDPRSQB_1_inst.IQN).
Loading native compiled code: Done
Design hierarchy summary:


Modules:	Instances	Unique
UDPs:	1958	38
Primitives:	283969	4
Timing outputs:	46232	835
Registers:	26	56
Scalar wires:	53518	-
Expanded wires:	26	2
Vectored wires:	2	-
Always blocks:	11	5
Initial blocks:	6	6
Cont. assignments:	96	7188
Pseudo assignments:	2	2
Timing checks:	35678	4813
Interconnect:	108636	47869
Simulation timescale:	1ps	

Writing initial simulation snapshot: worklib.SAEDRVIT14_FSDN_V2_0P5_func.v
Loading snapshot worklib.SAEDRVIT14_FSDN_V2_0P5_func.v Done
Verdi Loading libscore ius152.so
xcelium> source /usr/cad/cadence/XCELIUM/XCELIUM_22.03.003/tools/xcelium/files/xmsimrc
xcelium> run

** WEIGHT ALL CORRECT ! **
**

** IMG ALL CORRECT ! **
**

** Congratulations !! **
** Simulation PASS!! **


Simulation complete via \$finish(1) at time 69704250 PS + 3
./top.tb.v:246 \$finish;
xcelium> exit
TOOLS: xsverilog 22.03-003: Exiting on Apr 22, 2023 at 05:30:36 CST (total: 00:03:57)
visl2397: /home/user2/vl2397/visl2397/Desktop/Lab7/StudentID1/lab7_1/sim %

Terminal [Terminal] lab7_1 [area_syn_00.png]

SYN tb3

Applications Places System

Terminal

Sat Apr 22, 1:33 PM visl2397

File Edit View Search Terminal Help

xmelab: *W_UDPRDT (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,15605[2]): UDP table entry is redundant.
f ? ? ? ? : ? : - ;
|
xmelab: *W_UDPRDT (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,15624[2]): UDP table entry is redundant.
f ? ? ? ? : ? : - ;
|
xmelab: *W_UDPRDT (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,15643[2]): UDP table entry is redundant.
f ? ? ? ? : ? : - ;
|
xmelab: *W_UDPRDT (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,15662[2]): UDP table entry is redundant.
buf MGH BG 0(ON, IQN);
|
xmelab: *W_CSINF1 (/usr/cad/CBDK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v,13767[23]): implicit wire has no fanin (SAEDRVIT14_LDPRSQB_1.SAEDRVIT14_LDPRSQB_1_inst.IQN).
Loading native compiled code: Done
Design hierarchy summary:


Modules:	Instances	Unique
UDPs:	1958	38
Primitives:	283969	4
Timing outputs:	46232	835
Registers:	26	56
Scalar wires:	53518	-
Expanded wires:	26	2
Vectored wires:	2	-
Always blocks:	11	5
Initial blocks:	6	6
Cont. assignments:	96	7188
Pseudo assignments:	2	2
Timing checks:	35678	4813
Interconnect:	108636	47869
Simulation timescale:	1ps	

Writing initial simulation snapshot: worklib.SAEDRVIT14_FSDN_V2_0P5_func.v
Loading snapshot worklib.SAEDRVIT14_FSDN_V2_0P5_func.v Done
Verdi Loading libscore ius152.so
xcelium> source /usr/cad/cadence/XCELIUM/XCELIUM_22.03.003/tools/xcelium/files/xmsimrc
xcelium> run

** WEIGHT ALL CORRECT ! **
**

** IMG ALL CORRECT ! **
**

** Congratulations !! **
** Simulation PASS!! **


Simulation complete via \$finish(1) at time 69704250 PS + 3
./top.tb.v:246 \$finish;
No Items in Trash

Terminal [Terminal] lab7_1 [area_syn_00.png]

Lab7_2

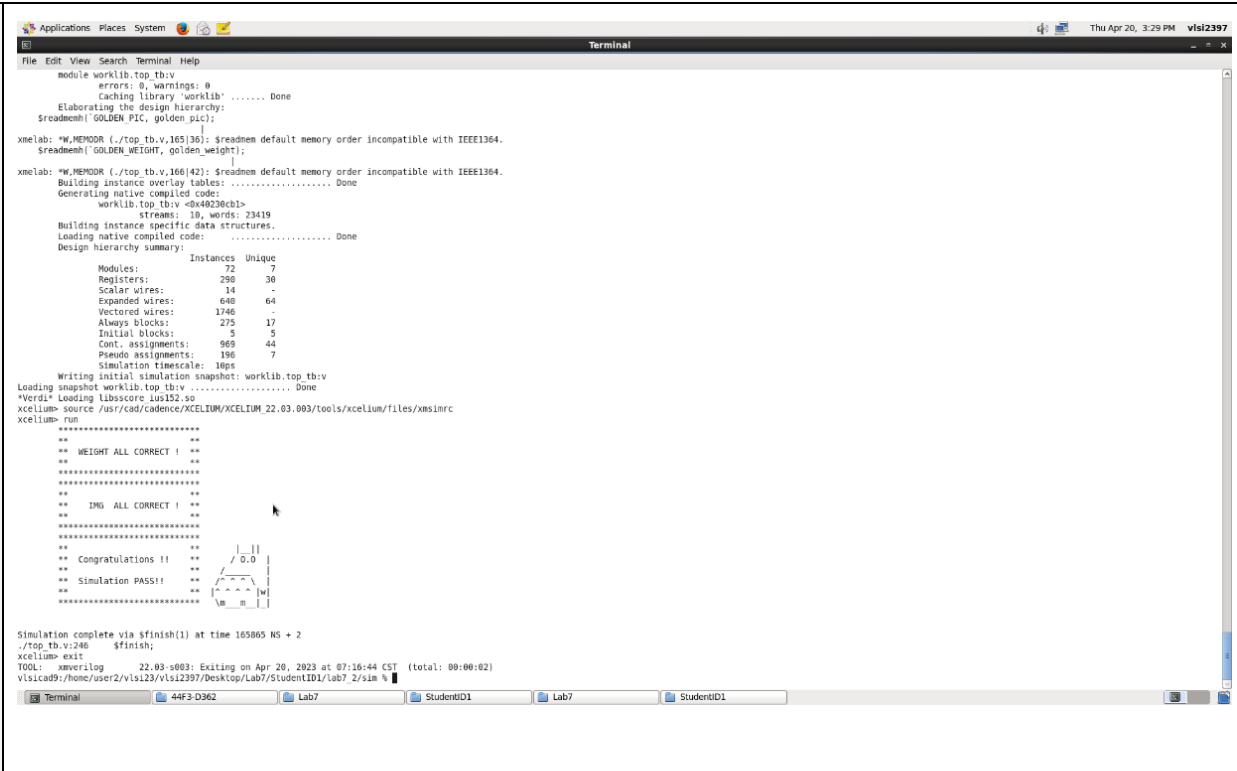
RTL tb0

```
Applications Places System
Terminal
File Edit View Search Terminal Help
xmelab: %MEMODR (./top tb.v,166[42]): $readmem default memory order incompatible with IEEE1364.
Building instance overlay tables: ..... Done
Generating native compiled code: ..... Done
worklib.fsr.v <8x22cfc3>
streams: 3, words: 1786
worklib.controller.v <8x2b12386>
streams: 5, words: 4752
worklib.top.tb.v <8x48238cb1>
streams: 18, words: 23413
worklib.wsc.v <8x34a86c5>
streams: 7, words: 4677
worklib.top.v <8x7e68091>
streams: 19, words: 6806
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Modules: 72 7
Registers: 290 30
Scalar wires: 14 -
Expanded wires: 640 64
Vectored wires: 1746 -
Always blocks: 275 17
Initial blocks: 5 5
Cont. assignments: 969 44
Pseudo assignments: 196 7
Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.top.tb.v
Loading snapshot worklib.top.tb.v ..... Done
*Verdi* Loading libscore_ius152.so
xcelium source /usr/cad/cadence/XCELIUM/XCELIUM 22.03.003/tools/xcelium/files/xmsimrc
xcelium run
*****
** WEIGHT ALL CORRECT ! **
**
*****
** IMG ALL CORRECT ! **
**
*****
** Congratulations !! **
**
** Simulation PASS!! **
**
*****
Simulation complete via $finish(1) at time 165865 NS + 2
./top.tb.v:246 $finish;
xcelium exit
TOOL: xmvcrillog 22.03-s003: Exiting on Apr 20, 2023 at 07:16:17 CST (total: 00:00:03)
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/Lab7_2/sim %
```

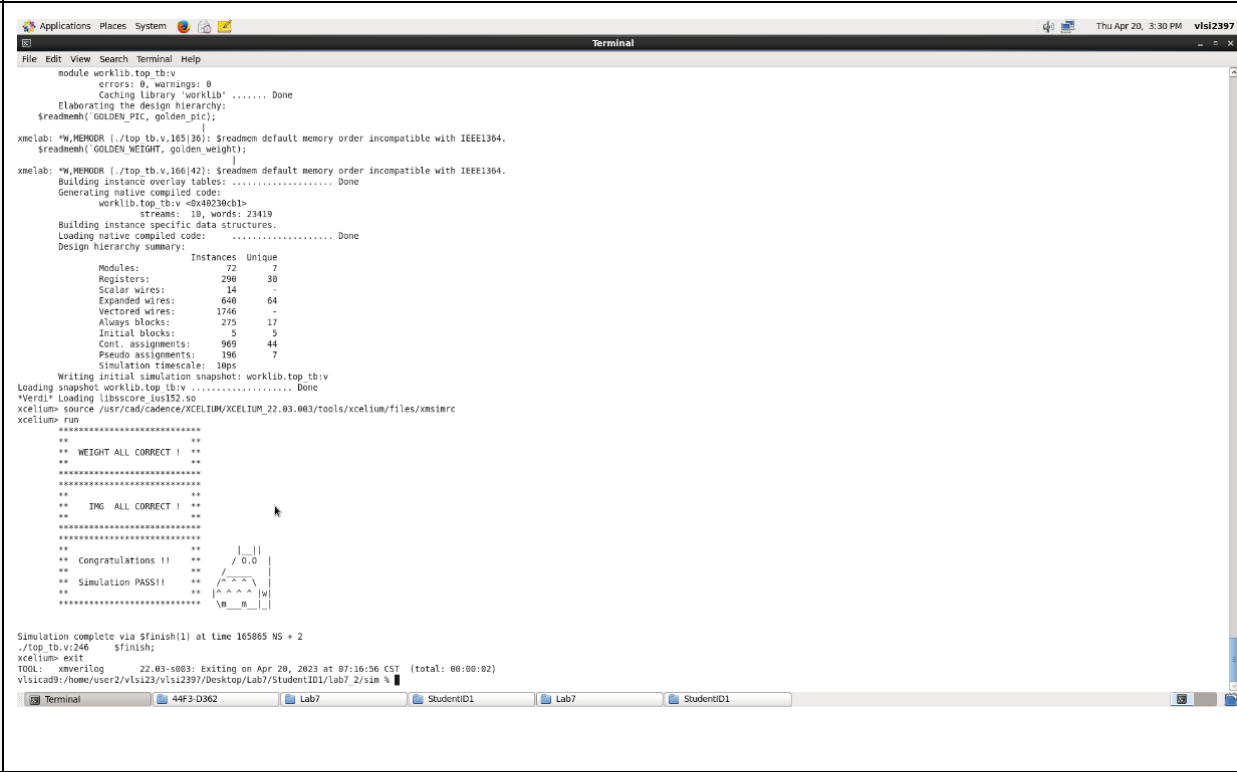
RTL tb1

```
Applications Places System
Terminal
File Edit View Search Terminal Help
module worklib.top.tb.v
errors: 0, warnings: 0
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
$readmem('GOLDEN.PIC, golden.pic);
xmelab: %MEMODR (./top tb.v,165[30]): $readmem default memory order incompatible with IEEE1364.
$readmem('GOLDEN.WEIGHT, golden.weight);
xmelab: %MEMODR (./top tb.v,166[42]): $readmem default memory order incompatible with IEEE1364.
Building instance overlay tables: ..... Done
Generating native compiled code: ..... Done
worklib.top.tb.v <8x48238cb1>
streams: 10, words: 23416
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Modules: 72 7
Registers: 290 30
Scalar wires: 14 -
Expanded wires: 640 64
Vectored wires: 1746 -
Always blocks: 275 17
Initial blocks: 5 5
Cont. assignments: 969 44
Pseudo assignments: 196 7
Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.top.tb.v
Loading snapshot worklib.top.tb.v ..... Done
*Verdi* Loading libscore_ius152.so
xcelium source /usr/cad/cadence/XCELIUM/XCELIUM 22.03.003/tools/xcelium/files/xmsimrc
xcelium run
*****
** WEIGHT ALL CORRECT ! **
**
*****
** IMG ALL CORRECT ! **
**
*****
** Congratulations !! **
**
** Simulation PASS!! **
**
*****
Simulation complete via $finish(1) at time 165865 NS + 2
./top.tb.v:246 $finish;
xcelium exit
TOOL: xmvcrillog 22.03-s003: Exiting on Apr 20, 2023 at 07:16:30 CST (total: 00:00:02)
vlsicad9:/home/user2/vlsi23/vlsi2397/Desktop/Lab7/StudentID1/Lab7_2/sim %
```

RTL tb2



RTL tb3



SYN tb0

ApplicationsPlacesSystem

Terminal

File Edit View Search Terminal Help

xmelab: *W_UDPRODT (/usr/cad/CBOK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15624|2): UDP table entry is redundant.
f ? ? ? ? ? : - ;
|
xmelab: *W_UDPRODT (/usr/cad/CBOK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15643|2): UDP table entry is redundant.
f ? ? ? ? ? : ? - ;
|
xmelab: *W_UDPRODT (/usr/cad/CBOK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15662|2): UDP table entry is redundant.
buf MGH_B6_0 QN, ION ;
|
xmelab: *W_CSINF1 (/usr/cad/CBOK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.13767|23): implicit wire has no fanin (SAEDRV14_LDPRSQB_1.SAEDRV14_LDPRSQB_1_inst.IQN).
Loading native compiled code: Done
Design hierarchy summary:

	Instances	Unique
Modules:	94319	2911
UDPs:	1999	38
Primitives:	212960	4
Timing outputs:	51838	867
Registers:	26	56
Scalar wires:	59275	-
Expanded wires:	26	2
Vectored wires:	2	-
Always blocks:	11	5
Initial blocks:	6	6
Cont. assignments:	138	8098
Pseudo assignments:	2	2
Timing checks:	36375	4888
Interconnect:	114891	53725
Simulation timescale:	1ps	

Writing initial simulation snapshot: worklib.SAEDRV14_FSDN_V2_0P5_func.v
Loading snapshot worklib.SAEDRV14_FSDN_V2_0P5_func.v Done
Verdi Loading libscore_1us152.s0
xcelium> source /usr/cad/cadence/XCELIUM/XCELIUM.22.03.003/tools/xcelium/files/xmsimrc
xcelium> run

**
** WEIGHT ALL CORRECT ! **
**

**
** IMG ALL CORRECT ! **
**

**
** Congratulations !! **
**
** Simulation PASS!! **
**

|_|
/ 0.0 |
/ ^ ^ ^ \ |
| ^ ^ ^ ^ |w|
|m m |
|_|
Simulation complete via \$finish(1) at time 165865 NS + 4
./top.tb.v:246 \$finish;
xcelium> exit
TOD: xneverilog 22.03+003: Exiting on Apr 20, 2023 at 07:34:12 CST (total: 00:03:17)
visicad6:/home/user2/vlsi23/vlsi23100/Lab7/StudentID1/Lab7_2/sin %
Terminal [controller (-/L... Terminal *<nWave:1> /h... [Terminal] visi23100 *<nWave:1> /h... (session_0) - ja... (session_0) - ja... Lab7 StudentID1

SYN tb1

ApplicationsPlacesSystem

Terminal

File Edit View Search Terminal Help

xmelab: *W_UDPRODT (/usr/cad/CBOK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15624|2): UDP table entry is redundant.
f ? ? ? ? ? : ? - ;
|
xmelab: *W_UDPRODT (/usr/cad/CBOK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15643|2): UDP table entry is redundant.
f ? ? ? ? ? : ? - ;
|
xmelab: *W_UDPRODT (/usr/cad/CBOK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.15662|2): UDP table entry is redundant.
buf MGH_B6_0 QN, ION ;
|
xmelab: *W_CSINF1 (/usr/cad/CBOK/SAED14_EDK_rvt/verilog/saed14nm_rvt.v.13767|23): implicit wire has no fanin (SAEDRV14_LDPRSQB_1.SAEDRV14_LDPRSQB_1_inst.IQN).
Loading native compiled code: Done
Design hierarchy summary:

	Instances	Unique
Modules:	94319	2911
UDPs:	1999	38
Primitives:	212960	4
Timing outputs:	51838	867
Registers:	26	56
Scalar wires:	59276	-
Expanded wires:	26	2
Vectored wires:	2	-
Always blocks:	11	5
Initial blocks:	6	6
Cont. assignments:	138	8098
Pseudo assignments:	2	2
Timing checks:	36375	4888
Interconnect:	114891	53725
Simulation timescale:	1ps	

Writing initial simulation snapshot: worklib.SAEDRV14_FSDN_V2_0P5_func.v
Loading snapshot worklib.SAEDRV14_FSDN_V2_0P5_func.v Done
Verdi Loading libscore_1us152.s0
xcelium> source /usr/cad/cadence/XCELIUM/XCELIUM.22.03.003/tools/xcelium/files/xmsimrc
xcelium> run

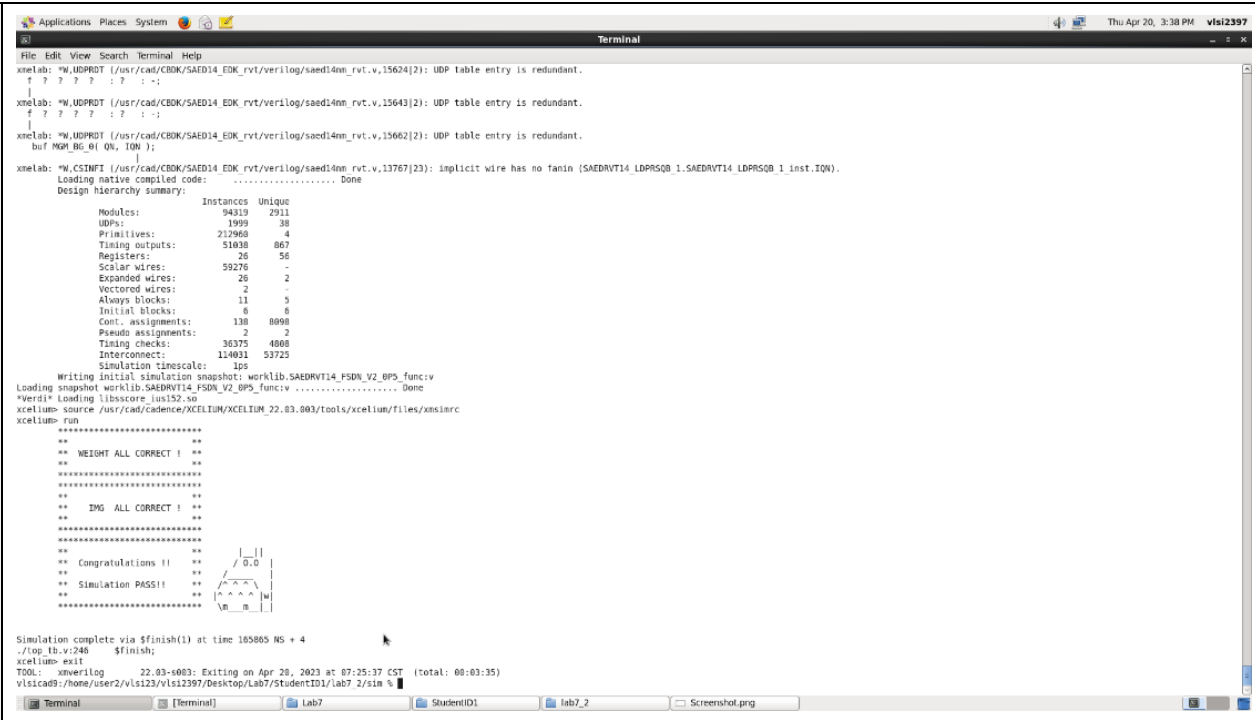
**
** WEIGHT ALL CORRECT ! **
**

**
** IMG ALL CORRECT ! **
**

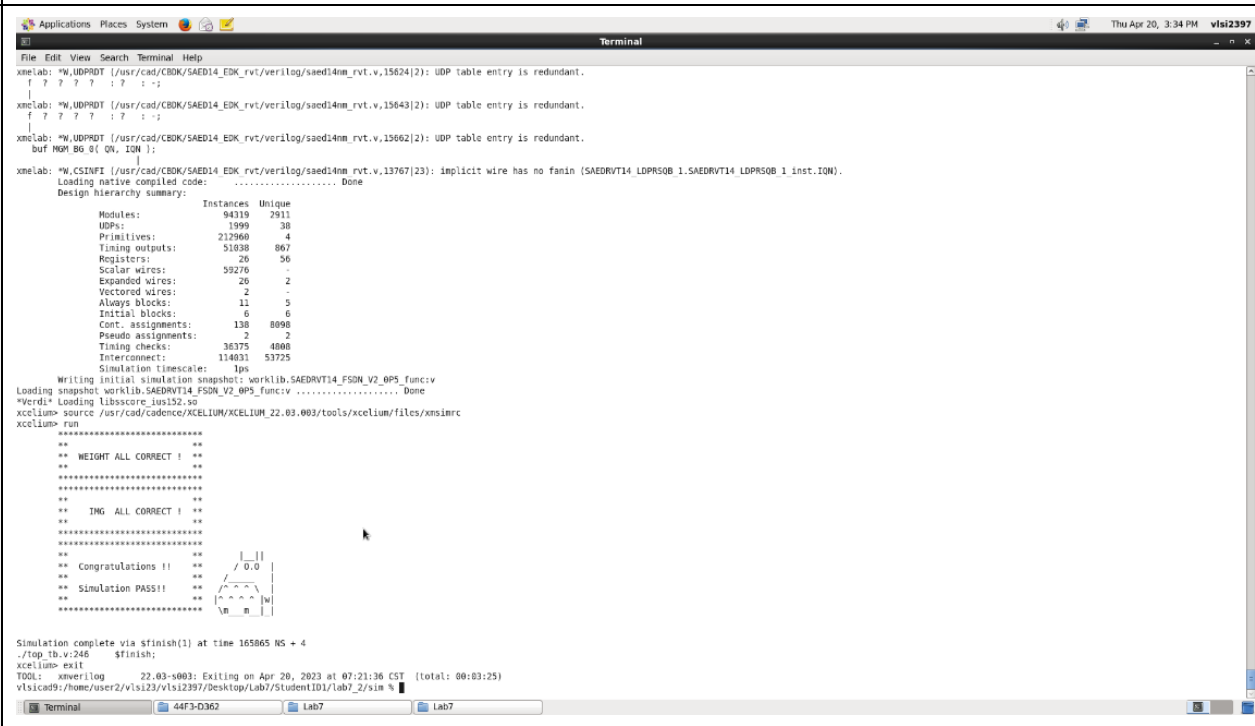
**
** Congratulations !! **
**
** Simulation PASS!! **
**

|_|
/ 0.0 |
/ ^ ^ ^ \ |
| ^ ^ ^ ^ |w|
|m m |
|_|
Simulation complete via \$finish(1) at time 165865 NS + 4
./top.tb.v:246 \$finish;
xcelium> exit
TOD: xneverilog 22.03+003: Exiting on Apr 20, 2023 at 07:38:55 CST (total: 00:03:10)
visicad6:/home/user2/vlsi23/vlsi23100/Lab7/StudentID1/Lab7_2/sin %
Terminal [controller v... Terminal *<nWave:1... [Terminal] visi23100 *<nWave:1... (session_0)... (session_0)... [Lab7] [StudentID1] 44F3-D362 Lab7

SYN tb2



SYN tb3











superlint

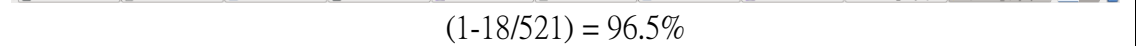
Lab7_1 TOOL: xmrerling 22.03-1603; Exitting on Apr 26, 2023 at 07:00:14 CST (total: 00:00:03)
 vsiscode:/home/user2/vls123/vls123100/Lab7/StudentID0/Lab7/1/sim & cd ...
 vsiscode:/home/user2/vls123/vls123100/Lab7/StudentID0/Lab7/1 \$ cd rtf/

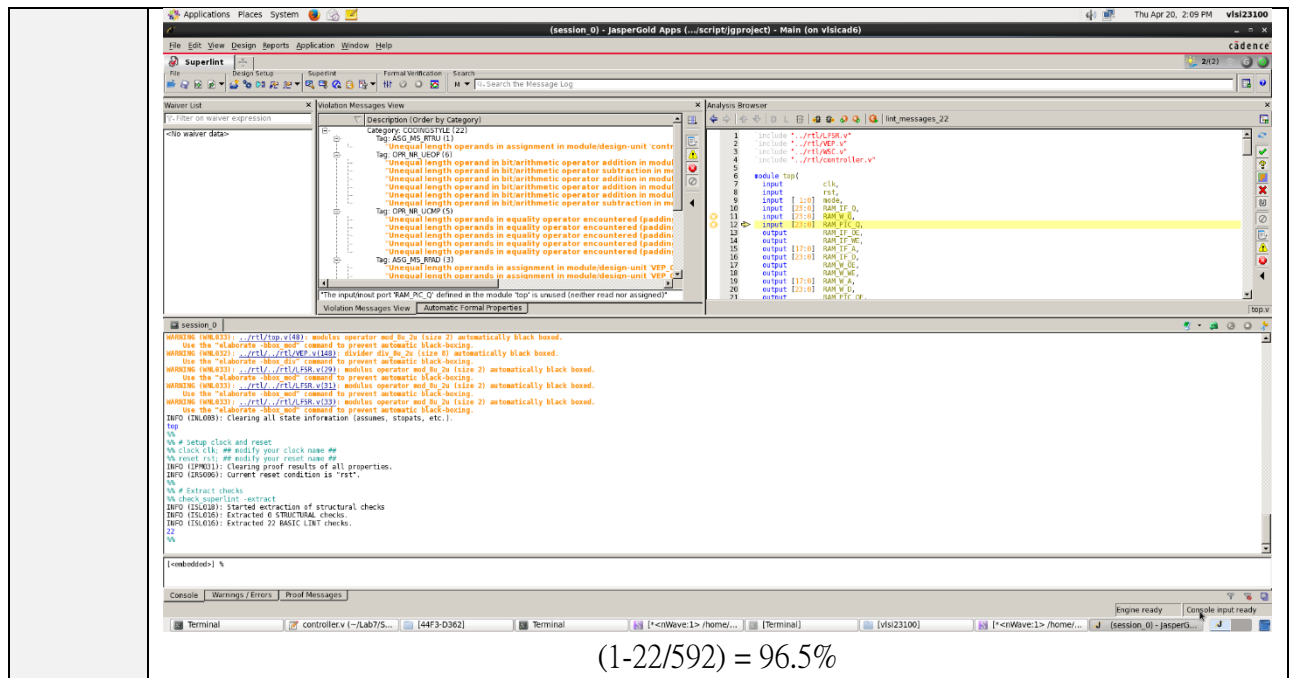
[illegible]

The screenshot shows a terminal window with the following command and output:

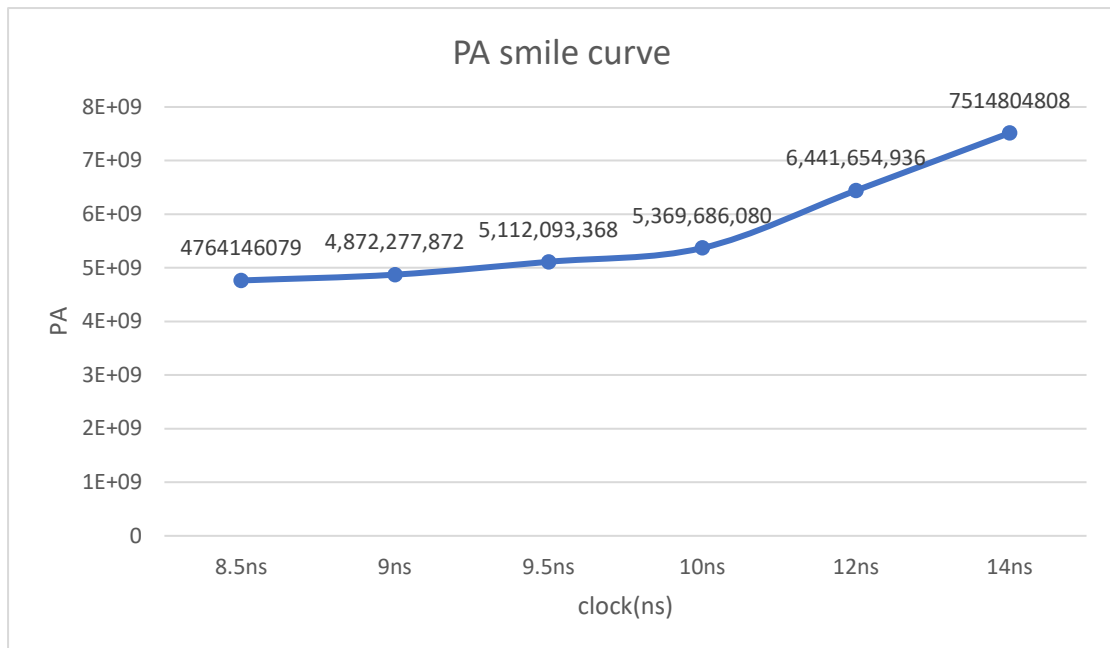
```
control@lv (~) [44F-D362] % jupyter lab --ip 0.0.0.0 --port 8888 --no-browser
[I 11:56:04.130] Starting JupyterLab application at http://0.0.0.0:8888/
[I 11:56:04.130] JupyterLab application started at http://0.0.0.0:8888/
```

Applications Places System                              

[illegible]



(5) Draw smile curve of your design



(6) Lessons learned

What is the Self-Organizing Map (SOM)?

In SOM, a set of neurons is arranged in a two-dimensional grid, and each neuron is associated with a weight vector. During the training process, the algorithm iteratively updates the weight vectors of the neurons based on the input data, which causes the neurons with similar weight vectors to be located close to each other in the output space. The neurons that are closest to the input data are called the "winning neurons," and they represent the input data in the output space. The weights of the neighboring neurons are also updated in a way that depends on a neighborhood function that decreases over time.

How we use Manhattan distance in this course?

In this course, the Manhattan distance is used as a measure of distance between the weight vectors of the neurons in the Self-Organizing Map (SOM) network and the input vectors. The Manhattan distance between two vectors is defined as the sum of the absolute differences between their corresponding components. In the context of SOM, it is used to find the neuron whose weight vector is closest to the input vector during both the training and inference phases. The neuron with the smallest Manhattan distance is called the winner neuron and is used to update its weight and the weights of its neighbors in the training phase, and to assign a value to the corresponding pixel in the output image in the inference phase.