**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2022)***

**Lab Session 3**

**Design of ALU and Fixed point Multiplication**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Student ID | | |
| 陳慕丞 | E94096097 | | |
| Practical Sections: | | Points | Marks |
| Prob A | | 20 |  |
| Prob B | | 30 |  |
| Prob C | | 30 |  |
| Report | | 15 |  |
| File hierarchy, naming…etc. | | 5 |  |
| Notes | | | |

**Due Date: 15:00, March 08, 2023 @ moodle**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** include source code in the paper report!

1. All homework requirements should be uploaded in this file hierarchy or you will not get the full credit.

NOTE: Please **DO NOT** upload waveforms!

1. Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
2. **If you upload a dead body which we can’t even compile you will get NO credit!**
3. **All Verilog file should get at least 90% superLint Coverage.**
4. **File hierarchy should not be changed; it may cause** your code can not be recompiled by TA successfully using the autograding commands

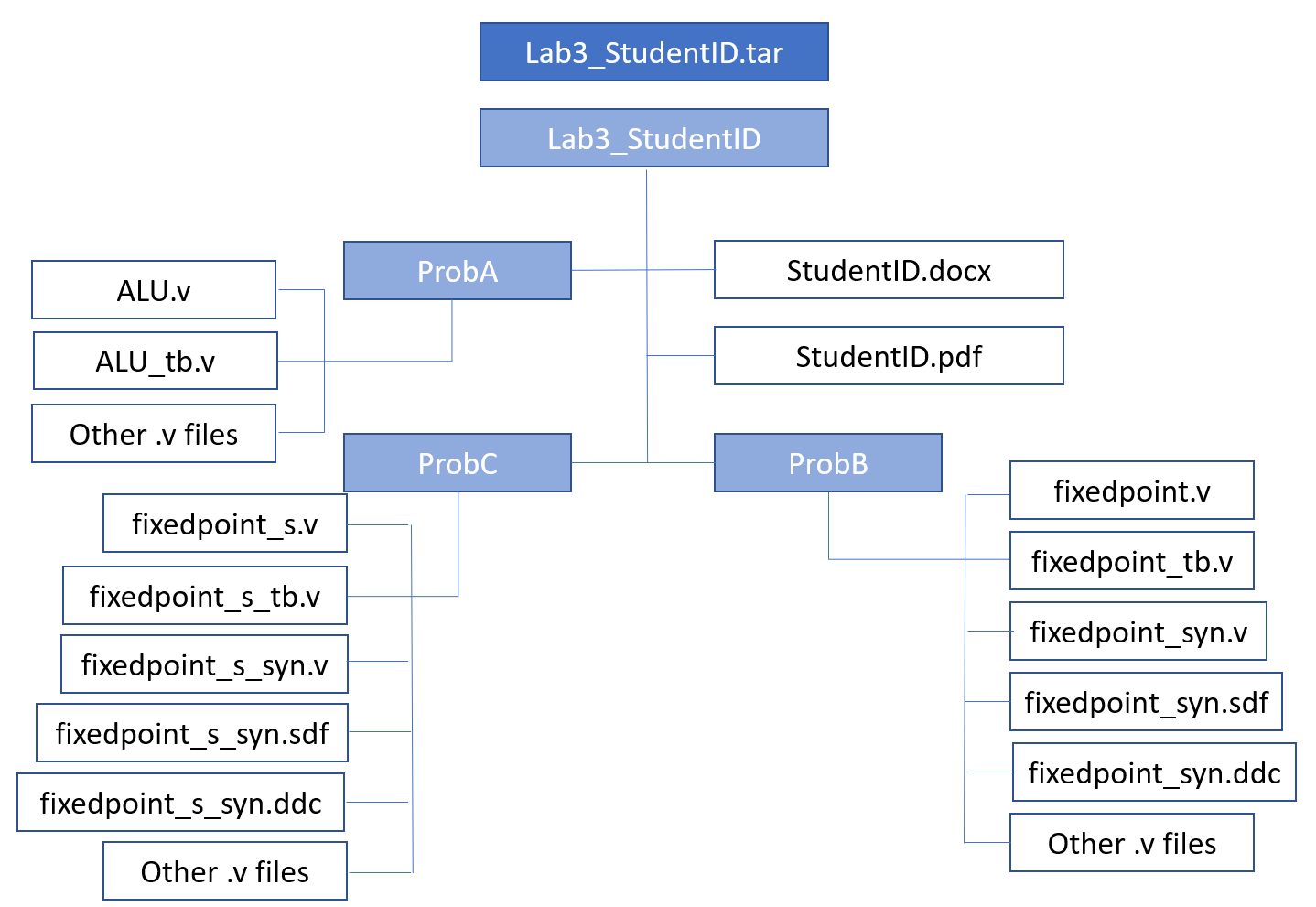
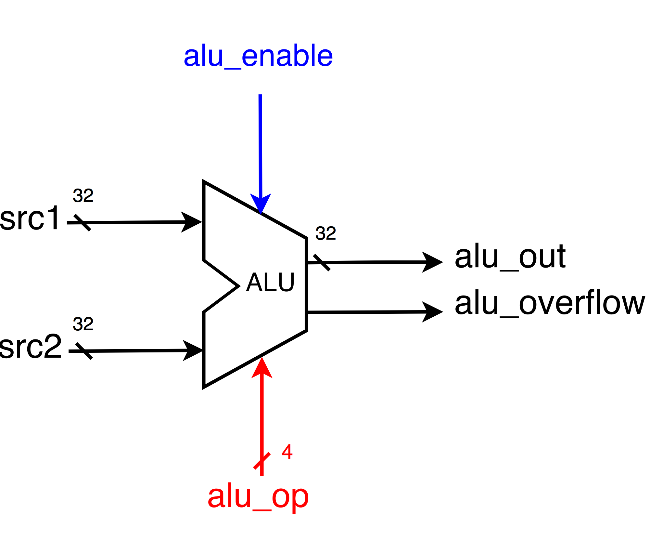


Fig.1 File hierarchy for Homework submission

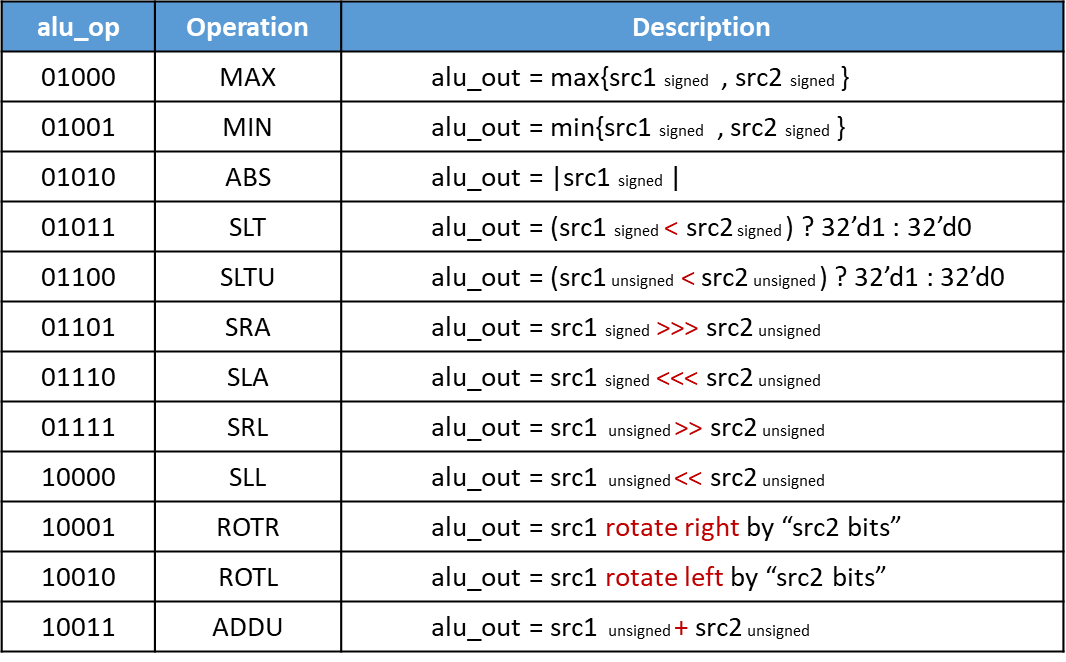
**Objectives:**

**Learn how to design an ALU.**

Prob A: Arithmetic Logic Unit



1. Based on the reference code, please implement the following operations.



* + **Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
|  |
| Your waveform : |
| Input:alu\_op,src1,src2  Output:alu\_overflow,alu\_out  src1\_s為src1轉成signed的wire; src2\_s為src2轉成signed的wire，當src1和src2訊號進來時src1\_s和src2\_s會馬上把值轉成signed的形式。  src1\_s\_add\_src2\_s為src1\_s加src2\_s的結果，也就是src1的signed形式加src2的signed形式; src1\_s\_sub\_src2\_s為src1\_s減src2\_s的結果，也就是src1的signed形式減src2的signed形式。  當alu\_op的值進來時，case判別要執行怎麼樣的運算，之後再利用src1,src2, src1\_s, src2\_s進行運算，alu\_out輸出結果，alu\_overflow則是在alu\_op=5’b00000(ADD), alu\_op=5’b00001(SUB), alu\_op=5’b10011(ADDU)時利用src1,src2, src1\_s, src2\_s, src1\_s\_add\_src2\_s, src1\_s\_sub\_src2\_s進行判別，最後輸出結果。 |
| SuperLint Coverage |
| Coverage:100% |

Prob B: Practice fixed point

**Design your Verilog code with the following specifications:** Number format: unsigned numbers.

* 1. The frame code and testbench are given. Follow the frame code to finish this homework. The decimal part should be rounded.
  2. Follow the PPT file to synthesize your code.

**After you synthesize your design, you may have some information about the circuit. Fill in the following form.**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **19.16** | **79.031998** |  |

**Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
| RTL:  Synthesis: |
| Your waveform (RTL & Synthesis) : |
| RTL:  Input:in1,in2  Output:out  raw\_result為in1\*in2的wire，而out利用raw\_result[7]判別是否輸出的raw\_result[15:8]需加1，最後輸出。  Synthesis:  在合成過後模擬時會出現out在值變換時波形不穩定的情形，如圖中圈起來所示，且變換時機明顯落後於input值的變化，此原因為電路在output前需要時間運算，且在運算時out的值會變換且不穩定。 |
| SuperLint Coverage |
| Coverage:92.31% |

Prob C: Practice fixed point (signed)

**Design your Verilog code with the following specifications:** Number format: signed numbers.

1. The frame code and testbench are given. Follow the frame code to finish this homework. The decimal part should be rounded.
2. Follow the PPT file to synthesize your code.

**After you synthesize your design, you may have some information about the circuit. Fill in the following form**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **18.94** | **98.701199** |  |

**Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
| RTL:  Synthesis: |
| Your waveform (RTL & Synthesis) : |
| RTL:  Input:in1,in2  Output:out  In1\_s為in1轉換成signed形式的wire；In2\_s為in2轉換成signed形式的wire； raw\_result\_s為in1\_s\*in2\_s的wire；raw\_result\_s\_twos為(~raw\_result\_s)+1的wire；raw\_result\_s\_twos\_add為raw\_result\_s\_twos[15:8]+1的wire；raw\_result\_s\_twos\_add\_twos為(~raw\_result\_s\_twos\_add)+1；zero為值為0的wire。  out利用raw\_result\_s\_twos[7], raw\_result\_s[7], raw\_result\_s和zero判別，若raw\_result\_s為負數且需進位，out為raw\_result\_s\_twos\_add\_twos；若raw\_result\_s為正數且需進位，out為raw\_result\_s[15:8]+1；其餘的out則為raw\_result\_s[15:8]。  Synthesis: |
| 在合成過後模擬時會出現圖中圈起來的部分在值變換時波形不穩定的情形，且變換時機明顯落後於input值的變化，此原因為電路在值到各個wire和output前需要時間運算，且在運算時各個wire和output的值會變換且不穩定。 |
| SuperLint Coverage |
| Coverage:96.43% |

**At last, please write the lessons learned from this lab session, or some suggestions for this lab session. Thank you.**

**在Lab3學到如何利用behavior level寫出combinational的電路，也學到ALU和fixed point的概念與實現方法，還有如何將寫完的電路正確的合成。**

Appendix A : Commands we will use to check your homework

|  |  |  |
| --- | --- | --- |
| **Problem** |  | **Command** |
| **ProbA** | Compile | % ncverilog ALU.v |
| Simulate | % ncverilog ALU\_tb.v +define+FSDB +access+r |
| **ProbB** | Compile | % ncverilog fixedpoint.v |
| Simulate | % ncverilog fixedpoint\_tb.v +define+FSDB +access+r |
| Synthesis | % ncverilog fixedpoint\_tb.v +define+FSDB+syn +access+r |
| ProbC | Compile | % ncverilog fixedpoint\_s.v |
| Simulate | % ncverilog fixedpoint\_s\_tb.v +define+FSDB +access+r |
| Synthesis | % ncverilog fixedpoint\_s\_tb.v +define+FSDB+syn +access+r |