**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2023)***

**Lab Session 4**

**Register Files, Manhattan Distance and LFSR**

|  |  |  |
| --- | --- | --- |
| Name | Student ID | |
| 陳慕丞 | E94096097 | |
| **Practical Sections** | **Points** | **Marks** |
| Prob A | 25 |  |
| Prob B | 25 |  |
| Prob C | 25 |  |
| Report | 15 |  |
| File hierarchy, naming…etc. | 5 |  |
| Superlint | 5 |  |
| Notes: | | |

**Due Date: 15:00, March 23, 2020 @ moodle**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** paste source code in the report!

1. Noted! TA will use commands in Appendix A to check your design in SoC Lab. If TA can not compile your code with the commands, you will not get full credit.
2. **If you upload a dead body which we can’t even compile, you will get NO credit!**
3. **All Verilog file should get at least 85% SuperLint Coverage.**
4. All homework requirements should be uploaded in this file hierarchy or you will not get full credit.

NOTE: Please **DO NOT** upload waveforms!

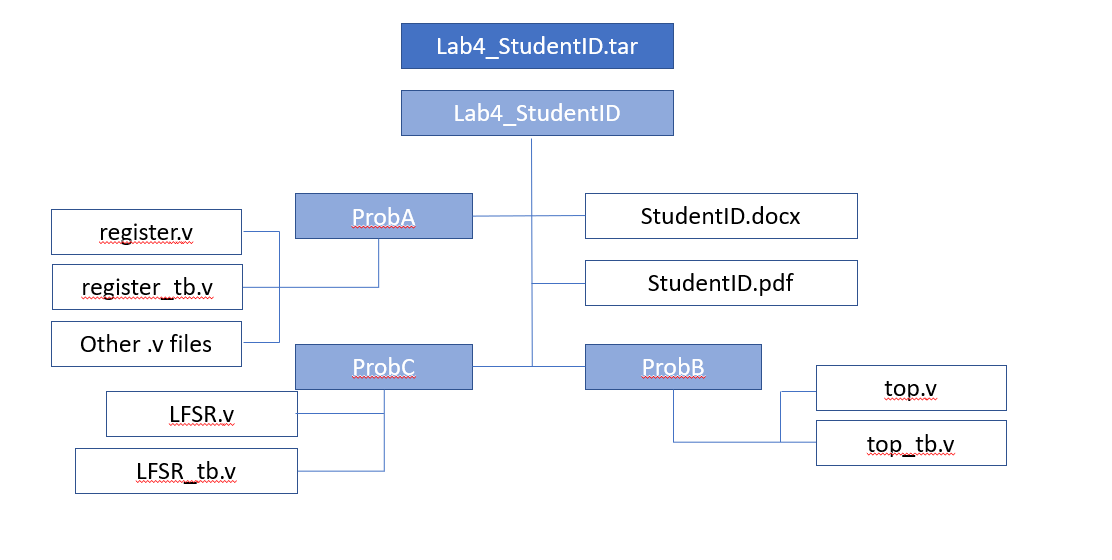
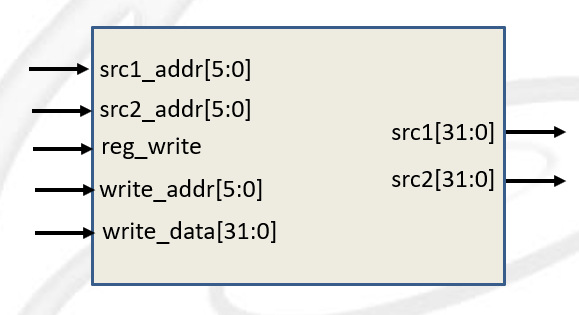
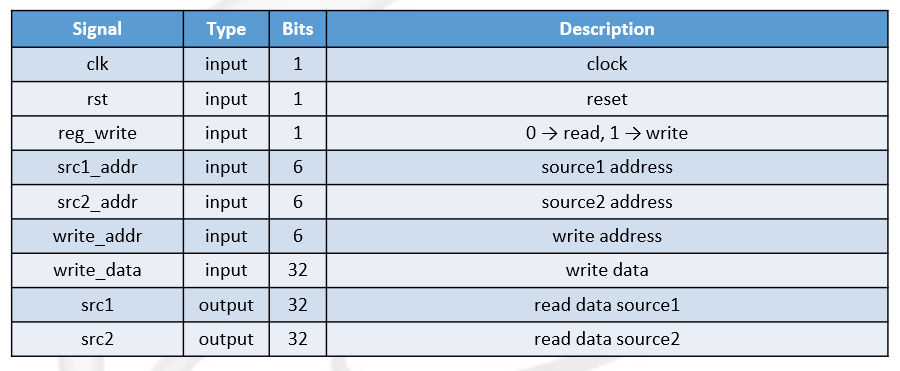


Fig.1 File hierarchy for Homework submission

Prob A: Register File



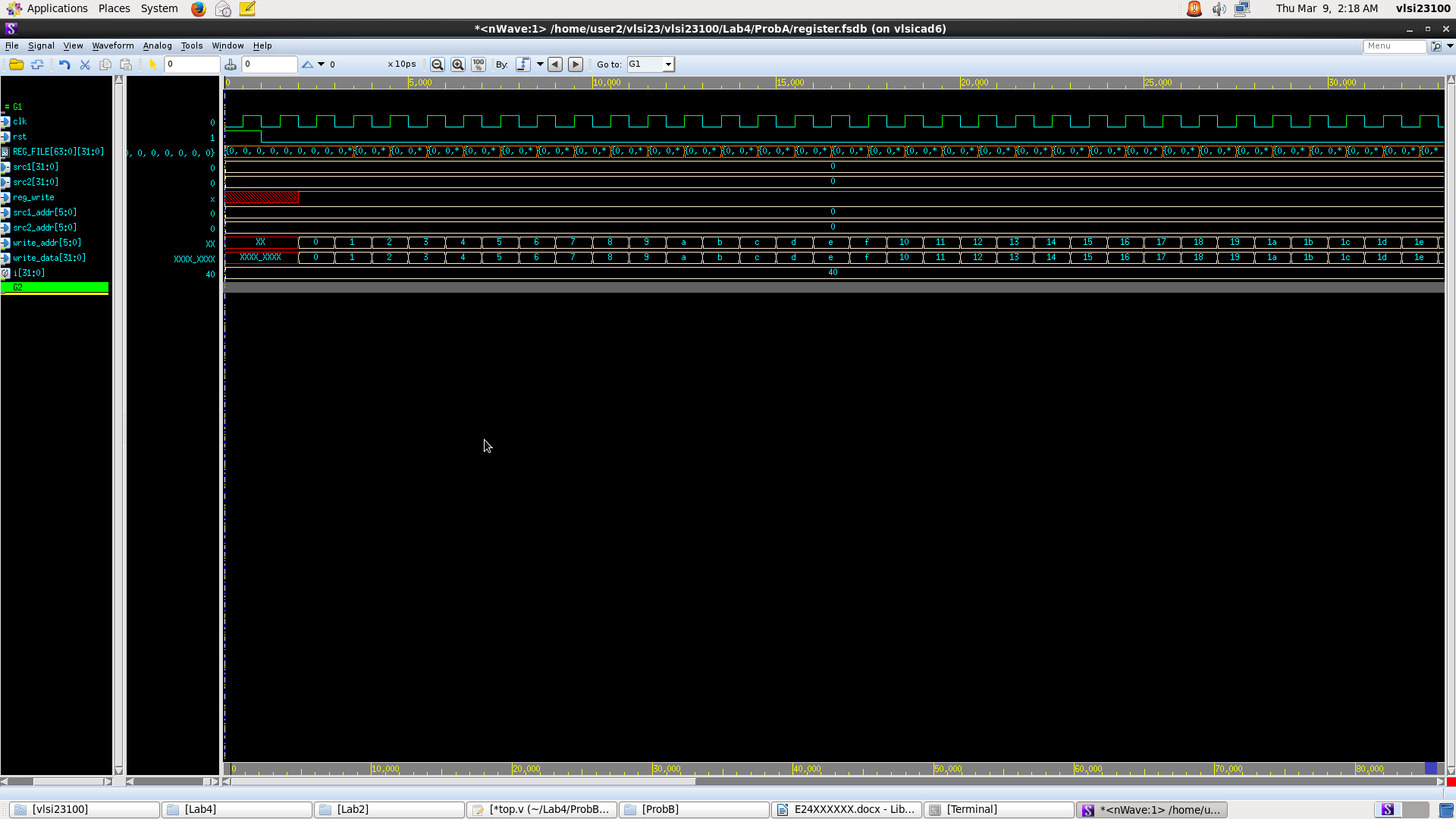
1. Based on the register file structure in LabA, please design a 64 x 32 register file by yourself.
2. Port list



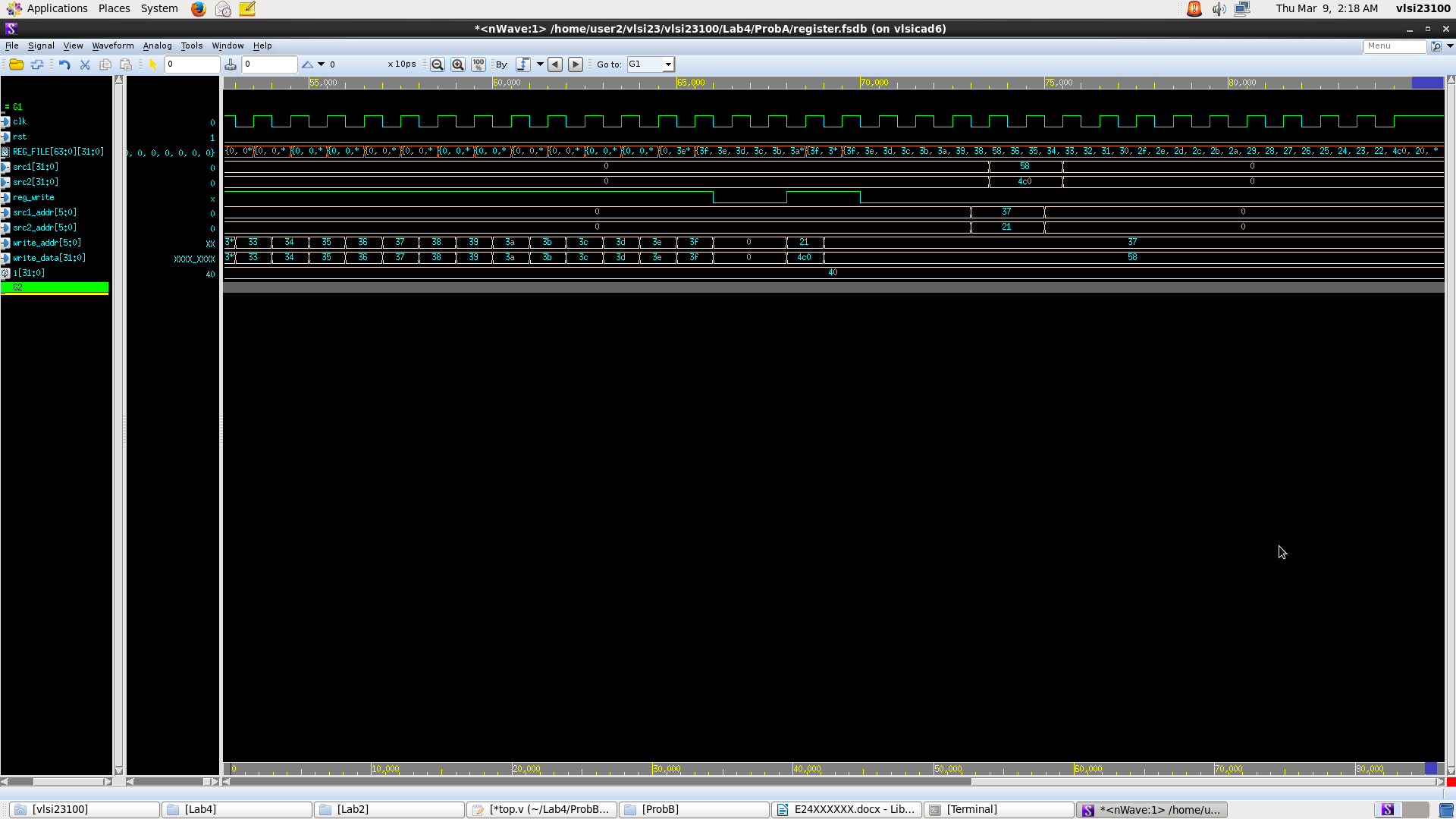
1. You should follow the file name rules as follow.

* Register file
  + File name: **register.v**
  + Module name: **register**
* Register file testbench
  + File name: **register\_tb.v**

1. Show waveforms to explain that your register work correctly when read and write.

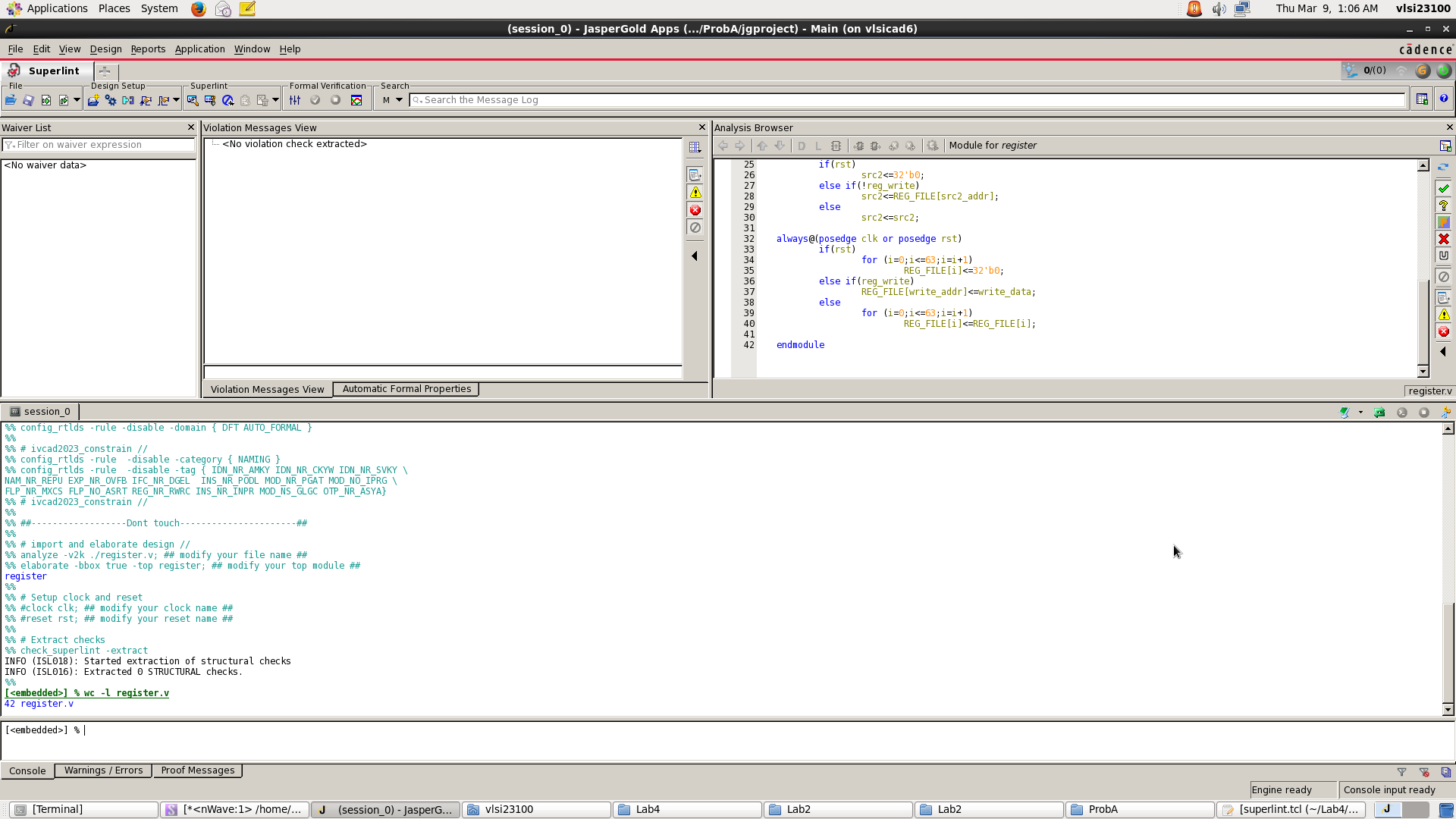


當reg\_write=1，clock falling edge送入write\_data時，下一個cycle的clock rising edge將write\_data寫入REG\_FILE[write\_addr]，如上圖所示。



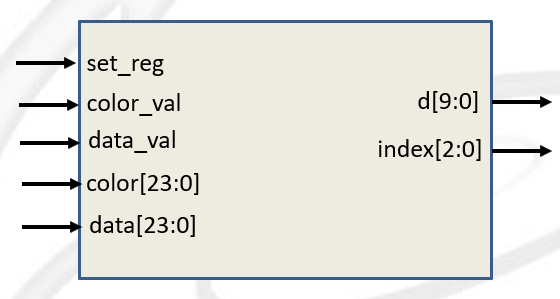
當reg\_write=0，clock falling edge送入src1\_addr和src2\_add時，下一個cycle的clock rising edge將REG\_FILE[src1\_addr]輸出到src1，REG\_FILE[src2\_add]輸出到src2，如上圖所示。

1. Show SuperLint coverage



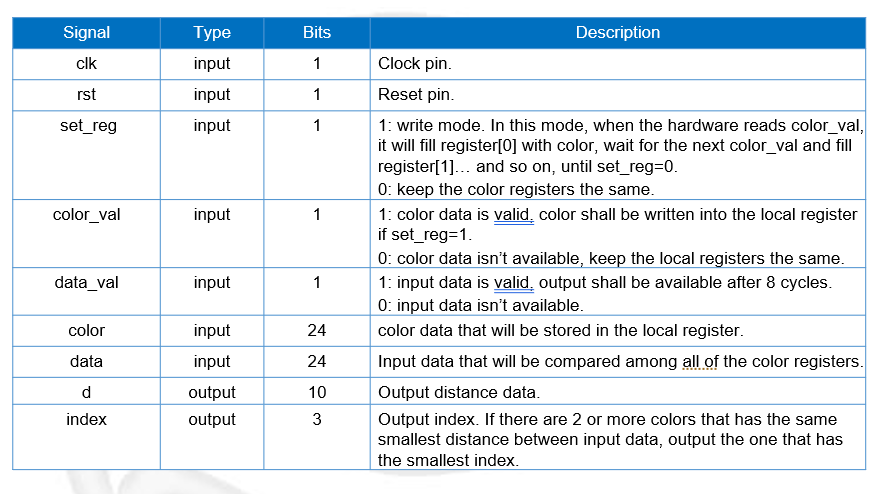
Coverage:100%

Prob B: Finding Smallest Distance

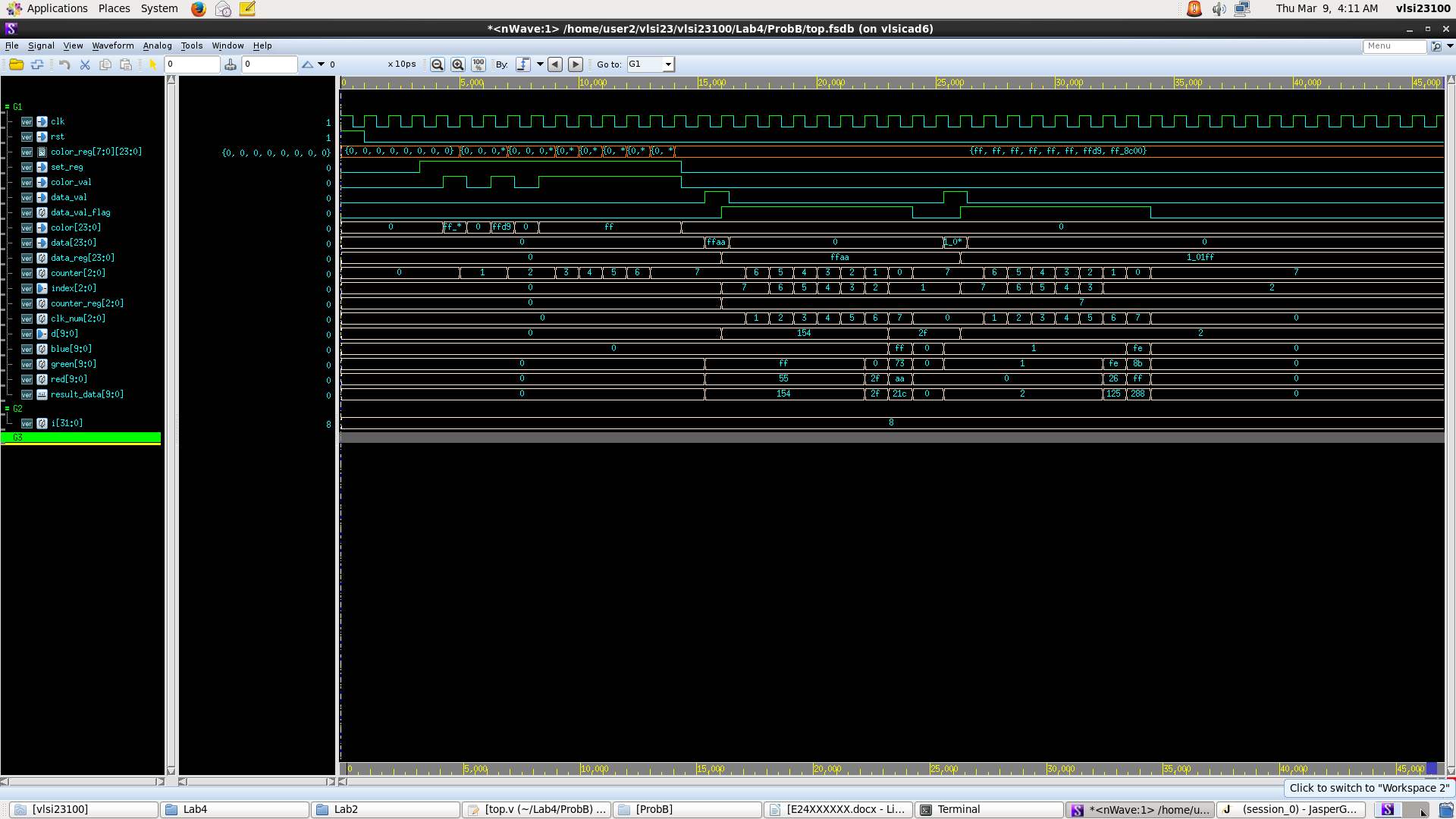


Please design a circuit that will find the smallest distance between the local registers and the input data, based on the structure given in the LAB4 slide.

Port list



1. Show waveforms to explain that your design works correctly.

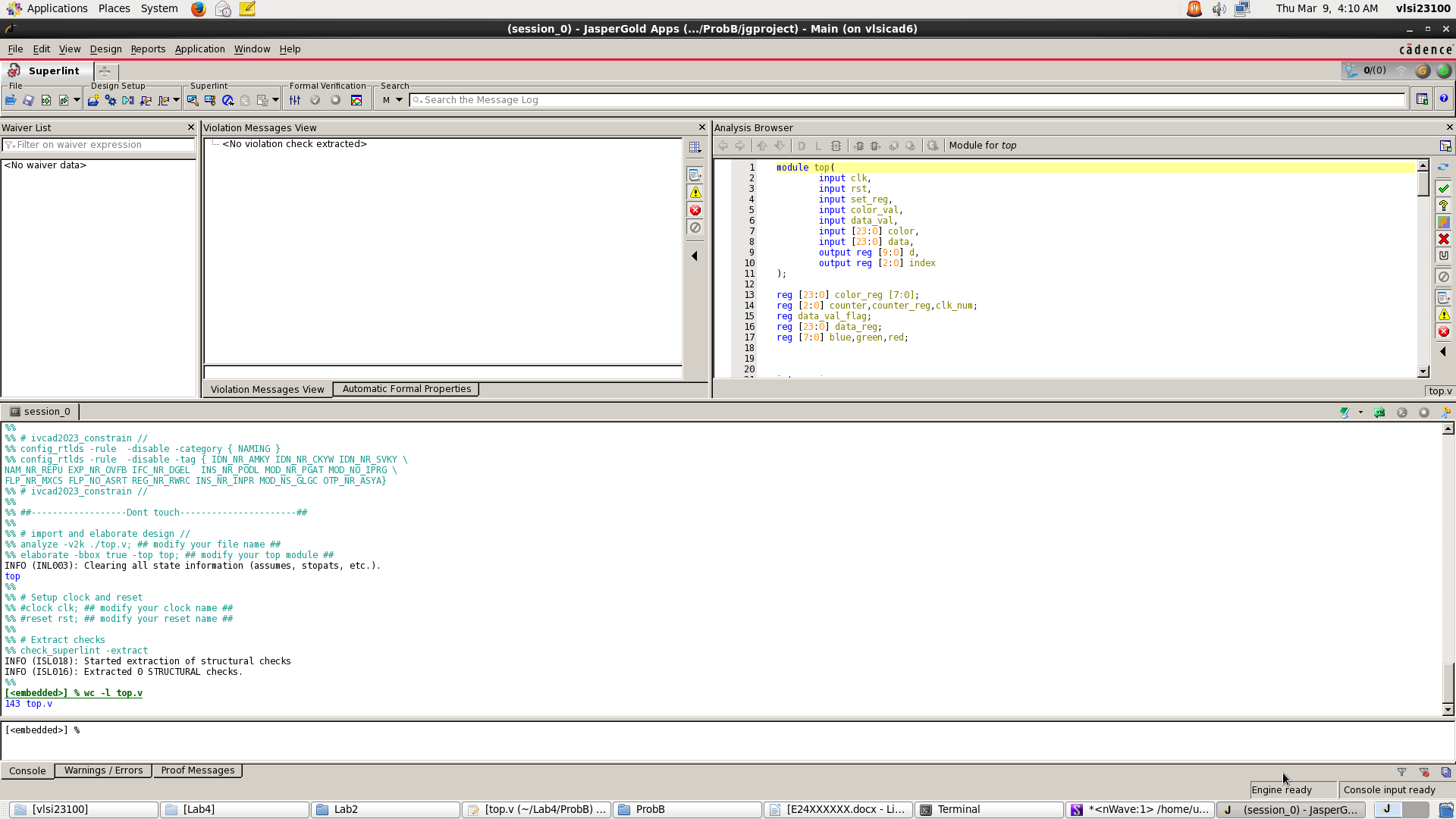


Input: clk, rst, set\_reg, color\_val, data\_val, color, data

Output: d, index

當set\_reg和color\_val為1時，將color存進color\_reg [counter]中，並將counter加1；當data\_val為1時，將1存進data\_val\_flag，將data存進data\_reg，將counter的值存進counter\_reg(記住存到第幾個color\_reg)；當data\_val或data\_val\_flag為1時，counter每個cycle減1(每個cycle用color\_reg [counter]中的值比較)，clk\_num每個cycle加1(負責數是否到第8個cycle)；運算中blue為|Bi-Bj|，green為|Gi-Gj|，red為|Ri-Rj|；若比較後距離等於或小於d中的值，則將距離的值存進d中，counter的值存進index中；最後當clk\_num=7時，重設counter為counter\_reg中的值，data\_val\_flag為0。

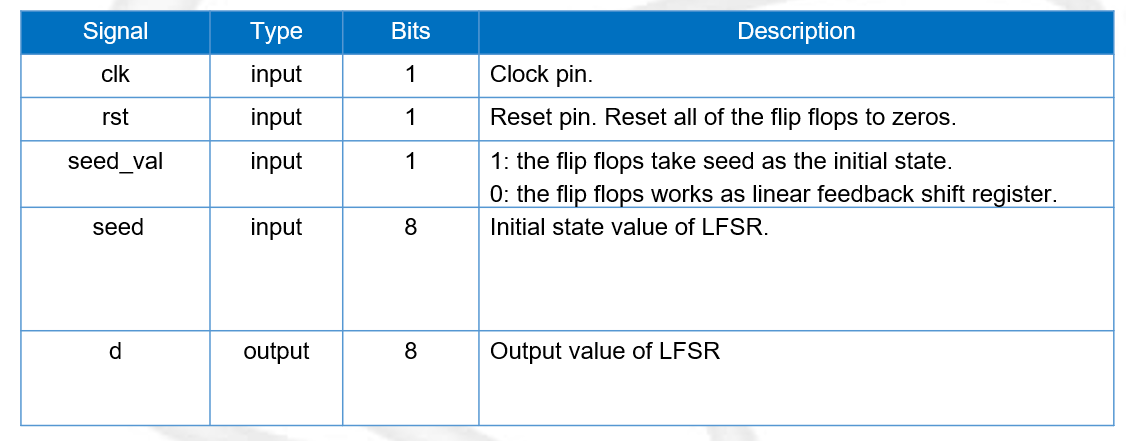
1. Show SuperLint coverage



Coverage:100%

Prob C: LFSR

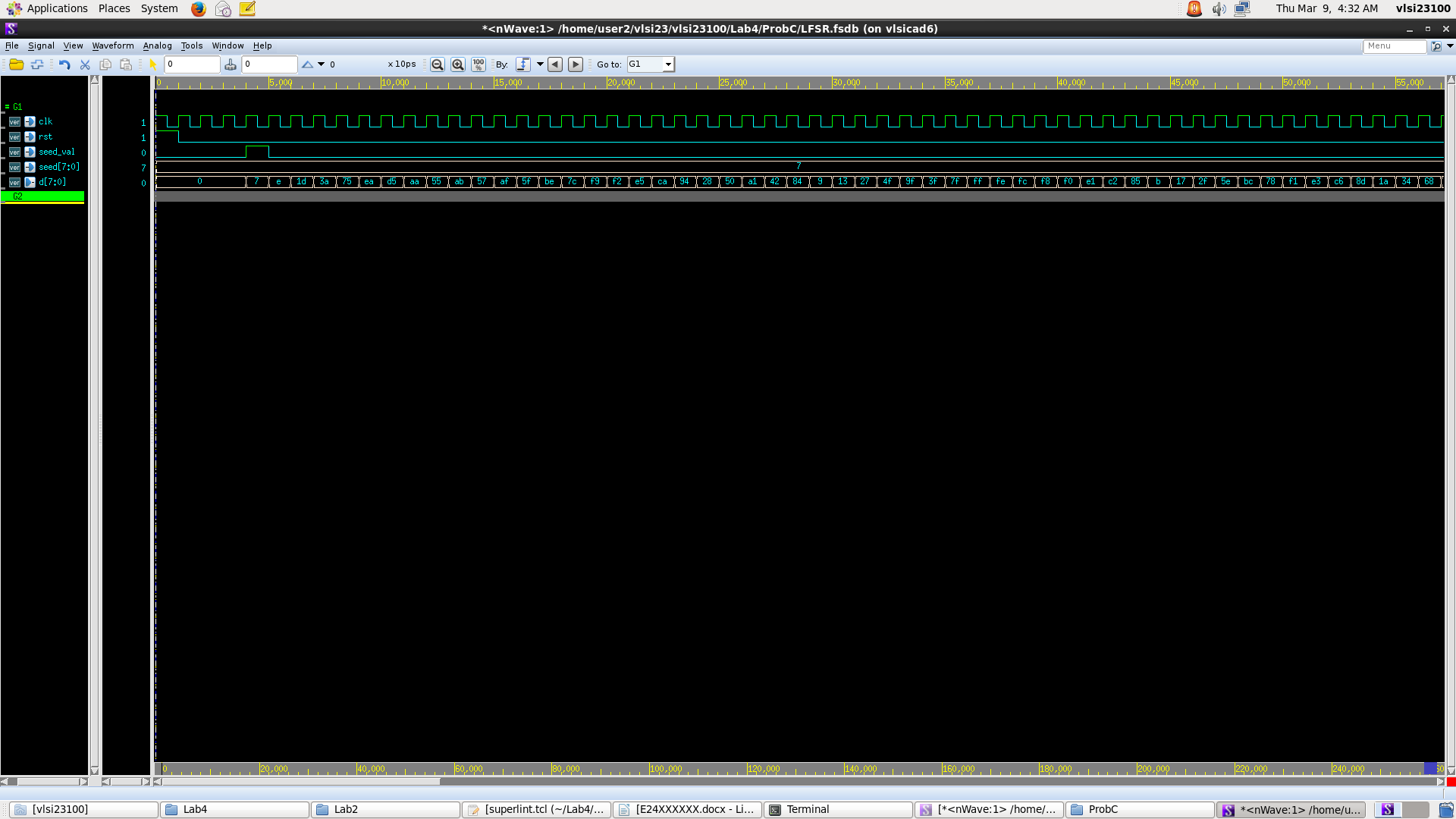
1. Please design an 8-bit-LFSR, with the given feedback function in the LAB4 slide.
2. Port list



1. Feedback function

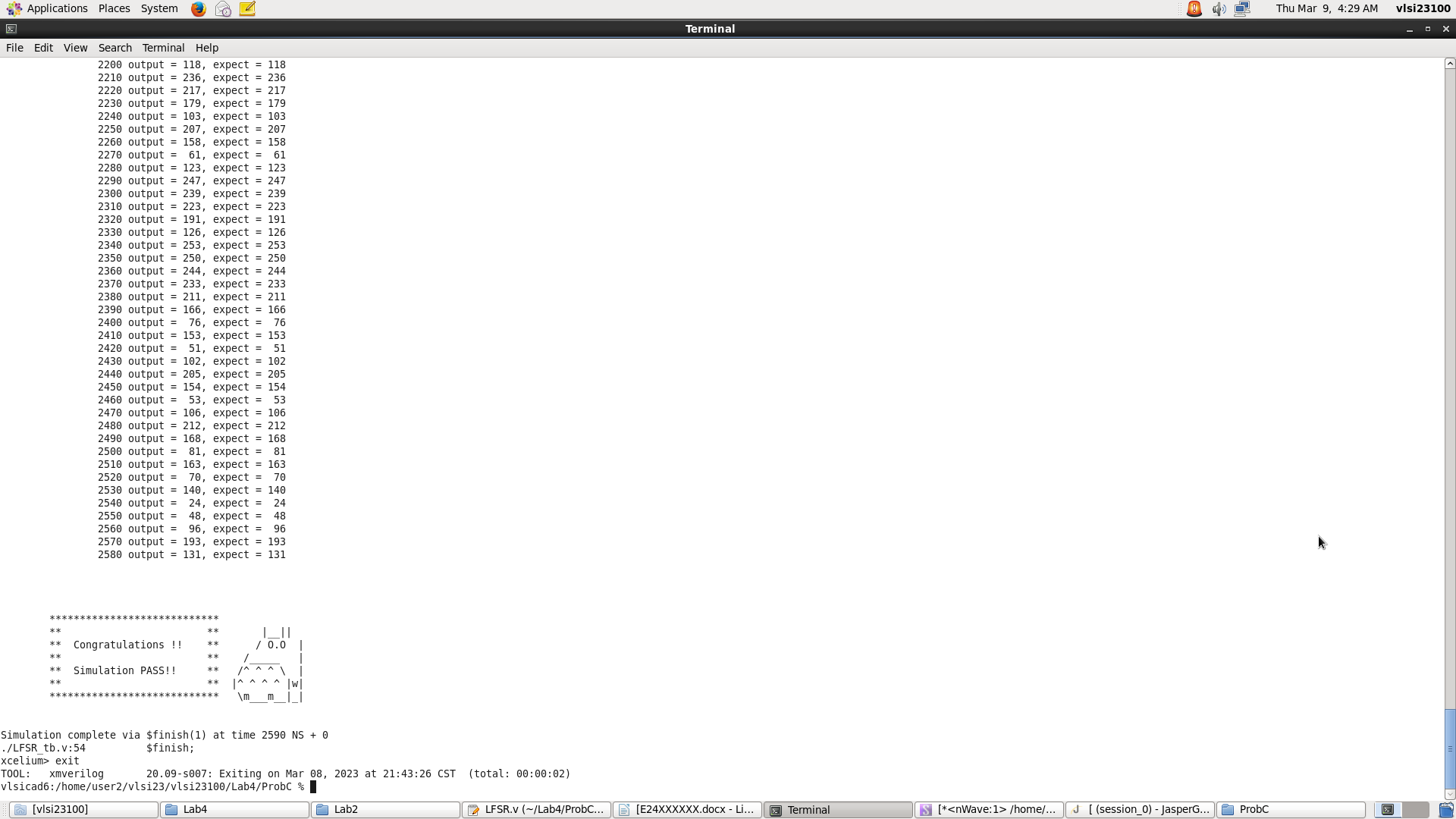


1. Show waveforms to explain that your LFSR module works correctly.

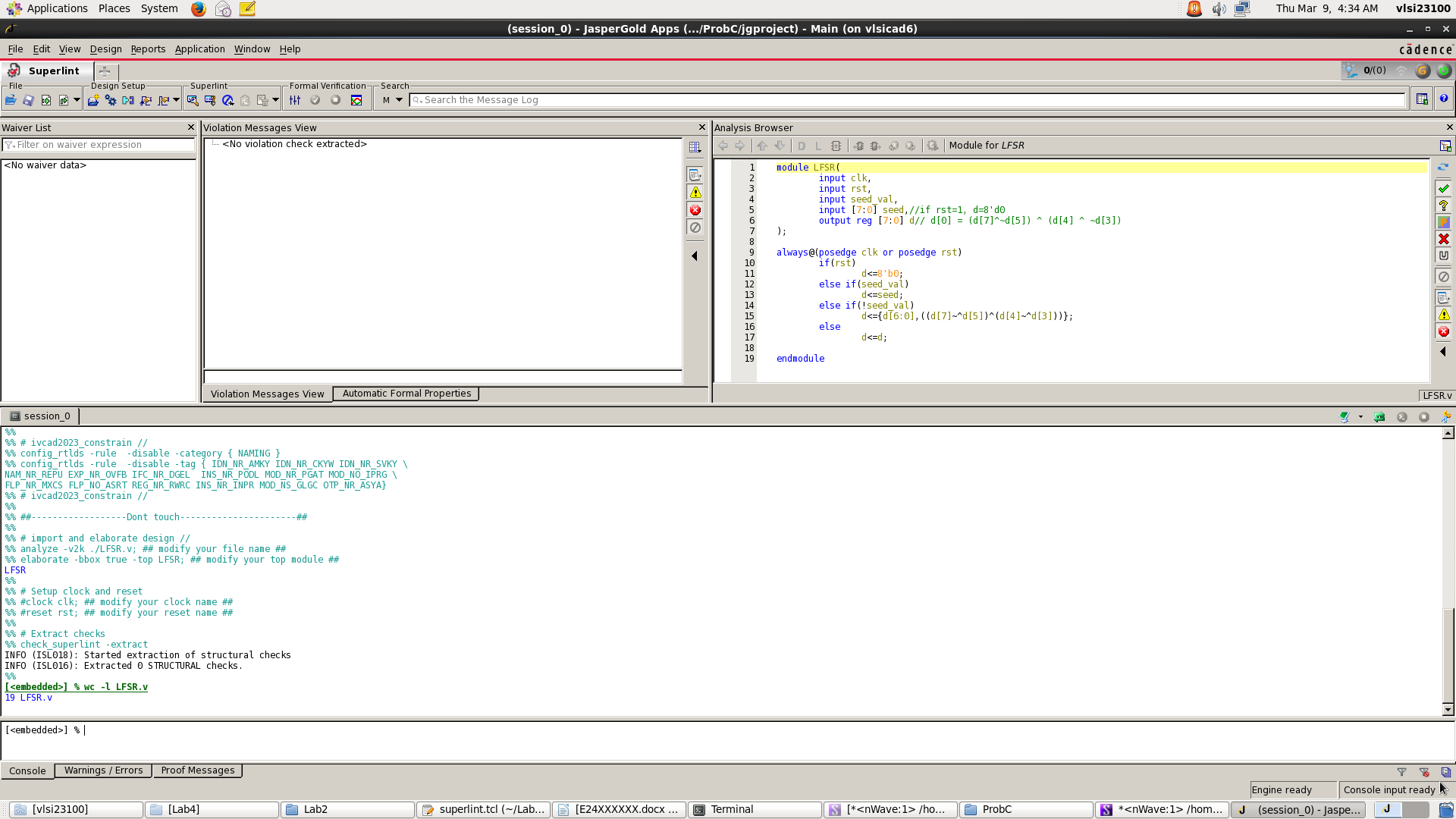


當seed\_val=1時，d被initial成seed的值7，如上圖所示，當seed\_val=0時，d為{d’[6:0],((d’[7]~^d’[5])^(d’[4]~^d’[3]))} (上一個cycle的d值為d’)。

1. Show the simulation result on the terminal.



1. Show SuperLint coverage



Coverage:100%

1. At last, please write the lesson you learned from Lab4

在Lab4中我學到如何實作sequential電路並應用在register,LFSR等電路中，並利用sequential電路做運算，也學到如何結合combinational和sequential電路實作比絕對值距離大小。

Appendix A : Commands we will use to check your homework

