**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2023)***

**Lab Session 5**

**Synthesis of Sequential Logic and Some Tips**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Student ID | | |
| 陳慕丞 | E94096097 | | |
| Practical Sections: | | Points | Marks |
| ProbA | | 30 |  |
| ProbB | | 35 |  |
| ProbC | | 35 |  |
| Notes | | | |

**Due Date: 14:59, March 22, 2023 @ moodle**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** include source code in the paper report!

1. All homework requirements should follow the naming rule in this file hierarchy or you will not get the full credit.

NOTE: Please **DO NOT** upload waveforms!

1. Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
2. **If you upload a dead body, which we cannot even compile, you will get NO credit!**
3. **All Verilog file before synthesizing should get at least 95% Superlint Coverage.**
4. Lab5\_Student\_ID.tar (English alphabet of Student\_ID should be **capital**.)

Lab5\_studentID.tar

Lab5\_studentID

studentID.docx

ProbA

det\_seq.v

det\_seq\_tb.v

det\_seq\_syn.v

det\_seq\_syn.sdf

ProbB

mini\_vending.v

mini\_vending\_tb.v

mini\_vending\_syn.v

mini\_vending\_syn.sdf

ProbC

pattern\_gen.v

pattern\_gen\_syn.v

pattern\_gen\_syn.sdf

pattern\_gen\_tb.v

Fig.1 File hierarchy for Homework submission

**Objectives:**

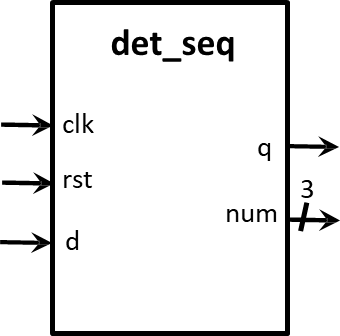
**To make you be familiar with some designs of sequential logic and Design Complier. You can follow this document to practice. Please show your best.**

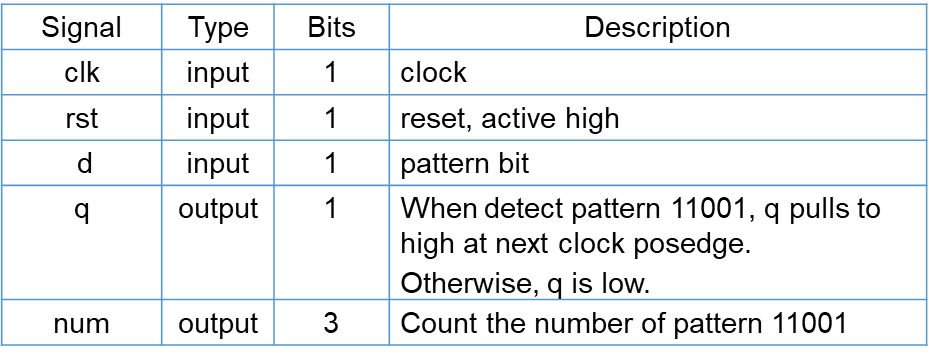
Note that you can extend the spacing if it is not enough for you to answer.

All labs should be synthesized, and clock period should not over 10 ns.

ProbA: Design a circuit “detecting pattern 11001”

1. **Design a pattern seq-detecting circuit that can be synthesized with moore machine. The following is det\_seq module’s specification. (Do NOT add or delete I/O ports, but you can change their behavior.)**





1. **Please describe your FSM in detail**

|  |
| --- |
| Explanation about your FSM |
| IDLE會直接到FIRST  當d符合11001的input順序時，state順序為FIRST->SECOND->THIRD->FORTH->FITH->VALID，否則，當11001其中一個不符合時會出現不同的狀況，FIRST不符合時會回到FIRST，SECOND不符合時會回到FIRST，THIRD不符合時會回到THIRD，FORTH不符合時會回到SECOND，FITH不符合時會回到FIRST，到VALID時會拉起q並將num加1，VALID會有兩種情況，當input為1時會和前一個input形成11，因此會回到THIRD，否則當input為0時回到FIRST從頭開始。 |

1. **After synthesizing your design, you may have some information about the circuit. Please fill in the following form.**

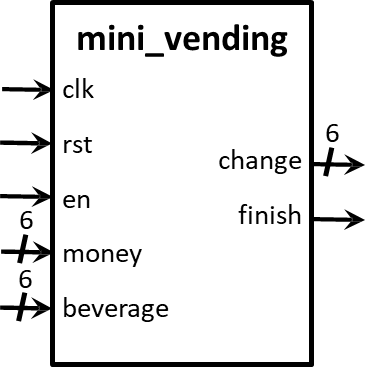
|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **3.51** | **381.914994** |  |

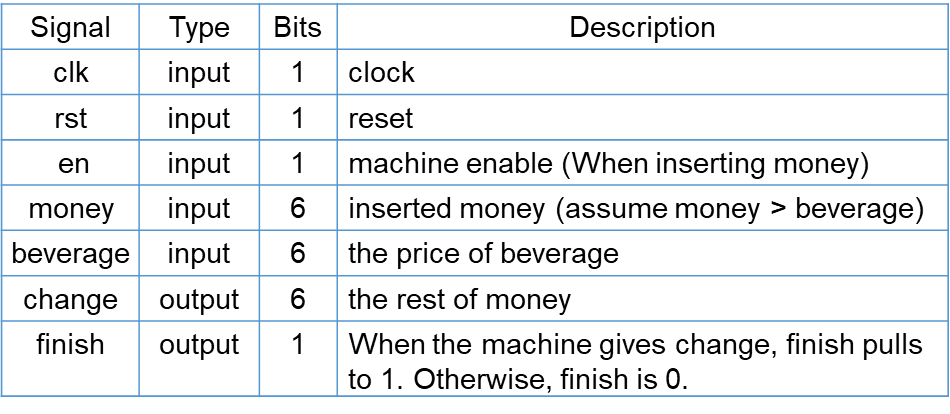
1. **Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
| RTL:    Synthesys: |
| Your waveform : |
| RTL:    Synthesys: |
| Explanation of your waveform : |
| Input:clk,rst,d  Output:q,num  當rst時state為IDLE，next\_state為FIRST，當next\_state換狀態時，在下一個clk的posedge state就會跟著換狀態。當d符合11001且狀態順利走到VALID時q就會拉起且num加1。 |
| Superlint Coverage |
| Coverage:100% |

ProbB: Design a mini vending machine

1. **Design a mini vending machine with moore machine. The following is mini vending machine module’s specification.** **(Do NOT add or delete any I/O ports, but you can change their behavior.)**





1. **Please describe your FSM in detail.**

|  |
| --- |
| Explanation about your FSM |
| 一開始為IDLE，然後直接進入MONEY，當en拉起時代表money輸入，因此進入BAVERAGE，否則回到MONEY，進入BAVERAGE時把 money\_reg-beverage存進 money\_reg，當en下降時代表baverage輸入，因此進入CHANGE，否則回到BAVERAGE，進入CHANGE時會拉升finish並將 money\_reg輸出到change，之後再回到MONEY。 |

1. **After synthesizing your design, you may have some information about the circuit. Please fill in the following form.**

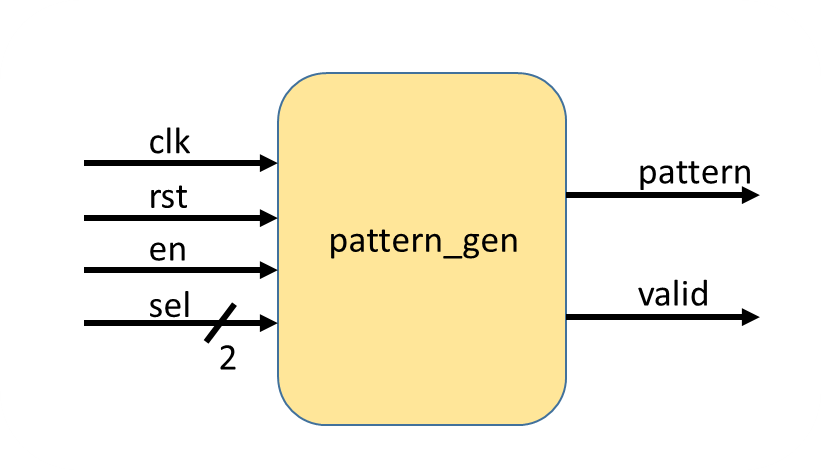
|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **1.03** | **675.565201** |  |

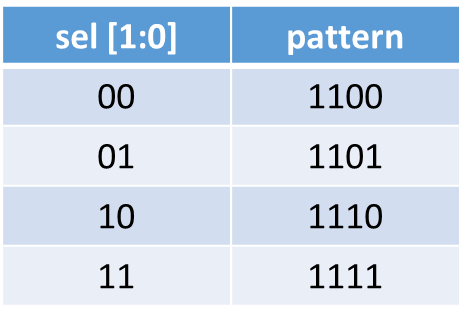
1. **Please attach your design waveforms.**

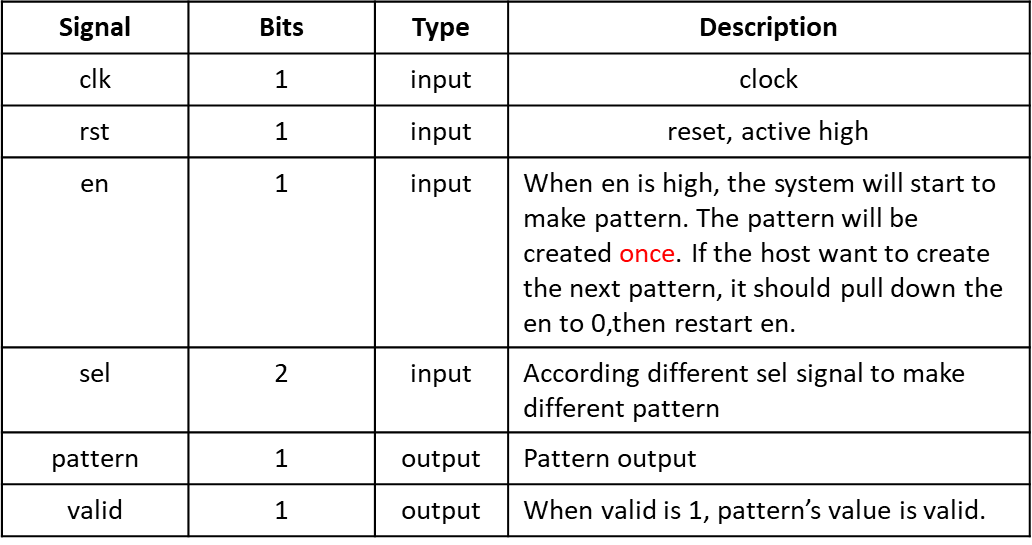
|  |
| --- |
| Your simulation result on the terminal. |
| RTL:    Synthesys: |
| Your waveform : |
| RTL:    Synthesys: |
| Explanation of your waveform : |
| Input: clk, rst, en, money, beverage  Output: change, finish  當rst時state為IDLE，next\_state為MONEY，當next\_state換狀態時，在下一個clk的posedge state就會跟著換狀態。當en拉起時state會到BAVERAGE並將money存到money\_reg中，當en下降時state會到CHANGE，money\_reg存進money\_reg-beverage，finish拉起並將money\_reg輸出到change，之後再回到MONEY。 |
| Superlint Coverage |
| Coverage:100% |

ProbC: Design a pattern generator

1. **Design a pattern generator which can create pattern 1100, 1101, 1110, 1111 and use mealy machine. The following is pattern generator specification.**

****

****

****

1. **Please describe your FSM in detail.**

|  |
| --- |
| Explanation about your FSM |
| 一開始為IDLE，若en下降則回到IDLE，否則en拉升則進入FIRST(pattern輸出1)->SECOND(pattern輸出1)->THIRD(pattern輸出sel[1])->FORTH(pattern輸出sel[0])->ENDD，在ENND中，若en拉起則回到ENDD，否則en下降則進入LOW，在LOW中若en下降則回到LOW，否則en拉起則回到FIRST。另外，當在IDLE、ENDD、LOW時valid輸出0，其餘的輸出1。 |

1. **After synthesizing your design, you may have some information about the circuit. Please fill in the following form.**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **3.35** | **224.056798** |  |

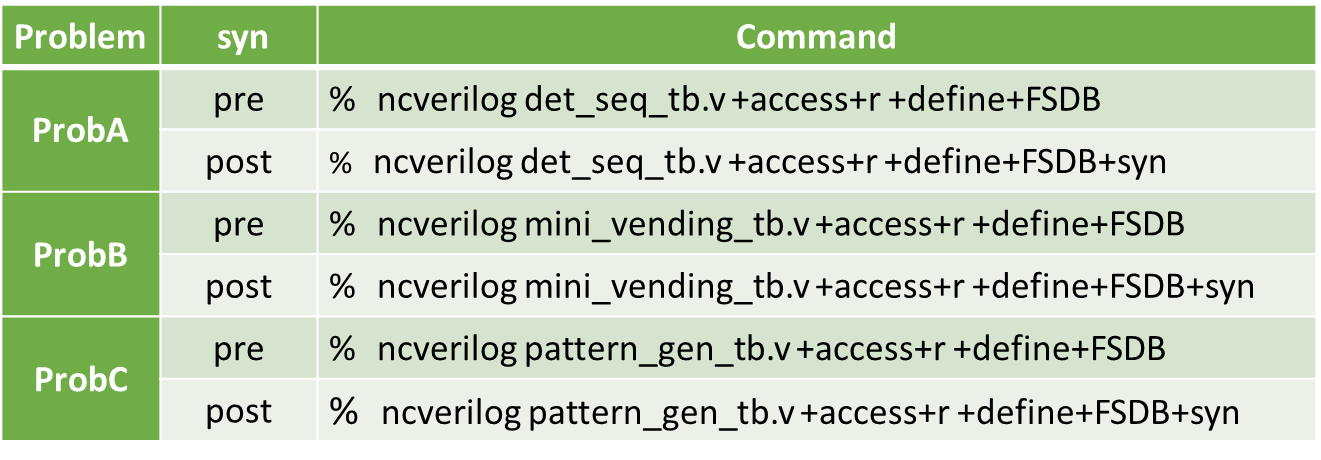
1. **Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
| RTL:    Synthesys: |
| Your waveform : |
| RTL:    Synthesys: |
| Explanation of your waveform : |
| Input: clk, rst, en, sel  Output: pattern, valid  當rst時state為IDLE，next\_state為IDLE，當next\_state換狀態時，在下一個clk的posedge state就會跟著換狀態。在en拉起時state進入FIRST，當state在FIRST、SECOND時，pattern輸出1，當state在THIRD時，pattern輸出sel[1]，在FORTH時，pattern輸出sel[0]，當pattern輸出完畢時state進入ENDD，當en下降時state進入LOW，當en再次上升時state就再次進入FIRST。Valid只在state為FIRST、SECOND、THIRD、FORTH時拉升，其餘為下降。 |
| Superlint Coverage |
| Coverage:100% |

1. **At last, please write the lessons learned from this lab session, or some suggestions for this lab session. Thank you.**

**在此lab我學到了moore和mealy狀態機的差別和如何分別實作出來，也學到如何使用Verdi查看code的FSM圖。**

Appendix A : Commands we will use to check your homework

****