VLSI DESIGN
CSE460
SECTION : 05L
Assignment 2 [Lab]
Deadline: 29/03/2022 10:00 AM

Rules:

1. You need to submit the code, the compilation report and the simulation report with a brief description for each of the problems.
2. Prepare your assignment in a doc file. For each of the problems, paste the code in the doc file (Not screenshot, copy-paste the code), add screenshots (full screen) of the compilation and simulation report and give a brief description of how your timing diagrams manifest expected outputs.The explanation can either be typed or scanned. Next, export the doc as pdf and rename it as **ID_LabAssignment2_CSE460.pdf.**
3. Finally, submit the pdf within the deadline.

Problem 1: (marks: 8)

An FSM has an input w and an output z. The machine has to generate **z = 1** when the following patterns in w are detected: **1010**; otherwise, **z = 0**. The machine should reset when (Reset = 0).

Requirements:

A. What type of FSM method should be used?
B. Draw the state diagram,
C. Write the state-assigned table
D. Write the Verilog code
E. Run simulations, and verify your answer (timing diagram with the clock's period = 50ns) with respect to the timing diagram chart in Table 1.

Table 1

clock	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9
w	0	**1**	**0**	**1**	**0**	**1**	**0**	0	0
z	0	0	0	0	**1**	0	**1**	0	0

Problem 2: (marks: 12)

You have to design a vending machine for a **15 Tk product**. User's money, returned money by the machine, and product bought condition is represented as **mny (2-bit input), chg (output), and buy (1-bit output)**.

The vending machine can only accept inputs: no money (mny = 00), Tk 10 (mny = 01), and Tk 20 (mny = 10). If no money is inserted into the machine, it will immediately return the user's money back. Once an acceptable input is more than or equal to 20 Tk, the machine immediately generates an output (**buy=1**), goes back to the initial state, and gives back the change (if required).

Requirements:

A. Draw the state diagram.
B. How many types of changes will the machine produce? Address this situation by completing the chg output in Table 2. How many bit/bits should chg output have to represent the returned money in the code?
C. Write the state-assigned table.
D. Write the Verilog code.
E. Run the simulation, and verify your answer (timing diagram with the clock's period = 50ns) with respect to the timing diagram chart in Table 2.

Table 2

clock	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
mny	0	**10**	0	0	**10**	**10**	0	0	**20**	0
buy	0	**0**	0	0	0	**1**	0	0	**1**	0
chg	?	?	?	?	?	?	?	?	?	?

Submission Link