19101283, MD MUSFALLIAH HOSSAIN BHUYAIN

Problem - 1

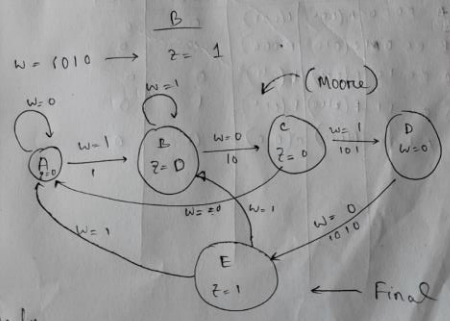
machine has to generate $Z=1$ when $W=1010$, otherwise $Z=0$.

A

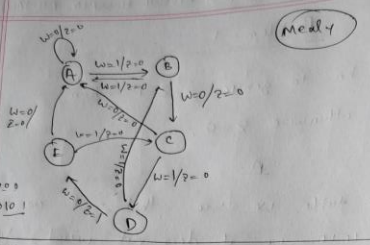
seeing the table, we see that $Z=1$ as soon as, $W=1010$ i.e it does not wait for one cycle

∴ we will use Mealy type FSM.

B



* Mealy type next page

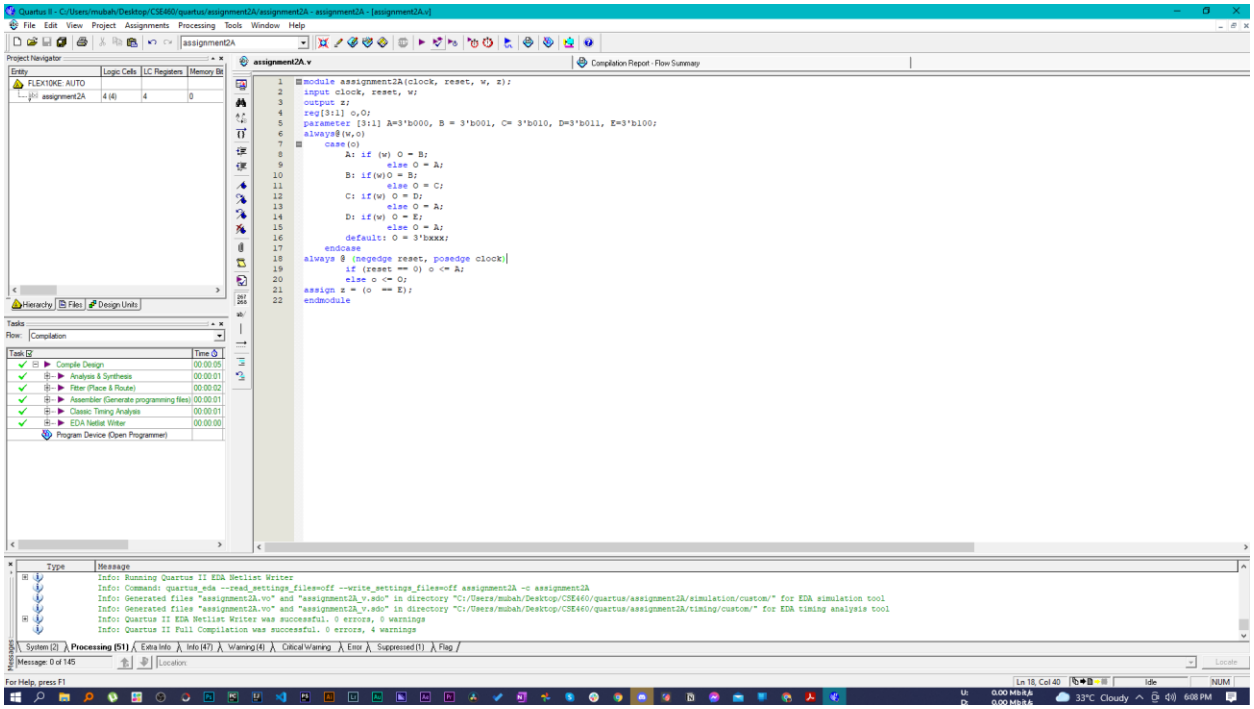


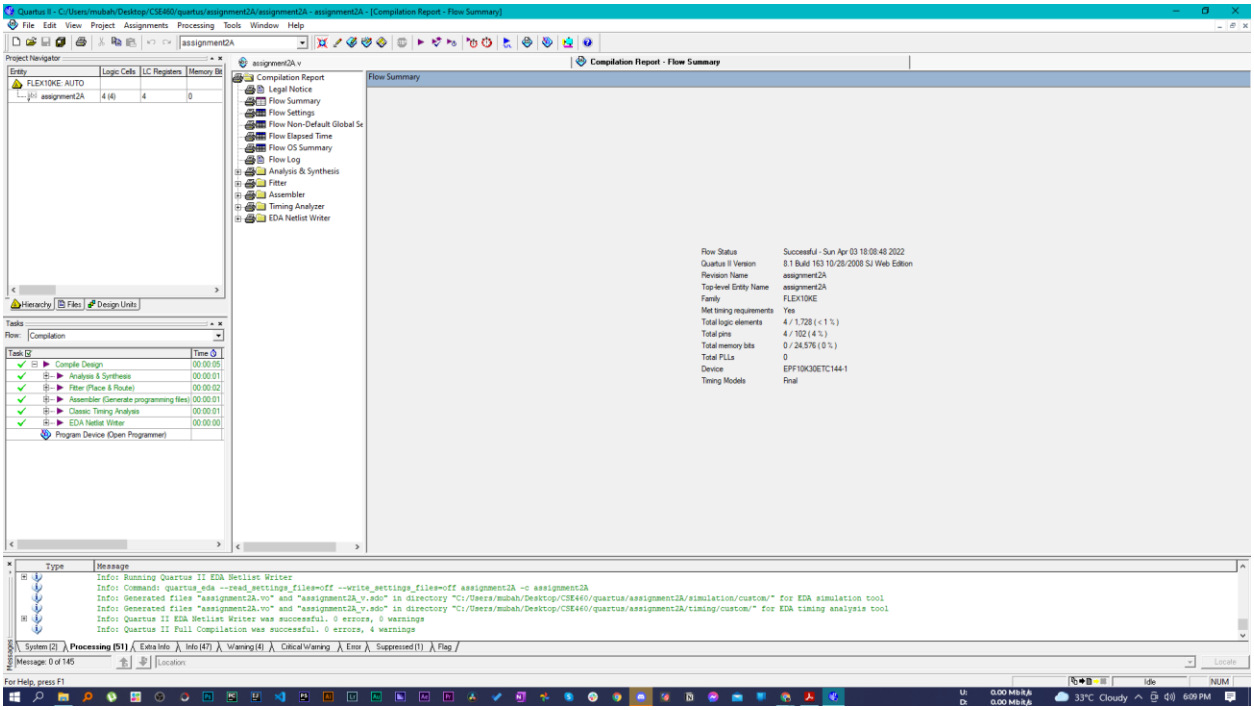
C

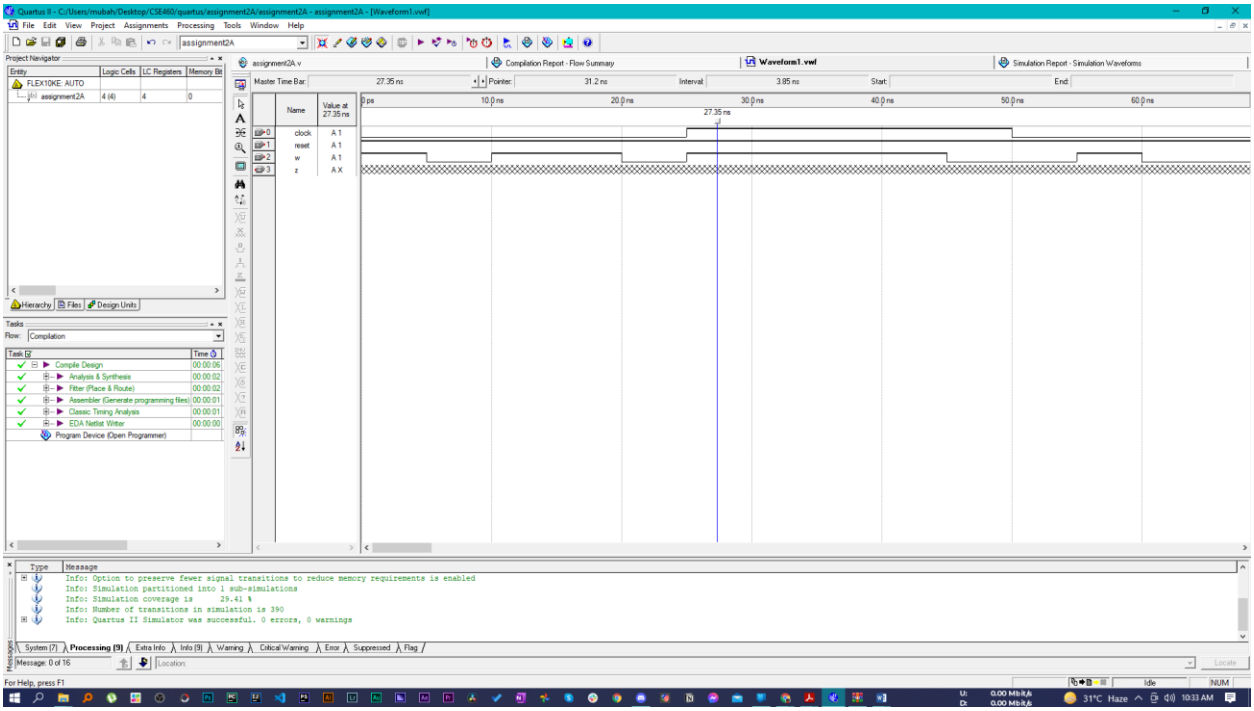
State Assigned Table

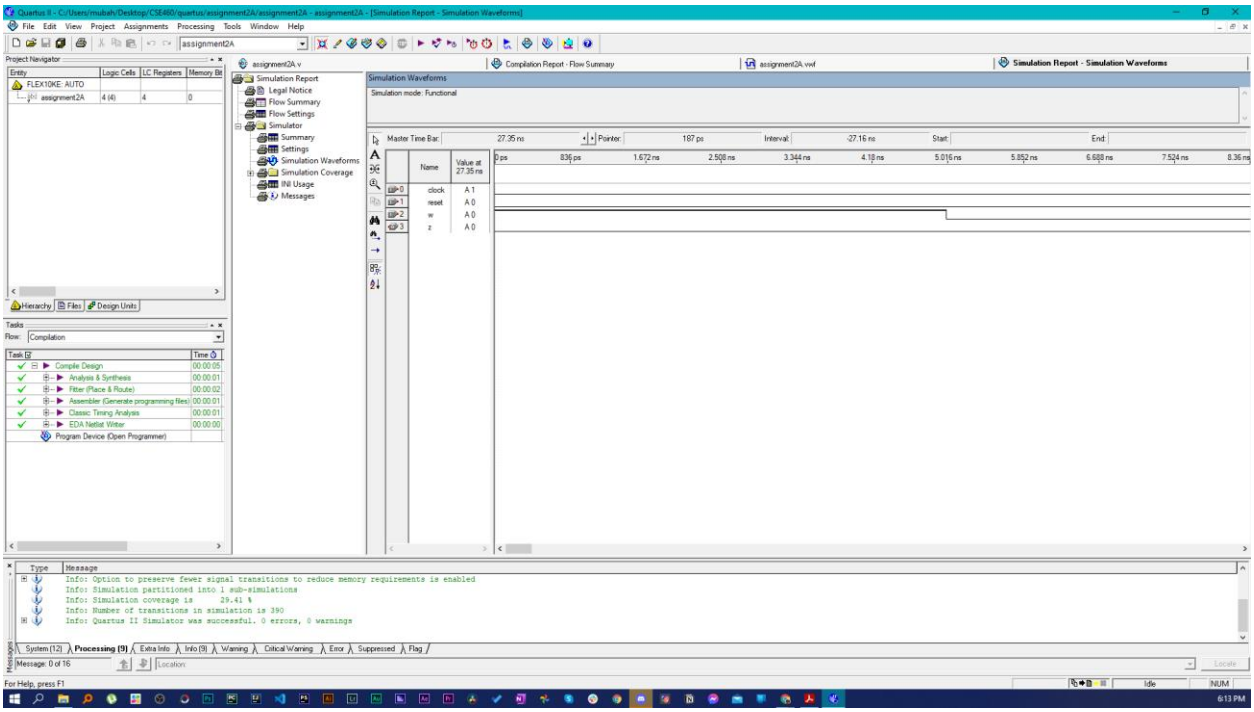
PS	N.S W=0	N.S W=1	Z W=0	Z W=1
A 000	A(000)	B(001)	0	0
B 001	C(010)	A(000)	0	0
C 010	A(000)	D(011)	0	0
D 011	E(100)	B(001)	1	0
E 100	A(000)	C(010)	0	0

```
module assignment2A(clock, reset, w, z);
input clock, reset, w;
output z;
reg[3:1] o,O;
parameter [3:1] A=3'b000, B = 3'b001, C= 3'b010, D=3'b011, E=3'b100;
always@(w,o)
        case(o)
                A: if (w) O = B;
                                else O = A;
                B: if(w)O = B;
                                else O = C;
                C: if(w) O = D;
                                else O = A;
                D: if(w) O = E;
                                else O = A;
                default: O = 3'bxxx;
        endcase
always @ (negedge reset, posedge clock)
                if (reset == 0) o <= A;
                else o <= O;
assign z = (o  == E);
endmodule
```


Quartus II - C:/Users/mubah/Desktop/CSE460/quartus/assignment2A/assignment2A - assignment2A - [assignment2A.v]
File Edit View Project Assignments Processing Tools Window Help
assignment2A
Project Navigator
Entity Logic Cells LC Registers Memory Bit
FLEX10KE: AUTO
assignment2A 4 (4) 4 0
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task Time
Compile Design 00:00:05
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:02
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:00
Program Device (Open Programmer)
assignment2A.v
Compilation Report - Flow Summary
1 module assignment2A(clock, reset, w, z);
2 input clock, reset, w;
3 output z;
4 reg[3:1] o,O;
5 parameter [3:1] A=3'b000, B = 3'b001, C= 3'b010, D=3'b011, E=3'b100;
6 always@(w,o)
7 case(o)
8 A: if (w) O = B;
9 else O = A;
10 B: if(w)O = B;
11 else O = C;
12 C: if(w) O = D;
13 else O = A;
14 D: if(w) O = E;
15 else O = A;
16 default: O = 3'bxxx;
17 endcase
18 always @ (negedge reset, posedge clock)
19 if (reset == 0) o <= A;
20 else o <= O;
21 assign z = (o == E);
22 endmodule
Type Message
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off assignment2A -c assignment2A
Info: Generated files "assignment2A.vo" and "assignment2A_v.sdo" in directory "C:/Users/mubah/Desktop/CSE460/quartus/assignment2A/simulation/custom/" for EDA simulation tool
Info: Generated files "assignment2A.vo" and "assignment2A_v.sdo" in directory "C:/Users/mubah/Desktop/CSE460/quartus/assignment2A/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 4 warnings
System (2) Processing (51) Extra Info Info (47) Warning (4) Critical Warning Error Suppressed (1) Flag
Message: 0 of 145
Location:
For Help, press F1
Ln 18, Col 40
Idle
NUM
33°C Cloudy
6:08 PM

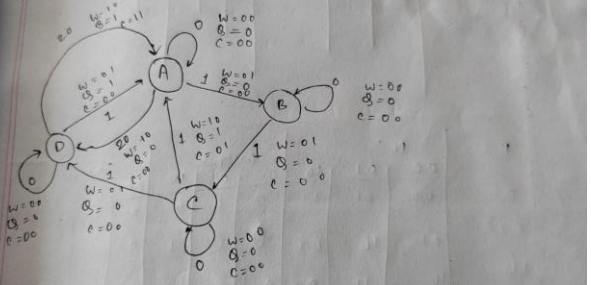

Quartus II - C:/Users/mubah/Desktop/CSE460/quartus/assignment2A/assignment2A - assignment2A - [Compilation Report - Flow Summary]
File Edit View Project Assignments Processing Tools Window Help
assignment2A
Project Navigator
Entity Logic Cells LC Registers Memory Bit
FLEX10KE: AUTO
assignment2A 4 (4) 4 0
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task Time
Compile Design 00:00:05
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:02
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:00
Program Device (Open Programmer)
assignment2A.v
Compilation Report - Flow Summary
Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global Se
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer
Flow Summary
Flow Status Successful - Sun Apr 03 18:08:48 2022
Quartus II Version 8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name assignment2A
Top-level Entity Name assignment2A
Family FLEX10KE
Met timing requirements Yes
Total logic elements 4 / 1,728 (< 1 %)
Total pins 4 / 102 (4 %)
Total memory bits 0 / 24,576 (0 %)
Total PLLs 0
Device EPF10K30ETC144-1
Timing Models Final
Type Message
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off assignment2A -c assignment2A
Info: Generated files "assignment2A.vo" and "assignment2A_v.sdo" in directory "C:/Users/mubah/Desktop/CSE460/quartus/assignment2A/simulation/custom/" for EDA simulation tool
Info: Generated files "assignment2A.vo" and "assignment2A_v.sdo" in directory "C:/Users/mubah/Desktop/CSE460/quartus/assignment2A/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 4 warnings
System (2) Processing (51) Extra Info Info (47) Warning (4) Critical Warning Error Suppressed (1) Flag
Message: 0 of 145
Location:
For Help, press F1
Idle
NUM
33°C Cloudy
6:09 PM


Quartus II - C:/Users/mubah/Desktop/CSE460/quartus/assignment2A/assignment2A - assignment2A - [Waveform1.vwf]
File Edit View Project Assignments Processing Tools Window Help
assignment2A
Project Navigator
Entity
Logic Cells
LC Registers
Memory Bit
FLEX10KE: AUTO
assignment2A
4 (4)
4
0
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design 00:00:06
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:02
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:00
Program Device (Open Programmer)
assignment2A.v
Compilation Report - Flow Summary
Waveform1.vwf
Simulation Report - Simulation Waveforms
Master Time Bar: 27.35 ns
Pointer: 31.2 ns
Interval: 3.85 ns
Start:
End:
Name
Value at 27.35 ns
clock A 1
reset A 1
w A 1
z A X
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
27.35 ns
Type
Message
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 29.41 %
Info: Number of transitions in simulation is 390
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (7)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
31°C Haze
10:33 AM


Quartus II - C:/Users/mubah/Desktop/CSE460/quartus/assignment2A/assignment2A - assignment2A - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
assignment2A
Project Navigator
Entity
Logic Cells
LC Registers
Memory Bit
FLEX10KE: AUTO
assignment2A
4 (4)
4
0
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design 00:00:05
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:02
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:00
Program Device (Open Programmer)
assignment2A.v
Compilation Report - Flow Summary
assignment2A.vwf
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 27.35 ns
Pointer: 187 ps
Interval: -27.16 ns
Start:
End:
Name
Value at 27.35 ns
clock A 1
reset A 0
w A 0
z A 0
0 ps
836 ps
1.672 ns
2.508 ns
3.344 ns
4.18 ns
5.016 ns
5.852 ns
6.688 ns
7.524 ns
8.36 ns
Type
Message
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 29.41 %
Info: Number of transitions in simulation is 390
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (12)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
6:13 PM

Problem – 2

* We us consider
00 → no money
01 → Tk 10
10 → Tk 20
11 → don't care

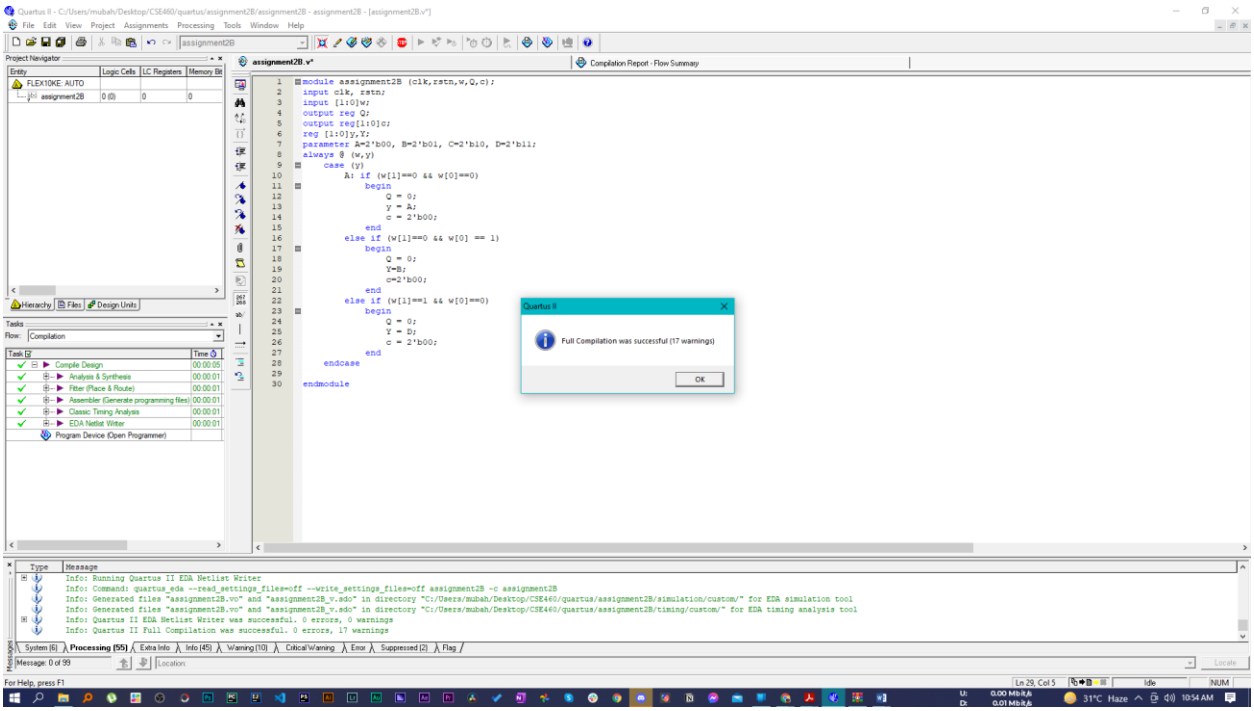


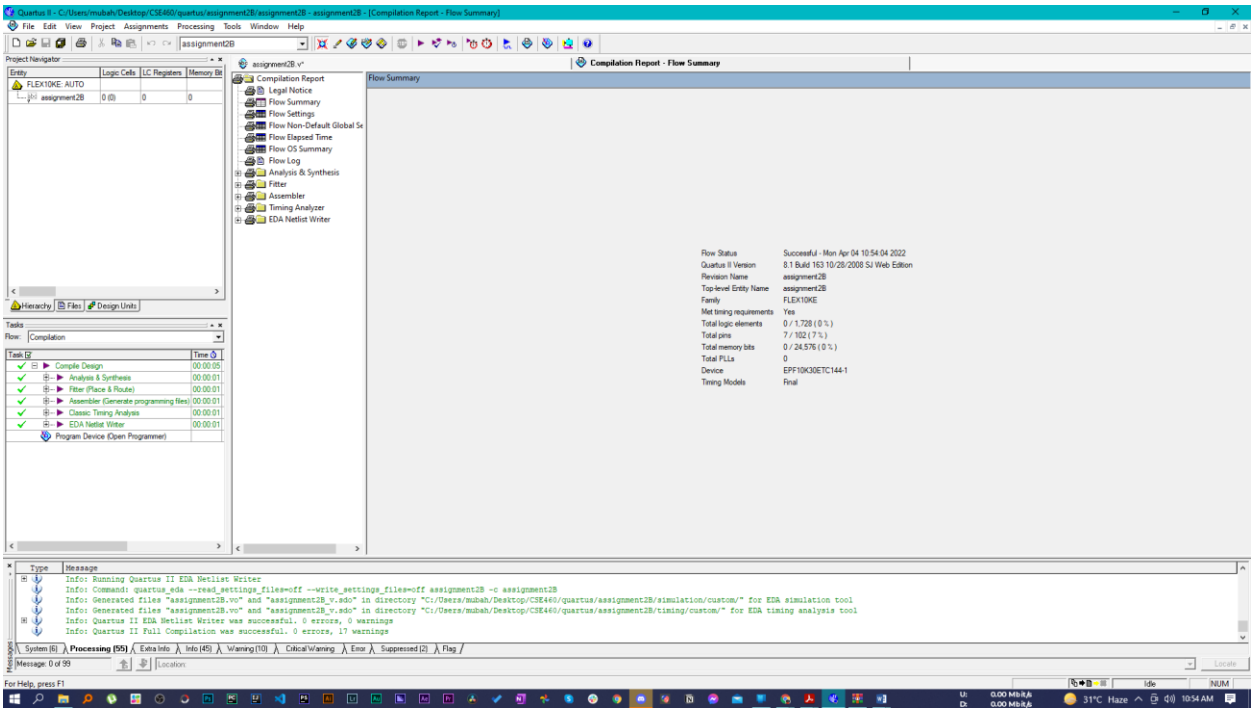
P.S	N.S 00	01	10	Output 00	01	10	Change 00	01	10
A	A	B	D	0	0	0	00	00	00
B	B	C	A	0	0	1	00	00	00
C	C	D	A	0	0	1	00	00	01
D	D	A	A	0	1	1	00	00	11

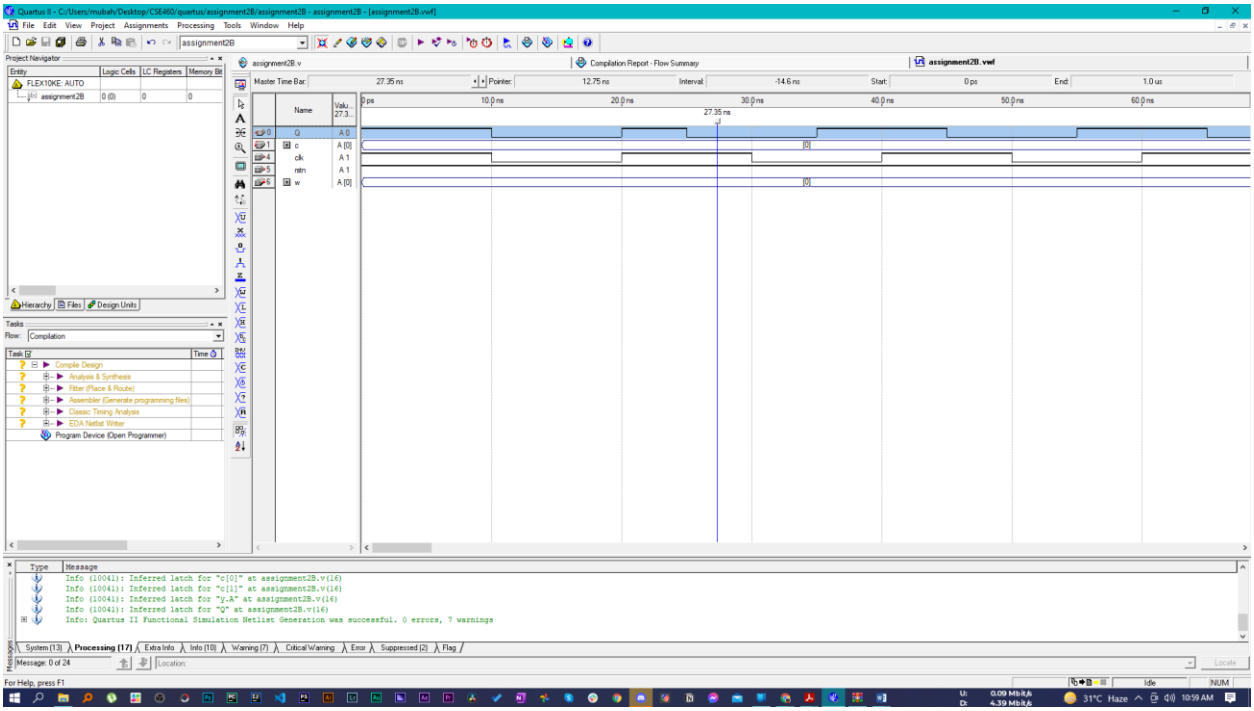
P.S	N.S 00	01	10	Output 00	01	10	Change 00	01	10
00	00	01	11	0	0	0	00	00	00
01	01	10	00	0	0	1	00	00	00
10	10	11	00	0	0	1	00	00	11
11	11	00	00	0	1	1	00	00	11

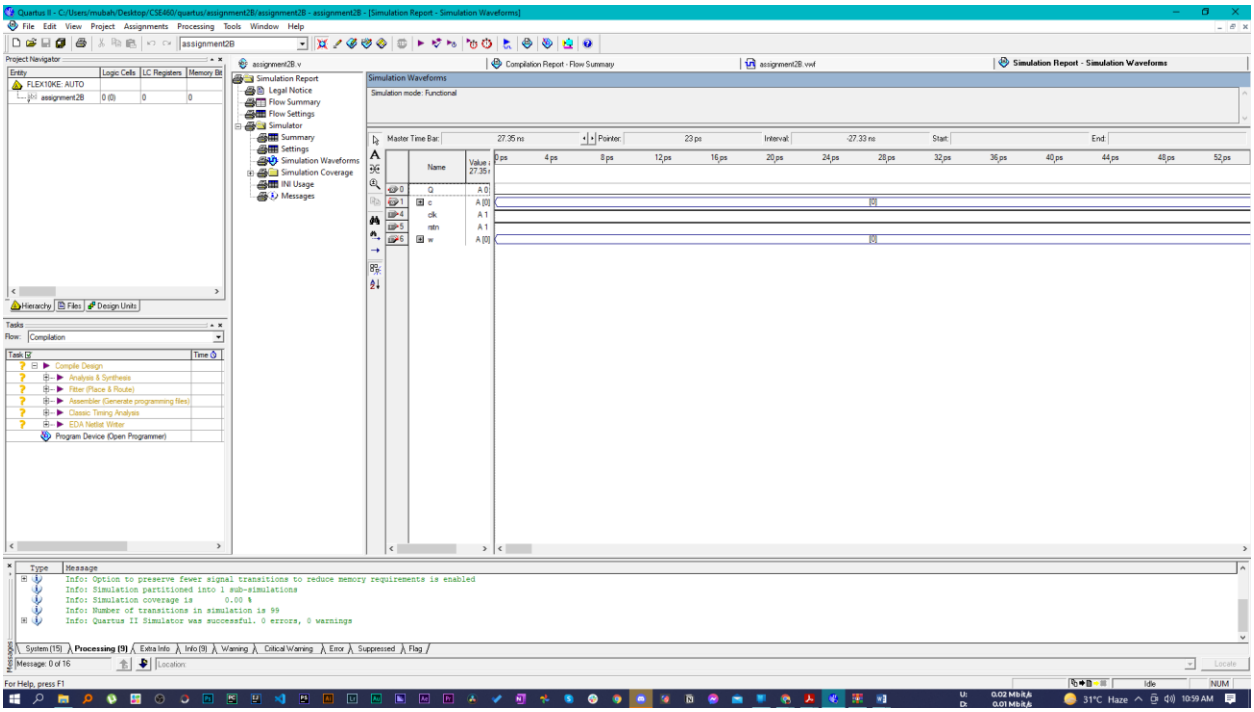
```
module assignment2B (clk,rstn,w,Q,c);
input clk, rstn;
input [1:0]w;
output reg Q;
output reg[1:0]c;
reg [1:0]y,Y;
parameter A=2'b00, B=2'b01, C=2'b10, D=2'b11;
always @ (w,y)
        case (y)
                A: if (w[1]==0 && w[0]==0)
                        begin
                                Q = 0;
                                y = A;
                                c = 2'b00;
                        end
                else if (w[1]==0 && w[0] == 1)
                        begin
                                Q = 0;
                                Y=B;
                                c=2'b00;
                        end
                else if (w[1]==1 && w[0]==0)
                        begin
                                Q = 0;
                                Y = D;
                                c = 2'b00;
                        end
        endcase

endmodule
```


Quartus II - C:/Users/mubah/Desktop/CSE460/quartus/assignment2B/assignment2B - assignment2B - [assignment2B.v*]
File Edit View Project Assignments Processing Tools Window Help
assignment2B
Project Navigator
Entity
Logic Cells
LC Registers
Memory Bit
FLEX10KE: AUTO
assignment2B
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design 00:00:05
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:01
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
assignment2B.v*
Compilation Report - Flow Summary
1 module assignment2B (clk,rstn,w,Q,c);
2 input clk, rstn;
3 input [1:0]w;
4 output reg Q;
5 output reg[1:0]c;
6 reg [1:0]y,Y;
7 parameter A=2'b00, B=2'b01, C=2'b10, D=2'b11;
8 always @ (w,y)
9 case (y)
10 A: if (w[1]==0 && w[0]==0)
11 begin
12 Q = 0;
13 y = A;
14 c = 2'b00;
15 end
16 else if (w[1]==0 && w[0] == 1)
17 begin
18 Q = 0;
19 Y=B;
20 c=2'b00;
21 end
22 else if (w[1]==1 && w[0]==0)
23 begin
24 Q = 0;
25 Y = D;
26 c = 2'b00;
27 end
28 endcase
29
30 endmodule
Quartus II
Full Compilation was successful (17 warnings)
OK
Type
Message
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off assignment2B -c assignment2B
Info: Generated files "assignment2B.vo" and "assignment2B_v.sdo" in directory "C:/Users/mubah/Desktop/CSE460/quartus/assignment2B/simulation/custom/" for EDA simulation tool
Info: Generated files "assignment2B.vo" and "assignment2B_v.sdo" in directory "C:/Users/mubah/Desktop/CSE460/quartus/assignment2B/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 17 warnings
System (6) Processing (55) Extra Info Info (45) Warning (10) Critical Warning Error Suppressed (2) Flag
Message: 0 of 99
Location:
For Help, press F1
Ln 29, Col 5
Idle
NUM
31°C Haze
10:54 AM


Quartus II - C:/Users/mubah/Desktop/CSE460/quartus/assignment2B/assignment2B - assignment2B - [Compilation Report - Flow Summary]
File Edit View Project Assignments Processing Tools Window Help
assignment2B
Project Navigator
Entity
Logic Cells
LC Registers
Memory Bit
FLEX10KE: AUTO
assignment2B
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design 00:00:05
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:01
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
assignment2B.v*
Compilation Report - Flow Summary
Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Global Se
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer
Flow Summary
Flow Status Successful - Mon Apr 04 10:54:04 2022
Quartus II Version 8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name assignment2B
Top-level Entity Name assignment2B
Family FLEX10KE
Met timing requirements Yes
Total logic elements 0 / 1,728 (0 %)
Total pins 7 / 102 (7 %)
Total memory bits 0 / 24,576 (0 %)
Total PLLs 0
Device EPF10K30ETC144-1
Timing Models Final
Type
Message
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off assignment2B -c assignment2B
Info: Generated files "assignment2B.vo" and "assignment2B_v.sdo" in directory "C:/Users/mubah/Desktop/CSE460/quartus/assignment2B/simulation/custom/" for EDA simulation tool
Info: Generated files "assignment2B.vo" and "assignment2B_v.sdo" in directory "C:/Users/mubah/Desktop/CSE460/quartus/assignment2B/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 17 warnings
System (6) Processing (55) Extra Info Info (45) Warning (10) Critical Warning Error Suppressed (2) Flag
Message: 0 of 99
Location:
For Help, press F1
Idle
NUM
31°C Haze
10:54 AM


Quartus II - C:/Users/mubah/Desktop/CSE460/quartus/assignment2B/assignment2B - assignment2B - [assignment2B.vwf]
File Edit View Project Assignments Processing Tools Window Help
assignment2B
Project Navigator
Entity
Logic Cells
LC Registers
Memory Bit
FLEX10KE: AUTO
assignment2B
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
assignment2B.v
Compilation Report - Flow Summary
assignment2B.vwf
Master Time Bar:
27.35 ns
Pointer:
12.75 ns
Interval:
-14.6 ns
Start:
0 ps
End:
1.0 us
Name
Value at 27.3...
Q
c
clk
rstn
w
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
27.35 ns
Type
Message
Info (10041): Inferred latch for "c[0]" at assignment2B.v(16)
Info (10041): Inferred latch for "c[1]" at assignment2B.v(16)
Info (10041): Inferred latch for "y_A" at assignment2B.v(16)
Info (10041): Inferred latch for "Q" at assignment2B.v(16)
Info: Quartus II Functional Simulation Netlist Generation was successful. 0 errors, 7 warnings
System (13)
Processing (17)
Extra Info
Info (10)
Warning (7)
Critical Warning
Error
Suppressed (2)
Flag
Message: 0 of 24
Location:
For Help, press F1
Idle
NUM
31°C Haze
10:59 AM


Quartus II - C:/Users/mubah/Desktop/CSE460/quartus/assignment2B/assignment2B - assignment2B - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
assignment2B
Project Navigator
Entity
Logic Cells
LC Registers
Memory Bit
FLEX10KE: AUTO
assignment2B
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
assignment2B.v
Compilation Report - Flow Summary
assignment2B.vwf
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar:
27.35 ns
Pointer:
23 ps
Interval:
-27.33 ns
Start:
End:
Name
Value at 27.35 ns
Q
c
clk
rstn
w
0 ps
4 ps
8 ps
12 ps
16 ps
20 ps
24 ps
28 ps
32 ps
36 ps
40 ps
44 ps
48 ps
52 ps
Type
Message
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 0.00 %
Info: Number of transitions in simulation is 99
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (15)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
For Help, press F1
Idle
NUM
31°C Haze
10:59 AM