SMARC Eval 2.0

SMARC-Eval2 Evaluation Carrier for SMARC 2.0

DRAWING REVISION HISTORY			
REV	DESCRIPTION	YYYY-MM-DD	APPROVED
0.1	Preliminary schematic	2016-10-06	
1.0	Rev 1100 - A00	2016-11-14	
2.0	Rev 1200 - B00	2017-04-07	
3.0	Rev 1300 - C00	2017-07-26	
4.0	Rev 1400 - D00	2017-11-17	

TABLE OF CONTENT

PAGE	DESCRIPTION
1	Cover
2	Block Diagram
3	Power Diagram
4	SMARC Carrier Connector
5	DP Connector
6	HDMI Connector
7	LVDS Connector
8	LVDS Backlight Connector
9	eDP Connector
10	Ethernet Connectors
11	USB 3.0 Connectors
12	USB 2.0 OTG Connector and USB 2.0 header
13	CAN Transeivers
14	mPCIe Connectors
15	PCIe Connectors
16	mSATA Connector
17	uSD Connector
18	High Speed Serial Ports
19	SPI Flash Socket, I2C Expander
20	Audio - HDA Codec
21	Audio - I2S Codec
22	Audio - Con + Mux
23	GPIO Headers
24	eSPI Header, Power Management Header, CSI
25	Buttons
26	Power Input connectors
27	Power 5V0, 3V3
28	Power 1V8, 1V5
29	Power Discharge, LEDs, RTC
30	Mechanics

NOTES

1. All resistor values are in Ohms. Tolerance shown for less than 1%
2. All capacitor values are in Farads.
3. A "NONE" next to a reference designator indicates a part that should not be installed.
4. A "#" in a signal name or pin name indicates an active logic level low.
5. Differential signal name are recognized by a trailing "+" for positive and "-" for negative pair members.
6. All voltage supply rails shall begin with the characters "V_". Grounding connections shall begin with "GND".
7. The following symbols represent global signals. Note that multiple instances of, for example, GND will append a trailing index as a visible netname for each isolated rail.

are digital ground (GND);

are analog ground (GNDA);

are chassis ground (SHIELD);

are specific voltage supply.

ZNL20
This symbol highlighting the layout recommendation.

This symbol highlighting configuration informations.

I2C Bus Signal	Ref Des	Address (7 bit)	Description
I2C GP	U53 U60	0x20 0x1A	IO Expander I2S Audio Codec
I2C PM	U78 U69 U74 J13 J20 J5 J2 U65 J22 J45	0x57 0x22 0x24 Device Device Device Device 0x6D Device Device	General Purposse EEPROM IO Expander IO Expander mPCIe Connector A mPCIe Connector B PCIe x1 Connector PCIe x1 Connector PCIe Clock Buffer mSATA Connector Power Management Header
I2C CAM0	J60	Device	CSI0 Camera Connector
I2C CAM1	J61	Device	CSI1 Camera Connector
I2C LCD	J3 U72	Device 0x50	LVDS Connector LVDS EEPROM

PROJECT: SMARC Eval 2.0

ADS2 - SMARC Eval 2.0

BLOCK ID: Schematic1 (1 of 30)

SHEET: 01 First Page

	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
VERIFIED:	KEEDC	MH	2017.11.20
APPROVED:			

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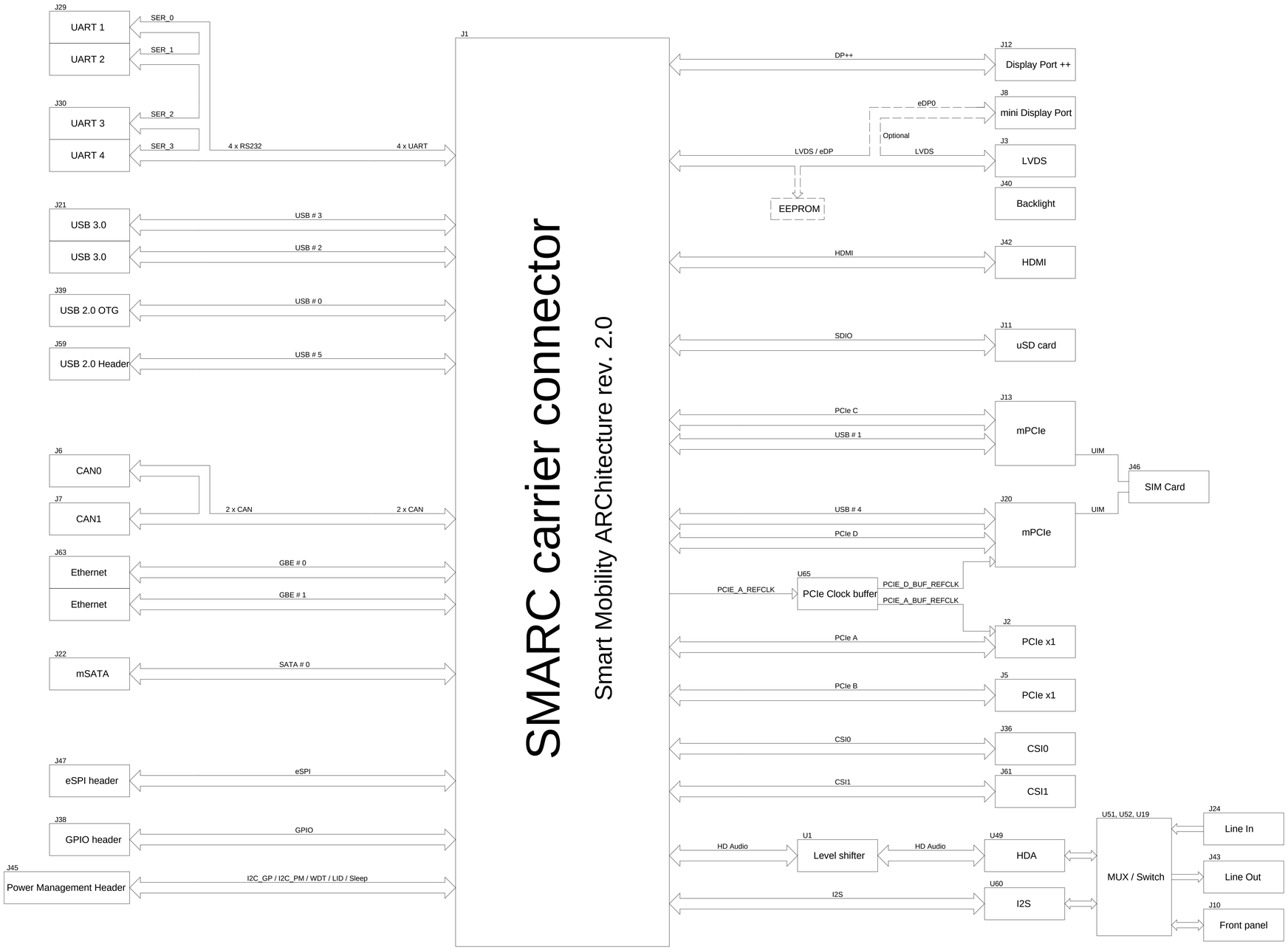
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	1 OF 30	SCH 1400	D00

Block Diagram



PROJECT	SMARC Eval 2.0				
	ADS2 - SMARC Eval 2.0				
BLOCK ID	Schematic1 (2 of 30)				
SHEET	02 Block Diagram				
		DIVISION	NAME	DATE YYYY-MM-DD	
	CREATED:	KEEDC	JM, JH ,MV	2017.11.17	
	VERIFIED:	KEEDC	MH	2017.11.20	
	APPROVED:				
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	2 OF 30	SCH 1400	D00

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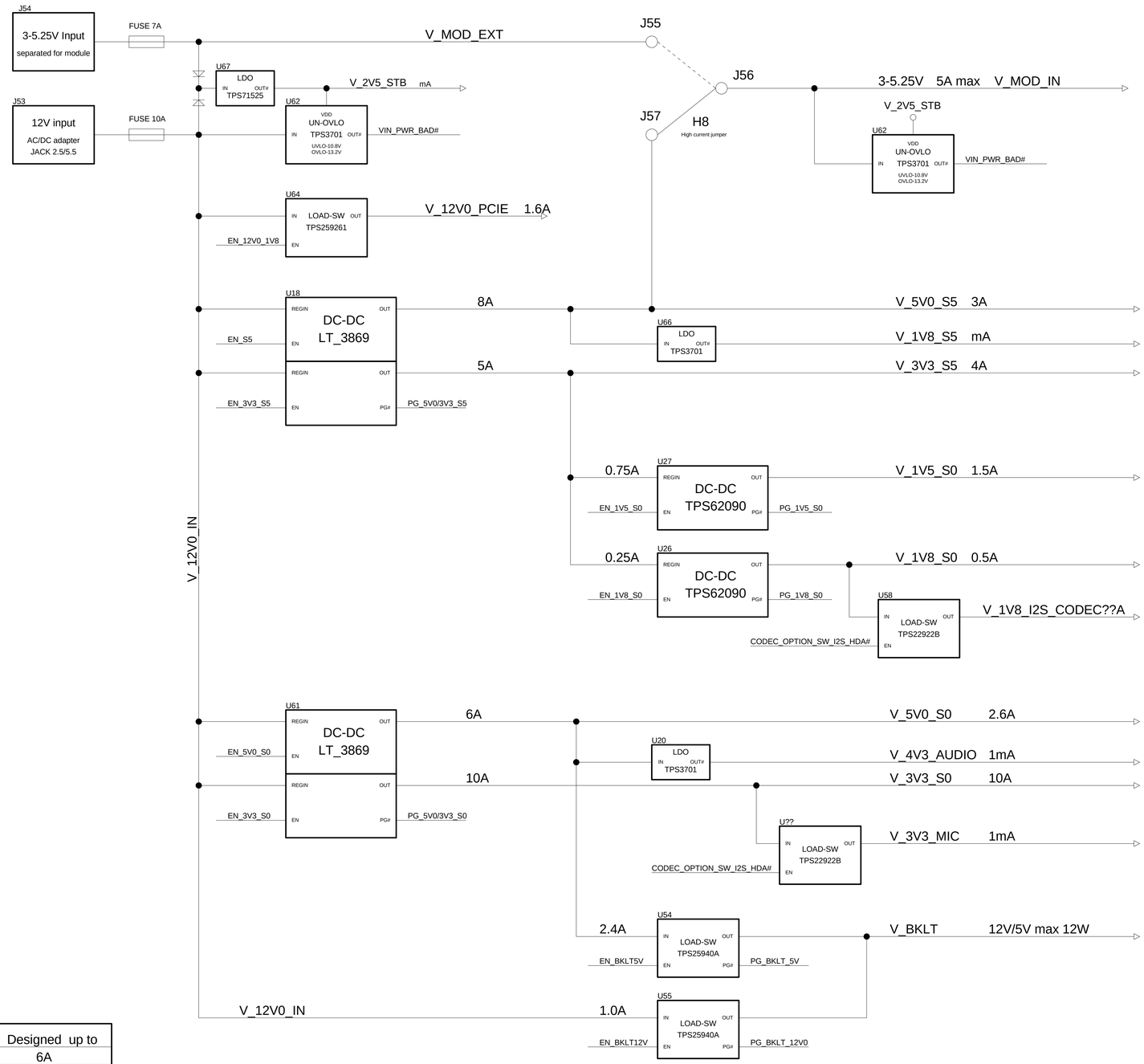
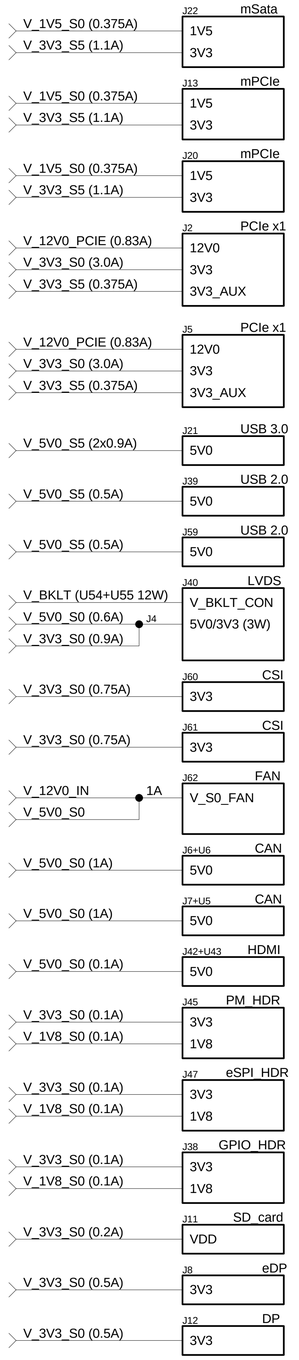
Power Diagram





Rail	Designed up to
V_5V0_S0	6A
V_5V0_S5	8A
V_3V3_S0	10A
V_3V3_S5	5A
V_1V8_S0	0.5
V_1V5_S0	1.5

PROJECT	SMARC Eval 2.0		
	ADS2 - SMARC Eval 2.0		
BLOCK ID	Schematic1 (3 of 30)		
SHEET	03 Power Diagram		
	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
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PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	3 OF 30	SCH 1400	D00

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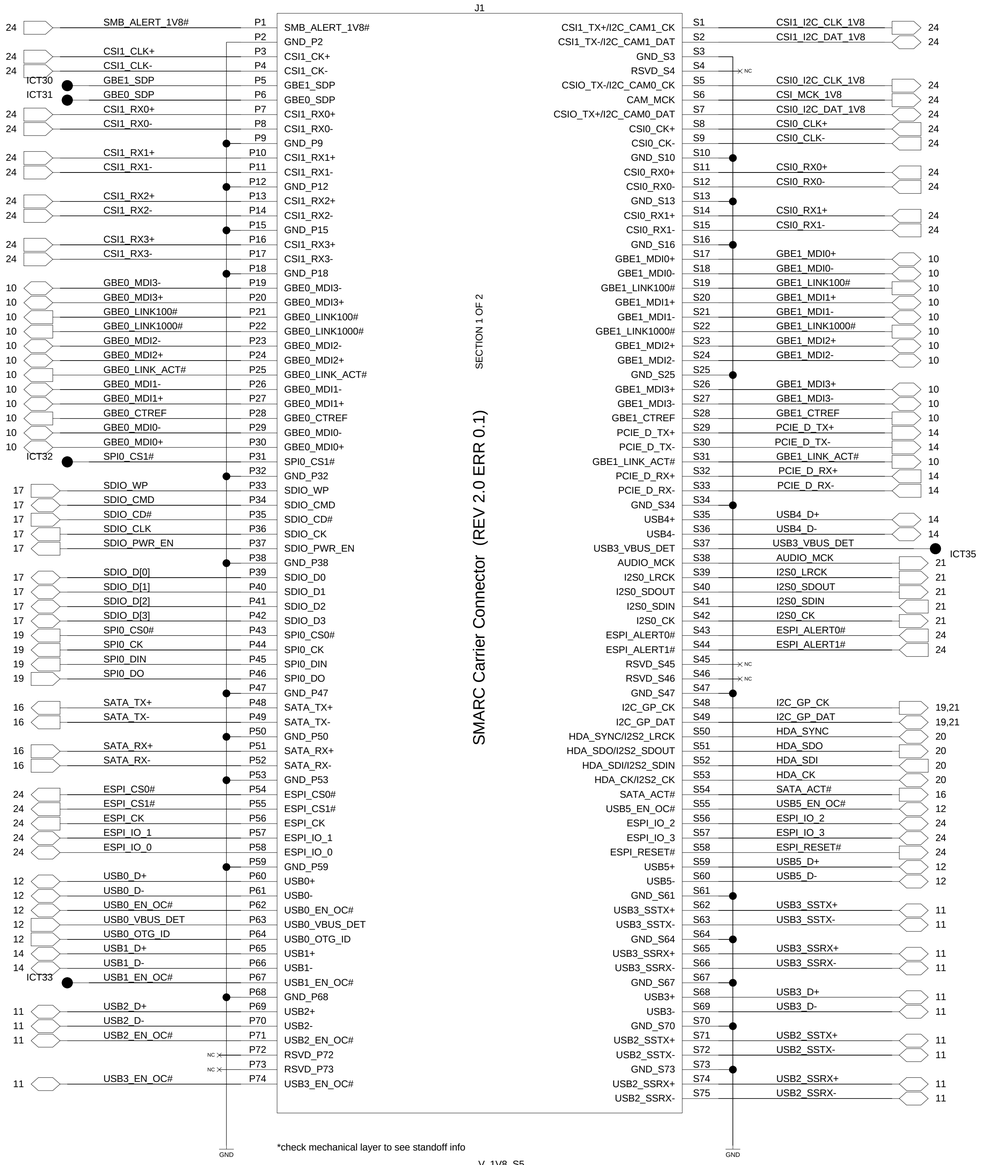
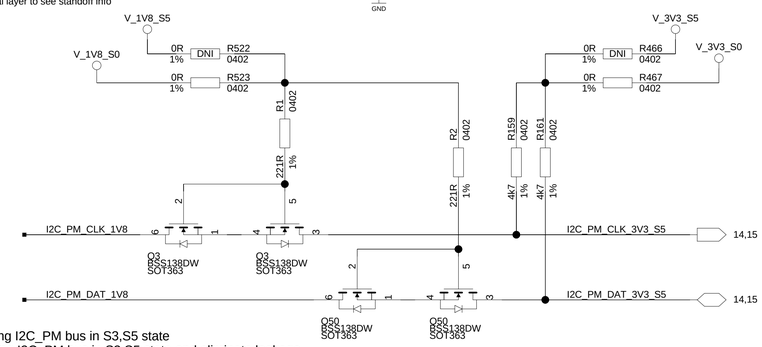
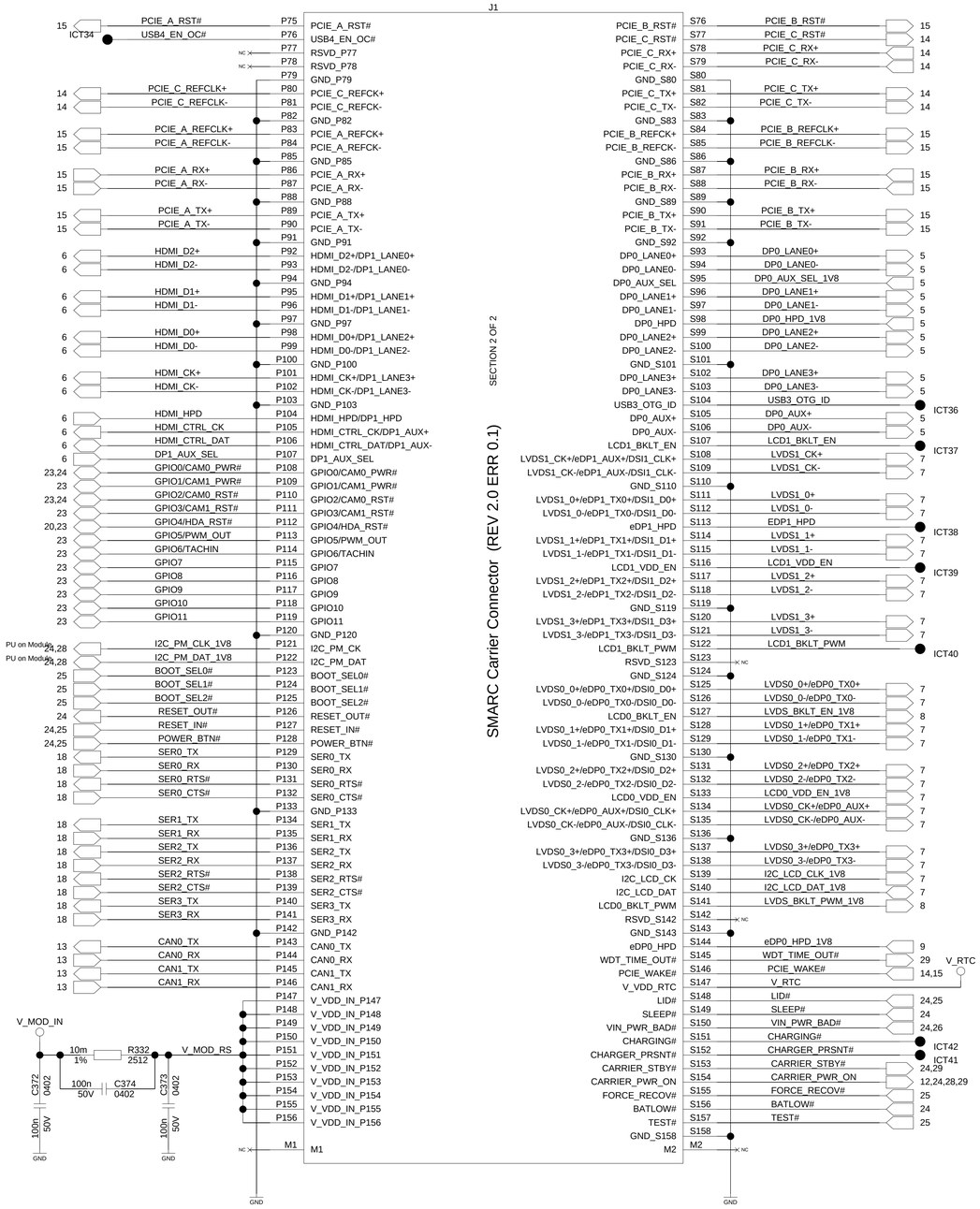
SMARC Connector





I2C_PM S5/S0 selection
Place R522, R466 for enabling I2C_PM bus in S3,S5 state
Place R523, R467 for disabling I2C_PM bus in S3,S5 state and eliminate leakage
Never place R522 and R523 at same time same as R466 with R467



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PROJECT	SMARC Eval 2.0		
	ADS2 - SMARC Eval 2.0		
BLOCK ID	Schematic1 (4 of 30)		
SHEET	04 SMARC con		
PCB ID	1062-0139	PCB INDEX	1400A
LAST MODIFIED	20/11/2017:15:03		
PAGE	4 OF 30		
DRAWING ID	SCH 1400	REV	D00

	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
VERIFIED:	KEEDC	MH	2017.11.20
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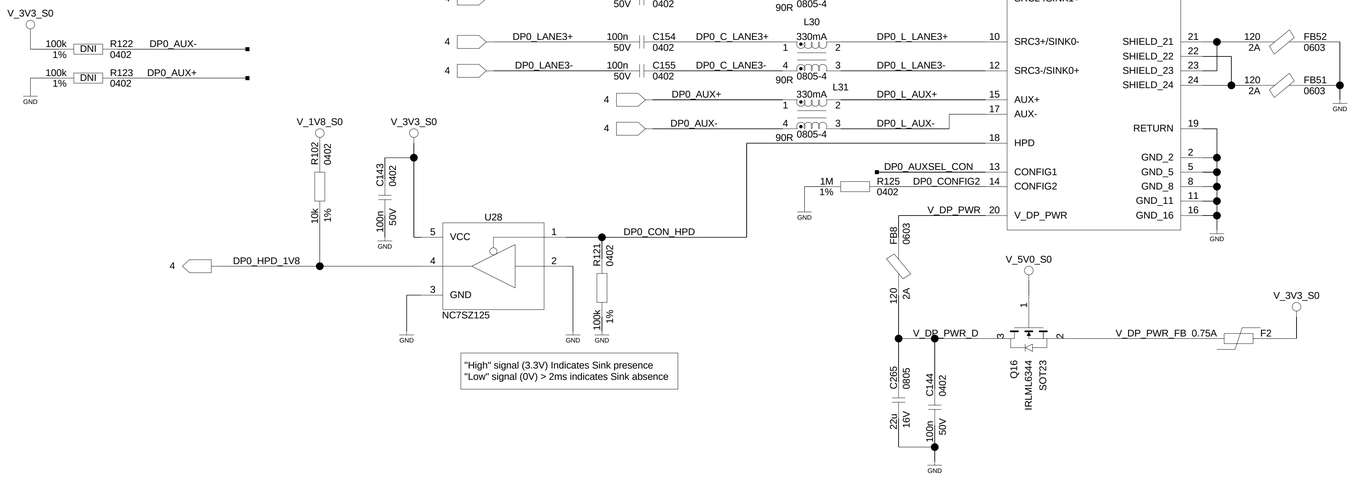
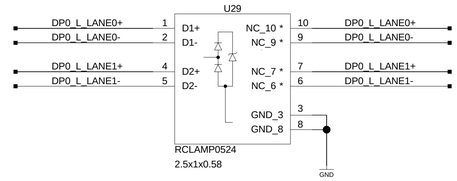
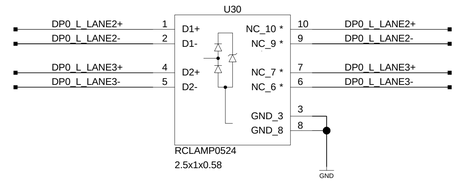
DP connector

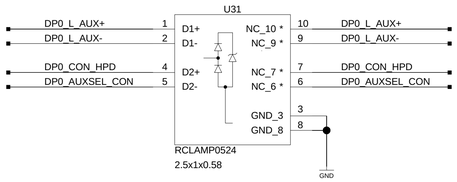


ESD protection

ZNL4
Place ESD Protection diodes close to connector







PROJECT: SMARC Eval 2.0 / ADS2 - SMARC Eval 2.0				kontron
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SHEET: 05 DP con	CREATED:	KEEDC	JM, JH ,MV	2017.11.17
	VERIFIED:	KEEDC	MH	2017.11.20
	APPROVED:			

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	5 OF 30	SCH 1400	D00

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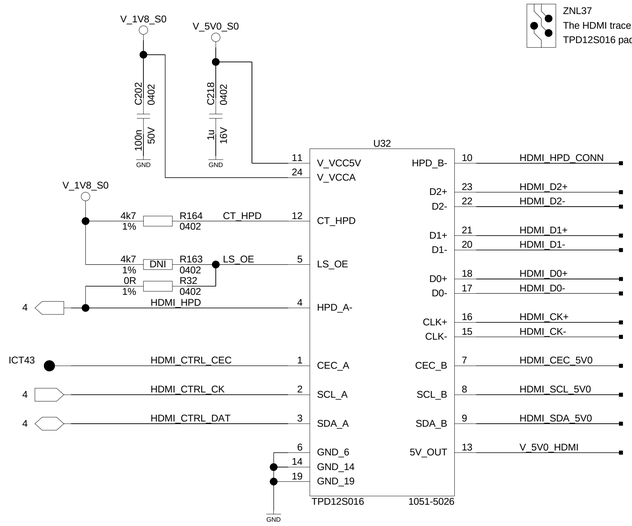
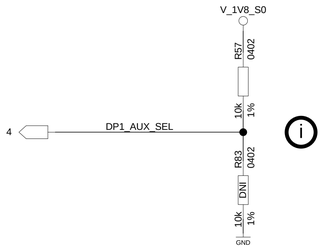
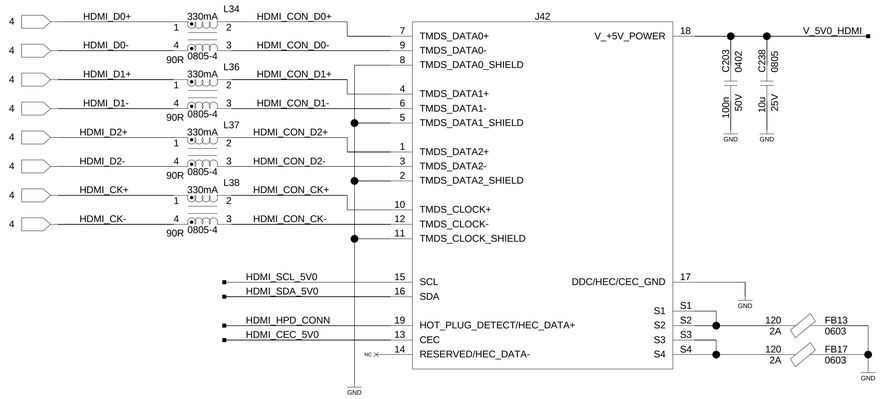
HDMI Connector

ZNL37
The HDMI trace pairs are to be routed from the SMARC connector, through the TPD12S016 pads and to the HDMI connector without any stubs





DP1_AUX_SEL setting:
HIGH: HDMI operation
LOW: DP1 operation



PROJECT	SMARC Eval 2.0				
	ADS2 - SMARC Eval 2.0				
BLOCK ID		DIVISION	NAME	DATE YYYY-MM-DD	
Schematic1 (6 of 30)		CREATED:	KEEDC	JM, JH ,MV	2017.11.17
SHEET		VERIFIED:	KEEDC	MH	2017.11.20
06 HDMI		APPROVED:			
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	6 OF 30	SCH 1400	D00

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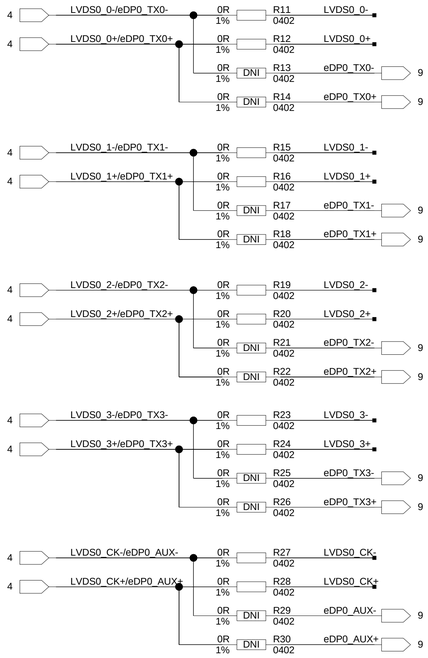
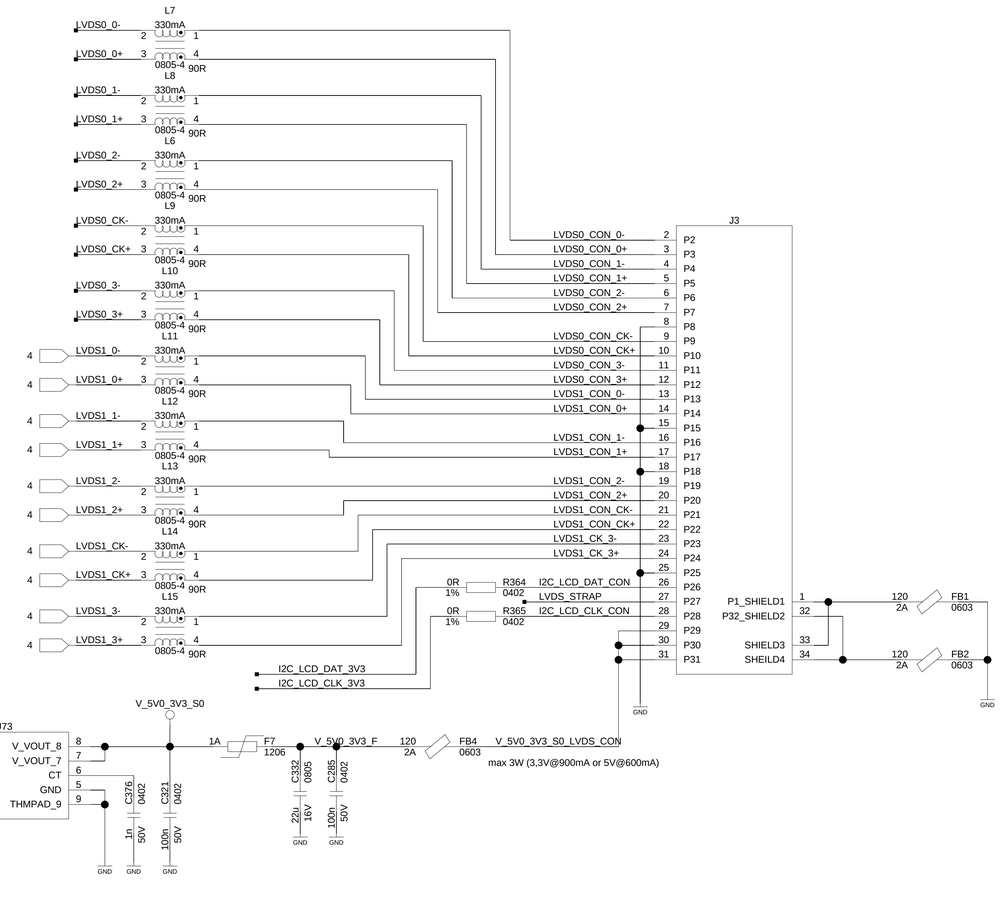
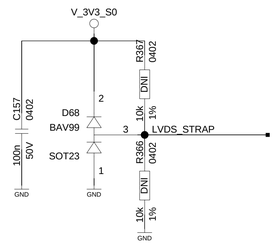
LVDS Data

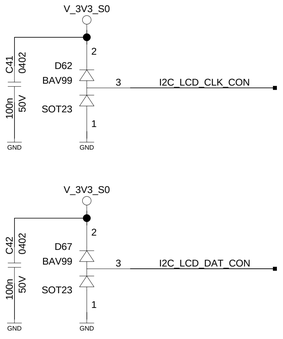
LVDS / eDP Option

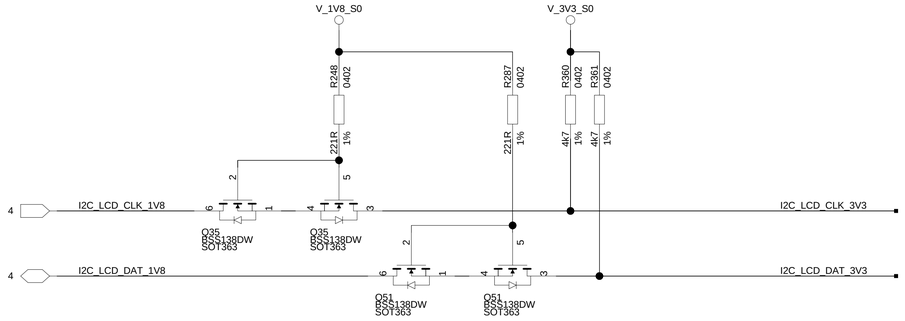
ZNL2
Place LVDS / eDP option resistors with shared common pad

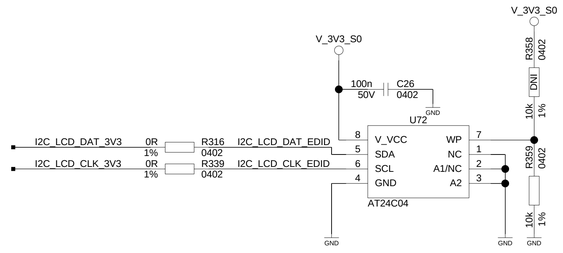












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PROJECT	SMARC Eval 2.0
	ADS2 - SMARC Eval 2.0
BLOCK ID	Schematic1 (7 of 30)
SHEET	07 LVDS

	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
VERIFIED:	KEEDC	MH	2017.11.20
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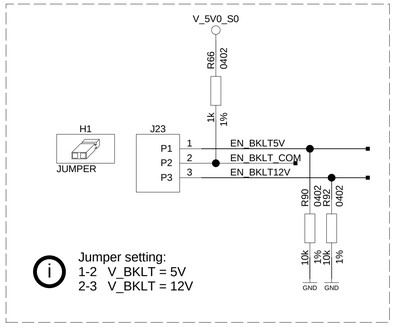
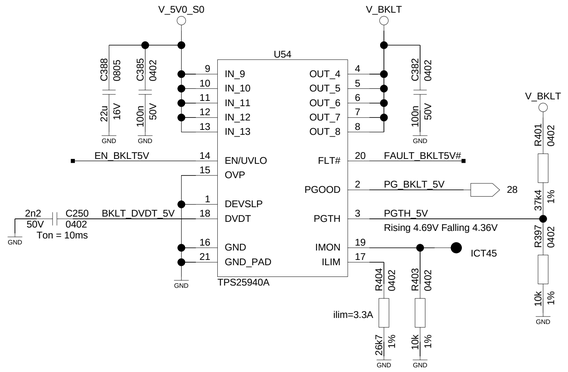
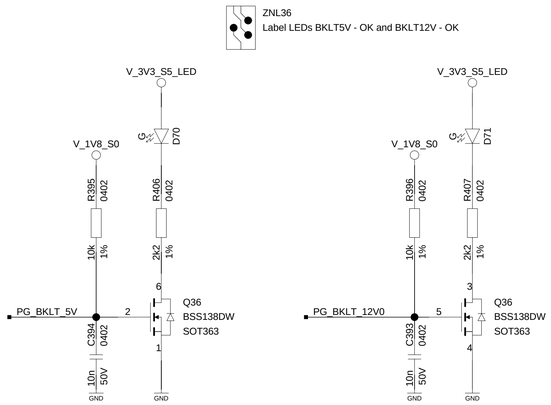
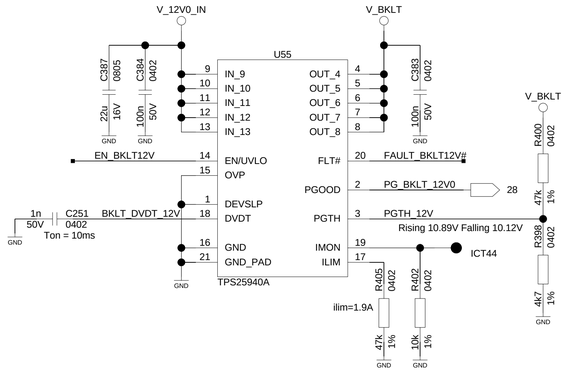
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	22/11/2017:12:31	7 OF 30	SCH 1400	D00

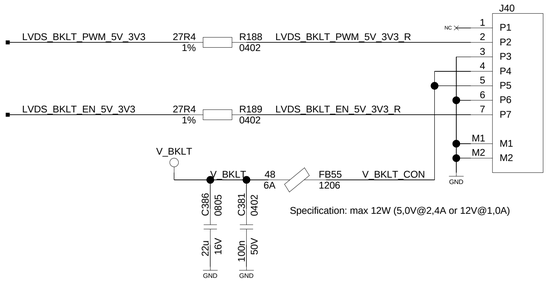
LVDS Backlight











PROJECT: SMARC Eval 2.0 / ADS2 - SMARC Eval 2.0			kontron
BLOCK ID: Schematic1 (8 of 30)		DIVISION / NAME / DATE YYYY-MM-DD	
SHEET: 08 LVDS Backlight		CREATED: KEEDC JM, JH ,MV 2017.11.17	
		VERIFIED: KEEDC MH 2017.11.20	
		APPROVED:	
PCB ID: 1062-0139	PCB INDEX: 1400A	LAST MODIFIED: 20/11/2017:15:03	
PAGE: 8 OF 30	DRAWING ID: SCH 1400	REV: D00	

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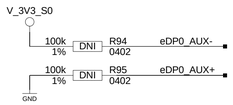
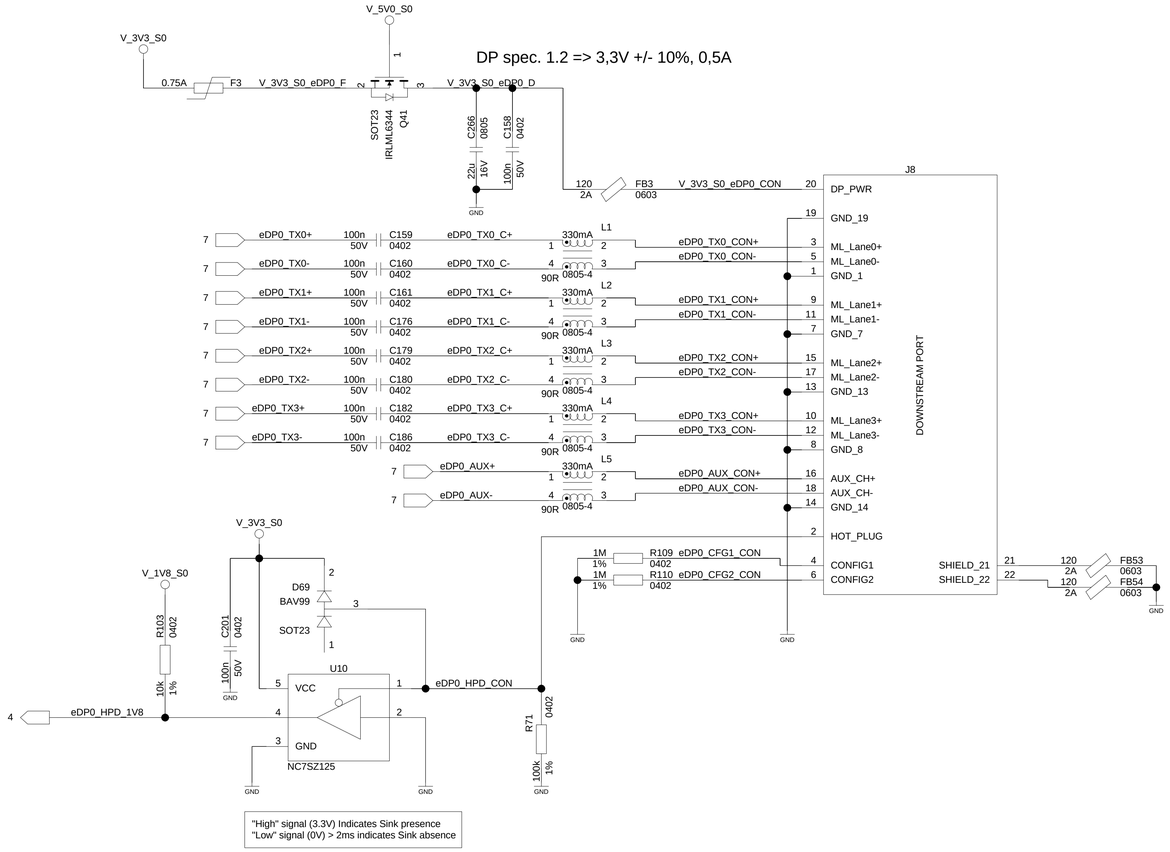
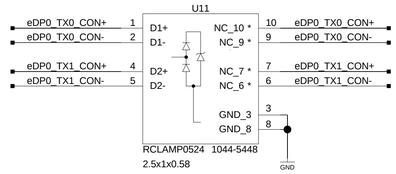
eDP connector



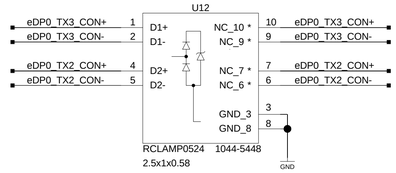


ESD protection

ZNL1
Place ESD Protection diodes close to connector



See datasheet for details on (*)



See datasheet for details on (*)

PROJECT: SMARC Eval 2.0 / ADS2 - SMARC Eval 2.0			kontron
BLOCK ID: Schematic1 (9 of 30)		DIVISION	NAME / DATE YYYY-MM-DD
SHEET: 09 eDP con	CREATED:	KEEDC	JM, JH ,MV 2017.11.17
	VERIFIED:	KEEDC	MH 2017.11.20
	APPROVED:		

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	9 OF 30	SCH 1400	D00

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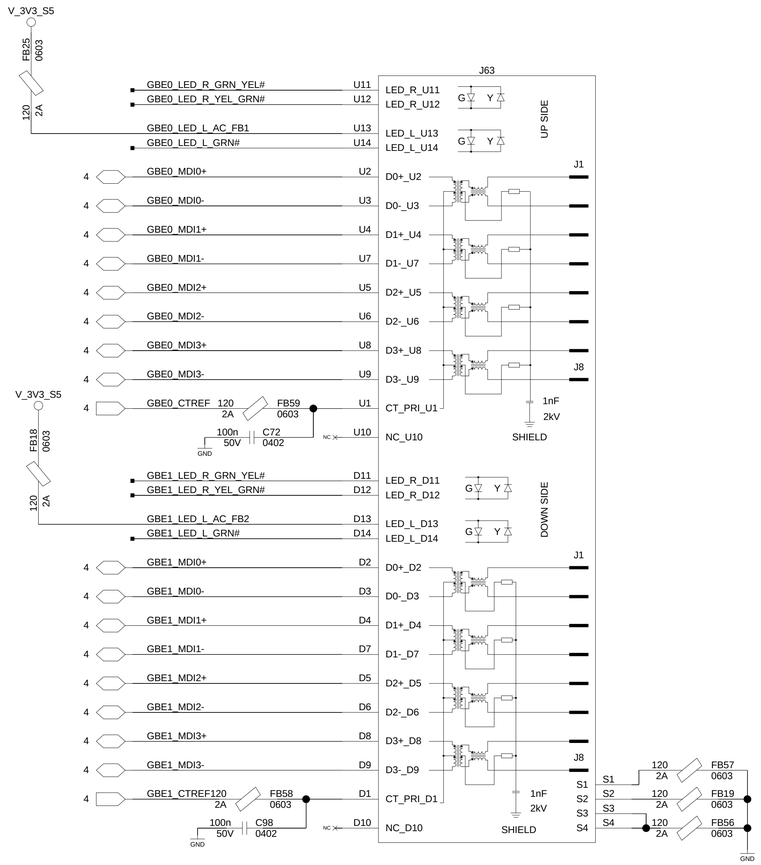
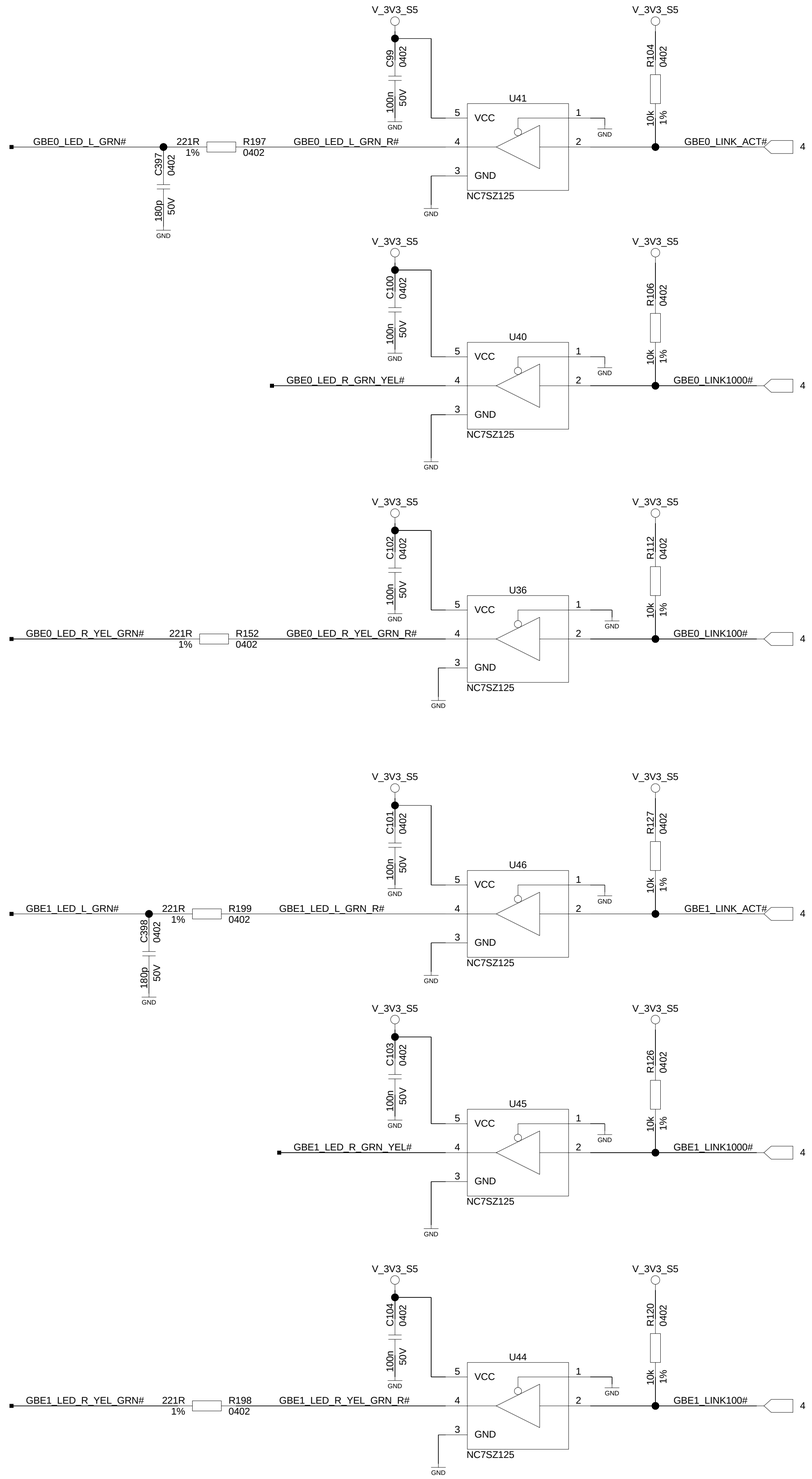
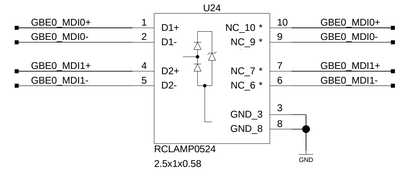
Ethernet Connectors





ESD protection acording IEC 61000-4-2

ZNL5
Place ESD Protection diodes close to connector



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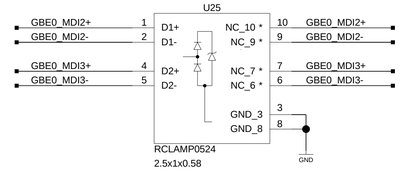
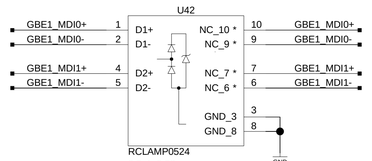
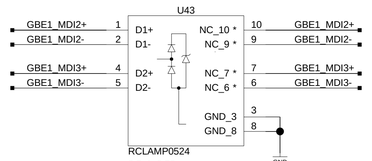


See datasheet for details on (*)



See datasheet for details on (*)



See datasheet for details on (*)

PROJECT	SMARC Eval 2.0		
	ADS2 - SMARC Eval 2.0		
BLOCK ID		DIVISION	NAME	DATE YYYY-MM-DD
Schematic1 (10 of 30)		CREATED: KEEDC	JM, JH ,MV	2017.11.17
SHEET		VERIFIED: KEEDC	MH	2017.11.20
10 ETH 0-1		APPROVED:		
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	10 OF 30	SCH 1400	D00

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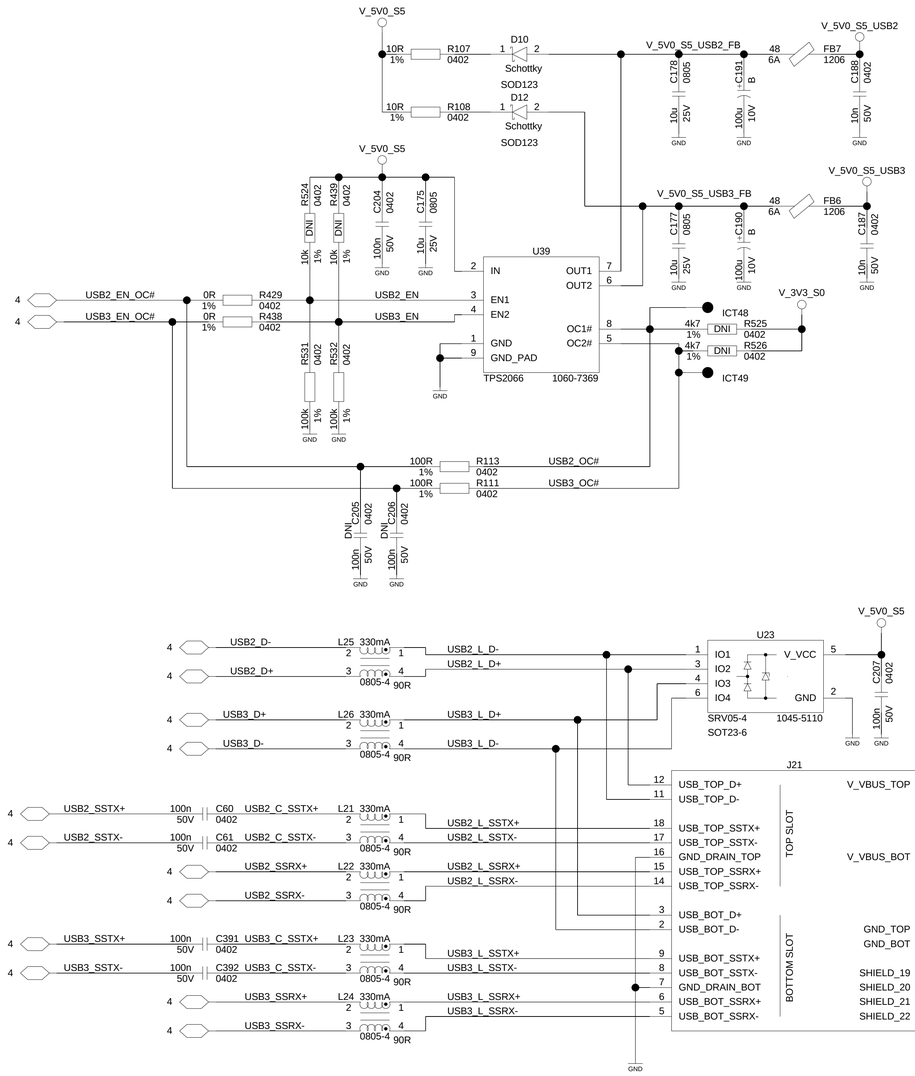
Refer to ERP BOM and assembly instruction for build values.

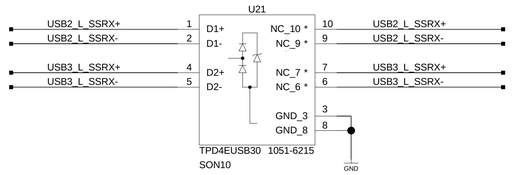
Created using CAD MGC VX 1.1

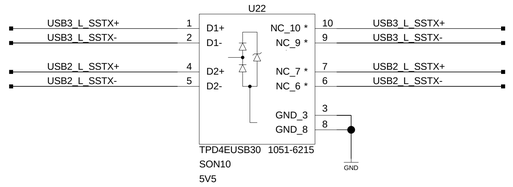
USB 3.0 Connectors



ESD protection

ZNL3
Place ESD Protection diodes close to connector





PROJECT	SMARC Eval 2.0		
	ADS2 - SMARC Eval 2.0		
BLOCK ID		DIVISION	NAME / DATE YYYY-MM-DD
Schematic1 (11 of 30)		CREATED: KEEDC	JM, JH ,MV 2017.11.17
SHEET		VERIFIED: KEEDC	MH 2017.11.20
11 USB 30		APPROVED:	

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	11 OF 30	SCH 1400	D00

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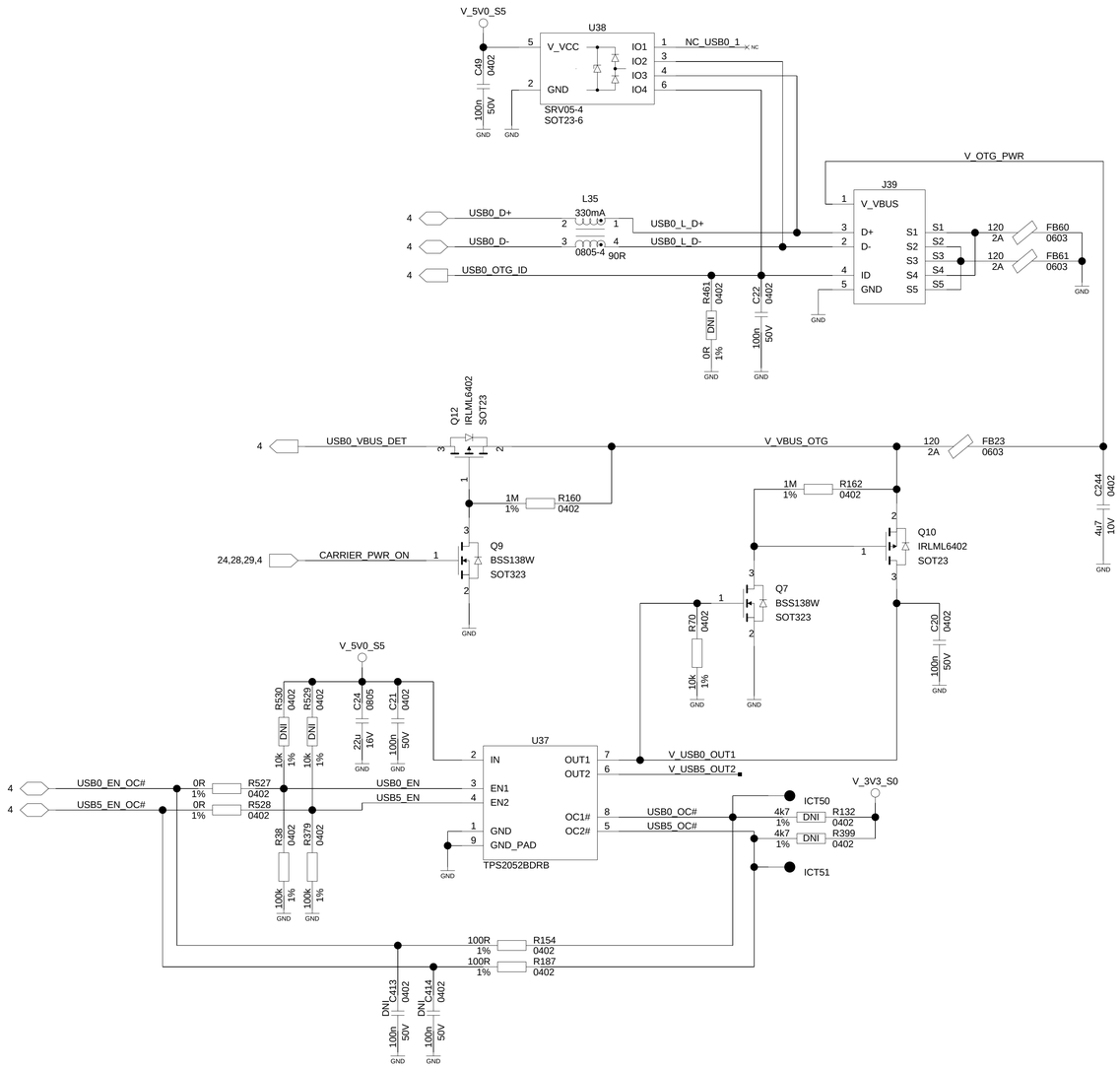
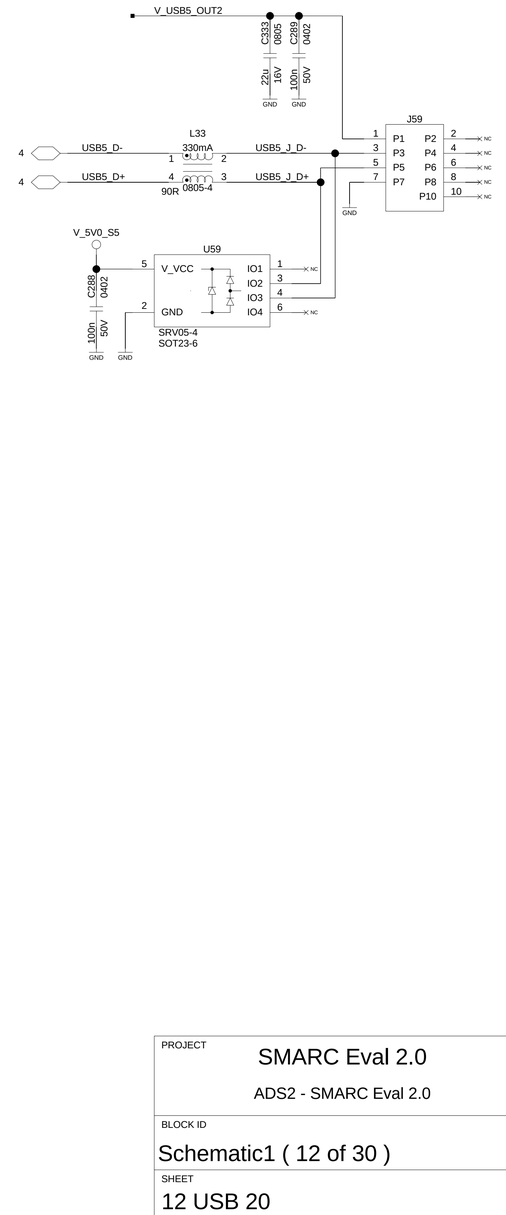
Created using CAD MGC VX 1.1

USB 2.0 OTG Connector



USB 2.0 Header



PROJECT: SMARC Eval 2.0 / ADS2 - SMARC Eval 2.0					kontron
BLOCK ID: Schematic1 (12 of 30)		DIVISION	NAME	DATE YYYY-MM-DD	
SHEET: 12 USB 20	CREATED:	KEEDC	JM, JH ,MV	2017.11.17	
	VERIFIED:	KEEDC	MH	2017.11.20	
	APPROVED:				

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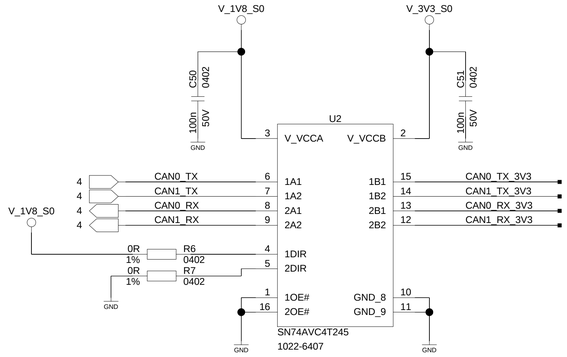
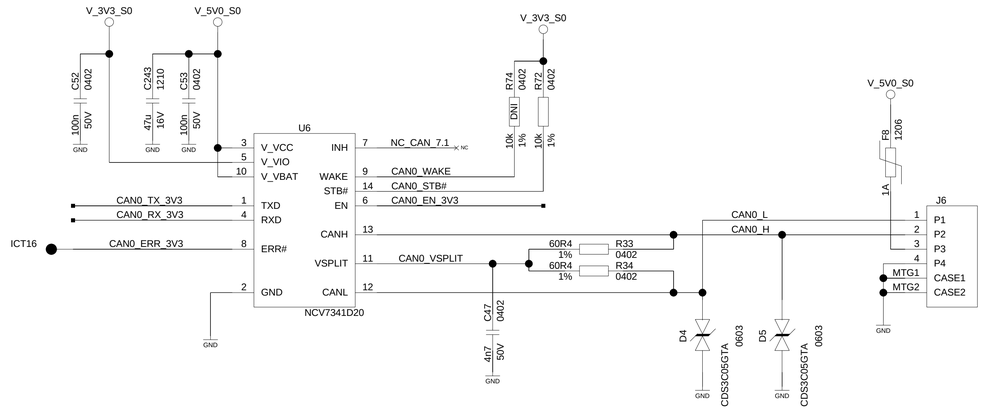
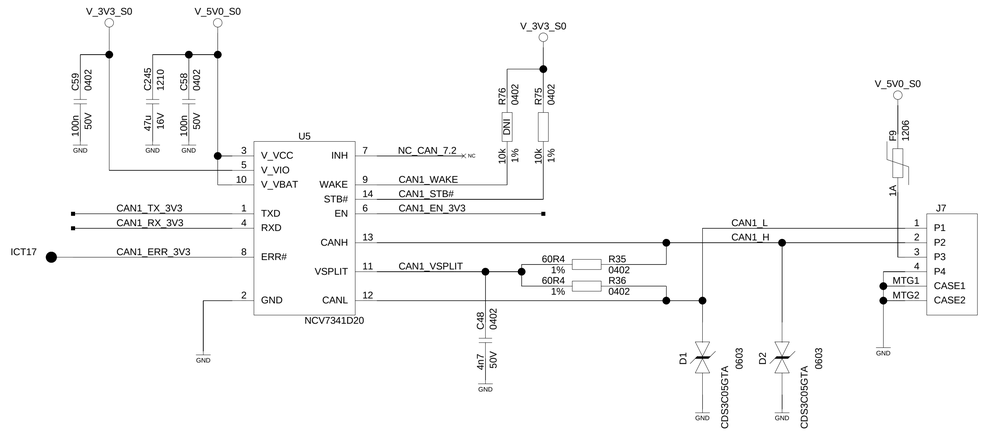
Created using CAD MGC VX 1.1

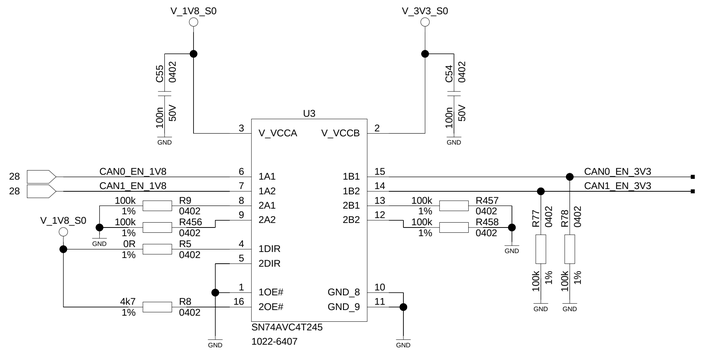
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	12 OF 30	SCH 1400	D00

CAN Transceivers









PROJECT	SMARC Eval 2.0				
	ADS2 - SMARC Eval 2.0				
BLOCK ID		DIVISION	NAME	DATE YYYY-MM-DD	
Schematic1 (13 of 30)		CREATED: KEEDC	JM, JH ,MV	2017.11.17	
SHEET		VERIFIED: KEEDC	MH	2017.11.20	
13 CAN con		APPROVED:			
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	13 OF 30	SCH 1400	D00

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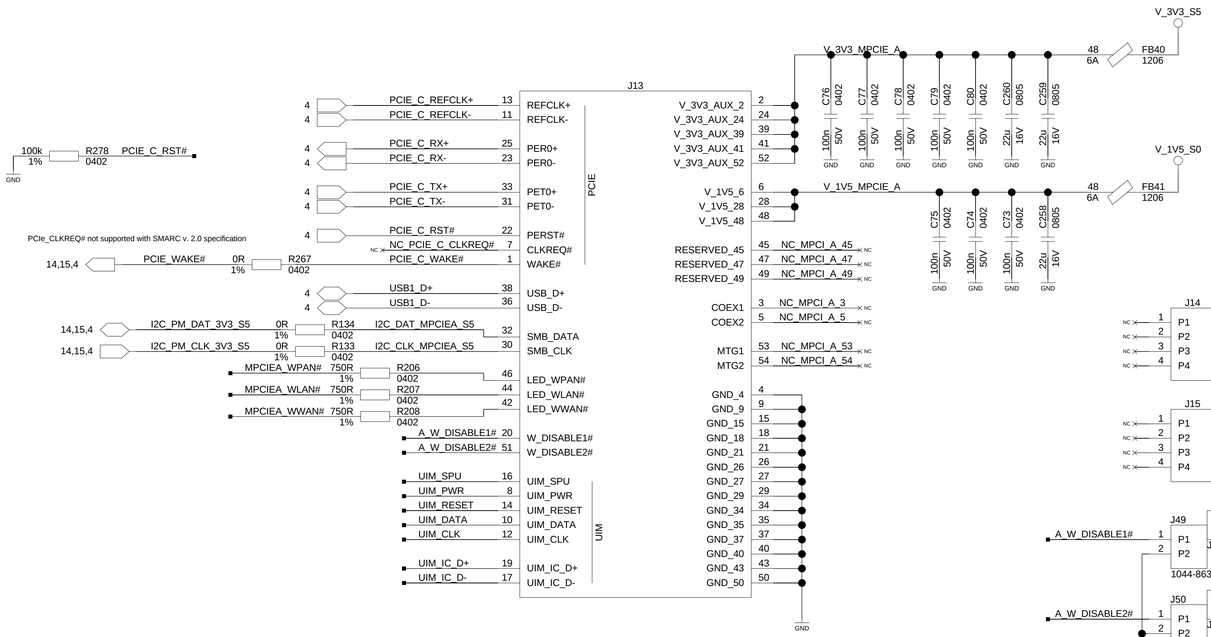
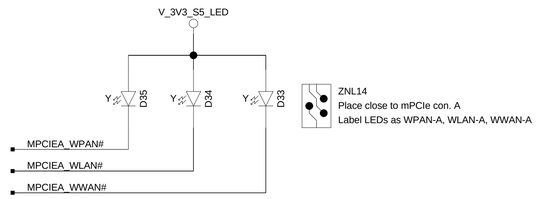
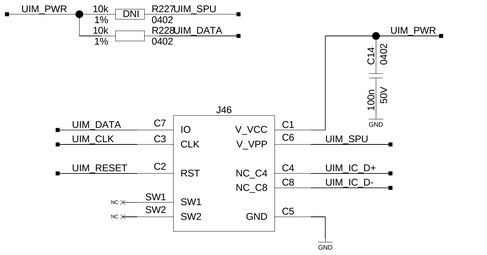
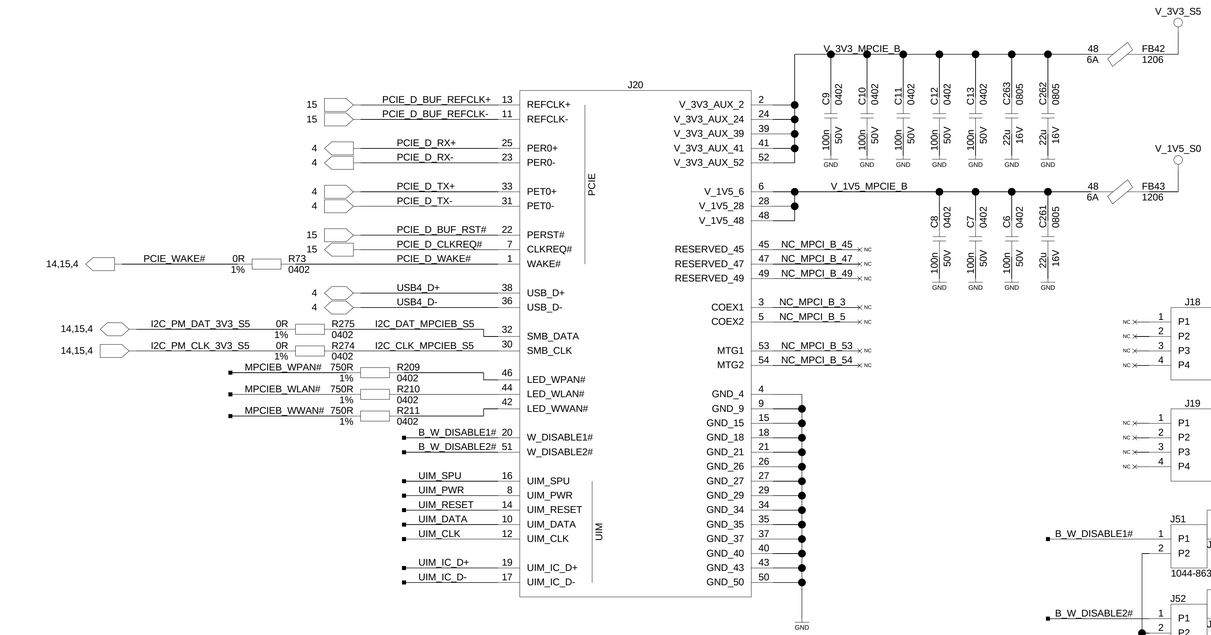
Created using CAD MGC VX 1.1

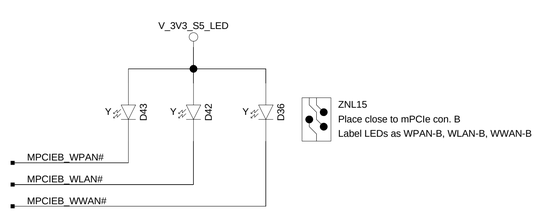
mPCIe Connectors











PROJECT: SMARC Eval 2.0 / ADS2 - SMARC Eval 2.0			kontron
BLOCK ID: Schematic1 (14 of 30)		DIVISION / NAME / DATE YYYY-MM-DD	
SHEET: 14 mPCIe	CREATED:	KEEDC / JM, JH ,MV / 2017.11.17	
	VERIFIED:	KEEDC / MH / 2017.11.20	
	APPROVED:		

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	01/12/2017:10:39	14 OF 30	SCH 1400	D00

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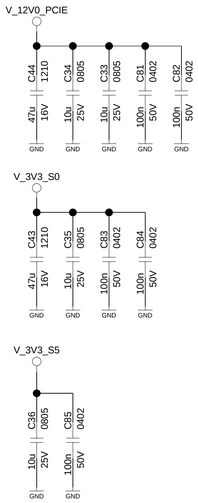
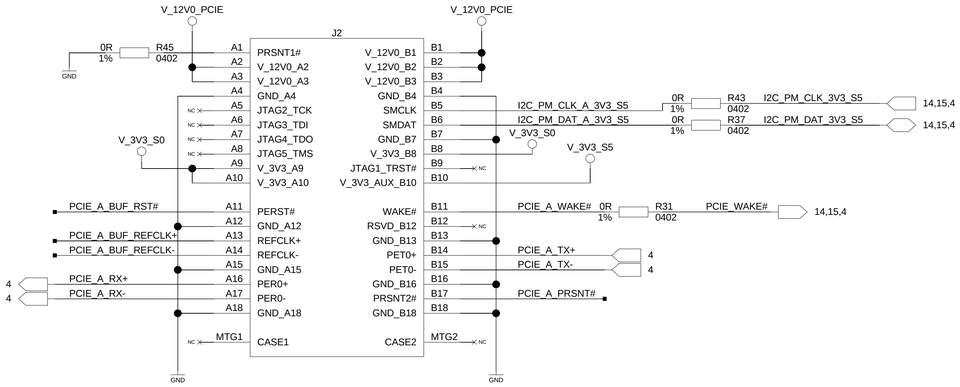
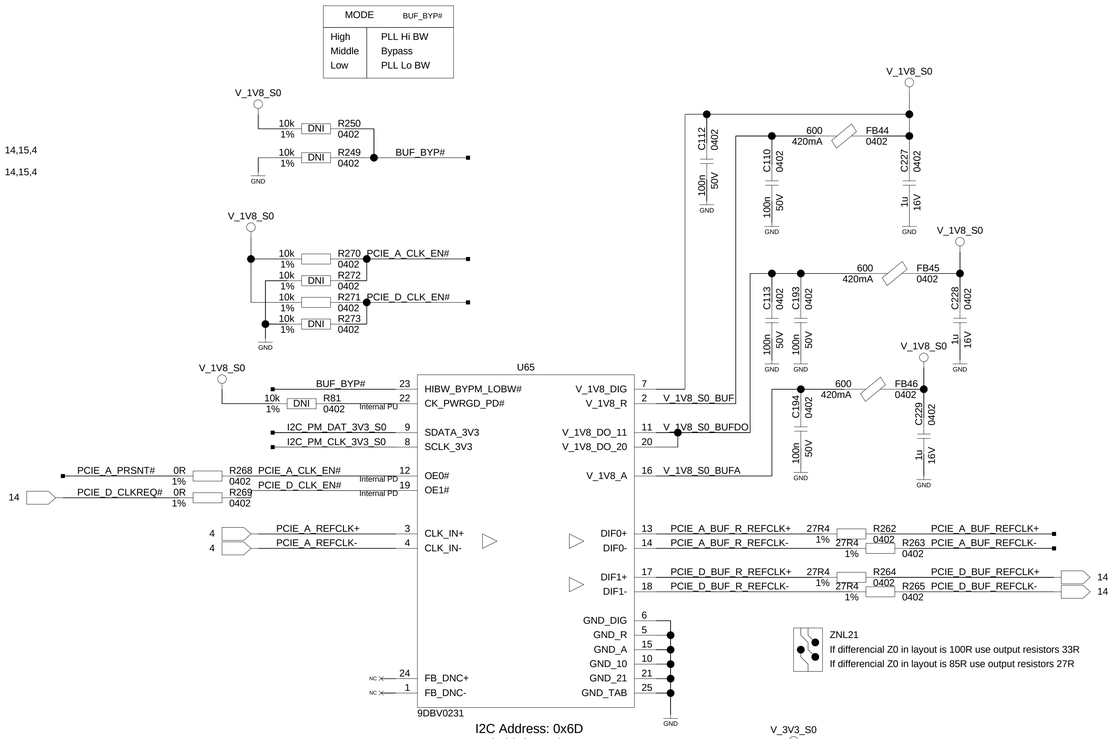
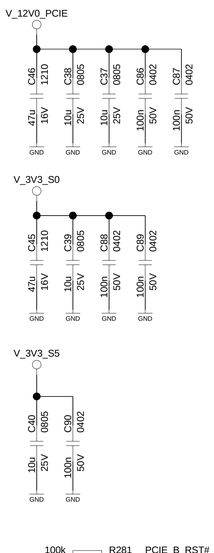
Created using CAD MGC VX 1.1

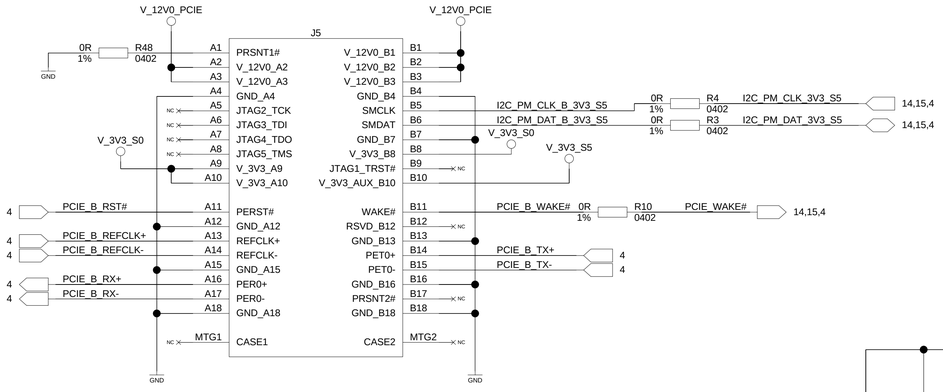
PCIe x1 Connectors, Clock Buffer

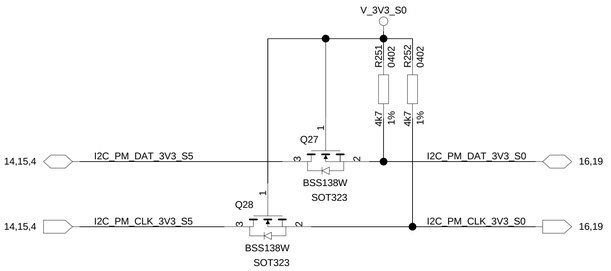


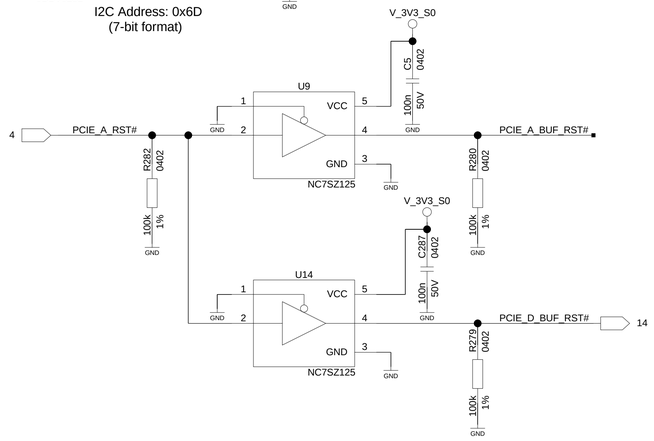












PROJECT	SMARC Eval 2.0 ADS2 - SMARC Eval 2.0
BLOCK ID	Schematic1 (15 of 30)
SHEET	15 PCIe x1 Clock Buffer

kontron

	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
VERIFIED:	KEEDC	MH	2017.11.20
APPROVED:			

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	15 OF 30	SCH 1400	D00

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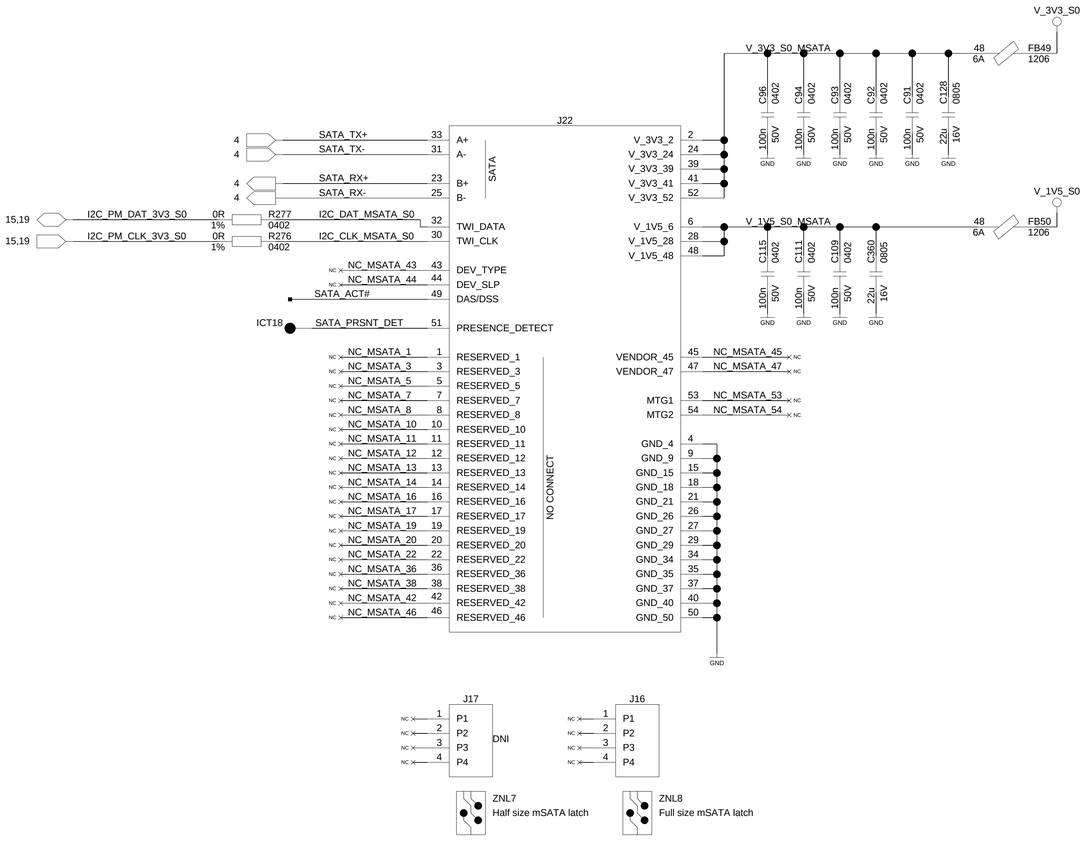
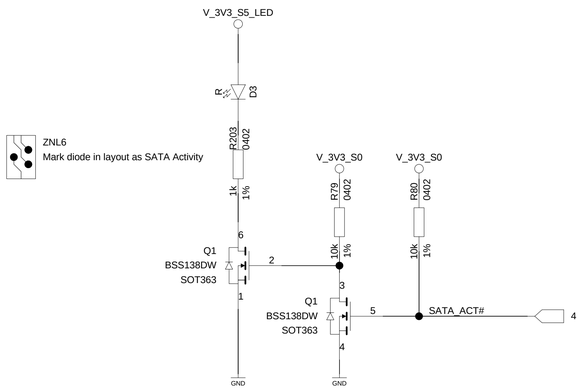
Created using CAD MGC VX 1.1

mSATA Connector





PROJECT: SMARC Eval 2.0			
ADS2 - SMARC Eval 2.0			
BLOCK ID: Schematic1 (16 of 30)			
SHEET: 16 mSATA			
	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
VERIFIED:	KEEDC	MH	2017.11.20
APPROVED:			
PCB ID: 1062-0139	PCB INDEX: 1400A	LAST MODIFIED: 20/11/2017:15:03	
PAGE: 16 OF 30	DRAWING ID: SCH 1400	REV: D00	

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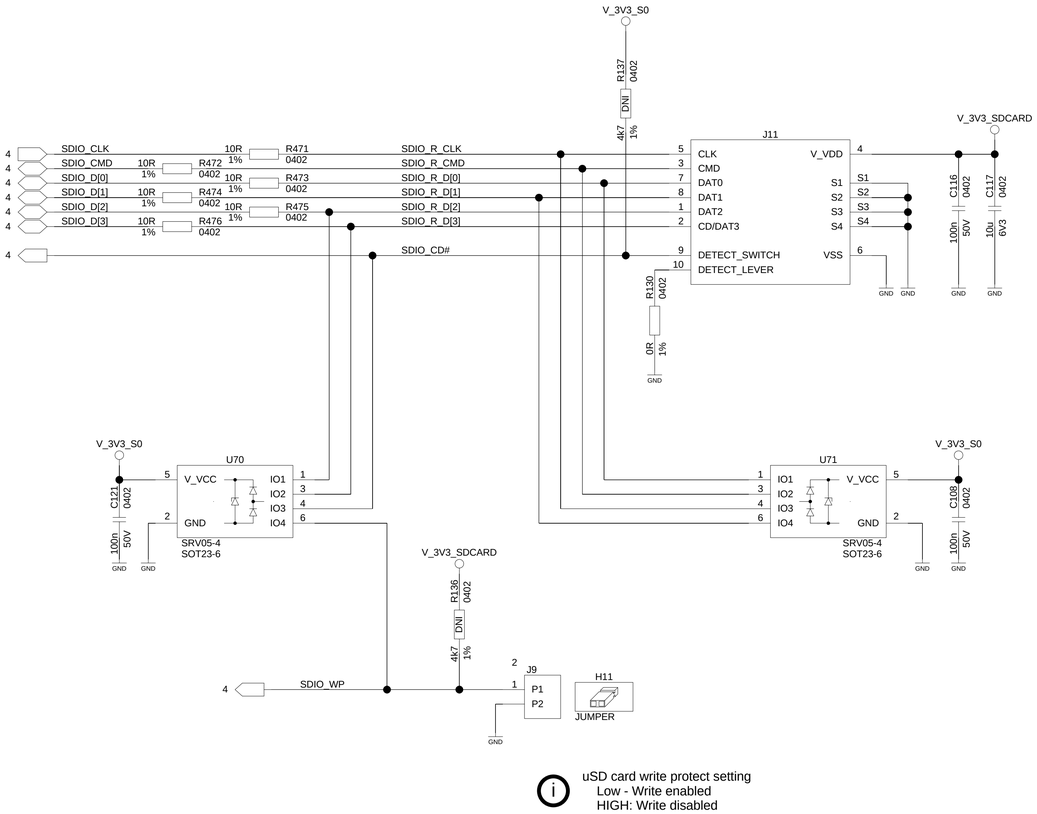
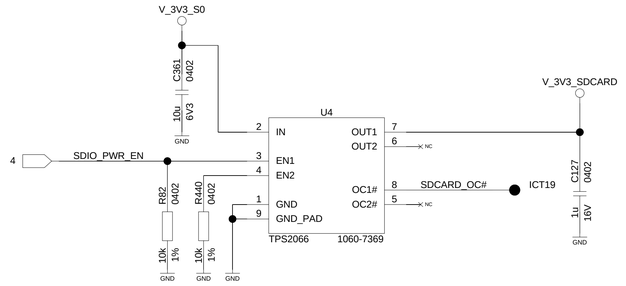
Refer to ERP BOM and assembly instruction for build values.

Created using CAD MGC VX 1.1

uSD Connector





DISCHARGE

uSD card write protect setting
Low - Write enabled
HIGH: Write disabled

PROJECT: SMARC Eval 2.0 / ADS2 - SMARC Eval 2.0			kontron
BLOCK ID: Schematic1 (17 of 30)		DIVISION / NAME / DATE YYYY-MM-DD	
SHEET: 17 uSD		CREATED: KEEDC JM, JH ,MV 2017.11.17	
		VERIFIED: KEEDC MH 2017.11.20	
		APPROVED:	
PCB ID: 1062-0139	PCB INDEX: 1400A	LAST MODIFIED: 20/11/2017:15:03	
PAGE: 17 OF 30		DRAWING ID: SCH 1400	REV: D00

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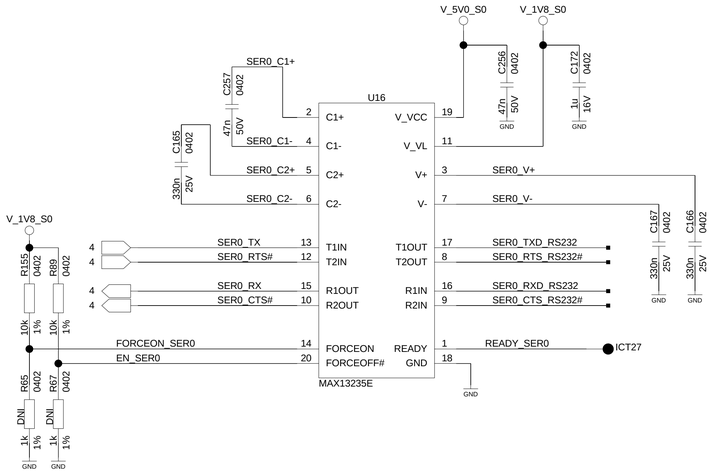
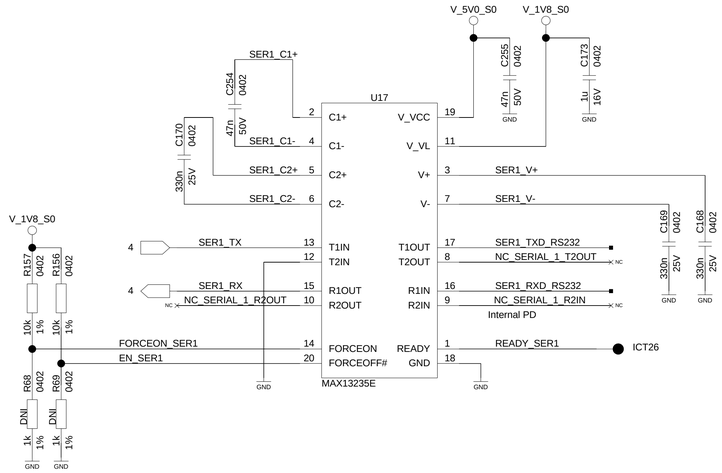
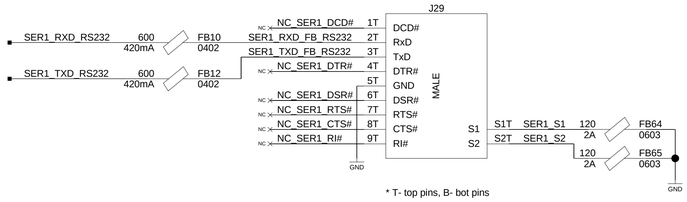
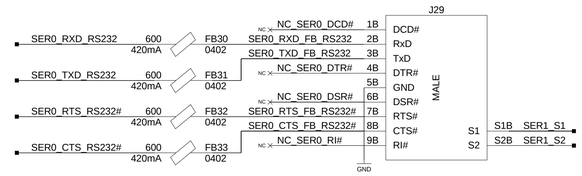
Created using CAD MGC VX 1.1

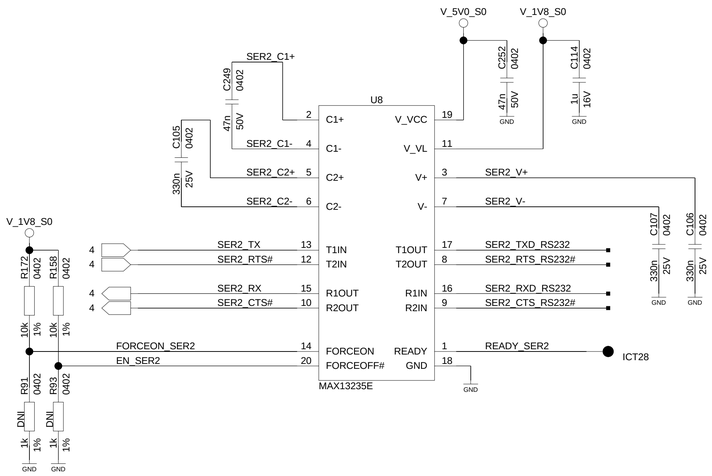
High Speed Serial Ports

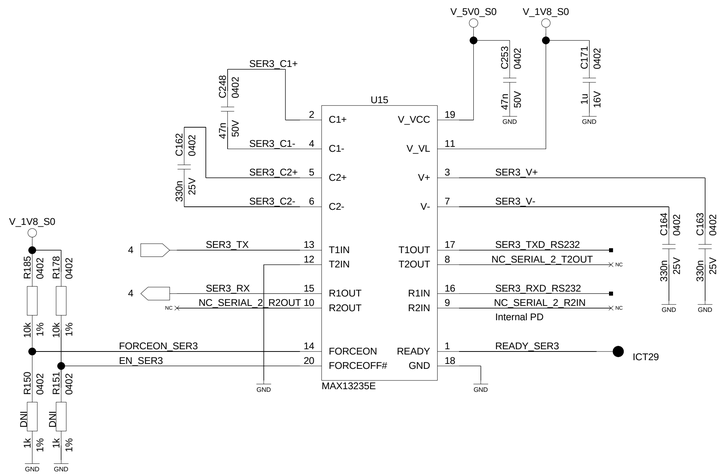


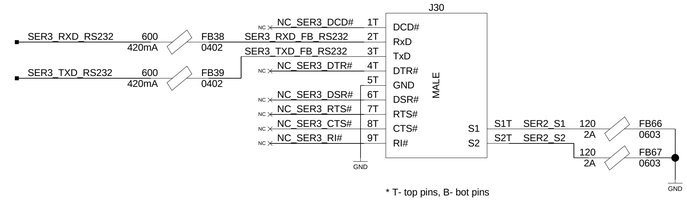


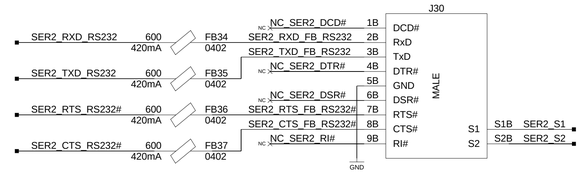












PROJECT	SMARC Eval 2.0		
	ADS2 - SMARC Eval 2.0		
BLOCK ID	Schematic1 (18 of 30)		
SHEET	18 High Speed Serial Ports		

	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
VERIFIED:	KEEDC	MH	2017.11.20
APPROVED:			

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	18 OF 30	SCH 1400	D00

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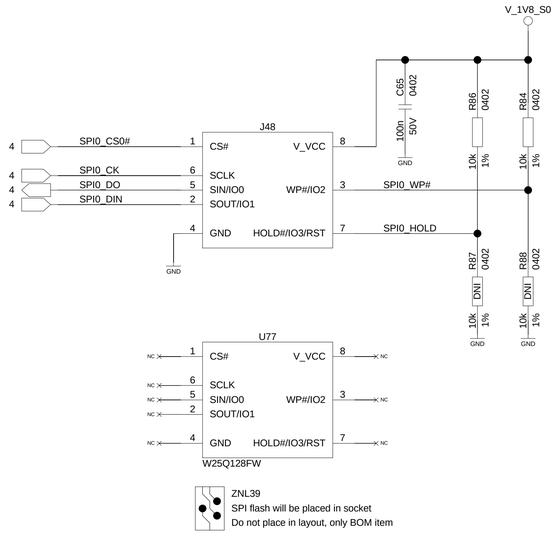
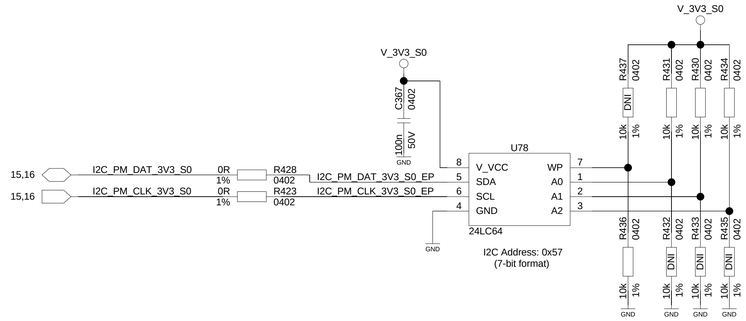
Created using CAD MGC VX 1.1

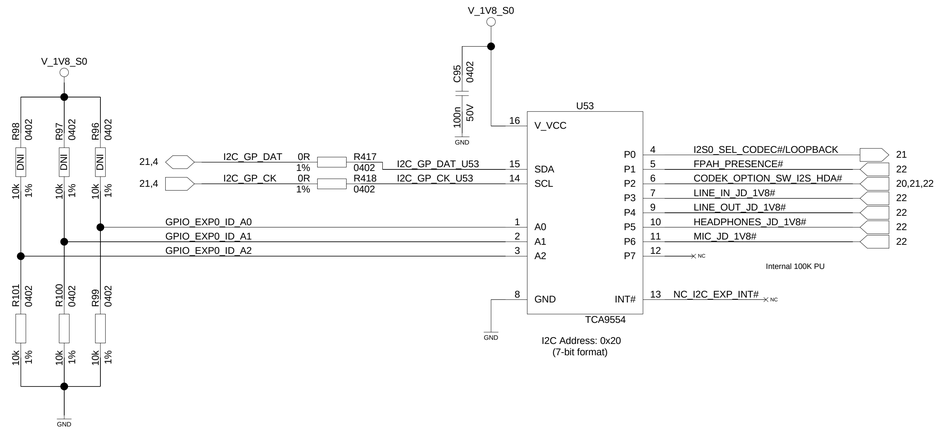
SPI Flash Socket



General Purposed I2C EEPROM



I2C Expander



PROJECT: SMARC Eval 2.0 / ADS2 - SMARC Eval 2.0					kontron
BLOCK ID: Schematic1 (19 of 30)		DIVISION	NAME	DATE YYYY-MM-DD	
SHEET: 19 SPI Flash Socket I2C Epander	CREATED:	KEEDC	JM, JH ,MV	2017.11.17	
	VERIFIED:	KEEDC	MH	2017.11.20	
	APPROVED:				

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	19 OF 30	SCH 1400	D00

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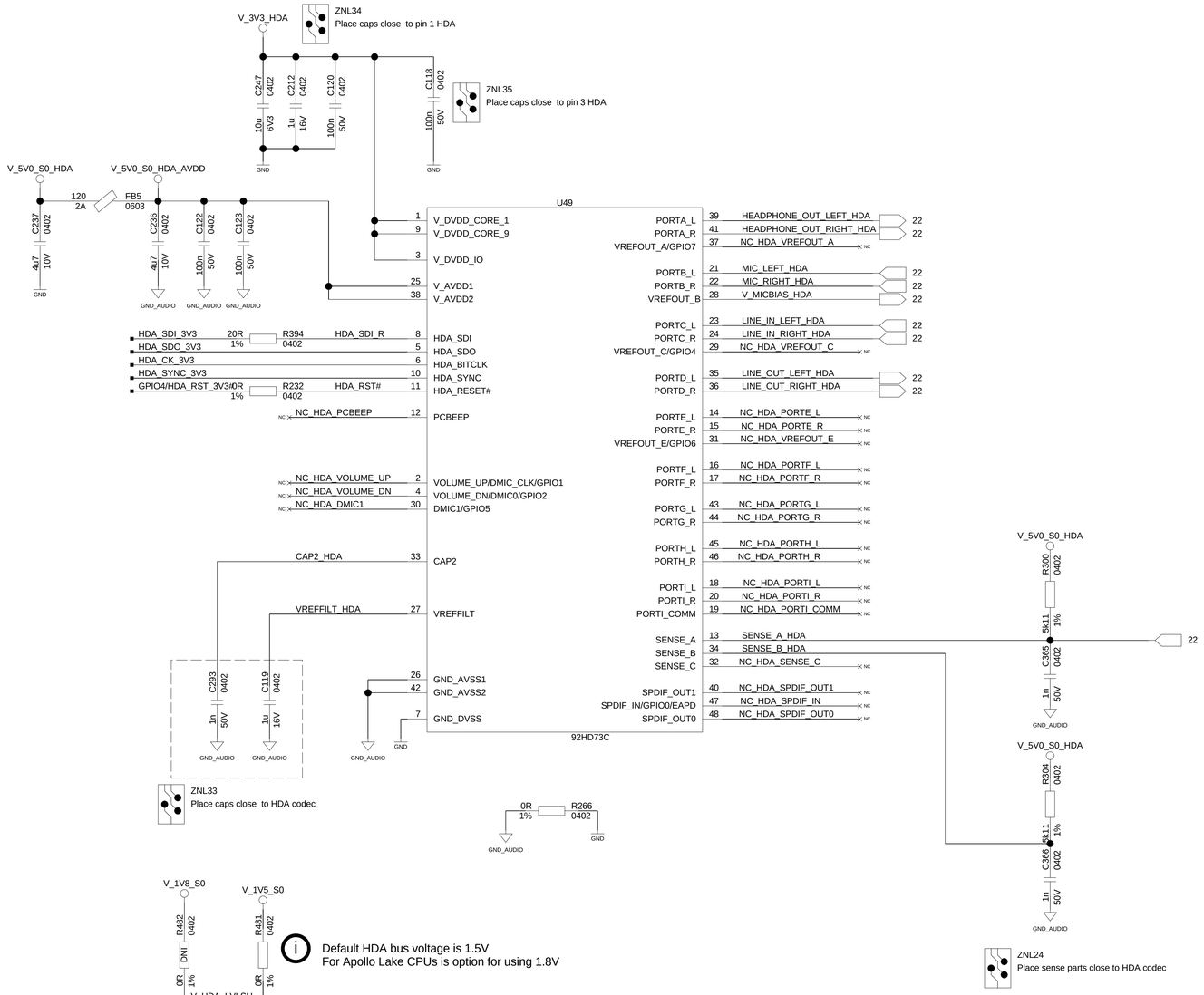
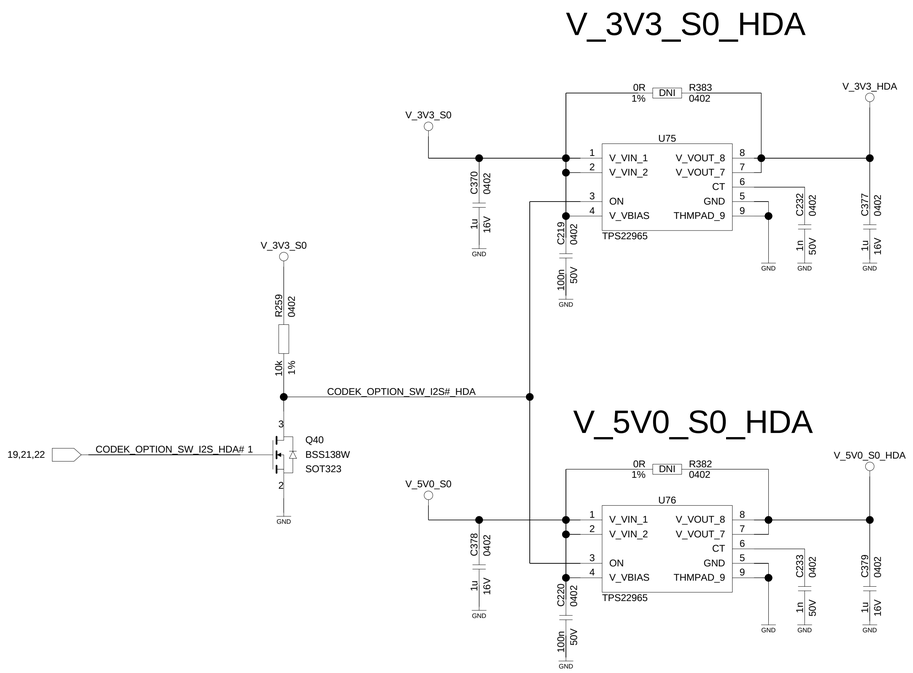
Created using CAD MGC VX 1.1

Audio HDA Codec





PROJECT	SMARC Eval 2.0 ADS2 - SMARC Eval 2.0	kontron	
BLOCK ID	Schematic1 (20 of 30)	DIVISION / NAME / DATE YYYY-MM-DD	
		CREATED: KEEDC JM, JH ,MV 2017.11.17	
SHEET	20 Audio - HDA Codec	VERIFIED: KEEDC MH 2017.11.20	
		APPROVED:	

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	20 OF 30	SCH 1400	D00

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Refer to ERP BOM and assembly instruction for build values.

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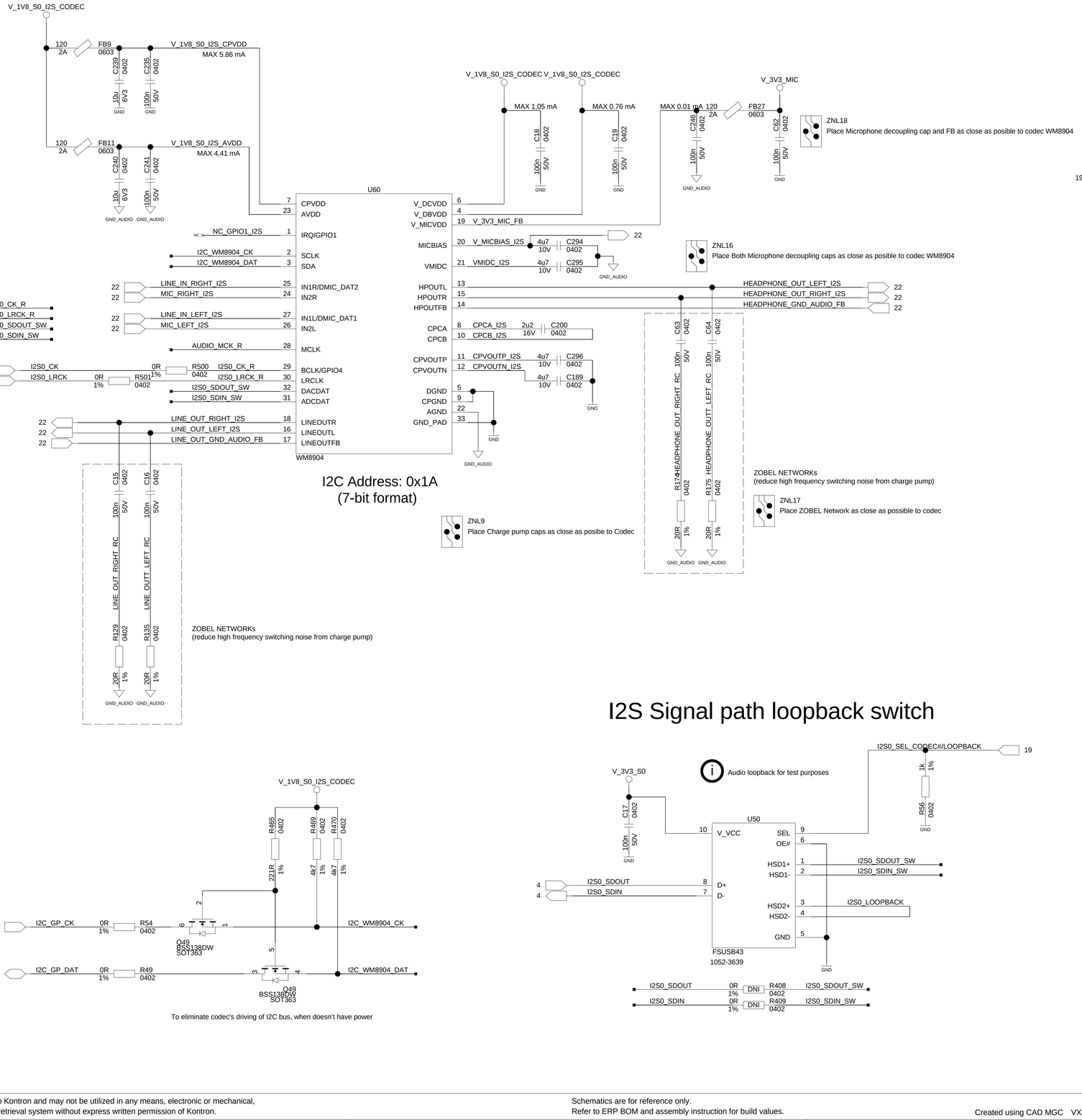
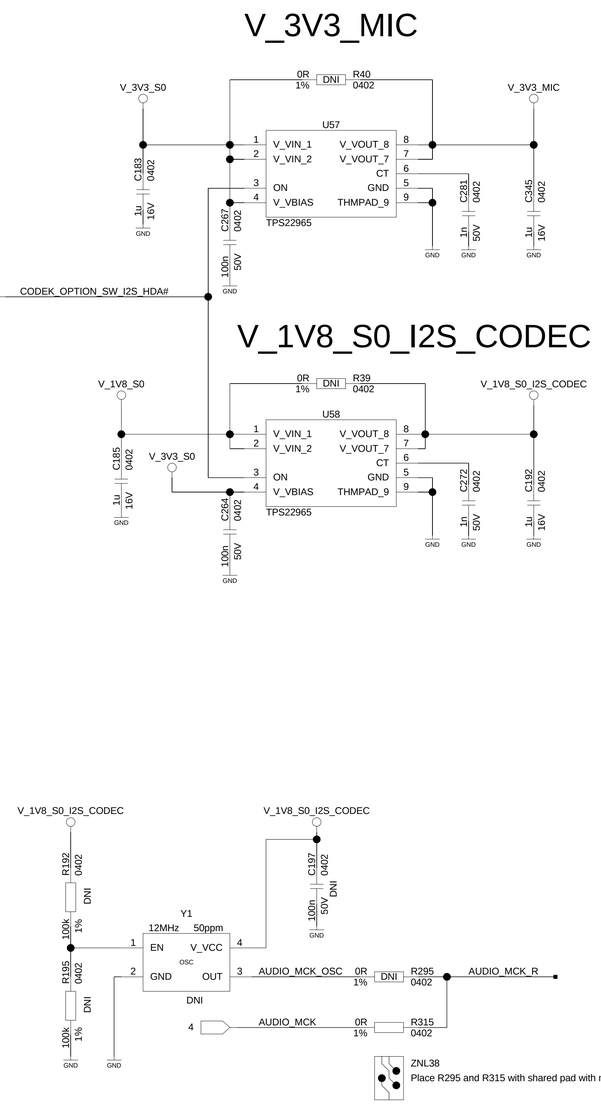
Audio I2S Codec WM8904





I2S Signal path loopback switch

PROJECT	SMARC Eval 2.0 ADS2 - SMARC Eval 2.0		
BLOCK ID	Schematic1 (21 of 30)		
SHEET	21 Audio - I2S Codec		
	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
VERIFIED:	KEEDC	MH	2017.11.20
APPROVED:			
PCB ID	PCB INDEX	LAST MODIFIED	
1062-0139	1400A	20/11/2017:15:03	
PAGE	21 OF 30		
DRAWING ID	SCH 1400	REV	D00

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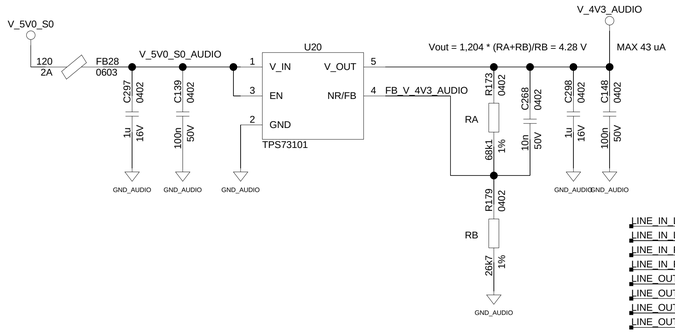
Audio connectors and Analog Multiplexers

V_4V3_AUDIO

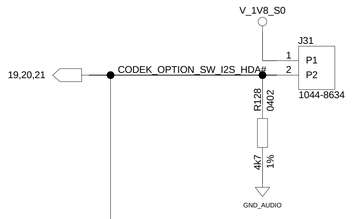


ZNL28
Place bypass resistors on oposit side of PCB
than IC MUX to make stabs as short as possible

Mux Bypass resistors

LINE_IN_LEFT_HDA	0R 1%	DNI	R288 0402	LINE_IN_LEFT_MUX
LINE_IN_LEFT_I2S	0R 1%	DNI	R298 0402	
LINE_IN_RIGHT_HDA	0R 1%	DNI	R299 0402	LINE_IN_RIGHT_MUX
LINE_IN_RIGHT_I2S	0R 1%	DNI	R301 0402	
LINE_OUT_LEFT_HDA	0R 1%	DNI	R302 0402	LINE_OUT_LEFT_MUX
LINE_OUT_LEFT_I2S	0R 1%	DNI	R306 0402	LINE_OUT_LEFT
LINE_OUT_RIGHT_HDA	0R 1%	DNI	R307 0402	LINE_OUT_RIGHT_MUX
LINE_OUT_RIGHT_I2S	0R 1%	DNI	R308 0402	LINE_OUT_RIGHT

Adio Codec Multipexor HDA (default) / I2S Codec



H3
JUMPER

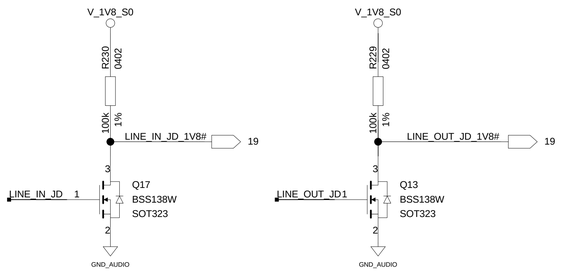
J31	CODEC
OPEN	HDA
SHORTED	I2S

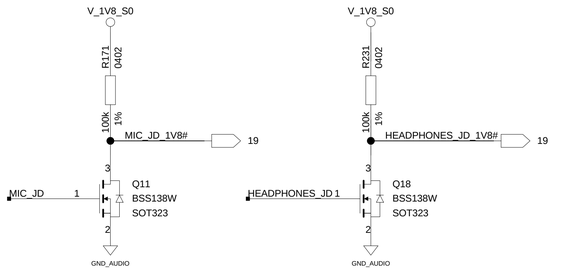
JACK DETECT SIGNALS FOR I2S CODEC (Connected to 4x GPI of I2C Expander)

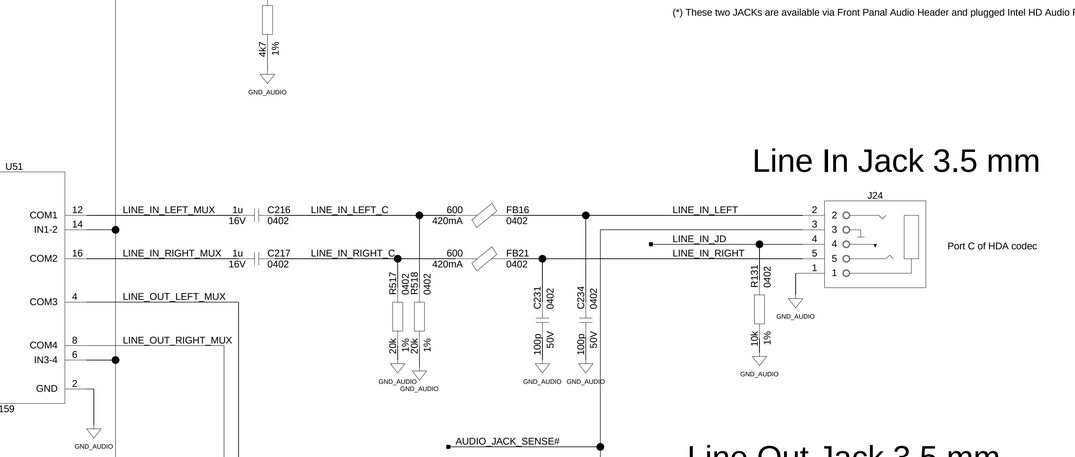
JACK	Signal	Function	Voltage	Log
LINE IN	LINE_IN_JD	Plug	5V	1
		Unplug	0	0
LINE OUT	LINE_OUT_JD	Plug	5V	1
		Unplug	0	0
MIC (*)	MIC_JD	Plug	5V	1
		Unplug	0	0
HEADPHONES (*)	HEADPHONES_JD	Unplug	5V	1
		Plug	0	0

(*) These two JACKs are available via Front Panal Audio Header and plugged Intel HD Audio Front panel dongle

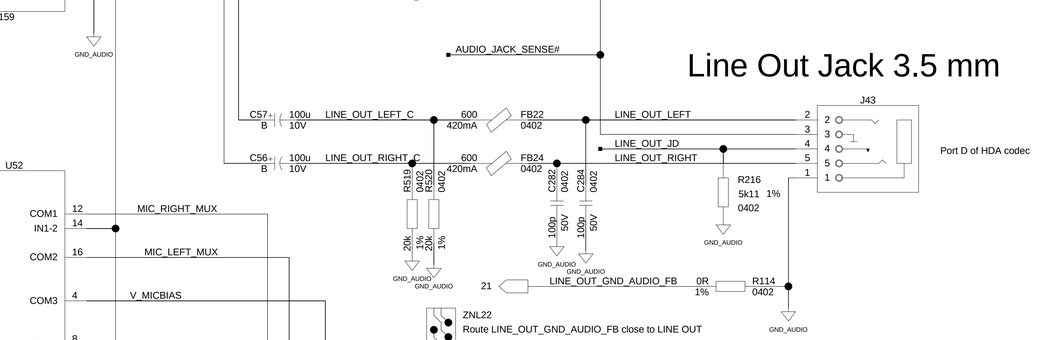
TO GPIO Expander (For I2S codec jack detection functionality)







Line In Jack 3.5 mm



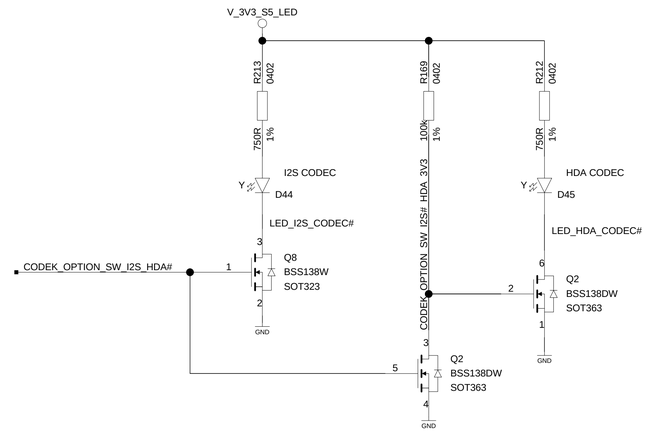
Line Out Jack 3.5 mm

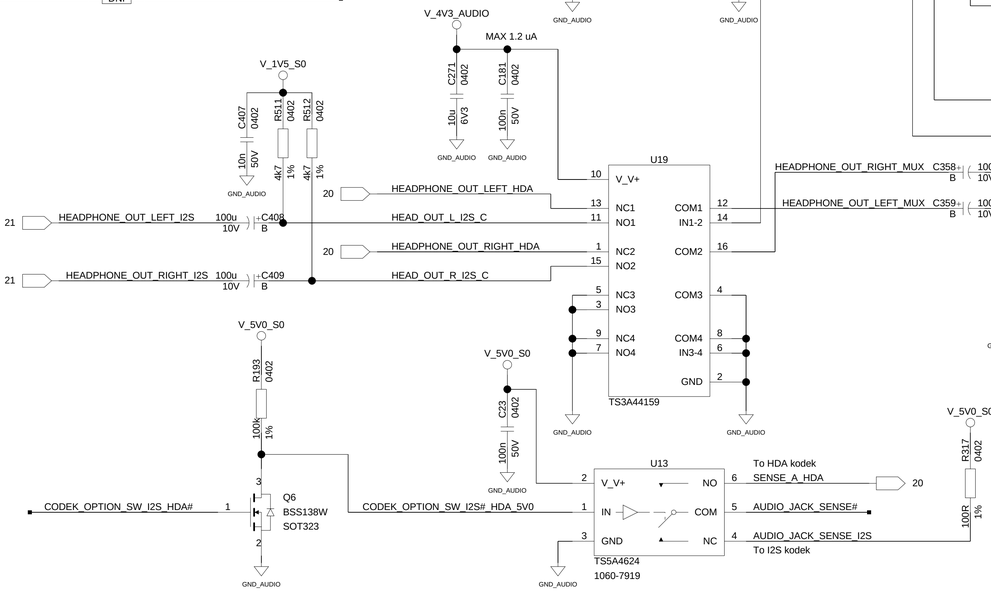
ZNL22
Route LINE_OUT_GND_AUDIO_FB close to LINE OUT
audio signals, to reduce noise

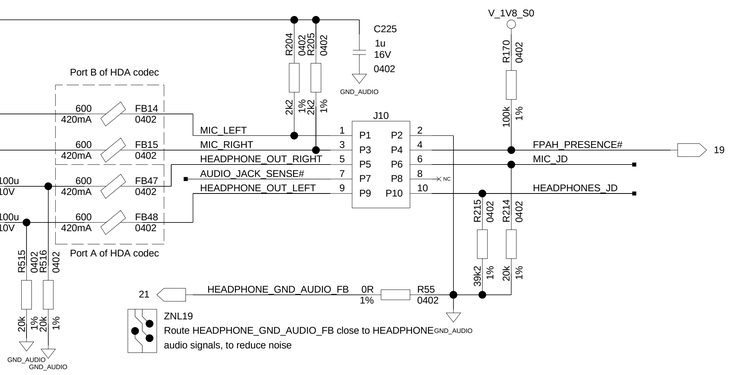
Front panel Analog Header

HEADPHONE_OUT_LEFT_HDA	0R 1%	DNI	R326 0402	HEADPHONE_OUT_LEFT_MUX
HEADPHONE_OUT_LEFT_I2S	0R 1%	DNI	R327 0402	HEADPHONE_OUT_LEFT
HEADPHONE_OUT_RIGHT_HDA	0R 1%	DNI	R328 0402	HEADPHONE_OUT_RIGHT_MUX
HEADPHONE_OUT_RIGHT_I2S	0R 1%	DNI	R329 0402	HEADPHONE_OUT_RIGHT

HDA / I2S Audio codec LEDs indication







ZNL19
Route HEADPHONE_GND_AUDIO_FB close to HEADPHONE
audio signals, to reduce noise

PROJECT	SMARC Eval 2.0 ADS2 - SMARC Eval 2.0	kontron	
BLOCK ID	Schematic1 (22 of 30)	DIVISION / NAME / DATE YYYY-MM-DD	
SHEET	22 Audio - con + mux	CREATED: KEEDC JM, JH ,MV	2017.11.17
		VERIFIED: KEEDC MH	2017.11.20
		APPROVED:	
PCB ID 1062-0139	PCB INDEX 1400A	LAST MODIFIED 20/11/2017:15:03	
PAGE 22 OF 30	DRAWING ID SCH 1400	REV D00	

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Refer to ERP BOM and assembly instruction for build values.

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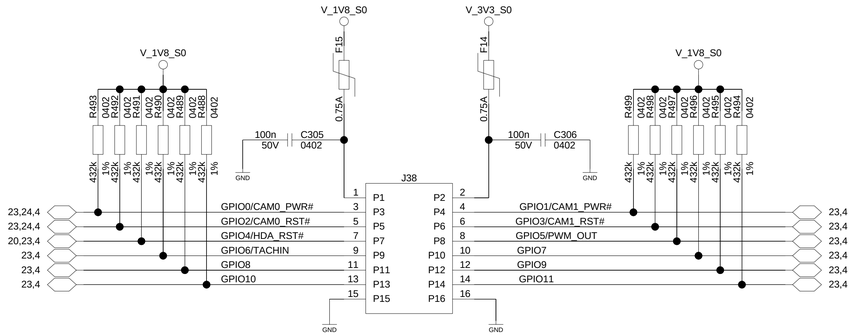
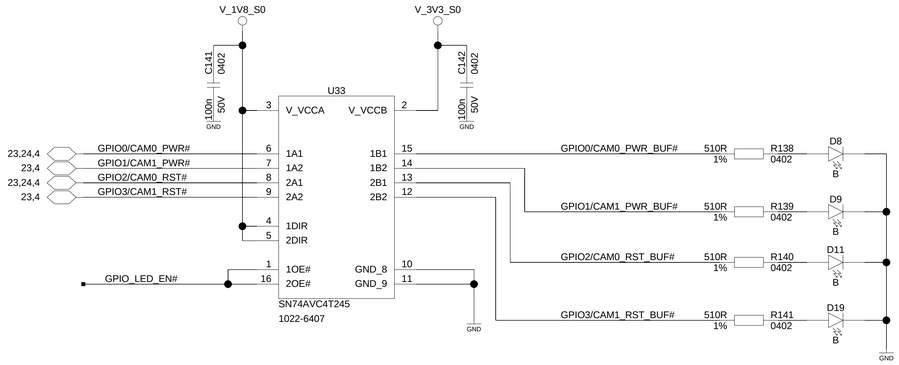
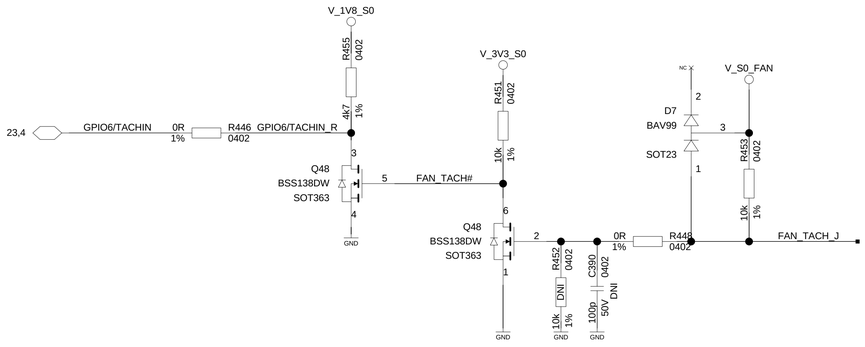
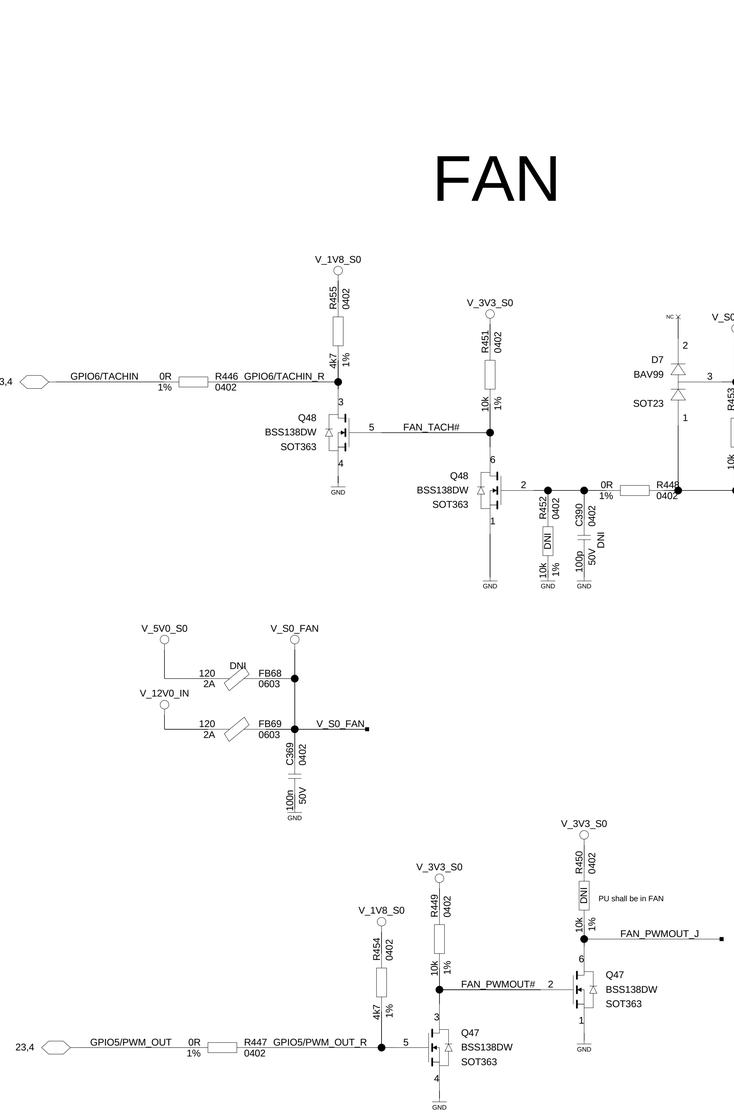
GPIO Header

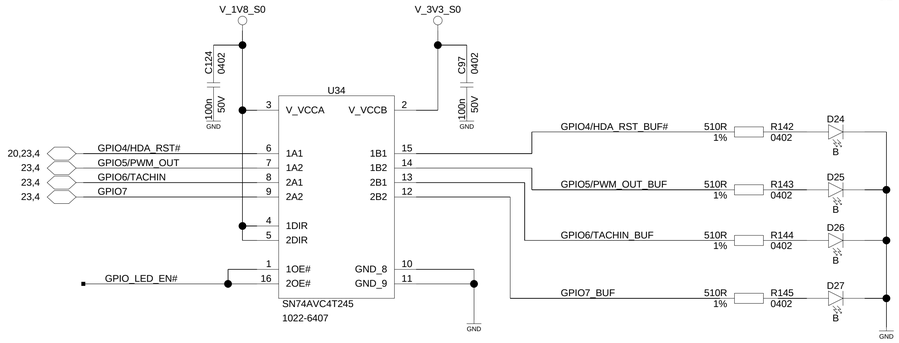


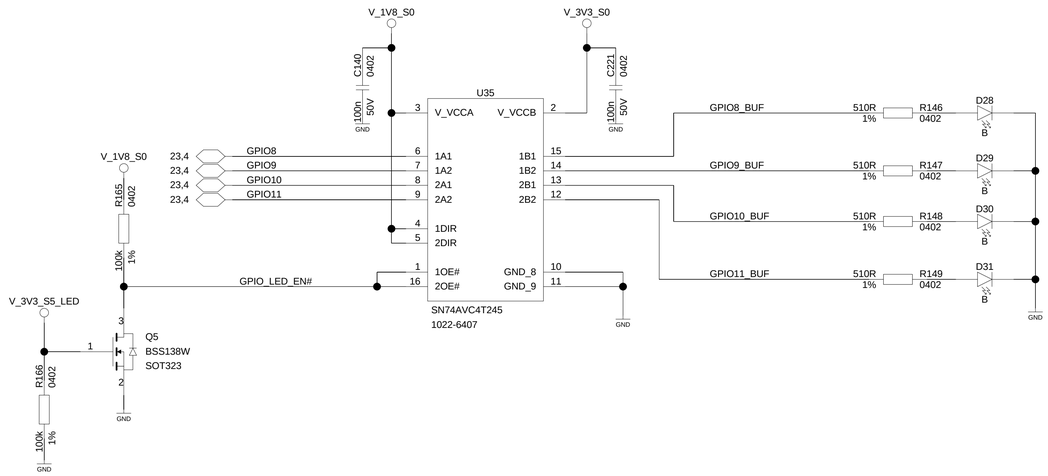


FAN









PROJECT: SMARC Eval 2.0				kontron
ADS2 - SMARC Eval 2.0				
BLOCK ID: Schematic1 (23 of 30)		DIVISION	NAME	DATE YYYY-MM-DD
	CREATED:	KEEDC	JM, JH ,MV	2017.11.17
SHEET: 23 GPIO Header	VERIFIED:	KEEDC	MH	2017.11.20
	APPROVED:			

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	23 OF 30	SCH 1400	D00

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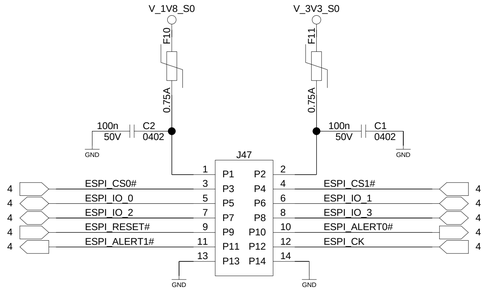
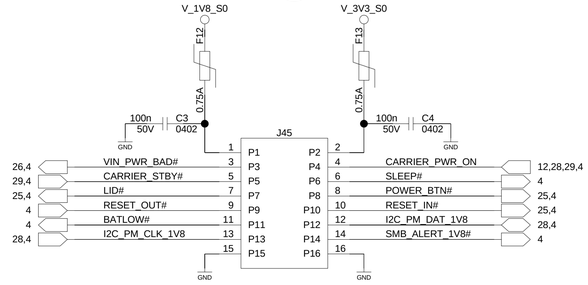
eSPI Header

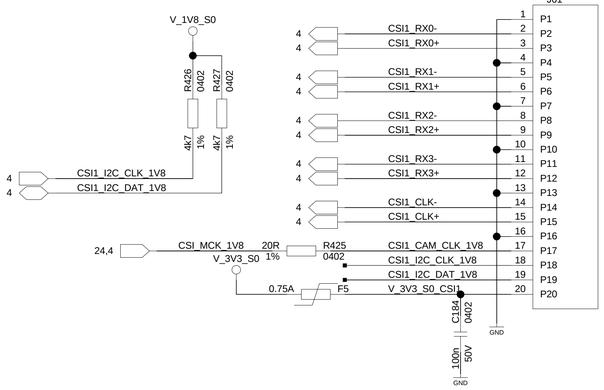


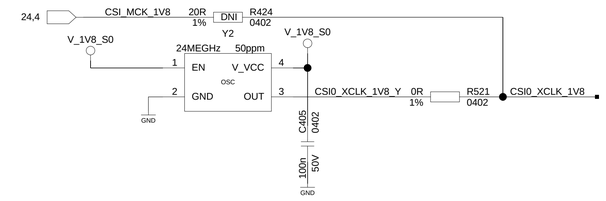
Power Management Header



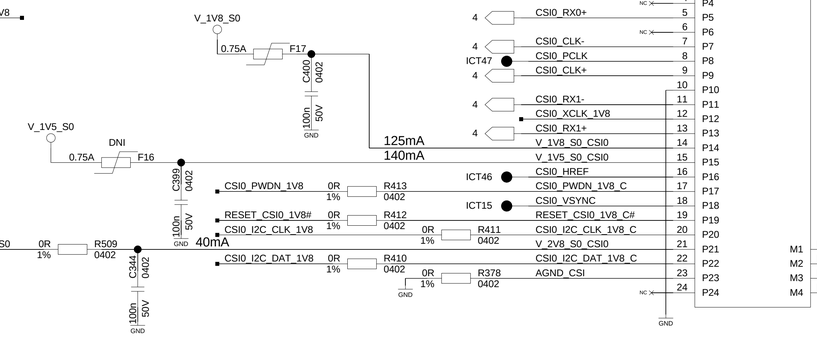
Camera Interface

CSI1



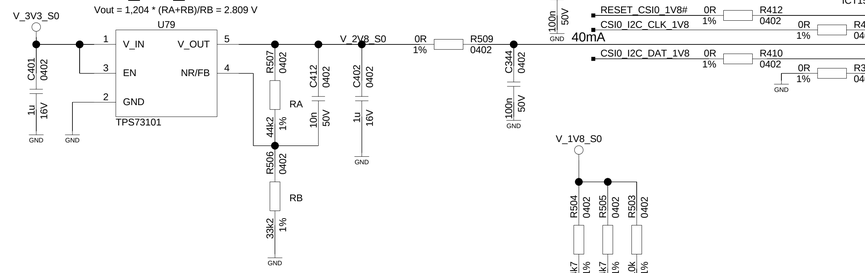


CSI0

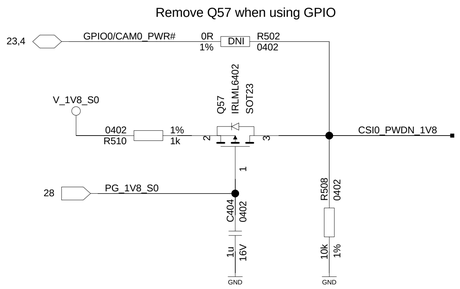


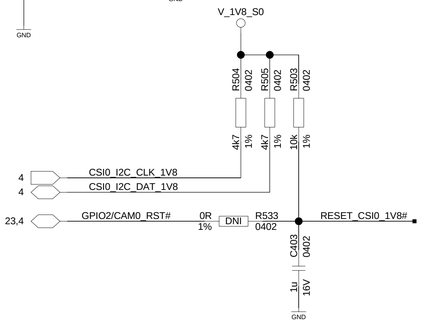
V_2V8_S0

Vout = 1,204 * (RA+RB)/RB = 2.809 V



Remove Q57 when using GPIO





PROJECT: SMARC Eval 2.0 / ADS2 - SMARC Eval 2.0			kontron
BLOCK ID: Schematic1 (24 of 30)		DIVISION	NAME / DATE YYYY-MM-DD
	CREATED:	KEEDC	JM, JH ,MV 2017.11.17
SHEET: 24_eSPI Header Power header CSI	VERIFIED:	KEEDC	MH 2017.11.20
	APPROVED:		
PCB ID: 1062-0139	PCB INDEX: 1400A	LAST MODIFIED: 20/11/2017:15:03	
PAGE: 24 OF 30	DRAWING ID: SCH 1400	REV: D00	

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Schematics are for reference only.
Refer to ERP BOM and assembly instruction for build values.

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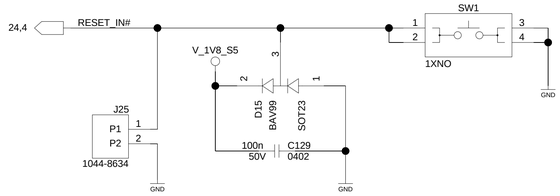
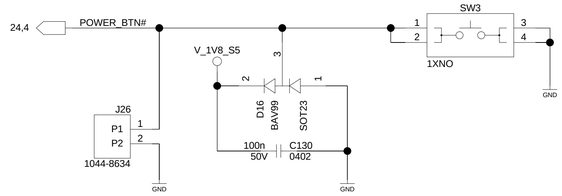
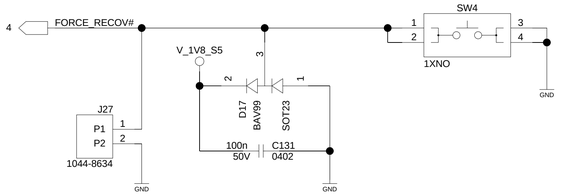
Reset



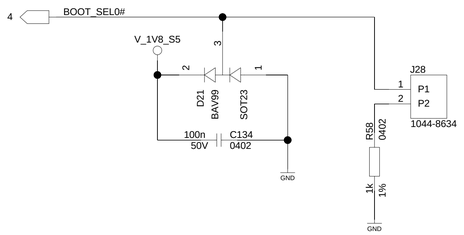
Power ON

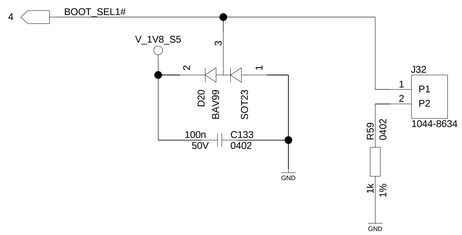


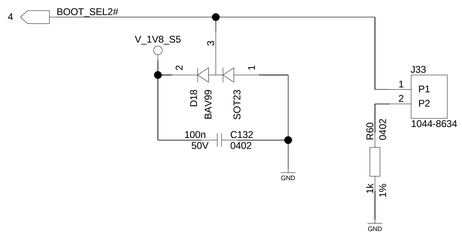
Force Recovery



Boot Selection

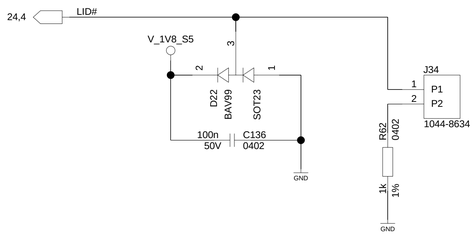




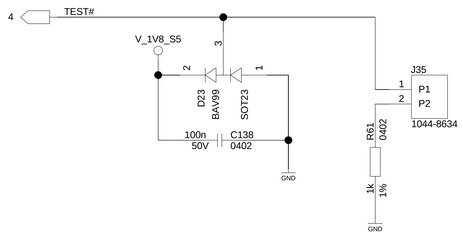


BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	Boot Source
GND	GND	GND	Carrier SATA
GND	GND	Float	Carrier SD Card
GND	Float	GND	Carrier eSPI (CS0#)
GND	Float	Float	Carrier SPI (CS0#)
Float	GND	GND	Module NAND/NOR Flash
Float	GND	Float	Remote boot (GBE, serial)
Float	Float	GND	Module eMMC Flash
Float	Float	Float	Module SPI

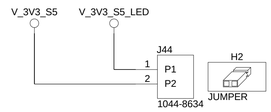
LID



TEST



LEDs ENABLE



PROJECT	SMARC Eval 2.0			
	ADS2 - SMARC Eval 2.0			
BLOCK ID		DIVISION	NAME	DATE YYYY-MM-DD
Schematic1 (25 of 30)		CREATED: KEEDC	JM, JH ,MV	2017.11.17
SHEET		VERIFIED: KEEDC	MH	2017.11.20
25 Buttons		APPROVED:		
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID / REV
1062-0139	1400A	20/11/2017:15:03	25 OF 30	SCH 1400 / D00

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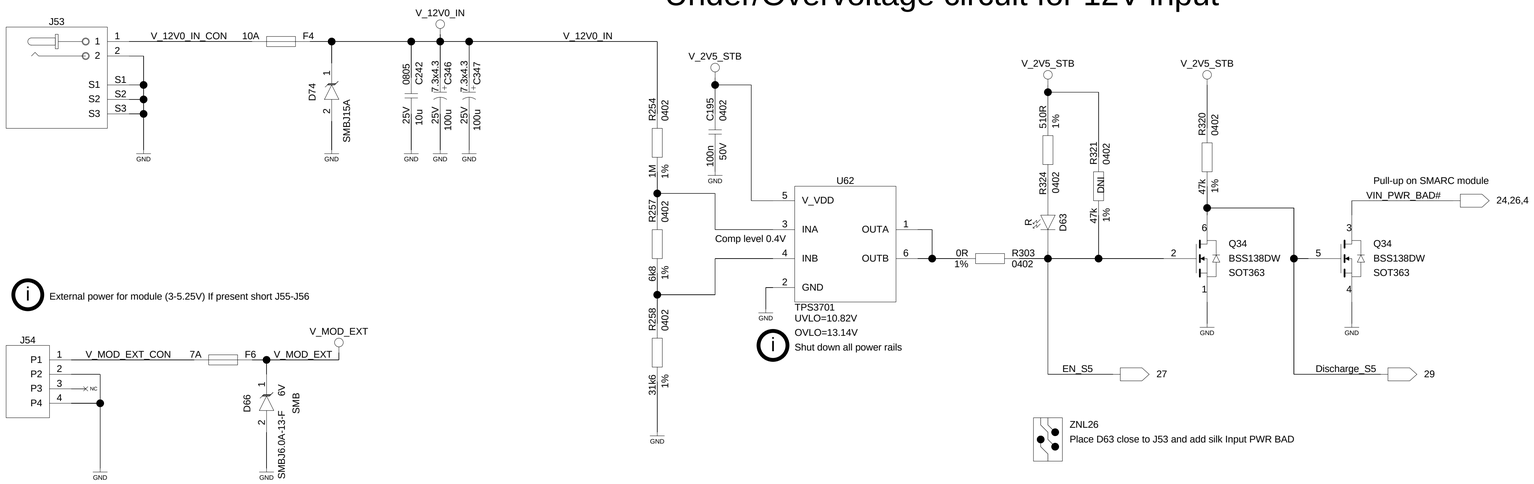
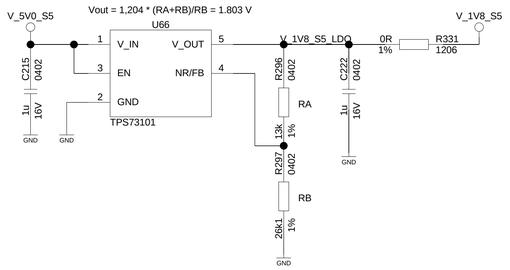
Input Power

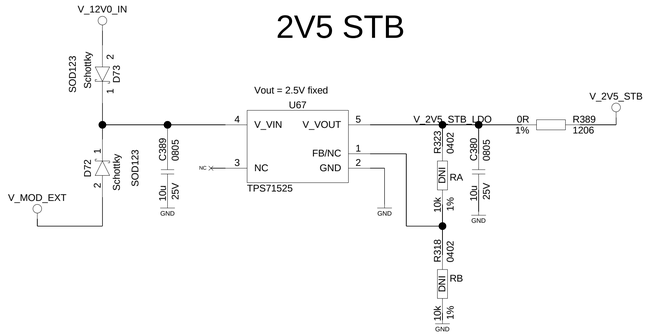
Under/Overvoltage circuit for 12V input



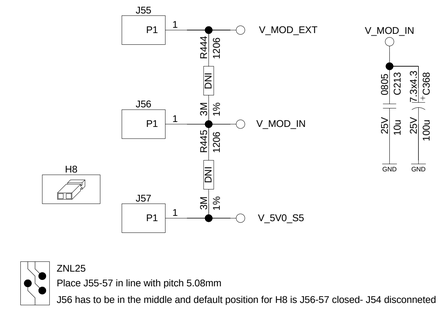
V_1V8_S5



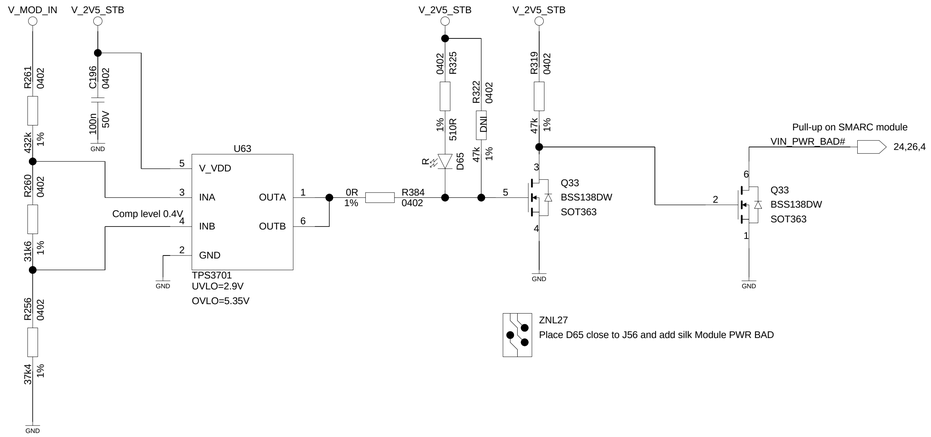
2V5 STB



SMARC mod EXT/INT power



Under/Overvoltage circuit SMARC module



PROJECT	SMARC Eval 2.0				
	ADS2 - SMARC Eval 2.0				
BLOCK ID		DIVISION	NAME	DATE YYYY-MM-DD	
Schematic1 (26 of 30)		CREATED:	KEEDC	JM, JH ,MV	2017.11.17
SHEET		VERIFIED:	KEEDC	MH	2017.11.20
26 Power		APPROVED:			
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	26 OF 30	SCH 1400	D00

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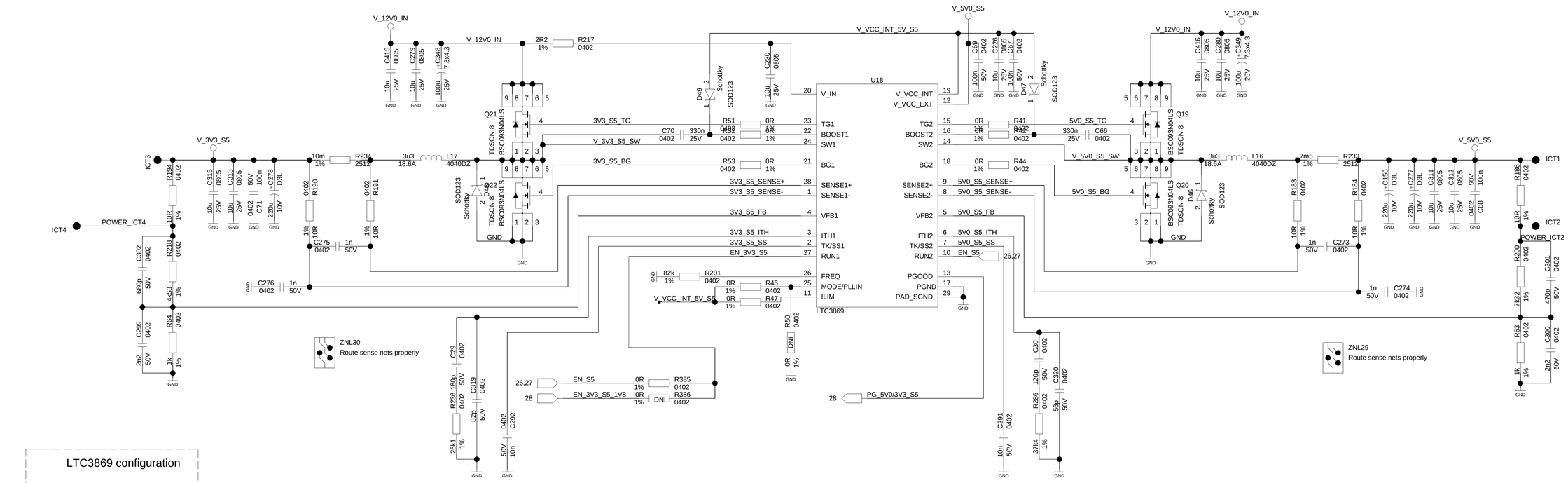
5V0_S5 and 3V3_S5



5V0_S0 and 3V3 S0

LTC3869 configuration

Mode pin 25 configuration
GND=CCM
INTVCC=Pulse-skipping
FLOAT= Burst

Freq pin 26 configuration Vfreq=R*10uA
250kHz (Vfreq=0V)
500kHz (Vfreq=1.2V)
780kHz (Vfreq>=2.4V)

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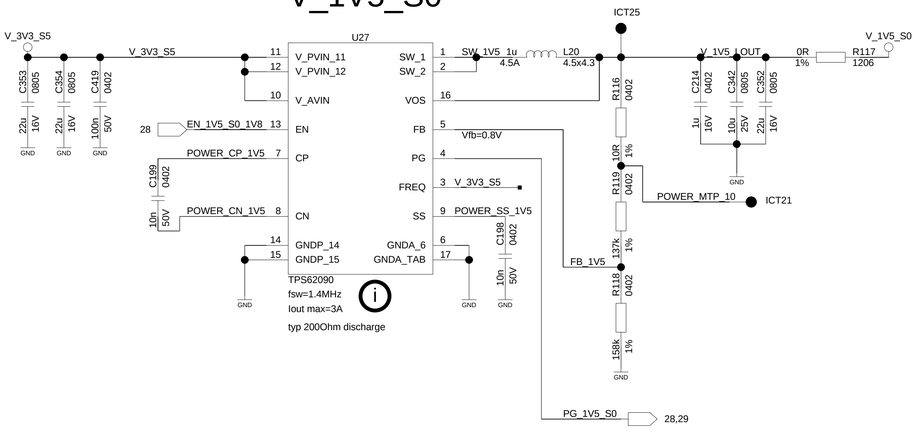
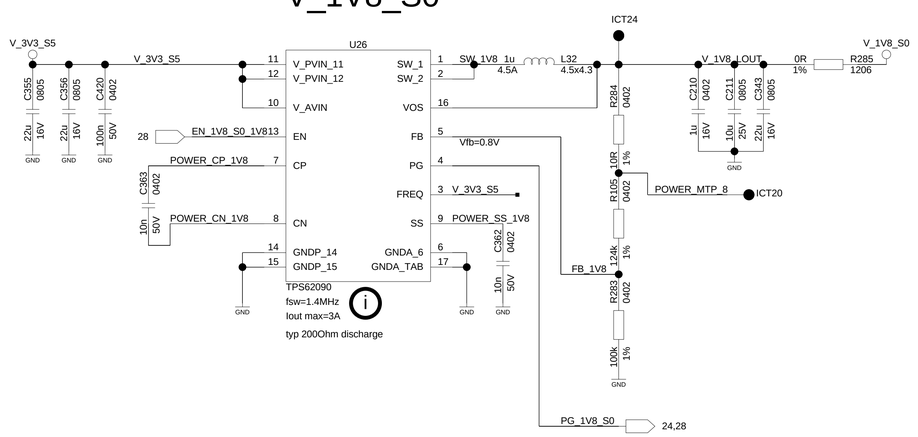
PROJECT	SMARC Eval 2.0		
	ADS2 - SMARC Eval 2.0		
BLOCK ID		DIVISION	NAME	DATE YYYY-MM-DD
Schematic1 (27 of 30)		CREATED: KEEDC	JM, JH ,MV	2017.11.17
SHEET		VERIFIED: KEEDC	MH	2017.11.20
27 Power		APPROVED:		
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	27 OF 30	SCH 1400	D00

1V8 and 1V5 S0, PM GPIO

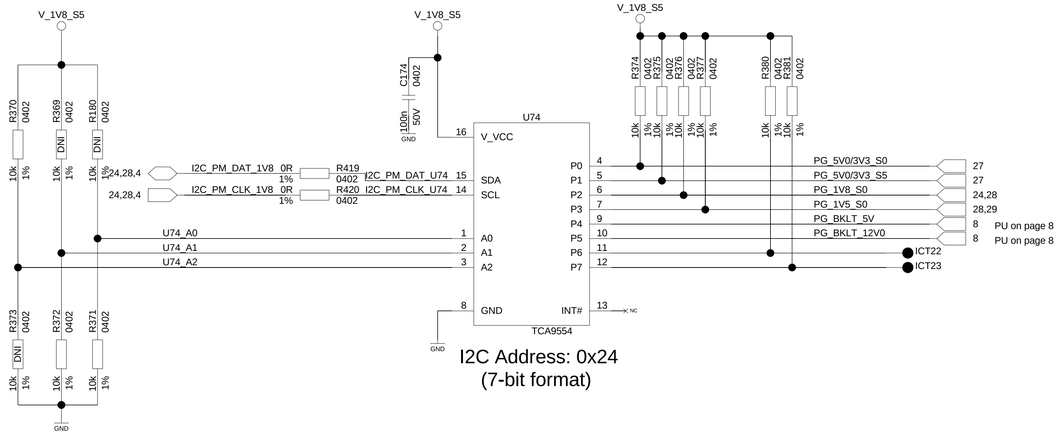
V_1V5_S0



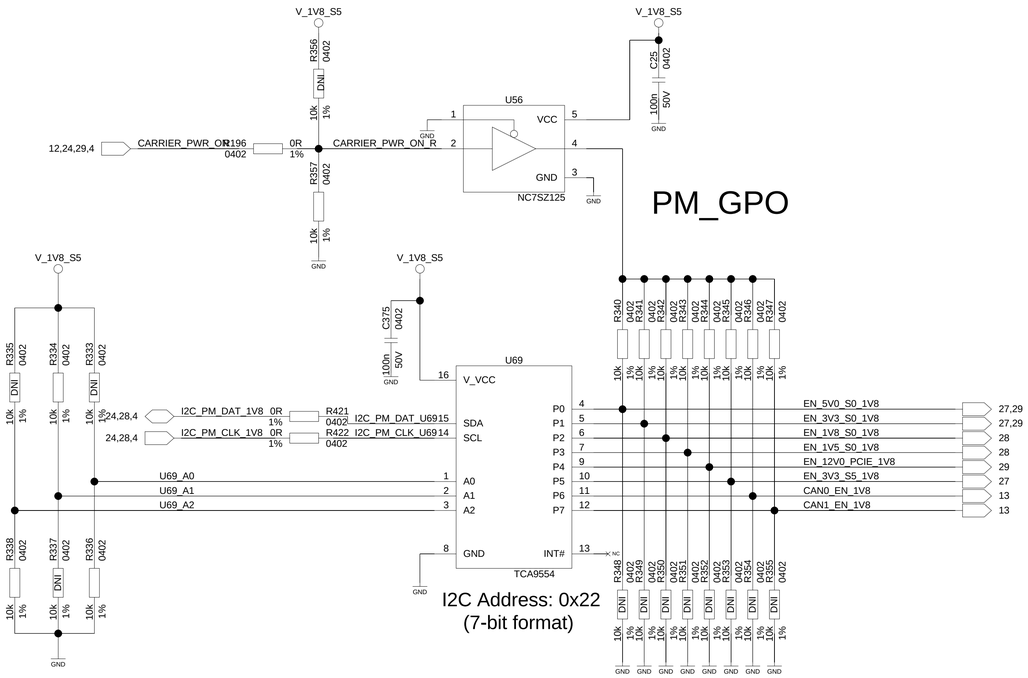
V_1V8_S0



PM_GPI



PM_GPO



PROJECT	SMARC Eval 2.0				
	ADS2 - SMARC Eval 2.0				
BLOCK ID	Schematic1 (28 of 30)		DIVISION	NAME	DATE YYYY-MM-DD
		CREATED:	KEEDC	JM, JH ,MV	2017.11.17
SHEET	28 Power	VERIFIED:	KEEDC	MH	2017.11.20
		APPROVED:			
PCB ID	1062-0139	PCB INDEX	1400A	LAST MODIFIED	20/11/2017:15:03
PAGE	28 OF 30	DRAWING ID	SCH 1400	REV	D00

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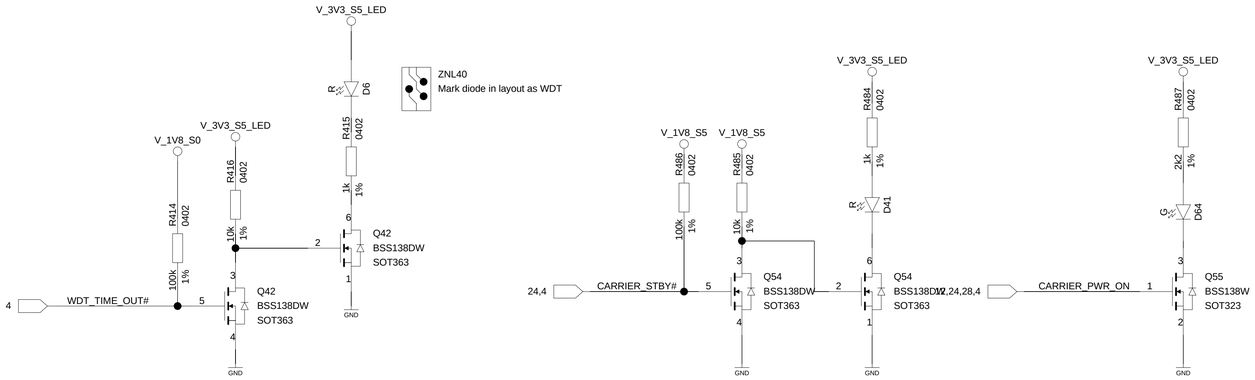
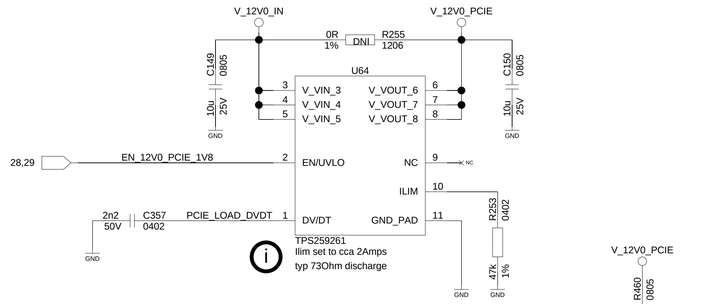
LEDs, Discharge, RTC

WDT

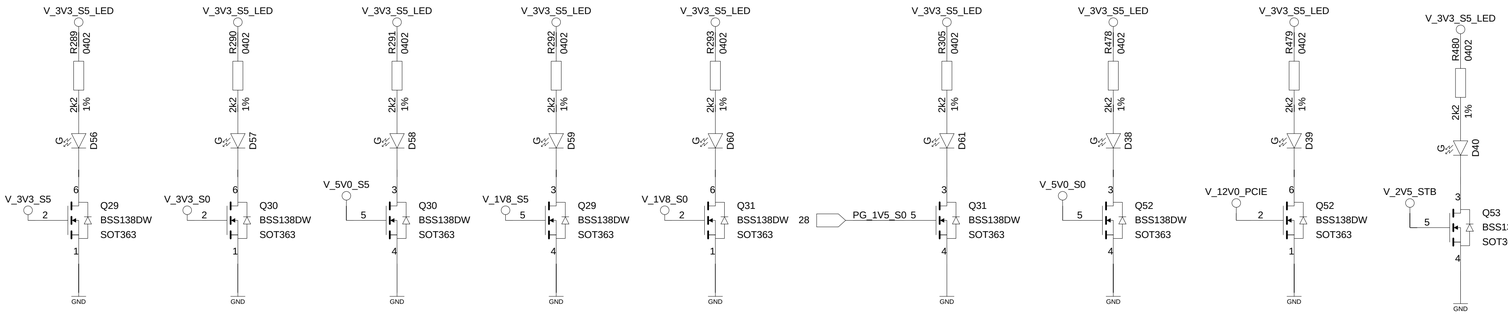


LOAD switch for PCIE

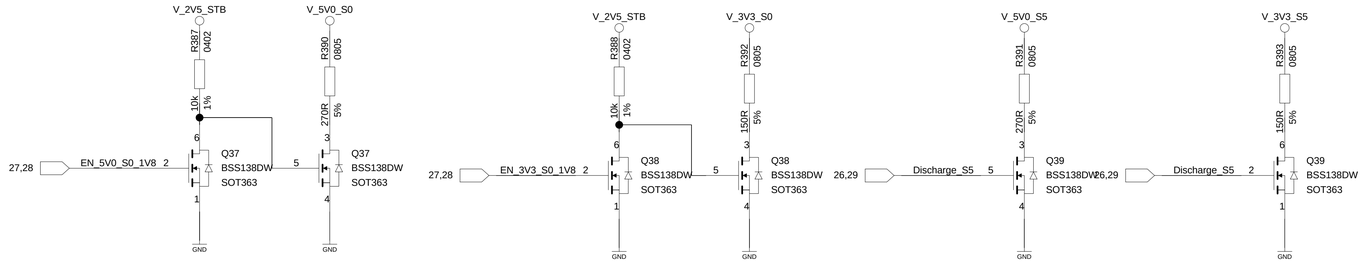


PWR LEDs

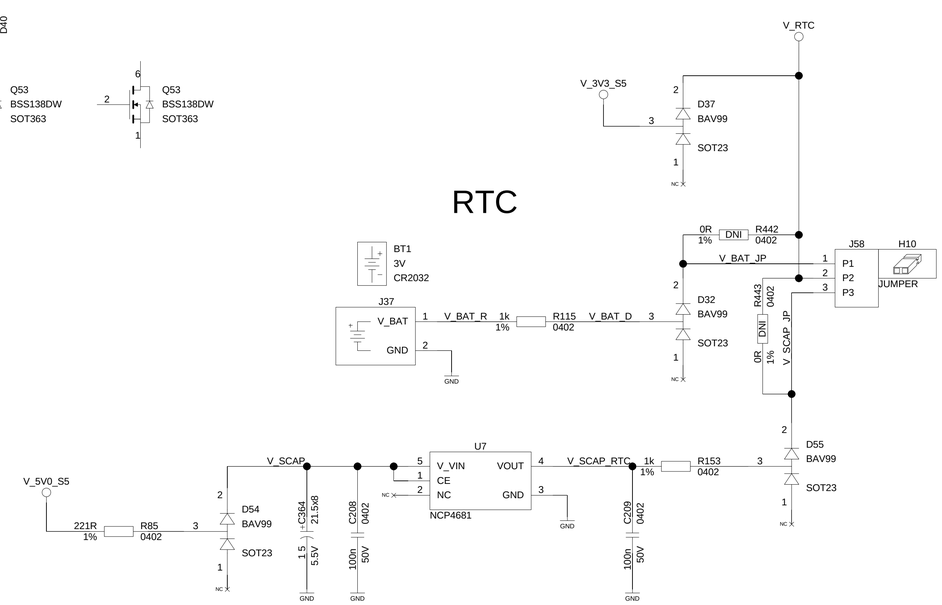
ZNL23
Add silk desc. for all LEDs based on the UGS i.e D59 3V3_S5



DISCHARGE



RTC



PWR LEDs

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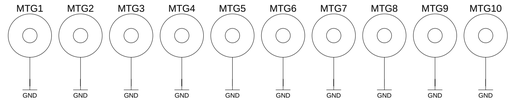
PROJECT	SMARC Eval 2.0		
	ADS2 - SMARC Eval 2.0		
BLOCK ID		DIVISION	NAME	DATE YYYY-MM-DD
Schematic1 (29 of 30)		CREATED: KEEDC	JM, JH ,MV	2017.11.17
SHEET		VERIFIED: KEEDC	MH	2017.11.20
29 Power		APPROVED:		

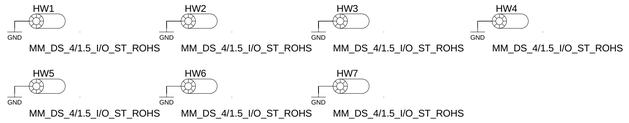
PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:03	29 OF 30	SCH 1400	D00

Mechanics

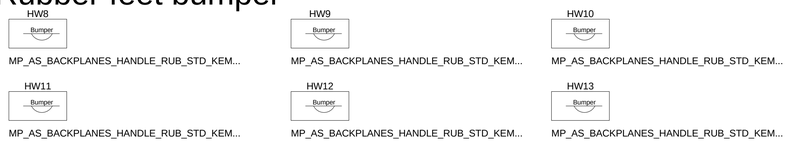
Baseboard mounting holes



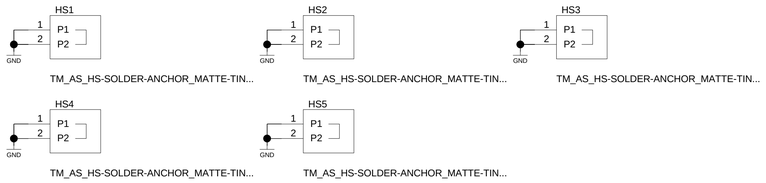
Module mounting holes

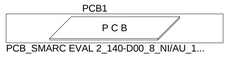


Rubber feet bumper



Ground connection





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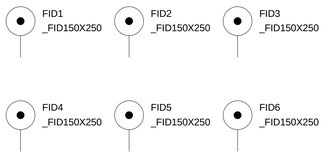
1062-0139

BOM SAP number: 1060-8921



PROJECT	SMARC Eval 2.0		
	ADS2 - SMARC Eval 2.0		
BLOCK ID	Schematic1 (30 of 30)		
SHEET	30 Mechanics		

	DIVISION	NAME	DATE YYYY-MM-DD
CREATED:	KEEDC	JM, JH ,MV	2017.11.17
VERIFIED:	KEEDC	MH	2017.11.20
APPROVED:			

PCB ID	PCB INDEX	LAST MODIFIED	PAGE	DRAWING ID	REV
1062-0139	1400A	20/11/2017:15:04	30 OF 30	SCH 1400	D00

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