

# ESI Workshop 3

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## 1. Bipolar Junction Transistor (BJT) Characteristics

- (a) Capture the output plot in step 5, identify the linear (active) region, the cut-off region, the saturation region. **(15 points)**

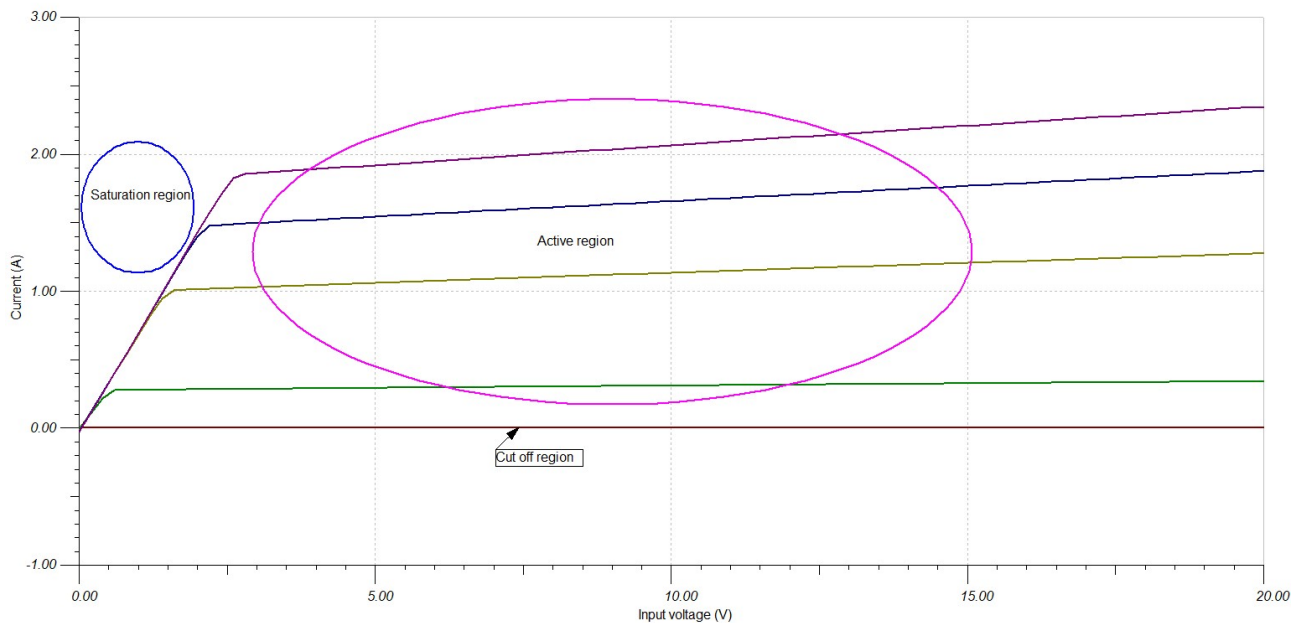


Figure 1: Operating regions BJT P2N2222A

- (b) Once you figure out the linear (active) region in question 1, take any 5 data points in the linear region ( $V_{ce}$ ,  $V_1$ ). And change your simulation circuit to the corresponding voltage, for example, in figure below, I pick ( $V_{ce}=5V$ ,  $V_1=1V$ ). Then click Analysis, DC analysis, Table of DC results, then you could get the results of  $I_b$ ,  $I_c$  and  $V_{be}$  under different bias conditions. Fill in those measurement values in the table **(10 points)**. Then calculate the current gain of the transistor **(5 points)**.

( $V_{ce}$ , $V_1$ )	$I_b$	$I_c$	$V_{be}$	$\beta$
(14.5,4)	75.16mA	2.19A	2.35V	29.14
(12,2)	23.72mA	1.16 A	1.48V	48.90
(11,1)	2.49mA	313.16mA	946.62mV	125.77
(10,1.5)	12.25mA	787.68mA	1.23V	64.30
(7.5,2)	24.28mA	1.1A	1.47V	45.30

(c) Compare the results you simulated with the datasheet. Do the measurement and calculation correspond to the datasheet recommend value? Give some comments. (5 points) \*datasheet: <https://www.onsemi.com/pdf/datasheet/pn2222a-d.pdf>

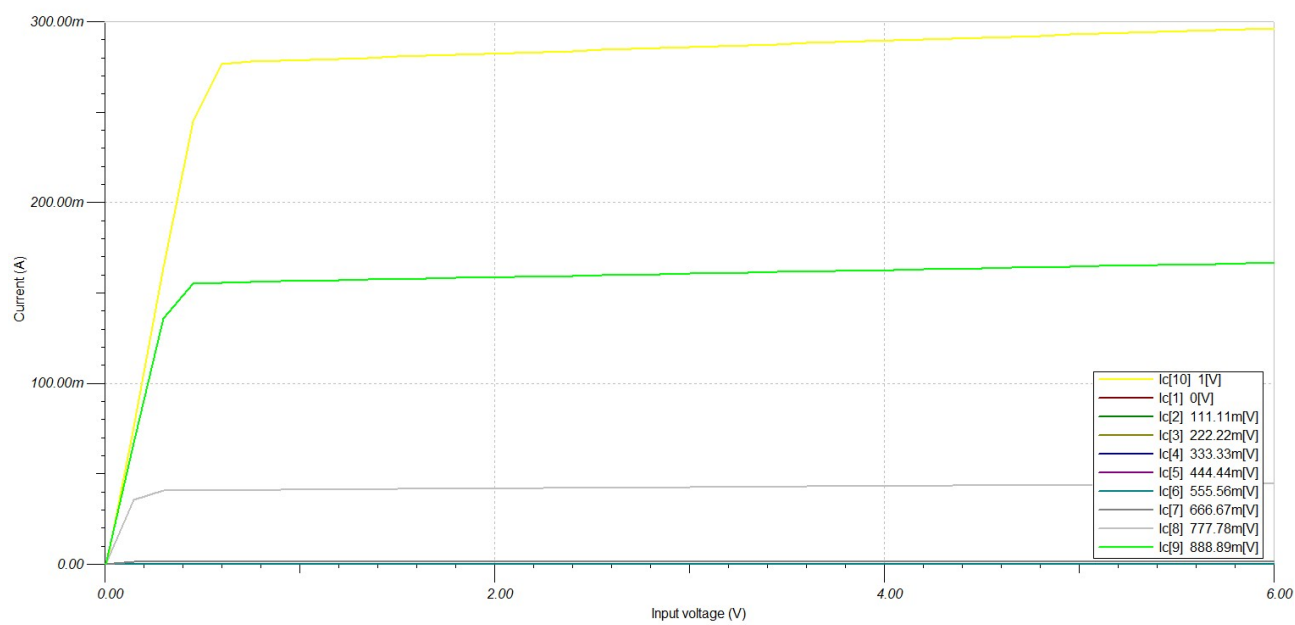


Figure 2: DC voltage sweep to find recommended value

Voltages/Currents	
I_R1[1,2]	998.45uA
I_R2[4,2]	60.89uA
I_R3[2,0]	5.78uA
Ib	1.05mA
Ic	174.21mA
V_Ib[2,3]	0V
V_Ic[4,5]	0V
V_R1[1,2]	21.97mV
V_R2[4,2]	9.13V
V_R3[2,0]	866.92mV
V_V1[1,0]	888.89mV
V_Vbe[3,0]	866.92mV
V_VCE[4,0]	10V
Vbe	866.92mV
VP_1	888.89mV
VP_2	866.92mV
VP_3	866.92mV
VP_4	10V
VP_5	10V
Show	
<input checked="" type="checkbox"/> Nodal Voltages	<input checked="" type="checkbox"/> Currents
<input checked="" type="checkbox"/> Other Voltages	<input checked="" type="checkbox"/> Outputs

Figure 3: Table of results

Datasheet recommends  $I_c$  of 150mA and 10V  $V_{CE}$  to achieve DC current gain between 100 to 300. From the figure 2, we can see that 150mA of  $I_c$  is reached by  $V_{in}$  of 888.88mV.

By simulating the circuit with these parameters we get  $I_b = 1.05\text{mA}$ ,  $I_c = 174.21\text{mA}$  as seen from figure 3. This gives  $\beta = 165.91$ , which is within the range of min and max  $\beta$  for recommended parameters.  $V_{in} = 870\text{mV}$  gives  $I_b = 859.53\mu\text{A}$   $I_c = 150.7\text{mA}$  (way closer to data-sheet recommendation), and  $\beta = 175.33$  (hasn't increased much).

## 2. BJT Switch Circuit

- (a) Please identify which region is the transistor working at when the LED (Light Emitting Diode) is on? And off? **(5 points)**

Saturation state as npn transistor will behave as a short circuit/closed switch.

- (b) Calculate the blinking frequency. **(5 points)**

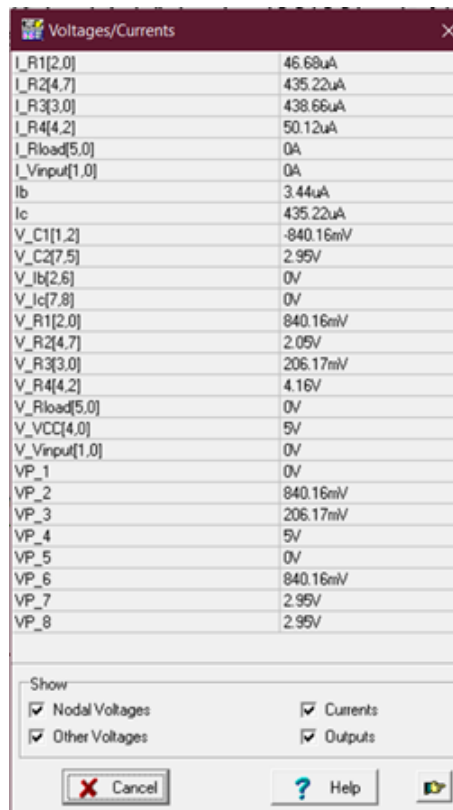
Led is on for 1 second and off for 1 second. So one cycle takes 2 seconds. Therefore blinking frequency is 0.5Hz

- (c) Modify the code, change the blinking frequency to 50 Hz. Include and submit your Arduino code. **(5 points)**

```
1 const int transistorPin = 3;
2 const int Hz = 50;
3 const int sec = (1000) / (HZ*2)
4 void setup()
5 {
6   pinMode (transistorPin, OUTPUT);
7 }
8 void loop()
9 {
10  digitalWrite (transistorPin, HIGH);
11  delay(sec);
12  digitalWrite (transistorPin, LOW);
13  delay(sec);
14 }
```

### 3. BJT Amplifier

- (a) Identify the BJT operation region under this bias point based on your simulation.  
(5 points)



I_R1[2,0]	46.68uA
I_R2[4,7]	435.22uA
I_R3[3,0]	438.66uA
I_R4[4,2]	50.12uA
I_Rload[5,0]	0A
I_Vinput[1,0]	0A
Ib	3.44uA
Ic	435.22uA
V_C1[1,2]	-840.16mV
V_C2[7,5]	2.95V
V_Ib[2,6]	0V
V_Ic[7,8]	0V
V_R1[2,0]	840.16mV
V_R2[4,7]	2.05V
V_R3[3,0]	206.17mV
V_R4[4,2]	4.16V
V_Rload[5,0]	0V
V_VCC[4,0]	5V
V_Vinput[1,0]	0V
VP_1	0V
VP_2	840.16mV
VP_3	206.17mV
VP_4	5V
VP_5	0V
VP_6	840.16mV
VP_7	2.95V
VP_8	2.95V

Show  
☒ Nodal Voltages  
☒ Other Voltages  
☒ Currents  
☒ Outputs

Cancel Help

Figure 4: Table of data to find bias point

From figure 4 we can see that :

$$V_b = V_{R1}[2, 0] = 840.16mV$$

$$V_e = V_{R3}[3, 0] = 206.17mV$$

$$V_c = V_{P8} = 2.95V$$

$$\text{Cut-off region: } V_b < V_e \implies V_{ib} < V_{R3} \implies V_{R1} < V_{R3}$$

$$\text{Active region: } V_e < V_b < V_c$$

$$\text{Saturated region: } V_b > V_c$$

$\therefore$  active region

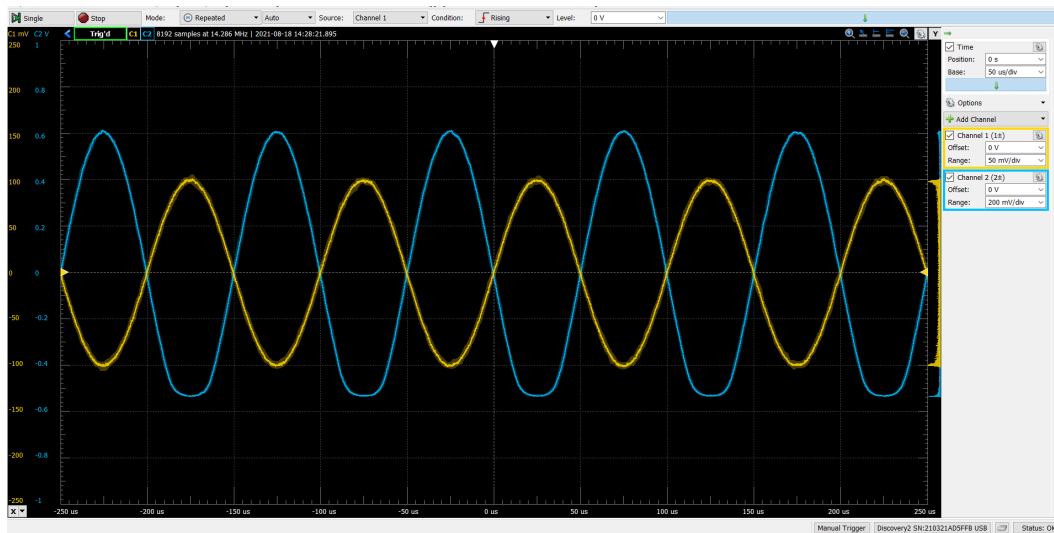
(b) Calculate the AC gain based on your simulation. **(5 points)**

From Figure 6 we can see that peak to peak  $V_{out} = 1.19V$  and peak to peak  $V_{in} = 200mV$ .

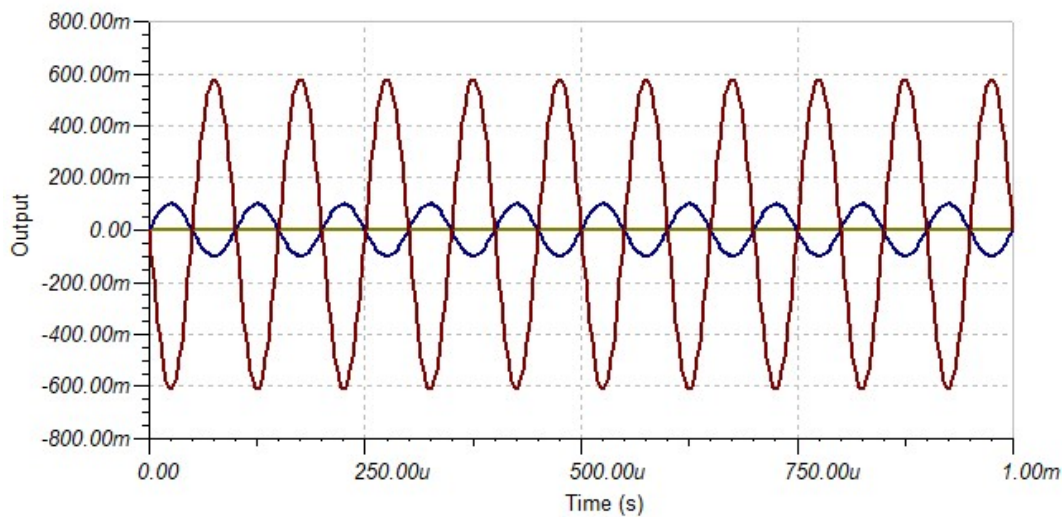
Therefore AC gain =  $\frac{1.19V}{200mV} = 5.94(V/V)$

(c) Explain why we need the capacitor C1 and C2? (Hint. Compare the differences between simulation and breadboard). **(5 points)**

We need the capacitor to smooth/filter out dc noise. A capacitor blocks dc, this allows us to ignore any dc bias and only amplify the AC portion of the signal. Still, in the actual breadboard (with  $2.2\mu F$  capacitor) voltage output was cut out from the bottom, suggesting transistor was not in linear region (Figure 5). These effects were not present in simulation waveform. Also note that if a capacitor was not used and a dc offset was not set, output will be approximately a dc.



(a) breadboard waveform



(b) simulation waveform

Figure 5: Side by side comparison of simulation and breadboard waveform with capacitors

- (d) Calculate the breadboard circuit AC gain and compare it with the simulation result. Give some comments. **(5 points)**

From Figure 7, it can be seen that peak-to-peak voltage of channel 1(output voltage) is 1.1372V\* and peak-to-peak voltage of channel 2 (input voltage) is 204.28mV. This gives us AC gain of 5.6.

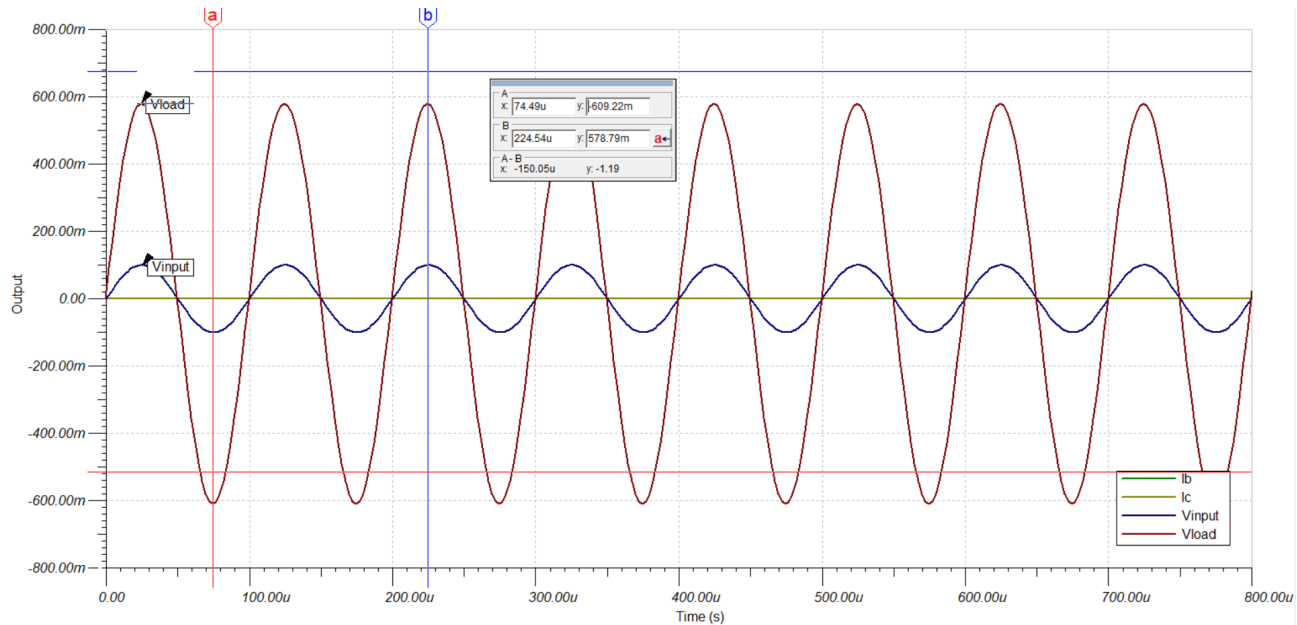


Figure 6: Simulation graph

We can do the same thing on Tina-TI. Reading from Figure 6, peak-to-peak output voltage is 1.19V and peak-to-peak input voltage is 200mV (100mV amplitude). This gives us an AC gain of 5.94, which is pretty close to our breadboard AC gain.

However on breadboard output signal was clipped and distorted for bottom half. This was probably due to not having exact component available, this resulted in lower VCC. To avoid this a higher VCC could be used to increase lower and upper saturation limits, so our output signal is always in linear region. Or breadboard resistors and capacitors value requirements should be met as closely as possible.

\* **Note:** There is a typo in labelling of cursors in Figure7. vin\_pX is vout\_pX.

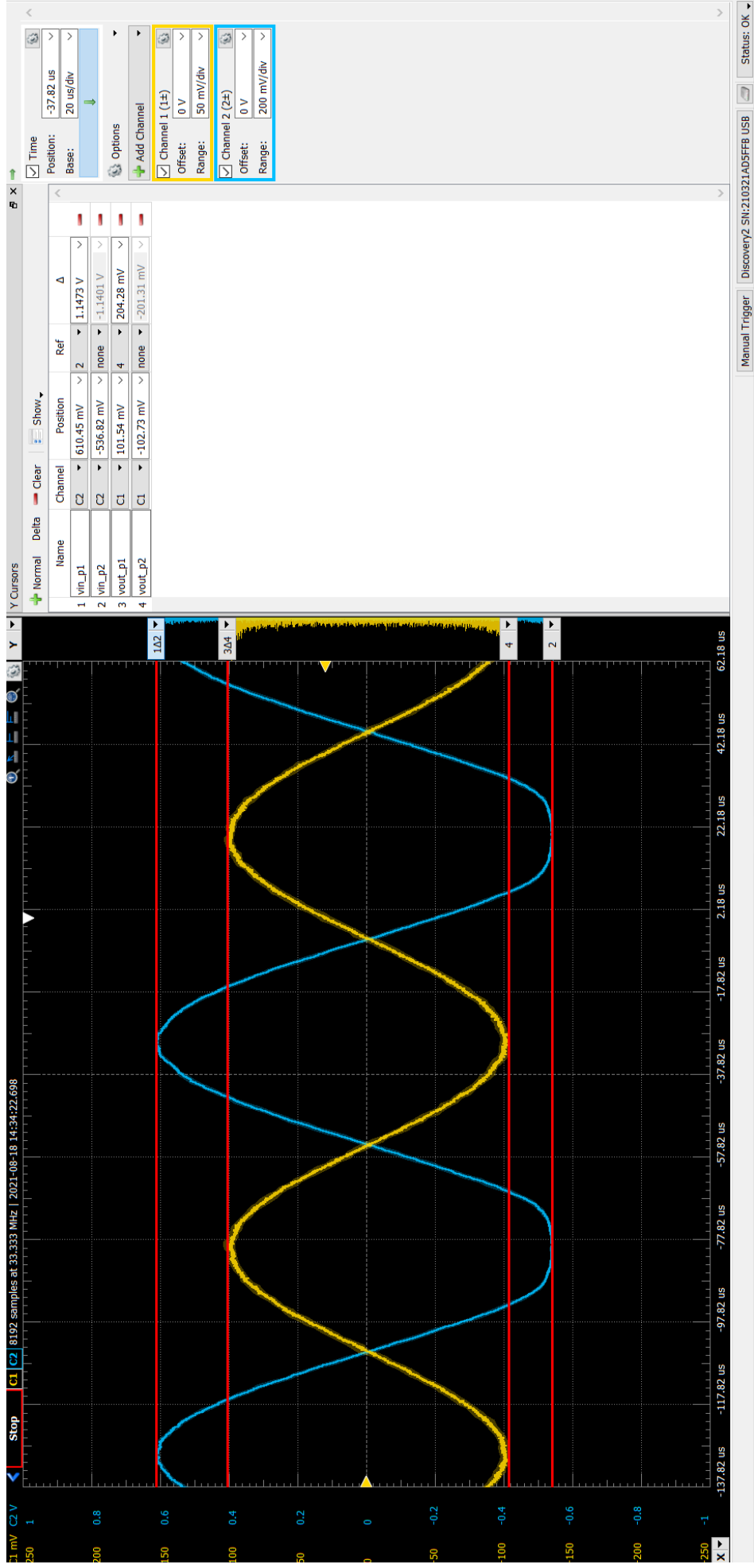


Figure 7: Peak to peak voltage measured using AD 2 discovery SN:210321AD5FFB