0105

National University of Computer and Emerging Sciences

Lahore Campus

Digital Logic Design (EE1005)

Sessional-II Exam

Total Time (Hrs): 1
Total Marks: 45
Total Questions: 3

Date: 12th April, 2025

Course Instructor(s)

Ms. Tamania Javaid

Mr. Ahmad Hamza

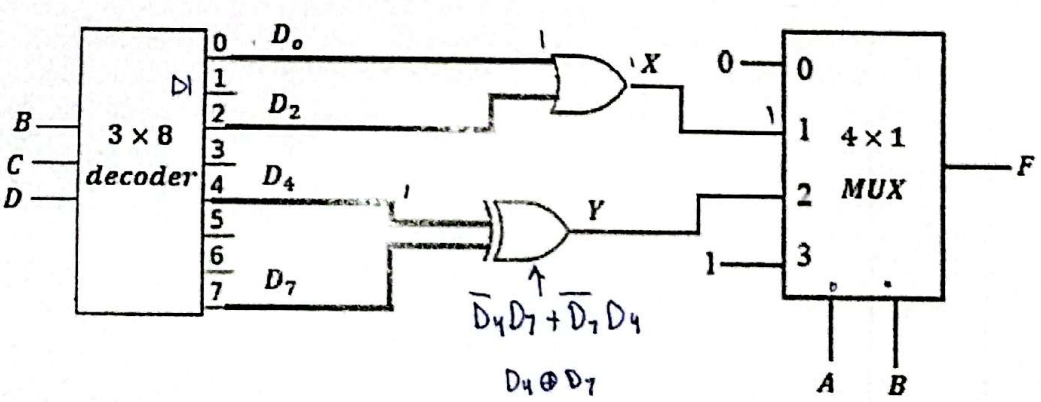
Roll No _____ Section _____ Student Signature _____

- **Attempt all the questions.**
- **Show complete working of each question.**
- **Multiple solutions of the same question will carry zero credit.**
- **State your valid assumptions clearly if you have to take any.**

CLO #3: Design combinational circuits using functional blocks.

Q1: **[15 marks]**

Construct the truth table of the following digital system.



$\bar{0} \cdot 0 + \bar{0} \cdot 0$
$1 \cdot 0 + 1 \cdot 0$
$0 + 0$

$\bar{1} \cdot 0 + \bar{0} \cdot 1$
$0 \cdot 0 + 1 \cdot 1$
$0 + 1 = 1$

$\bar{0} \cdot 1 + \bar{1} \cdot 0$
$1 \cdot 1 + 0 \cdot 0$
$1 + 0 = 1$

Take A, B, C, D as inputs and add columns to show X, Y and F as shown below. Make completely filled table on your answer sheet.

A	B	C	D	X	Y	F

CLO #3: Design combinational circuits using functional blocks

Q2: **[15 marks]**

Design a combinational circuit that take a 3-bit number as input and generates its 1's complement as output. Implement the circuit using 3-8 line decoder with active low enable and active high output and minimum additional logic

CLO #2: Design combinational circuits using functional blocks

Q3: **[15marks]**

Design a digital circuit that takes a 4 bit number X as input and increments it by 2 at the output. Use 1 bit full adder as a functional block. You can add the extra logic if required with any two input gates. Show complete working.