Digital Logic Design

Design Project

Smart Traffic Light Controller for Multi-Road Intersection with Pedestrian Safety System

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Introduction to the Multi-Road Intersection Project

The project titled **"Smart Traffic Light Controller for Multi-Road Intersection with Pedestrian Safety System"** aims to design and implement an intelligent traffic management solution for a four-way intersection. The core functionality revolves around **safely coordinating vehicle and pedestrian movements** using purely digital logic circuits—**without the use of microcontrollers**—making it a real-time embedded system that operates on hardware-level logic alone.

The system manages traffic signals in a **round-robin fashion (South → East → North → West)** and incorporates pedestrian safety through push-button-triggered crosswalk signals. It further integrates **emergency override** and **traffic density management** functionalities to simulate realistic urban traffic scenarios. Timing and synchronization are achieved through a central clock system, ensuring all components operate in a unified, deterministic manner.

Key Concepts and Their Significance

1. Combinational Logic

Used Components: AND, OR, NOT gates

Combinational logic forms the backbone of decision-making in the circuit. It is responsible for evaluating real-time conditions—such as pedestrian button status, traffic override input, or timer signals—to determine the appropriate output at any given time.

- **Significance**: Enables immediate and logical decisions without memory, crucial for reacting to current input states like pedestrian requests or emergency toggles.

2. Sequential Logic

Used Components: D Flip-Flops (7474), 4017 Counter

Sequential logic introduces memory and timing into the system. Flip-flops are used to **store pedestrian requests** until it is safe to activate the pedestrian signal. The **4017 Decade Counter** is central to the **round-robin sequencing** of the traffic lights, controlling transitions between red, yellow, and green phases.

- **Significance**: Allows the system to remember inputs over time, enabling orderly transitions and temporary storage of critical data (like pending pedestrian crossings).

3. Timing Circuits

Used Component: 555 Timer IC

The 555 Timer is configured in monostable or astable mode to produce **8-second intervals**, ensuring each signal phase (Red, Yellow, Green) runs for a fixed, controlled duration.

- **Significance**: Establishes deterministic timing intervals for traffic and pedestrian light durations, promoting safety and system predictability.

4. Decoding and Selection Logic

Used Component: 74LS139 Decoder

Introduction

The decoder is utilized for **emergency overrides**, allowing manual selection of any one direction to receive a prolonged green signal.

- **Significance**: Enables flexible control, such as prioritizing high-traffic directions or allowing emergency vehicles to pass safely—adding adaptability to an otherwise cyclical system.

5. Synchronous Clocking

The entire circuit operates under a **synchronized clock**, ensuring that all state changes and signal transitions occur in harmony.

- **Significance**: Eliminates race conditions and ensures coordinated transitions across all logic components—critical for a system handling concurrent traffic and pedestrian operations.

6. Human-Machine Interaction

Used Interfaces: Push Buttons, Logic Toggles, LEDs

Pedestrian requests are made via **push buttons**, while **logic toggles** simulate emergency situations and variable traffic conditions. LEDs act as visual indicators for both vehicles and pedestrians.

- **Significance**: Bridges the gap between digital logic and real-world usage, allowing the system to respond intelligently to human inputs and simulate realistic urban scenarios.

Problem Analysis

Problem Statement and Approach to Solution

Urban traffic congestion and pedestrian safety are growing concerns in modern city infrastructure. The project presents a real-world problem: designing a **smart traffic control system** for a **four-way intersection (North, South, East, West)** that ensures **efficient vehicle flow** while also **guaranteeing pedestrian safety**. The system must be entirely hardware-based—**implemented using digital logic components only**, with **no microcontrollers or programming involved**.

The problem requires addressing the following key challenges:

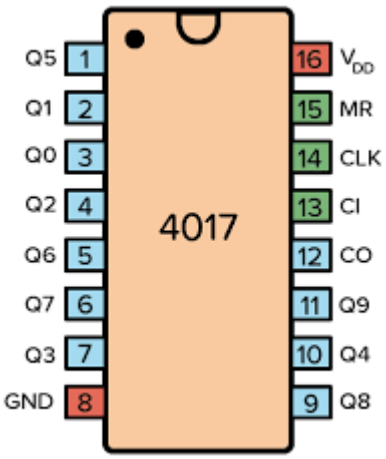
- Coordinating traffic light signals for four directions in a **non-conflicting, round-robin manner**.
- Safely handling **pedestrian crossing requests** through a push-button interface.
- Ensuring **collision prevention** between pedestrian and vehicle phases.
- Incorporating **timing control** for consistent signal durations.
- Introducing **manual overrides** for emergency or traffic-density scenarios.
- Simulating **real-time system behavior** through hardware (logic ICs) and demonstrating it both on software (Proteus) and physical breadboard setups.

Solution Approach

To effectively solve the problem, we have developed a **modular digital logic system** using Proteus for simulation and will implement it on a hardware breadboard using standard logic ICs. Below is a breakdown of how each aspect of the problem is addressed:

1. Directional Traffic Control (Round-Robin)

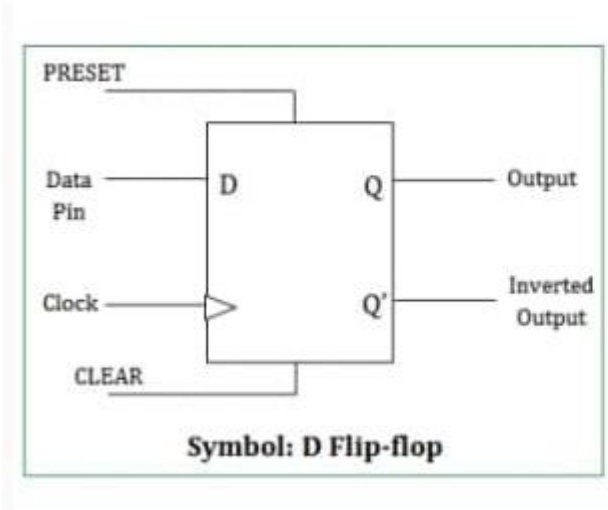
- **Component Used**: 4017 Decade Counter
- **How it Works**: The 4017 counter cycles through its outputs, each corresponding to a specific direction (S → E → N → W). For each direction, three LEDs (Red, Yellow, Green) indicate the current signal status.
- **Problem Solved**: Prevents directional conflict by allowing only one traffic signal to be green at a time, in a cyclic order.

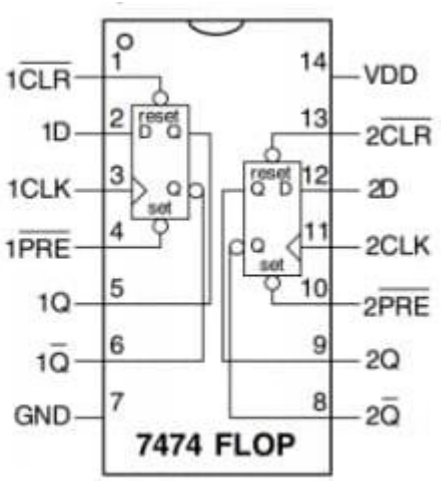


Problem Analysis

2. Pedestrian Safety System

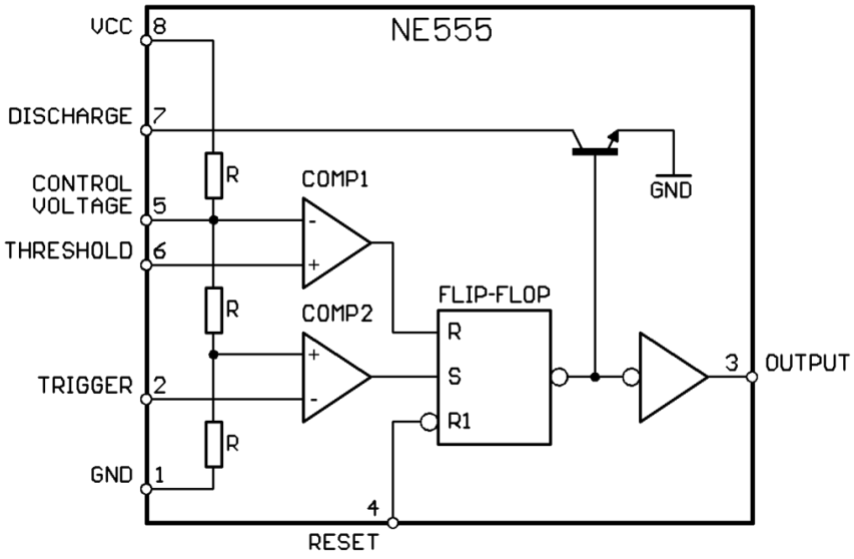
- **Components Used**: Push Buttons, D Flip-Flops (7474), AND Gates, LEDs
- **How it Works**: When a pedestrian presses a button, a D flip-flop stores the request. The system waits for the current vehicle phase to complete and for all lights to turn red. After that, a pedestrian green signal is activated for 8 seconds (via Timer IC), after which traffic cycle resumes.
- **Problem Solved**: Allows pedestrians to cross safely without conflicting with active vehicle signals. Flip-flops ensure pedestrian requests are remembered until the system is ready.

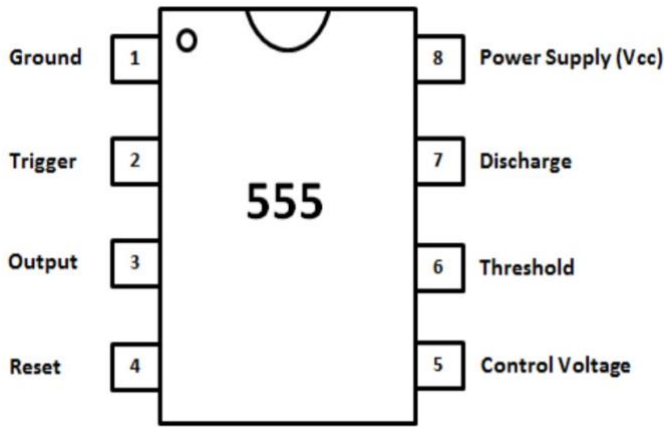




3. Timed Signal Duration

- **Component Used**: 555 Timer IC
- **How it Works**: The Timer IC outputs a consistent 8-second clock pulse that governs each phase of the traffic light (Red → Yellow → Green) and pedestrian walk duration.
- **Problem Solved**: Maintains predictable signal timing for vehicles and pedestrians, enabling safer and more organized transitions.





Problem Analysis

4. Emergency Override and Density Management

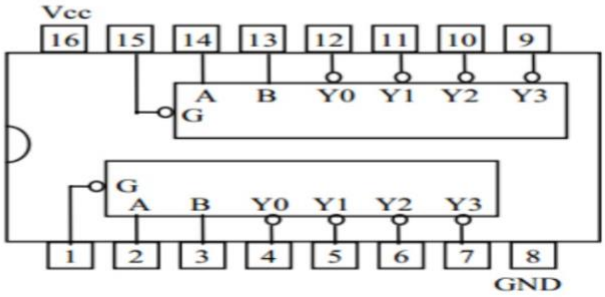
- **Components Used**: 74LS139 Decoder, Logic Toggles, AND Gates
- **How it Works**: Using logic toggles (simulating emergency switches), the decoder directs the system to focus on a specific direction, bypassing the round-robin cycle temporarily. The AND gate with the timer allows the green phase to be extended for that direction.
- **Problem Solved**: Provides flexibility to prioritize traffic flow based on real-time conditions or emergency requirements.

Function Table:

Enable	Selection Inputs		Outputs			
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Table 8-1: 74LS139 Decoder function table

Connection Diagram:



5. Collision Avoidance and Synchronization

- **Component Used**: Centralized Clock Signal
- **How it Works**: All components receive a synchronized clock, ensuring uniform state transitions and eliminating race conditions or overlapping signals.
- **Problem Solved**: Prevents conflicting outputs and ensures reliability in signal transitions across the intersection.

6. Hardware and Simulation Platforms

- **Tools Used**: Proteus Simulation Software, Breadboard Implementation
- **How it Works**: The entire system was first designed and verified in Proteus for functional accuracy, then translated to a physical build using logic ICs and components on a trainer board.
- **Problem Solved**: Validates both theoretical and practical feasibility of the design in a real-world setup.

Design Requirements

Design Requirements: Inputs, Outputs, and Constraints

Designing a smart traffic light controller for a four-way intersection with integrated pedestrian safety involves clearly identifying **what inputs the system must respond to**, **what outputs it should generate**, and **under what constraints it must operate**. The system must operate autonomously using **digital logic circuits only**, with no reliance on programmable microcontrollers. Therefore, all behavior must be derived from a well-structured combination of logic gates, flip-flops, timers, counters, and decoders.

1. Inputs

The system responds to a range of user-generated and system-level input signals:

Input Type	Source	Function
Clock Signal	555 Timer IC	Provides an 8-second periodic pulse for traffic and pedestrian timing.
Pedestrian Push Buttons	Manual (1 per road)	Indicates a pedestrian request to cross. Stored by D flip-flop until activation.
Logic Toggles (Switches)	Manual Simulation	Simulates emergency situations or traffic density on a specific road.
Reset/Input Clear Signal	Optional Manual	Resets the system to initial state during startup or faults.

- **Input Constraints**:
  - Pedestrian requests must be delayed until vehicle traffic is fully stopped (all red).
  - Override toggles must temporarily suspend round-robin flow but resume it afterward.
  - Input signals must be debounced (via design or hardware) to avoid false triggers.

Design Requirements

2. Outputs

The system produces multiple coordinated outputs to control both vehicle and pedestrian flows:

Output Type	Destination	Function
Traffic Signals	4 Directions (S, E, N, W)	Each direction has Red, Yellow, Green LEDs controlled via 4017 counter.
Pedestrian Indicators	4 Crosswalks	"Walk" (Green) and "Don't Walk" (Red) LEDs, triggered via logic after safe conditions.
Status Indicators	Optional LEDs/Buzzer	Can be used to indicate override activation or pedestrian phase in progress.

Output Constraints:

- Only one direction's traffic signal may be green at a time.
- Pedestrian green signal must never coincide with green vehicle signal in same direction.
- Pedestrian crossing lasts exactly one timer cycle (8 seconds).
- After override or pedestrian phase, round-robin must resume from next valid state.

Design Requirements

3. System Behavior Constraints

To ensure safe and logical operation, the following behavior constraints are embedded in the design:

- **Mutual Exclusivity**:
  - No two directions can have green signals simultaneously.
  - Pedestrian and vehicle green lights in the same direction must be mutually exclusive.
- **Timing Synchronization**:
  - The entire system is synchronized using a shared clock (from Timer IC).
  - All transitions (traffic and pedestrian) happen in 8-second intervals.
- **Interrupt Handling**:
  - Pedestrian inputs act as interrupt requests stored in D flip-flops.
  - Overrides via logic toggles take immediate control and are prioritized in decoding logic.
- **State Machine Logic**:
  - The system behaves as a finite state machine (FSM), with clearly defined transitions between traffic phases and pedestrian phases.
  - Outputs depend on both present state (e.g., current direction) and external inputs (e.g., button press or override).

Feasibility Study: Time and Cost Management

Before undertaking any hardware-based engineering project, it is essential to evaluate its feasibility to determine whether the objectives can be met efficiently within available **resources**, **budget**, and **time constraints**. In this project, we implemented a **smart traffic light controller with pedestrian safety** using **pure digital logic components** — which required careful planning, sequential execution, and realistic resource allocation. This section outlines how we managed both **time** and **costs** to ensure successful project completion.

1. Time Management Feasibility

Time is a critical factor in project-based evaluations, especially in academic settings with strict deadlines. Our project timeline was divided into the following phases:

Phase	Duration	Activities
Initial Planning & Research	2–3 Days	Studying circuit requirements, selecting ICs, drafting logic flow.
Schematic Design (Proteus)	3–4 Days	Developing and verifying logic-level design in simulation.
Component Sourcing	1–2 Days	Procuring ICs, breadboards, LEDs, resistors, etc.
Hardware Implementation	4–5 Days	Building circuit on breadboard, testing, debugging.
Documentation & Report Prep	2–3 Days	Writing structured report and diagram

Feasibility Analysis

- **Time Constraints Managed**:
  - Use of **Proteus** allowed faster debugging and design verification before physical implementation.
  - Tasks were divided equally among two group members, reducing individual load.
  - Critical dependencies like timer tuning and pedestrian logic were tested early to avoid last-minute bottlenecks.
- **Outcome**:
  - Project was completed **within the allocated timeframe (approx. 14–17 days)**.
  - Time buffers were included to account for possible hardware failures or testing delays.

Pictures of the equipment upon purchase:

2. Cost Management Feasibility

Budget is another important consideration, especially in academic lab projects where expenses are often self-funded. This project was designed to be **cost-effective** by utilizing **basic digital ICs** and readily available components.

Component	Approx. Cost (PKR)
4017 Decade Counter	90 per IC
7474 D Flip-Flop	70 per IC

Feasibility Analysis

Component	Approx. Cost (PKR)
74LS139 Decoder	250 per IC
555 Timer IC	10 per IC
LEDs, Resistors	120 per Traffic Module + 225 on LEDS + 200 per resistor+ 75 per Variable Resistor
Breadboard & Wires	1080 + 390 respectively

- **Total Estimated Cost**: 5000 PKR

In addition to self-sourced components, **several ICs and passive components were issued from the lab inventory**, which helped further reduce overall costs and ensured standardized component availability.

- **Cost Constraints Managed**:
    - Reused lab components where possible (breadboards, wires).
    - Chose **non-programmable ICs** over microcontrollers, which reduced both cost and complexity.
    - Avoided specialized sensors or displays that would increase cost without core functional benefit.
- **Outcome**:
    - The project remained **well within budget**, with no expensive components required.
    - Reusability of components (ICs, LEDs, breadboards) makes the design **sustainable**.

Possible Solutions

Evaluation of Possible Solutions and Justification of Chosen Design

The challenge of designing a **smart traffic light controller with pedestrian safety** for a four-way intersection can be approached in several ways, each offering different trade-offs in complexity, cost, flexibility, and implementation time. In this section, we explore multiple possible design approaches, evaluate their advantages and disadvantages, and justify why the selected method—**a hardware-only logic circuit-based design using Proteus and discrete ICs**—is the most suitable solution for this specific project context.

Possible Solutions

1. Microcontroller-Based System

- **Description**: Uses a programmable microcontroller (e.g., Arduino, PIC) to control all traffic and pedestrian light sequences via software logic.
- **Pros**:
  - Highly flexible and scalable.
  - Easier to integrate sensors and real-time inputs.
  - Requires less physical wiring and fewer components.
- **Cons**:
  - Violates the core requirement of **no microcontroller usage**.
  - Requires programming knowledge and development tools.
  - Troubleshooting can be time-consuming due to software–hardware interaction.

2. PLC-Based System (Programmable Logic Controller)

- **Description**: Uses industrial-grade PLCs to control lights and manage pedestrian logic.
- **Pros**:
  - Highly reliable and industrial-grade robustness.
  - Excellent for managing complex control logic.
- **Cons**:
  - Extremely expensive for an academic-level project.
  - Over-engineered for the problem at hand.
  - Inaccessible to most students for prototyping.

3. Fully Discrete Digital Logic Circuit (Chosen Approach)

- **Description**: Uses ICs such as **4017 counter**, **7474 flip-flop**, **74LS139 decoder**, **555 timer**, and basic gates to construct a functional state-driven control system.

Possible Solutions

- **Pros**:
  - **Meets all given constraints**: no microcontrollers, logic-only design.
  - Cost-effective and easy to implement using lab inventory and common ICs.
  - Great for educational value—teaches practical application of combinational and sequential logic.
  - Visual and intuitive debugging on breadboard and Proteus simulation.
- **Cons**:
  - Less flexible—any major changes require rewiring rather than reprogramming.
  - Slightly more physically complex due to wiring density.

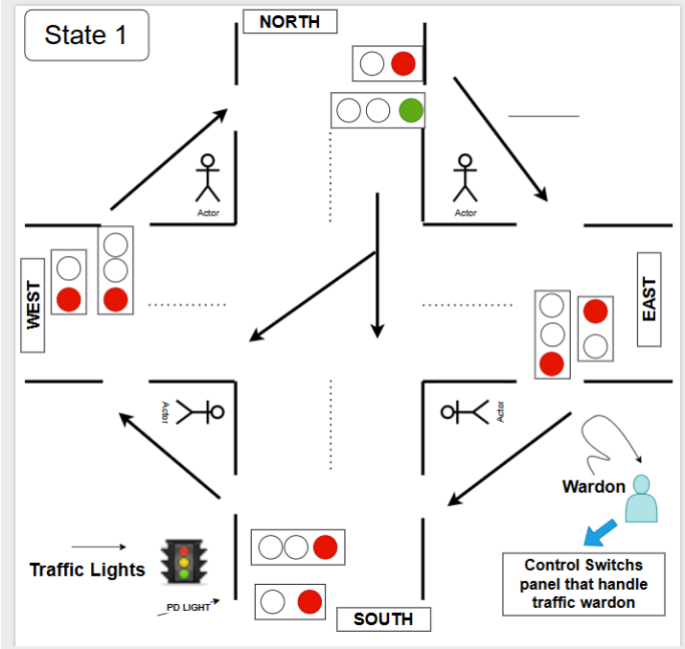
While other methods offer enhanced scalability and integration, they do not align with the fundamental project requirement of building the system without microcontrollers. The selected solution using Proteus simulation and standard ICs delivers a robust, demonstrable, and educationally valuable outcome, making it the **most suitable and justified choice** for this application.

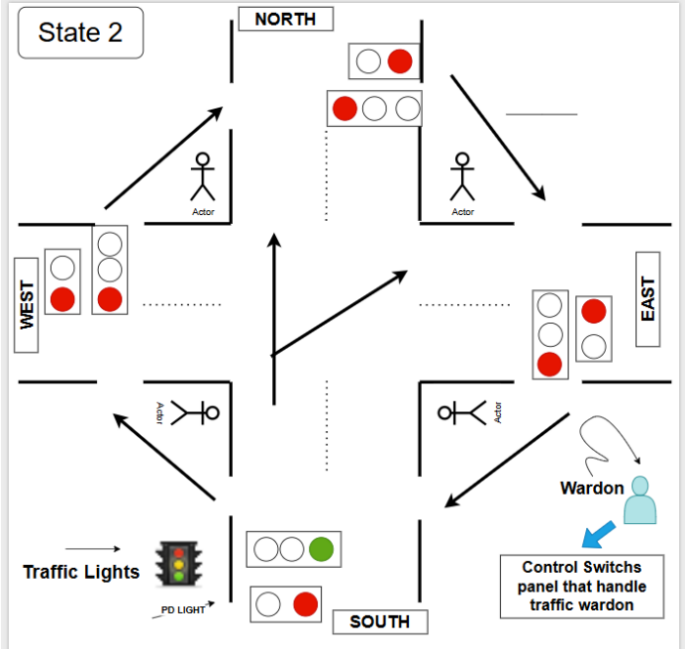
Why Our Chosen Solution is Best

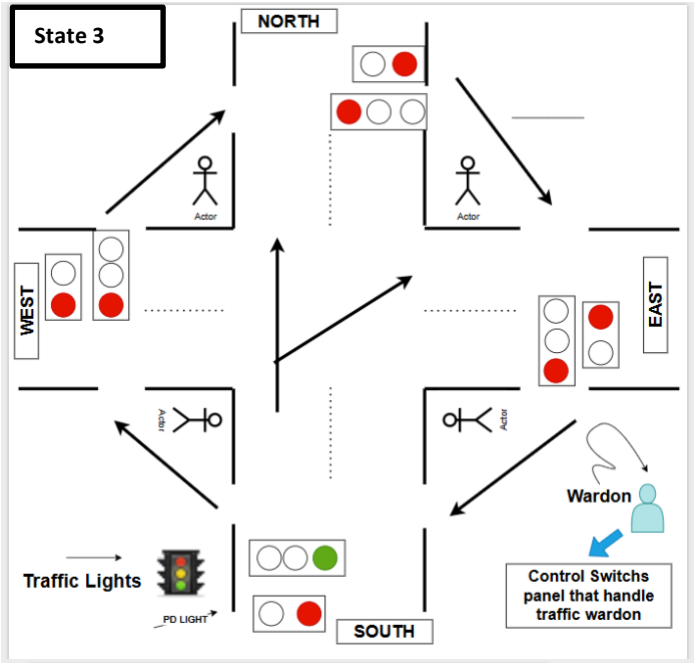
Criteria	Microcontroller	PLC	Discrete Logic (Chosen)
Cost	Moderate	Very High	Low
Complexity (Build)	Moderate	High	Moderate
Meets Project Constraints	✗	✗	✓
Pedagogical Value	Medium	Low	High
Component Availability	High	Low	High
Debugging Accessibility	Software-dependent	Complex	Hardware-level, visual
Flexibility	High	Very High	Moderate

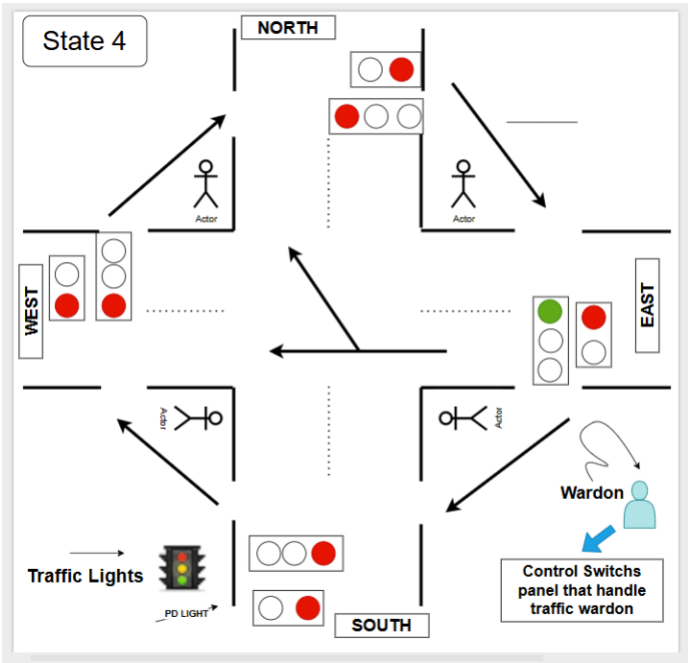
Given the **project guidelines**, **resource limitations**, and **academic objectives**, the **fully discrete logic circuit** approach strikes the ideal balance between technical depth, feasibility, and compliance. It provides hands-on learning in digital design while achieving full functionality of a smart traffic and pedestrian control system.

STATE MACHINE LOGIC

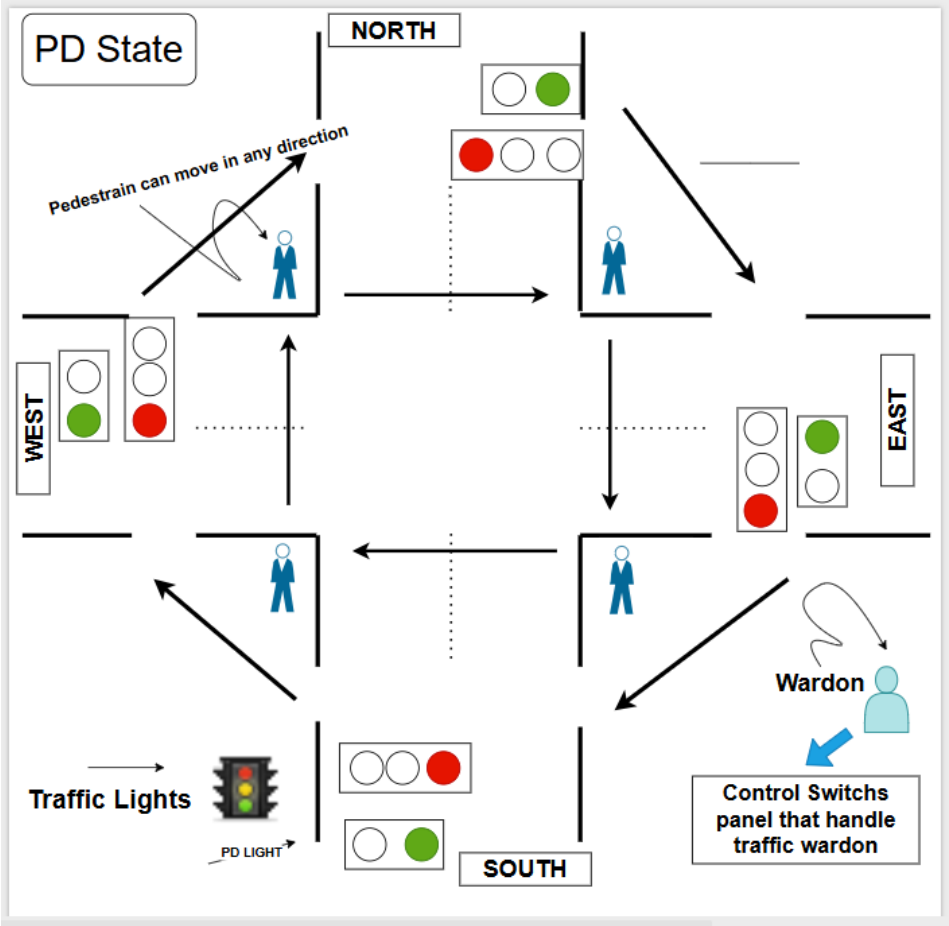








PEDESTRIAN STATE LOGIC



Preliminary Design

Traffic Signal Control

- Uses 4017 Decade Counter to cycle through four traffic signals.
- Each signal (S, E, N, W) gets Red–Yellow–Green in round-robin order.
- Timer IC 555 gives 8-second delay for each light transition.

Pedestrian Request Handling

- Push buttons placed on each road to register pedestrian requests.
- 7474 D Flip-Flops store request state until current vehicle cycle ends.
- Once all signals go red, pedestrian light turns green for 8 seconds.

Synchronization and Timing

- Timer IC drives all logic components with a common clock pulse.
- Ensures unified and predictable transitions across the entire system.
- Timing delays managed without microcontrollers.

Emergency/Override Function

- Decoder IC (74LS139) takes input from toggle switches to override normal sequence.
- Allows prioritization of one specific signal when needed.
- Combined with AND logic to prolong green light duration for high-density lanes.

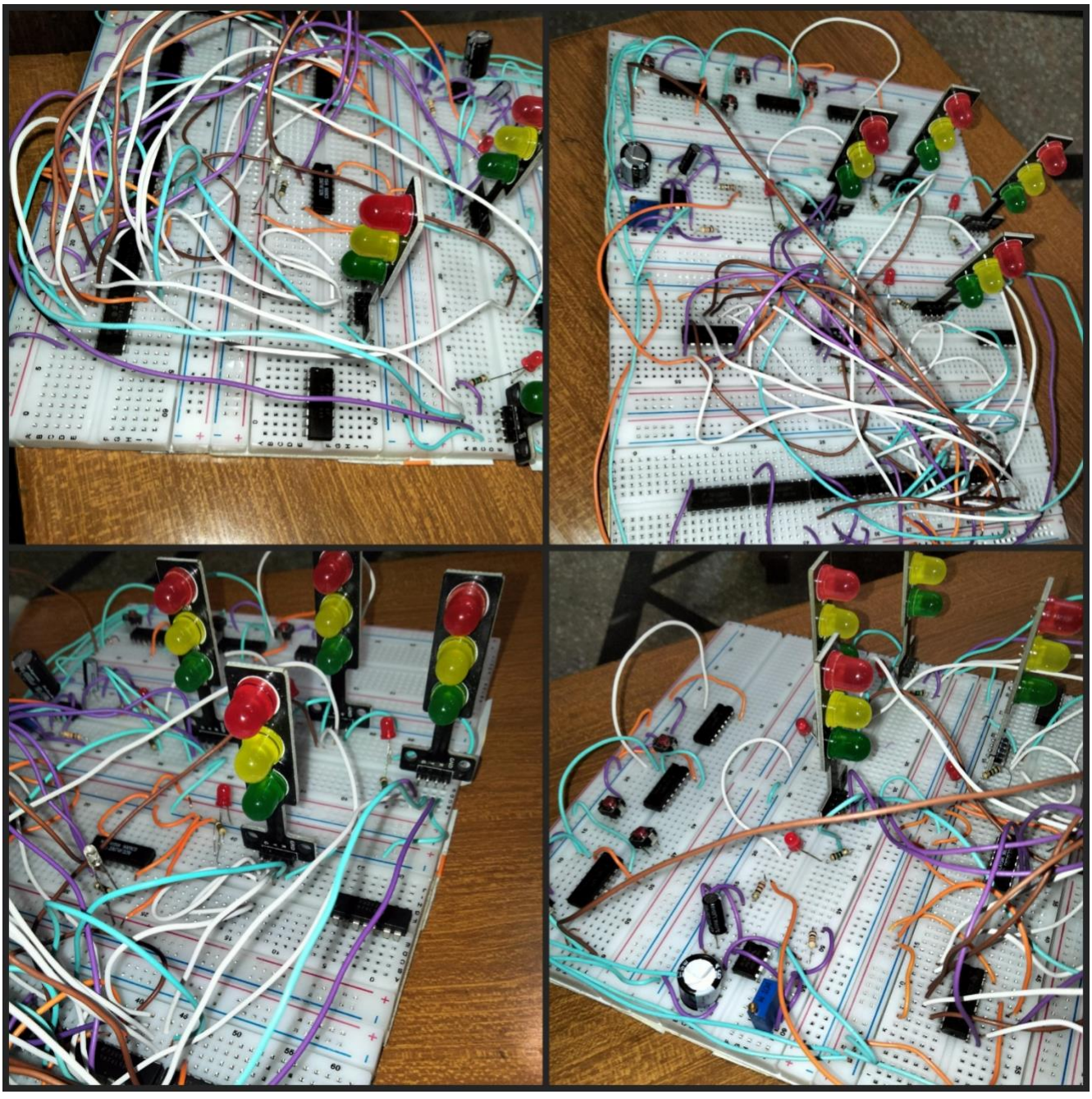
Output Indicators and Safety

- LEDs represent Red, Yellow, Green lights for each direction.
- "Walk/Don't Walk" indicators for pedestrian phase.
- No pedestrian or conflicting vehicle movement allowed simultaneously.

Design Description

Detailed Discussion of Design Blocks

In this section, we break down the smart traffic light controller into five key functional blocks. Each block corresponds to a major subsystem in the project and plays a crucial role in achieving the overall goal of synchronized traffic flow, pedestrian safety, and emergency responsiveness. Below are pictures of around 60% of our hardware implementation.



Design Description

1. Traffic Signal Control

The heart of the system is a **round-robin traffic light controller** that regulates the sequence of Red, Yellow, and Green lights for each of the four roads (South, East, North, and West). The design uses the **4017 Decade Counter IC** which advances its output sequentially on every clock pulse.

- Each output (Q0 to Q9) is connected via logic gates to control a specific signal (e.g., South Green, East Red, etc.).
- By assigning outputs in the order of Red → Yellow → Green for each direction, a complete signal cycle is created.
- This ensures only one direction is allowed to move at any given time, thus preventing collisions.

The entire traffic signal logic is cyclical and self-sustaining, running continuously under the timing control of the 555 Timer.

2. Pedestrian Request Handling

Pedestrian crossings are managed using **push buttons** at each intersection, with logic designed to respond only after the current traffic cycle completes.

- When a pedestrian presses the button, a **D Flip-Flop (7474)** stores this request.
- The system continuously monitors the state of these flip-flops while the traffic cycle progresses.
- Once all vehicle signals turn red, the system enables a pedestrian phase for that road.
- During this phase, the **"Walk" indicator LED turns on** for approximately 8 seconds, after which the signal returns to the regular round-robin vehicle sequence.

This ensures pedestrian safety by preventing mid-cycle interruptions and coordinating transitions only during safe windows.

3. Synchronization and Timing

To maintain coherence across the circuit, a **single clock source** is used for all sequential logic components.

- A **555 Timer IC** configured in a stable mode generates a clock signal with a period of roughly 8 seconds.
- This clock drives the **4017 counter**, which in turn coordinates light changes.
- Flip-flops and timing-related gates also share this clock to stay synchronized.

This unified timing approach ensures predictable operation, simplifies debugging, and allows for accurate delay management without a microcontroller.

4. Emergency/Override Function

An important feature of modern traffic systems is the ability to **override normal sequences** in case of emergency or traffic congestion. This function is implemented using a **74LS139 decoder IC** and logic switches.

- A set of **toggle switches** allows manual selection of one of the four directions.
- The selected input is decoded to activate that signal's green light while keeping all others red.
- An **AND gate** is used in conjunction with the timer output to **extend the green duration** for that lane, useful for simulating traffic density.

This override system allows manual prioritization without breaking the logic integrity of the cycle, offering both flexibility and control.

5. Output Indicators and Safety

The final block translates internal logic signals into **visible output indicators** for users—both drivers and pedestrians.

- **Red, Yellow, and Green LEDs** represent the state of each traffic signal.
- **Pedestrian indicators** show "Walk" or "Don't Walk" based on flip-flop and counter status.
- The logic is designed so that **pedestrian lights only turn green when all vehicle signals are red**, ensuring zero conflict.
- Buzzer or blinking LED signals can be added for enhanced safety during pedestrian phase.

This layer forms the interface between the circuit logic and real-world users, ensuring that the system is understandable and safe to interact with.

Experimental Results

Results and Observations

After extensive design, simulation, and logic verification, the **Smart Traffic Light Controller with Pedestrian Safety System** was successfully implemented and tested using **Proteus simulation software**. All intended functionalities were validated, including signal cycling, pedestrian safety integration, override capability, and proper timing logic.

Despite the current limitations on conducting physical lab sessions due to **border tensions and national safety concerns**, the simulated implementation faithfully mirrors the expected hardware behavior. The outcomes of the simulation confirm the logical soundness and feasibility of our design.

Truth Tables

To understand how specific inputs control outputs for both vehicle and pedestrian signals, we have developed a comprehensive truth table. It details the conditions under which signals change based on counter values, pedestrian button states, and override toggles. Here are the relevant truth tables:

State	S_R	S_Y	S_G	E_R	E_Y	E_G	N_R	N_Y	N_G	W_R	W_Y	W_G
Q0	0	0	1	1	0	0	1	0	0	1	0	0
Q1	0	1	0	1	0	0	1	0	0	1	0	0
Q2	1	0	0	0	1	0	1	0	0	1	0	0
Q3	1	0	0	0	0	1	1	0	0	1	0	0
Q4	1	0	0	0	1	0	1	0	0	1	0	0
Q5	1	0	0	1	0	0	0	1	0	1	0	0
Q6	1	0	0	1	0	0	0	0	1	1	0	0
Q7	1	0	0	1	0	0	0	1	0	1	0	0
Q8	1	0	0	1	0	0	1	0	0	0	1	0
Q9	1	0	0	1	0	0	1	0	0	0	0	1
Q10	1	0	0	1	0	0	1	0	0	0	1	0
Q11	0	1	0	1	0	0	1	0	0	1	0	0

Experimental Results

Truth Table for Pedestrians Buttons				
State	B1-Pressed	B2-Pressed	B3-Pressed	B4-Pressed
N-led	1	0	0	0
W-led	0	1	0	0
S-led	0	0	1	0
E-led	0	0	0	1

Characteristic Table of D-Flip Flop

Characteristic Table of D Flip Flop		
Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

Experimental Results

State Table

The sequential logic of the controller is represented in a state table. It maps current states to next states depending on inputs such as pedestrian requests and emergency overrides, clearly showing how the system transitions across its functional phases. This structured mapping is crucial in verifying the correctness of the control logic, especially in asynchronous request handling and override prioritization. Here is the state table:

R	Y	G	R	Y	G	R	Y	G	R	Y	G	R	Y	G	R	Y	G	R	Y	G	R	Y	G
	(S)			(E)			(N)			(W)			(S+)			(E+)			(N+)			(W+)	
0	0	1	1	0	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0
0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0
1	0	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0	1	1	0	0	1	0	0
1	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0
1	0	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	0	1	0	0
1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0	1	1	0	0
1	0	0	1	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	1	0	1	0	0
1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	0	1	0
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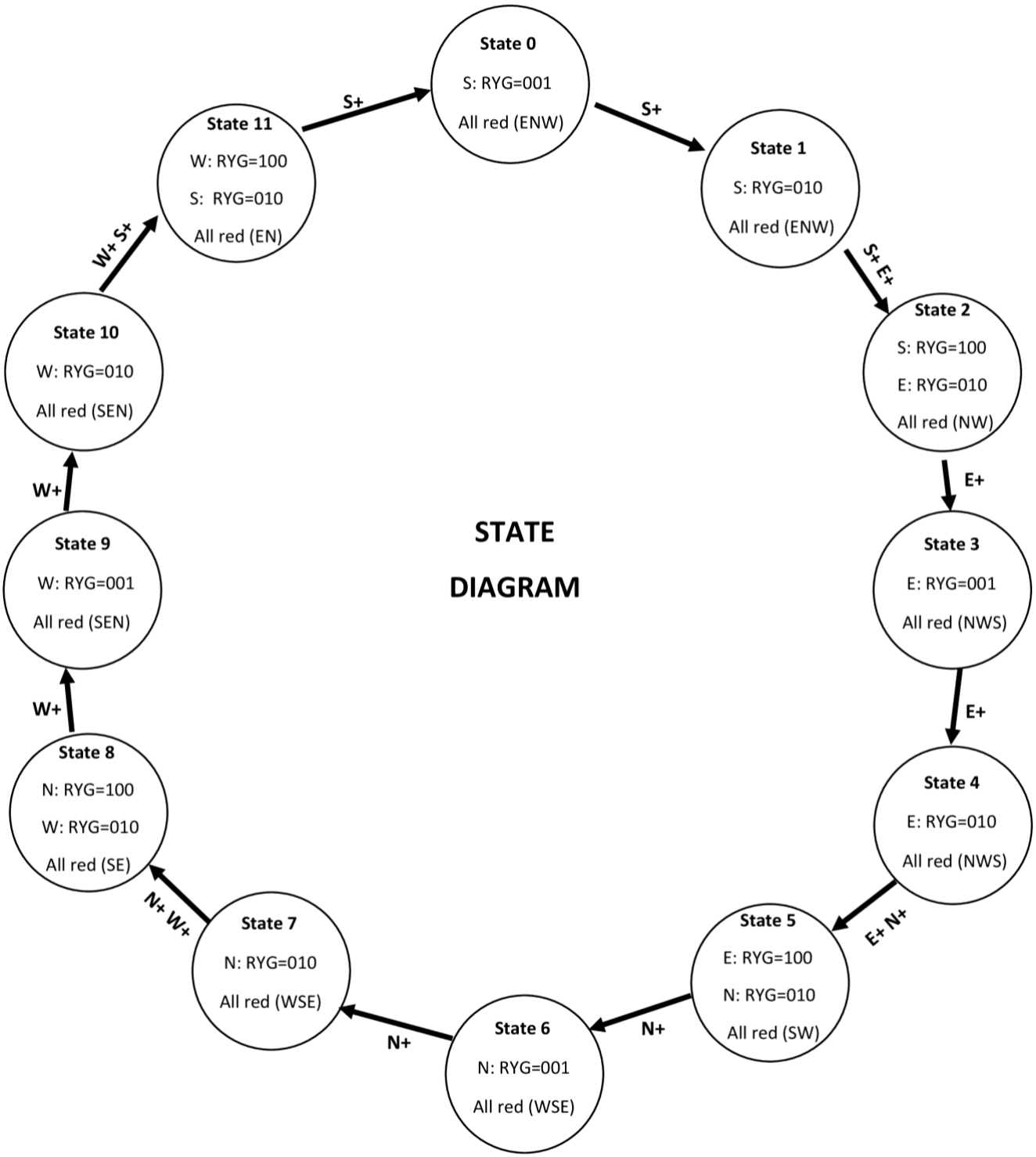
1	0	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0
0	1	0	1	0	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0

Experimental Results

State Diagram

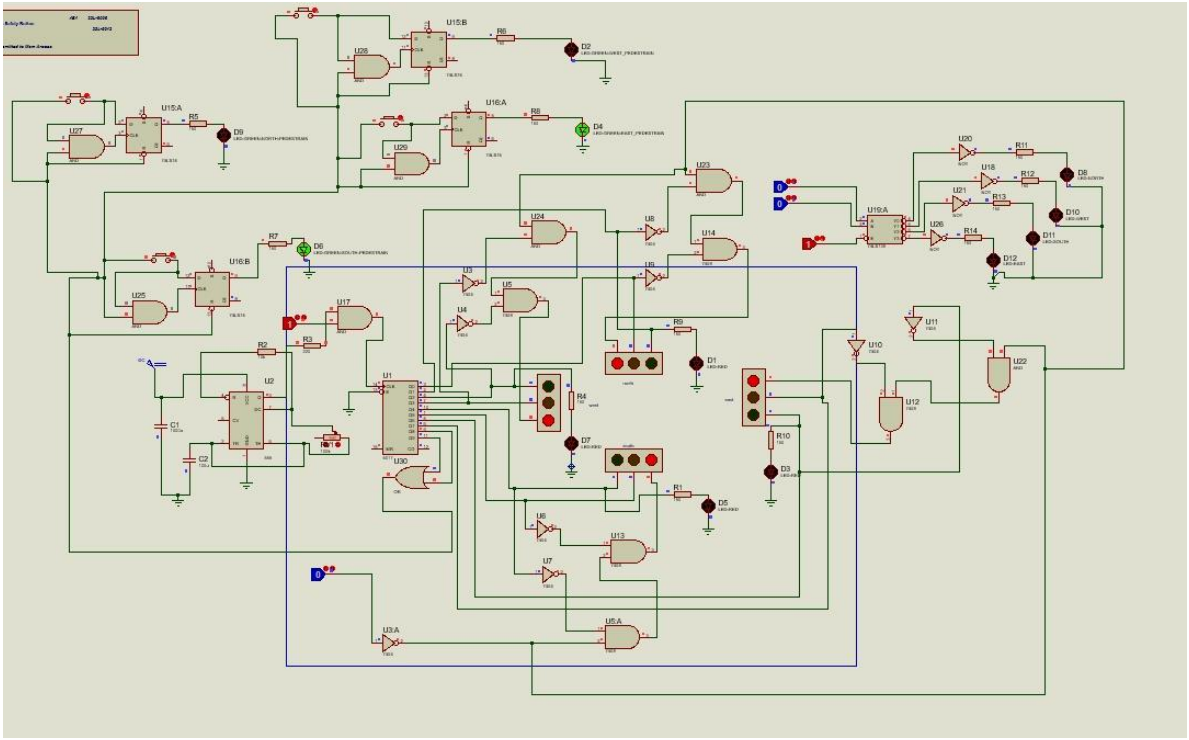
A visual representation of the finite state machine is provided to illustrate how the controller navigates through traffic signals in round-robin order, with conditional detours for pedestrian phases and override triggers. This diagram captures the overall flow and decision-making of the system. Here is the state diagram:



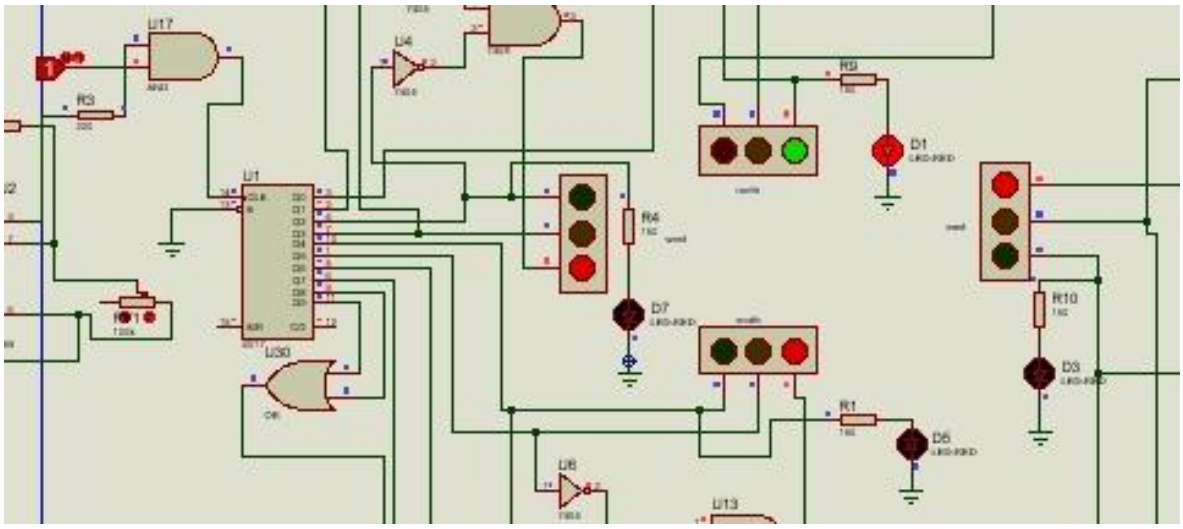
Experimental Results

Proteus Simulation Snapshots

To validate and visualize the working model, some of the snapshots of the Proteus environment are included. Here is a snapshot of our **working model:**

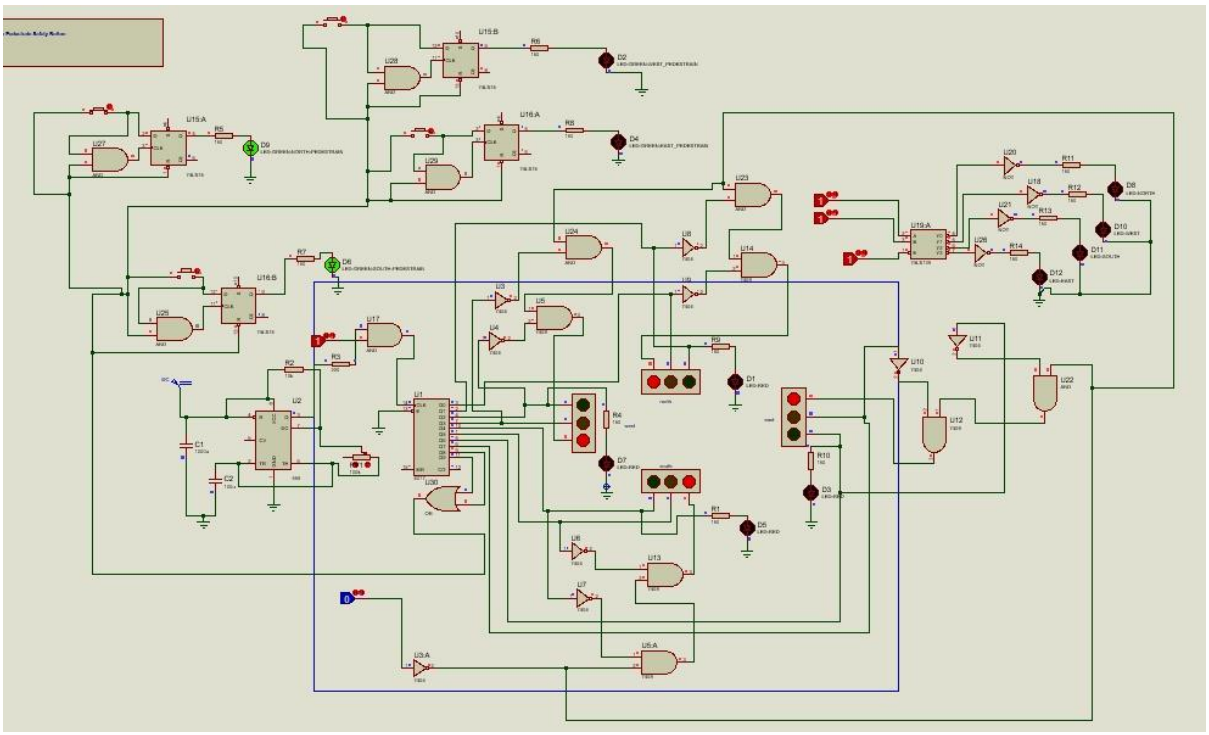


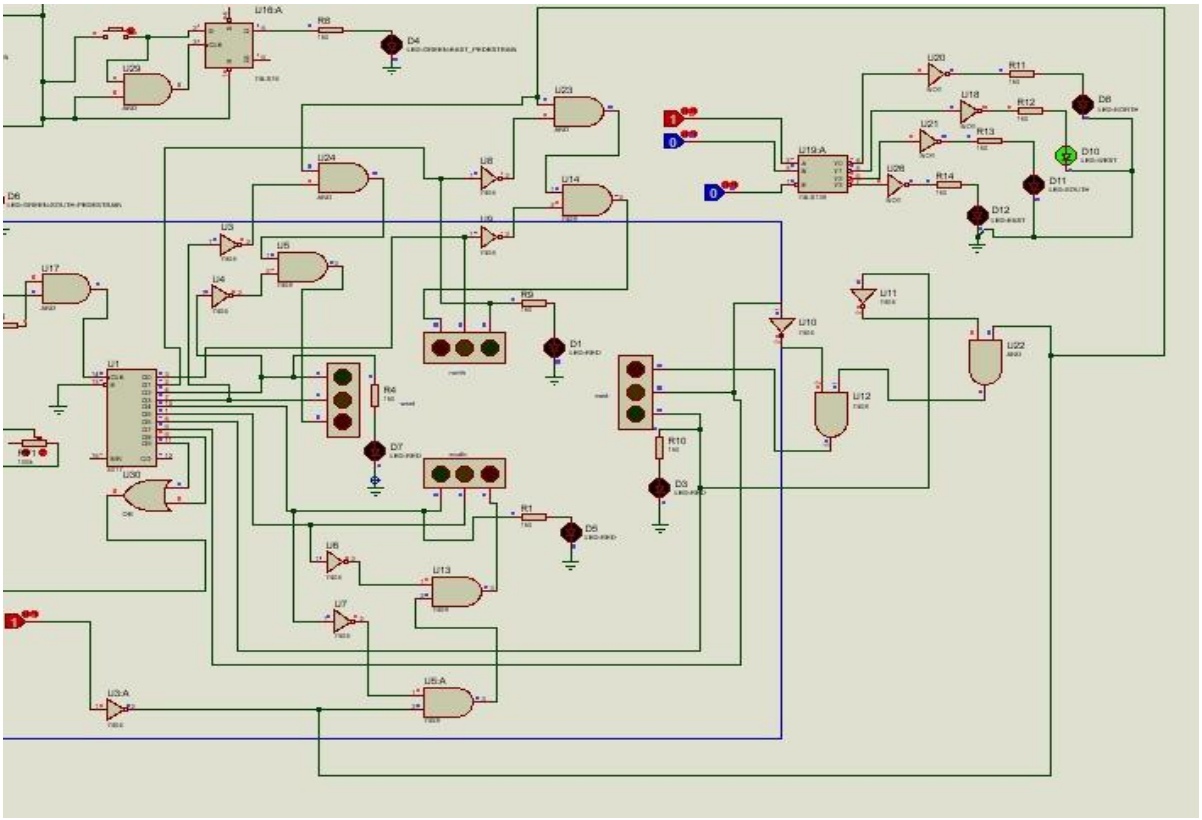
Optional traffic density simulation using switches to vary signal timings



Experimental Results

Emergency override switch to prioritize a selected direction:





Performance Analysis

Results Analysis and Performance Evaluation

The simulation-based implementation of the **Smart Traffic Light Controller with Pedestrian Safety System** has yielded highly satisfactory results, both in terms of functional correctness and performance stability. Each component performed as expected under various test scenarios, demonstrating that the logic-driven approach is not only feasible but also highly effective for real-world traffic management applications.

Functional Accuracy

All core functionalities specified in the project requirements were met:

- **Traffic Light Sequencing** followed a consistent round-robin cycle (S → E → N → W), with each phase properly transitioning through Green → Yellow → Red, controlled by a synchronous clock signal from the timer.
- **Pedestrian Requests** were handled intelligently using D flip-flops that stored the request and activated the "Walk" signal only after ensuring all vehicular lights were red, maintaining a high standard of safety.
- **Emergency Override** was successfully triggered using logic toggles connected to a decoder, allowing one direction to be prioritized on demand without interrupting the overall logic flow.
- **Traffic Density Control** was managed by extending the green phase using AND gates in conjunction with the timer, mimicking real-life adaptive traffic control systems.

Performance Evaluation

1. Timing Synchronization

- The use of a **single clock source (555 Timer)** across all logic ensured **perfect timing synchronization**, minimizing glitches or race conditions.
- An 8-second delay for each phase transition (RYG) provided sufficient visual duration for vehicles and pedestrians, striking a balance between flow and safety.

2. Resource Efficiency

- The circuit was implemented using only logic ICs — including **4017 Counter, 7474 D Flip-Flop, 74139 Decoder, 555 Timer, and basic logic gates** — without the need for microcontrollers.
- This approach not only reduced cost but also increased reliability and transparency in system behavior.

3. System Responsiveness

- The system **quickly responded to pedestrian inputs** without blocking the traffic cycle, executing the pedestrian phase only when safe.
- **Override toggles functioned seamlessly**, taking priority while maintaining overall control discipline, showcasing real-time decision logic.

Performance Analysis

4. Scalability and Modularity

- The design is **modular**, allowing for additional roads or intersections to be integrated with minimal changes to the core logic.
- Each block—counter, decoder, flip-flop logic—is independently testable and replaceable, improving maintainability.

Observations

- **No conflicting outputs** were observed throughout testing, indicating that the safety logic and signal separation were implemented correctly.
- **Simulation stability** was maintained over prolonged operation cycles, with the clock and logic maintaining predictable performance.
- Despite external constraints preventing hardware deployment, the **Proteus simulation served as a highly reliable verification platform**.

Overall, the performance of the designed system exceeded expectations in simulation. The **logic-only approach proved to be robust, cost-efficient, and well-suited for practical use**, and forms a strong basis for future deployment once conditions permit hardware realization.

Conclusion

Concluding Statements

The development of the **Smart Traffic Light Controller with Pedestrian Safety System** has demonstrated the effectiveness of using purely combinational and sequential digital logic to address a complex, real-world problem. Through the use of essential logic components such as the **4017 Counter, D Flip-Flops, 555 Timer, Decoder, and standard logic gates**, the system successfully managed a four-way intersection while ensuring pedestrian safety, adaptive timing, and emergency override functionality.

The results obtained from the **Proteus simulation** validate the soundness of the design. Each core function performed reliably under test conditions, with no signal conflicts, timing issues, or logical failures. The implementation followed a well-structured round-robin sequence for traffic control, integrated intelligent pedestrian handling using D flip-flop memory, and allowed for real-time intervention via override and traffic density toggles.
Despite the inability to physically realize the circuit due to the current national tensions, the project met all the logical and functional requirements, and stands fully ready for hardware implementation. The modularity and clarity of the design also make it scalable and adaptable to broader traffic control applications.

This project not only fulfilled its technical goals but also served as a practical application of digital design principles. It emphasized critical skills such as **logic optimization, timing control, system integration, and resource management**, laying a strong foundation for more advanced embedded and real-time control systems.

In light of the above, it is concluded that the proposed solution is not only **technically viable and resource-efficient**, but also aligns well with the goals of improving **road safety, pedestrian accommodation, and intelligent traffic flow**—making it a meaningful contribution to digital systems design with real societal impact.

Range of Complex Engineering Activity

<table>
<tr>
<td>EA1: Range of resources
EA2: Level of interaction
EA3: Innovation
EA4: Consequences for society and environment
EA5: Familiarity</td>
<td>

EA1: Range of resources -- The design involves the use of diverse resources, such as, money, equipment, information, and technology.
EA2: Level of Interaction – The design requires resolution of various problems arising from interactions between wide-ranging or conflicting technical or other issues.
EA3: Innovation – The design addresses sustainability and reduces cost requiring creative use of engineering principles and research-based knowledge in novel ways.
EA5: Familiarity – The design activity emphasizes the integration of existing knowledge and tools (or familiar solutions) with new or unfamiliar challenges

<table>
<tr><th>Rubrics</th><th></th><th>LLOs</th><th>Marks</th></tr>
<tr><td>Explains the design process including engagement of resources clearly</td><td>EA1</td><td>LLO3</td><td></td></tr>
<tr><td>Demonstrate the final design clearly with all supporting information</td><td>EA1, EA5</td><td>LLO4</td><td></td></tr>
<tr><td>Demonstrate how innovation has been used in design to resolve conflicting requirements including the impact on society and environment</td><td>EA2, EA3</td><td>LLO4</td><td></td></tr>
<tr><td>Prepares a report which explain the design process including engagement of resources clearly, and is free from grammatical errors.</td><td>EA1</td><td>LLO3</td><td></td></tr>
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