Electronic Devices and Circuits

Assignment-3(CEP)

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Design and Analysis of Single-Stage BJT Amplifier.

- Open circuit voltage gain

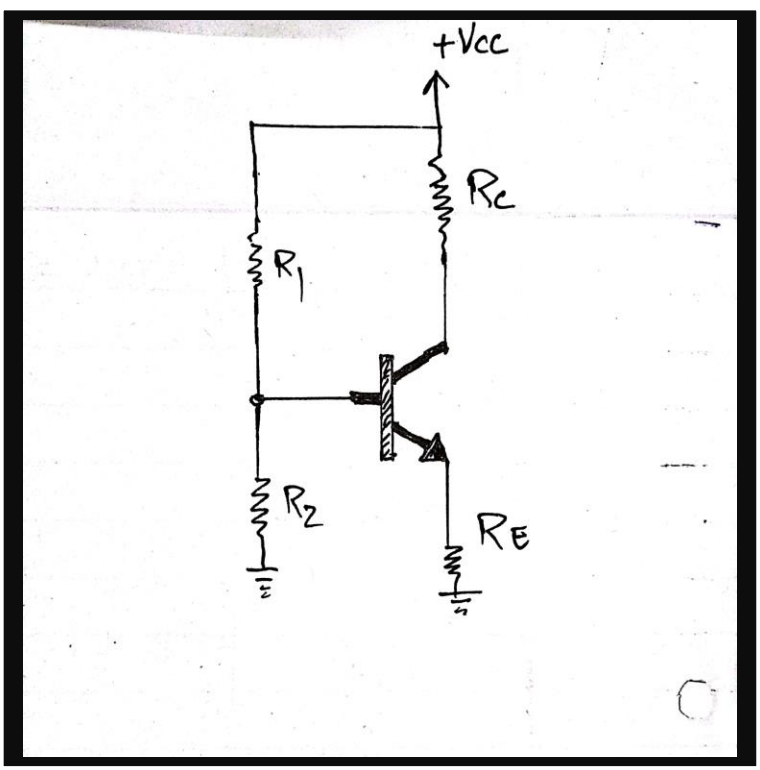
  Avo = 5 x (6 + 0 + 0 + 6) = 60

- Input resistance must be greater than 40kΩ
  Rin = (1+ β) (re + Re) > 40kΩ

- The output impedance should be less than 500 Ω
  Zout ≈ RC || RL < 500Ω

So first we do **DC Analysis**

- As a starting point, take DC operating current *Ic* = 1m at room temperature.
- Assume β = 100



Re = $\frac{Vt}{Ie}$ (IC ≈ IE)

Re = $\frac{26m}{1mA}$ = 26

VCC = +15V

We use Assumptions

VB = $\frac{VCC}{3}$ = $\frac{15}{3}$ = 5V

ICRC = $\frac{VCC}{3}$

RC = 5kΩ

VBE = VB – VE

VE = 5 – 0.7 = 4.3V

VE = IERE

RE = $\frac{VE}{IE}$ = 4.3kΩ

Take IB 10% if IE

IB = 0.1m

R1 + R2 = $\frac{VCC}{IB}$ = $\frac{15}{0.1m}$

R1 + R2 = 150k

Applying VDR

VB = VCC x $\frac{R2}{R1+R2}$

(150) $\frac{5}{15}$ = R2

R2 = 50kΩ

R1 + R2 = 150k

R1 = 100kΩ

R1 || R2 = 33.3kΩ

Rin = (1 + β) (re + Re) = 101 x (26 + 4.3k) = 436.92k > 40k

If we take RB parallel, then Rin is

Rin = RB || (1 + β) (re + Re) = 33.3k || 436.92k = 30.94k < 40k (false)

- Cheak the Open circuit voltage gain

Avo = $\frac{RC}{re+Re}$

= $\frac{5k}{26+4.3k}$ = 1.13, Our requirements are not fulfilled

So, we put Avo = 60

RE = $\frac{Rc}{Avo}$ - re = $\frac{5k}{60}$ – 26 = 57.33 Ω (Take standard 56Ω)

Avo = $\frac{RC}{re+Re}$

= $\frac{5k}{26+56}$ = 60.97

Cheak Rin

Rin = (1 + β) (re + Re) = 101 x (26 + 56) = 8282

Rin = RB || (1 + β) (re + Re) = 33.3k || 8282 = 6232.45Ω

gm = $\frac{Ic}{Vt}$ = $\frac{1m}{26m}$ = 0.0384

r π = $\frac{\beta}{gm}$ = 2.6kΩ

Output Impedance, take RL = 450Ω

RC || RL = $\frac{RC\ x\ RL}{RC+RL}$ = 5k || 450 = 395.94 < 500Ω (Condition true)

Av = $\frac{-gm\ (Rc||RL)}{1+gmRe}$ = 95.26m V/V.

- **Take Is= 10^−14 and VB = 0.7V at room temperature**

IC = Is x $e^{Vbe/Vt}$ -> Vt = 26m

IC = 4.92mA

ICRC = VCC/3

RC = 345.78Ω

We take RC = 360Ω

IE ≈ IC

RE = VE / IE

= $\frac{4.3}{4.92m}$ = 873.9Ω

We take 810Ω standard

re = Vt / Ie = 5.284Ω

Rin = (1 + β) (re + Re) = 101 x (5.284 + 810) = 82.3kΩ > 40kΩ

IB 10% of IE

IB = 0.492m

R1 + R2 = 15/0.492m

R1 + R2 = 30.48k

Apply VDR

R1 = 20.32kΩ

R2 = 10.16kΩ

RB = R1 || R2 = 6.77kΩ

➔ Take RB in parallel

Rin =RB || (1 + β) (re + Re) = 6.27kΩ (False)

➔ Take RB in the Series

Rin = $\frac{RB}{1+\beta}$ + (1 + β) (re + Re) = 82.367kΩ > 40kΩ

Consider a biasing scheme that provides thermal bias stability.

VE = 2V

Then RE = $\frac{VE}{IE}$ = 406Ω

->Take standard 390Ω

Rin = (1 + β) (re + Re) = 101 x (5.284 + 390) = 39.9kΩ < 40kΩ

->So, we improve it take 430Ω

Rin = (1 + β) (re + Re) = 101 x (5.284 + 430) = 43.9kΩ > 40kΩ

Avo = $\frac{Rc}{re+Re}$

60 = $\frac{360}{5.284+Re}$, Re = 0.716Ω

So, we adjusted Re so that our open circuit gain was equal to our requirement.

Avo = $\frac{Rc}{re+Re}$

= $\frac{390}{5.284+0.716}$

= $\frac{390}{5.284+1}$ take Re standard 1.0Ω, and adjust the RC = 390Ω

= 62.06

Check Output Impedance

Zout = RC || RL

Take RL = 2.2kΩ, RC = 390Ω

Zo = $\frac{RC\ x\ RL}{RC+RL}$ = $\frac{390*2.2k}{390+2.2k}$ = 331.27 < 500Ω

gm = $\frac{Ic}{Vt} = \frac{4.96m}{26m}$ = 0.1907

Av = $\frac{-gm\ (Rc||RL)}{1+gmRe}$ = -53.055 V/V

Temperature Analysis

The performance of the amplifier changes with temperature due to variations in the parameters of the BJT:

Effect on DC Parameters

1. **VBE:**
    - VBE decreases at −2mV/∘C.
    - At room temperature (25∘C), VBE = 0.7V.
    - At 60∘C: VBE=0.7V−2mV/∘C⋅ (60−25) = 0.63V
    - At −10∘C: VBE=0.7V+2mV/∘C⋅ (25−(−10)) = 0.76V
2. **IC:**
    - IC = Is x $e^{Vbe/Vt}$
    - As VBE decreases, IC increases exponentially.
    - IC approximately doubles for every 10∘C rise in temperature.
3. **VCE:**
    - VCE = VCC − ICRC
    - As IC increases, VCE decreases, reducing the available signal swing.

Effect on AC Parameters

1. **re:**
    - re=VT / IE
    - With VT increasing linearly and IC increasing exponentially, re decreases:

      $$re \propto \frac{1}{Ic}$$

    - At 25∘C, re=5.284Ω

- At 60∘C, assuming IC doubles (IC ≈ 9.84mA): re = 26m / 9.84 = 2.64Ω

2. **Open-Circuit Voltage Gain (Avo):**
   - Avo = $\frac{Rc}{re+Re}$
   - At 25∘C: re=5.284, Avo = $\frac{390}{5.284+1}$ = 62.06
   - At 60∘C, re=2.64Ω, Avo = $\frac{390}{2.64+1}$ = 110.57
   - The gain increases with temperature, which may lead to distortion.
3. **Input Resistance (Rin):**
   - Rin=(1+β) (re + RE)
   - At 25∘C, Rin=43.9kΩ
   - At 60∘C, re=2.64Ω, Rin=101 x (2.64Ω+1Ω) = 26.56kΩ
   - Rin decreases, which could cause input signal distortion.
4. **Output Resistance (Rout):**
   - Rout is determined primarily by RC ∥ RL and is less affected by temperature.

- **Signal Swing**

The signal swing is determined by the maximum VCE variation. For proper operation, VCE must remain above the saturation voltage (VCE (sat)) and below VCC.

1. **Maximum VCE:**

   VCE (max) = VCC − IC (min) RC

   - At 25∘C, IC=4.92mA, VCE (max) = 15V−(4.92mA·390Ω) = 13.08V
2. **Minimum VCE:**

   VCE (min) = VE

   - VCE (min)=2V
3. **Signal Swing:**

ΔVCE = VCE (max) − VCE (min)=13.08V−2V = 11.08V

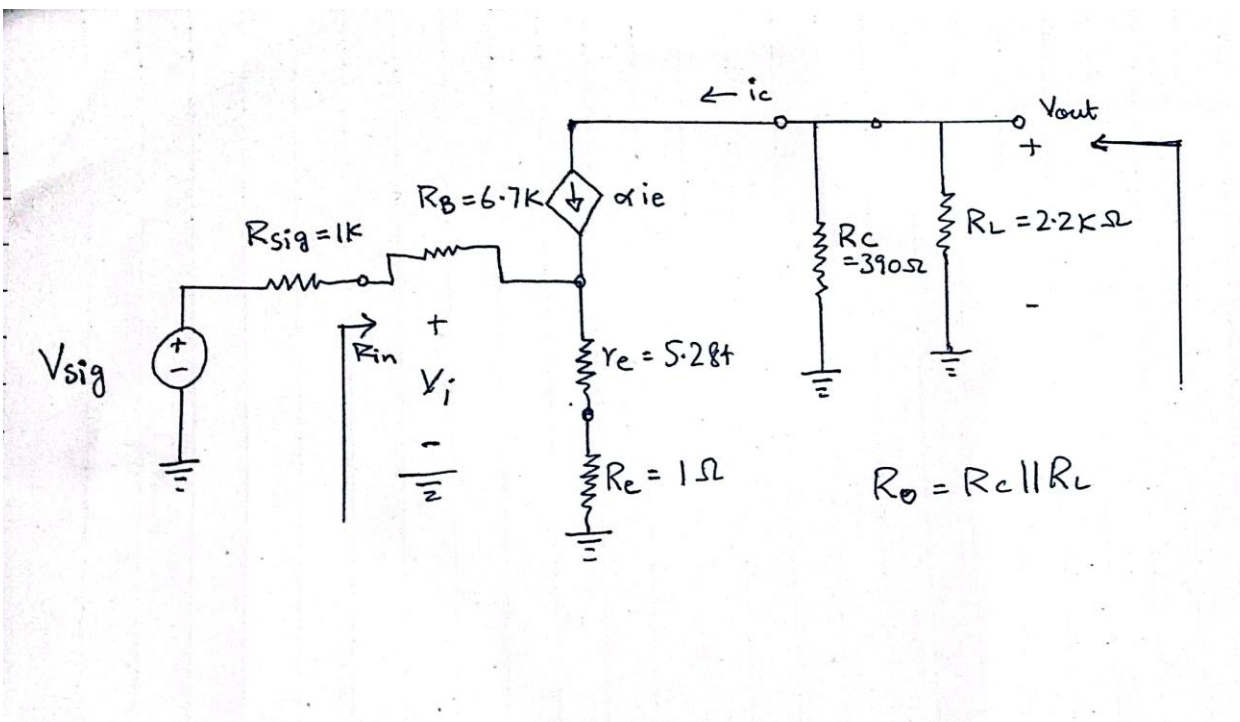
Using the open-circuit voltage gain   Av=62.06

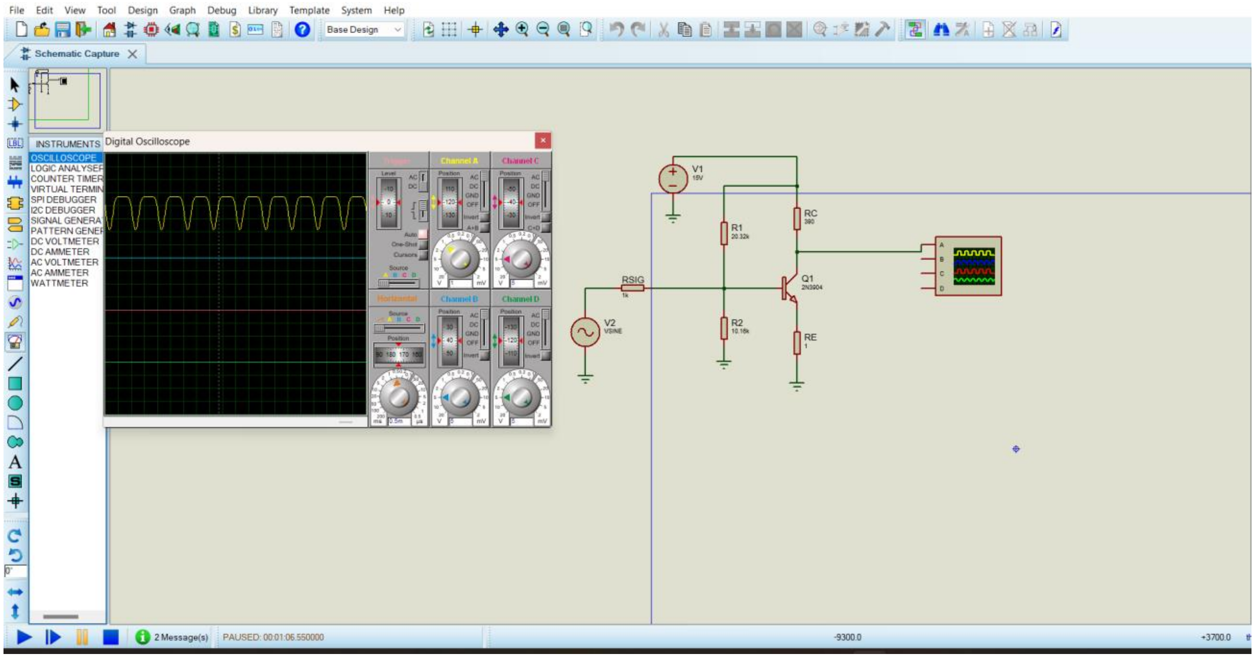
VP = 11.08/62.06 = 178.5mV this is too low, we take 300mV to achieve our requirements

➤ **Conflicting Requirements and Tradeoffs**

1. **Voltage Gain vs. Thermal Stability:**
    - To achieve a gain of 60, RE was minimized, reducing thermal stability.
    - This tradeoff can be mitigated by adding a bypass capacitor across RE, maintaining Avo while improving thermal stability.
2. **Input Resistance vs. Voltage Gain:**
    - Increasing RE improves Rin but reduces Avo. The chosen RE balances both requirements.
3. **Output Resistance vs. Signal Swing:**
    - A lower RC reduces Rout but also limits signal swing. The chosen RC provides an acceptable balance.

T – Model

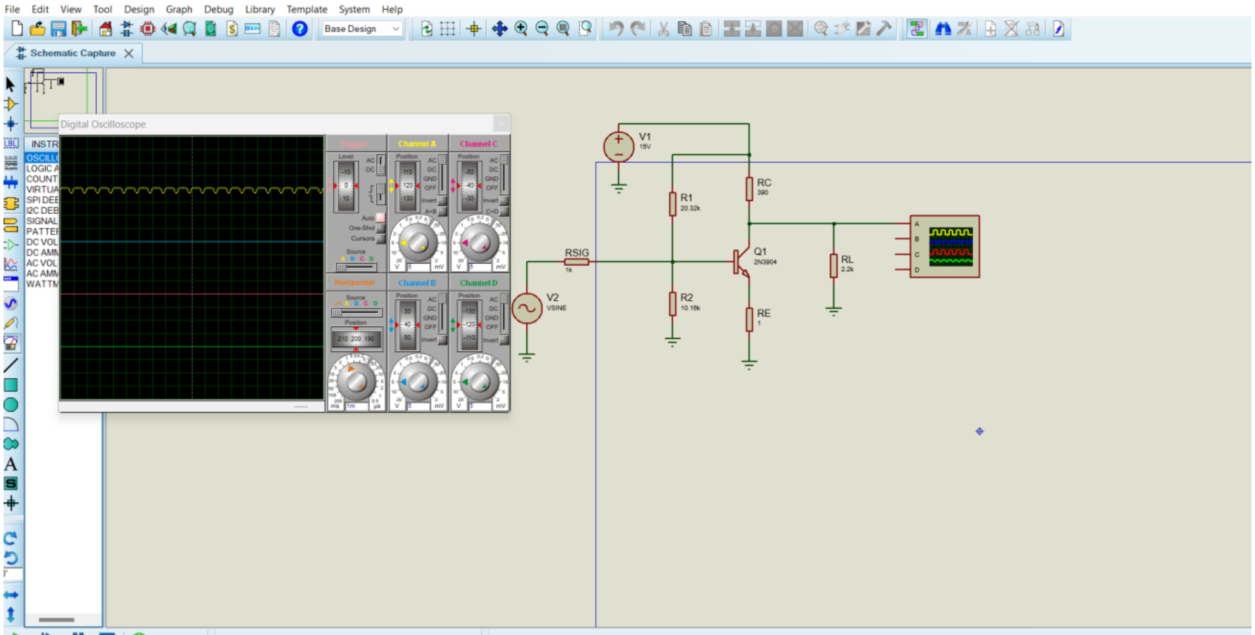




Rin = $\frac{Vin}{Vsig - Vin}$ x Rx

Rx is RSIG we take it 1kΩ

Rin = $\frac{300m}{306.2m - 300m}$ x 1k = 48.3k > 40kΩ



$$VL = \frac{RL}{Ro+RL} \times VOUT$$

$$Ro = \frac{Vout-VL}{VL} \times RL$$

$$= \frac{260.3m - 300m}{260.3m} \times 2.2k$$

$= 335.5\Omega$

Output Impedance

$Zout \approx RC \parallel RL < 500\Omega$