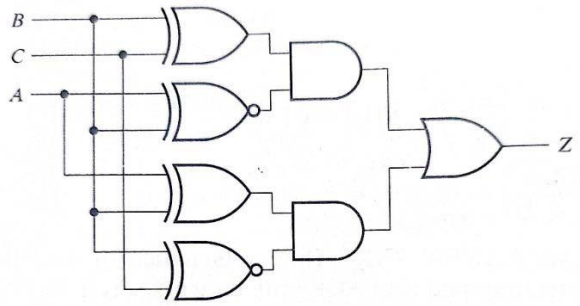
Q1:
Consider the following circuit



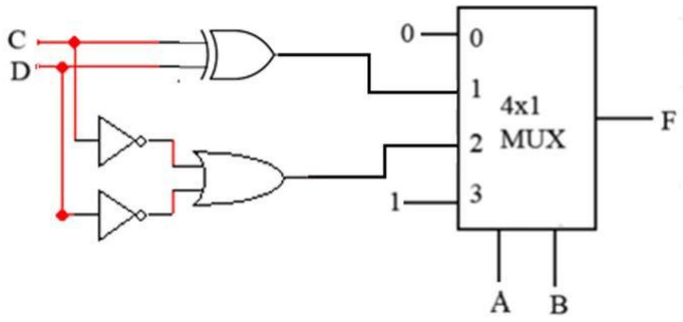
a) **Construct** the truth table for the function Z.
b) **Write** the function Z in canonical sum of product form (litle m notation).
c) **Simplify** the function to the minimum number of literals.

Q2:

a) **Design** a combinational multiplier that has two 2-bit inputs AA_1AA_0 and BB_1BB_0 and 4 bit output $FF_3FF_2FF_1FF_0$. **Construct** the truth table and implement it using 4 to 16 line decoder and gates of your choice.

b) **Construct** the Truth table and write F in ∑m notation.

Q3:



a) **Analyze** a sequential circuit with three D flip-flops (A, B, C) defined by the following next state equations

$$DD_{AA} = BB\overline{CC}$$
$$DD_{BB} = CC$$
$$DD_{CC} = \overline{BB} + XX$$

Where A, B and C are the outputs of the flip-flops A, B and C respectively, X is the external input and DD_{AA}, DD_{BB} and DD_{CC} are the input of flip-flops A, B and C respectively. Construct the state table and state diagram of this sequential circuit.

b) Consider a sequence recognizer circuit that has a serial input S and one output Z. The output becomes one when a sequence 1001 is detected and zero otherwise. **Generate** a state diagram only. Circuit implementation is not required.

Q4:

Design a synchronous binary arbitrary counter using T Flip-Flop to produce the sequence 1,4,7,3,1 and repeat.

a) **Construct** the state diagram and state table for the required circuit.

b) **Construct** the logic diagram of your design using T- flip flops and logic gates.

c) Include the unused states in the state diagram and explain if this counter has self correction capability.