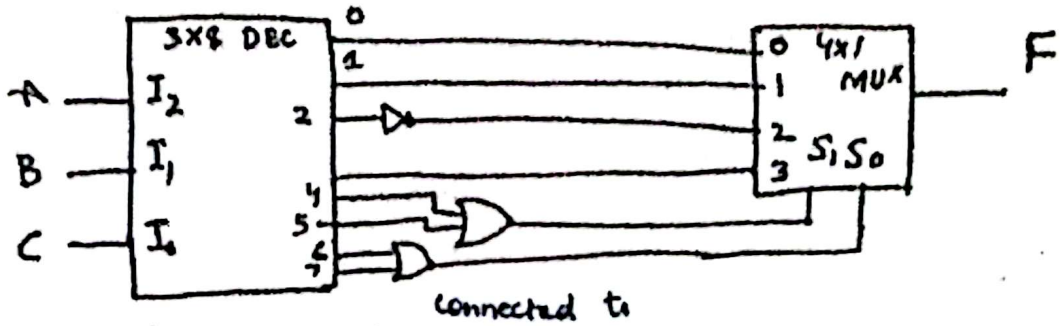
Q.1 Construct Truth Table F(A,B,C)



MUX Inputs:

	connected to
I_0	D0
I_1	D1
I_2	NOT(D2)
I_3	D3

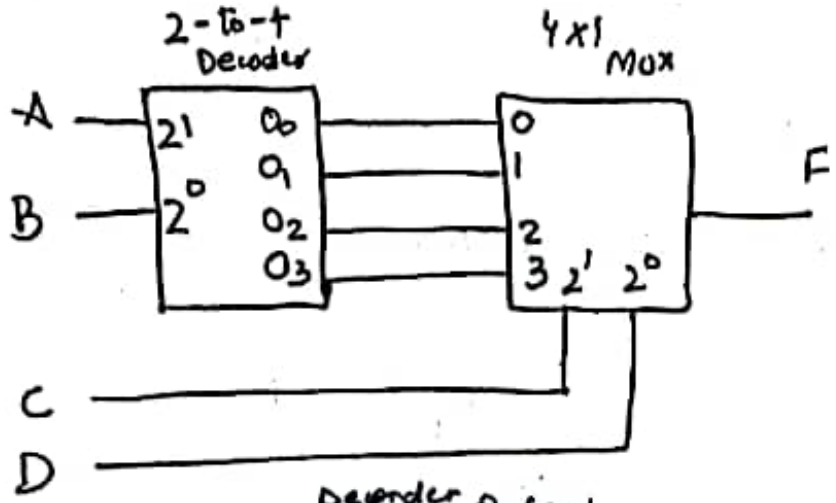
A	B	C	Decoder Output	S_1	S_0	MUX Select	MUX inputs used	F
0	0	0	$D_0 = 1$	0	0	00	D0 = 1	1
0	0	1	$D_1 = 1$	0	0	00	D0 = 0	0
0	1	0	$D_2 = 1$	0	0	00	D0 = 0	0
0	1	1	$D_3 = 1$	0	0	00	D0 = 0	0
1	0	0	$D_4 = 1$	1	0	10	NOT(D2) = 1	1
1	0	1	$D_5 = 1$	1	0	10	NOT(D2) = 1	1
1	1	0	$D_6 = 1$	0	1	01	D1 = 0	0
1	1	1	$D_7 = 1$	0	1	01	D1 = 0	0

As ABC = 101 → $D_5 = 1$ ⇒ $S_1 = D_4 + D_5 = 1$, $S_0 = 0$

→ MUX select 10 → I_2 = NOT(D_2) = NOT(0) = 1

F = 1

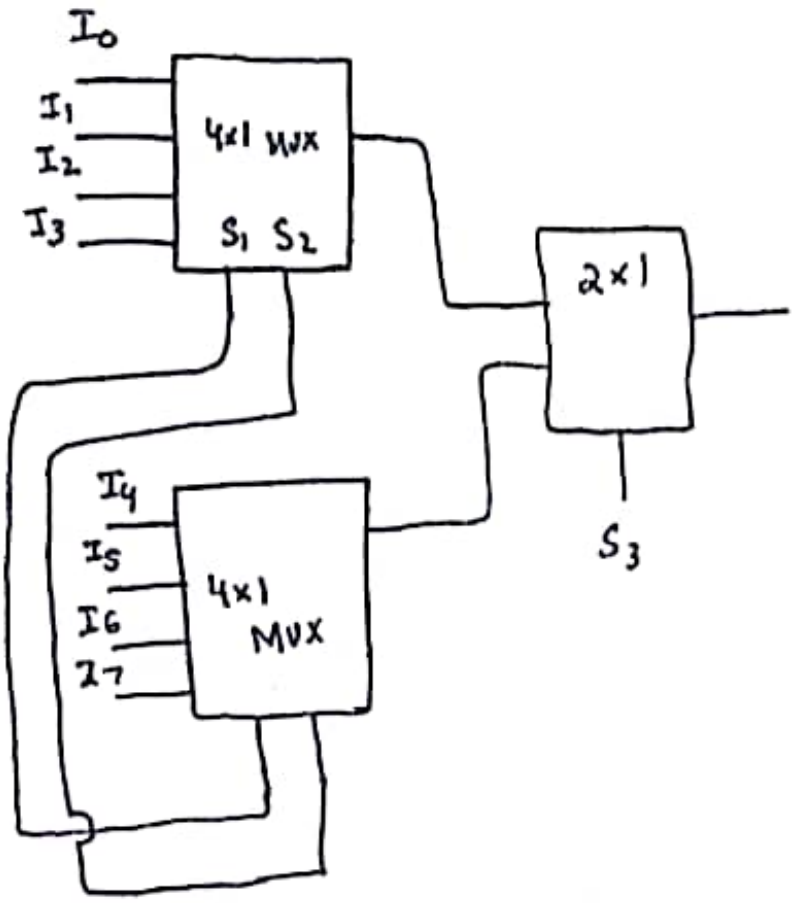
Q2 Construct Truth Table F(A, B, C, D)



Decoder Outputs | mux selection

A	B	C	D	O_0	O_1	O_2	O_3	C	D	F
0	0	0	0	1	0	0	0	0	0	1
0	0	0	1	1	0	0	0	0	1	0
0	0	1	0	1	0	0	0	1	0	0
0	0	1	1	1	0	0	0	1	1	0
0	1	0	0	0	1	0	0	0	0	0
0	1	0	1	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0	1	0	0
0	1	1	1	0	1	0	0	1	1	0
1	0	0	0	0	0	1	0	0	0	0
1	0	0	1	0	0	1	0	0	1	0
1	0	1	0	0	0	1	0	1	0	1
1	0	1	1	0	0	1	0	1	1	0
1	1	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	1	0	1	0
1	1	1	0	0	0	0	1	1	0	0
1	1	1	1	0	0	0	1	1	1	1

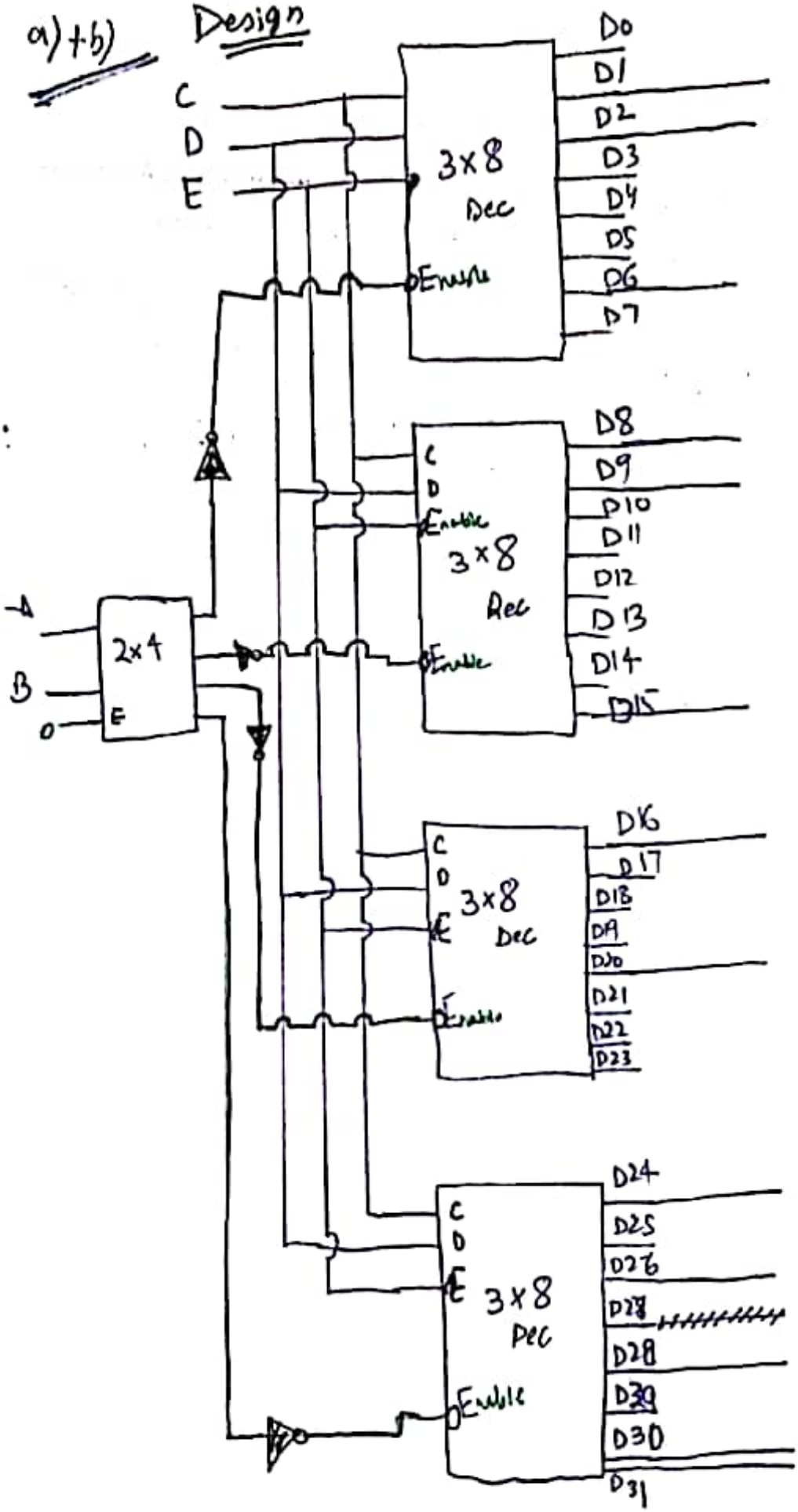
Q7 Design a 16x1 MUX with active low enable using dual 4x1 MUX's with active low enables & 2x1 MUX with low enable. Use minimum extra logic to design the required MUX.



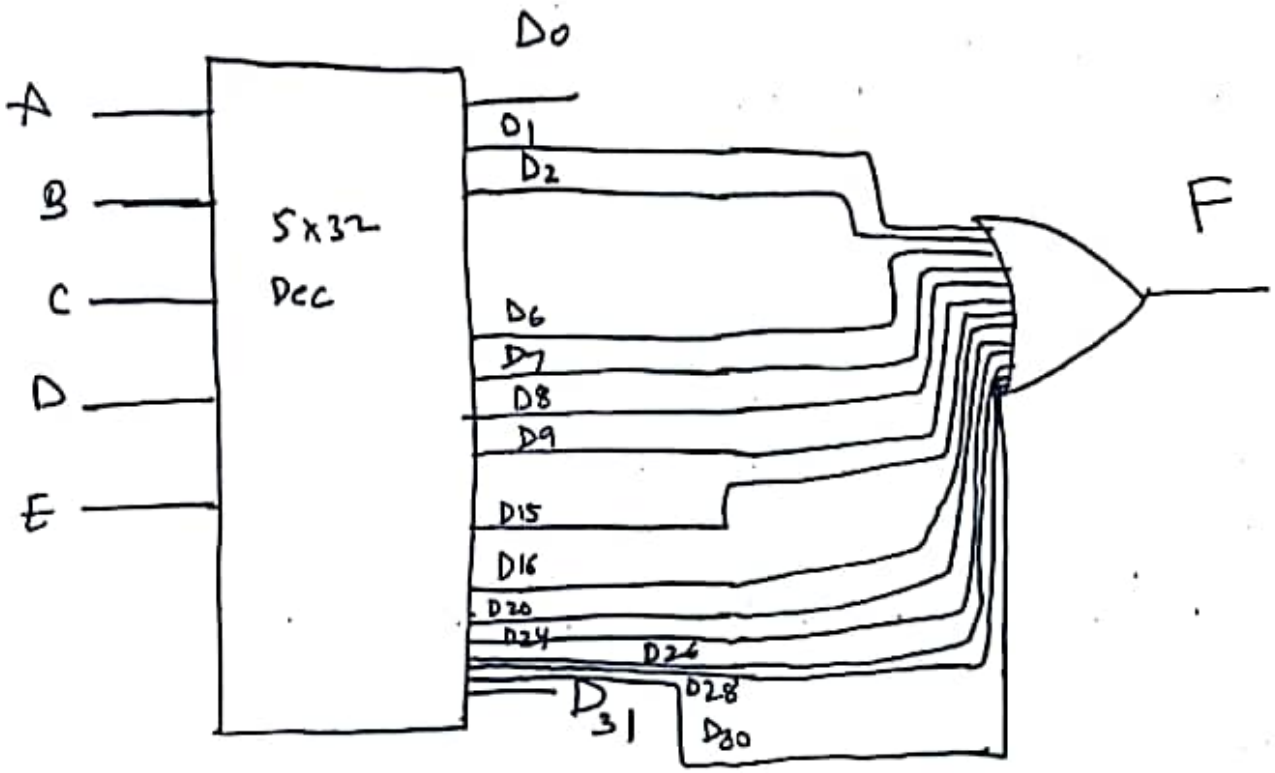
S_1	S_2	S_3	F
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

a) + b)

Design


C
D
E
3x8
Dec
Enable
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
A
B
0
2x4
E

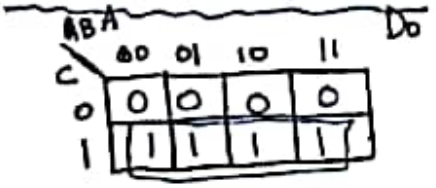
(c) 5x32


A
B
C
D
E
5x32
Dec
D0
D1
D2
D6
D7
D8
D9
D15
D16
D20
D24
D26
D28
D31
D30
F

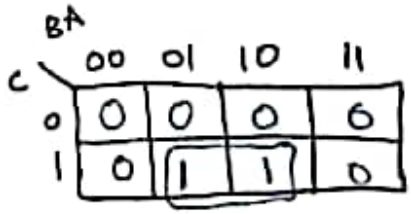
Q5 Design a circuit using 4x1 MUX, that accepts 3-bit input & generates a 6-bit binary number as output that is equal to Square of input number. Use minimum or .... 4x1 mux

X	A	B	C	X^2	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	1
2	0	1	0	4	0	0	0	1	0	0
3	0	1	1	9	0	0	1	0	0	1
4	1	0	0	16	0	1	0	0	0	0
5	1	0	1	25	0	1	1	0	0	1
6	1	1	0	36	1	0	0	1	0	0
7	1	1	1	49	1	1	0	0	0	1

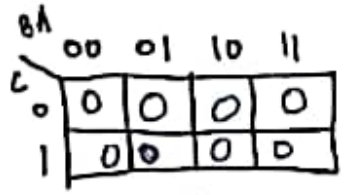
A and B are selections:



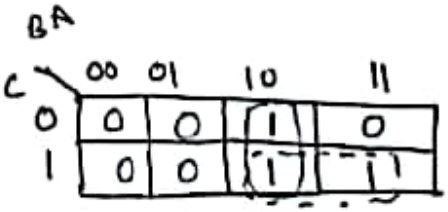
$D_0 = C$



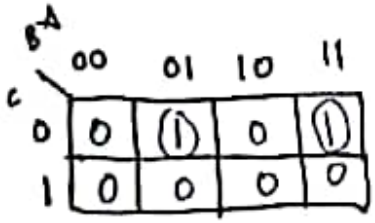
$D_3 = C$



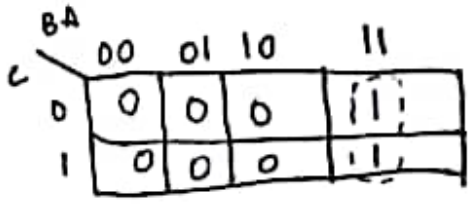
$D_1 = 0$



$D_4 = \bar{A}B$
$= B\bar{A}$



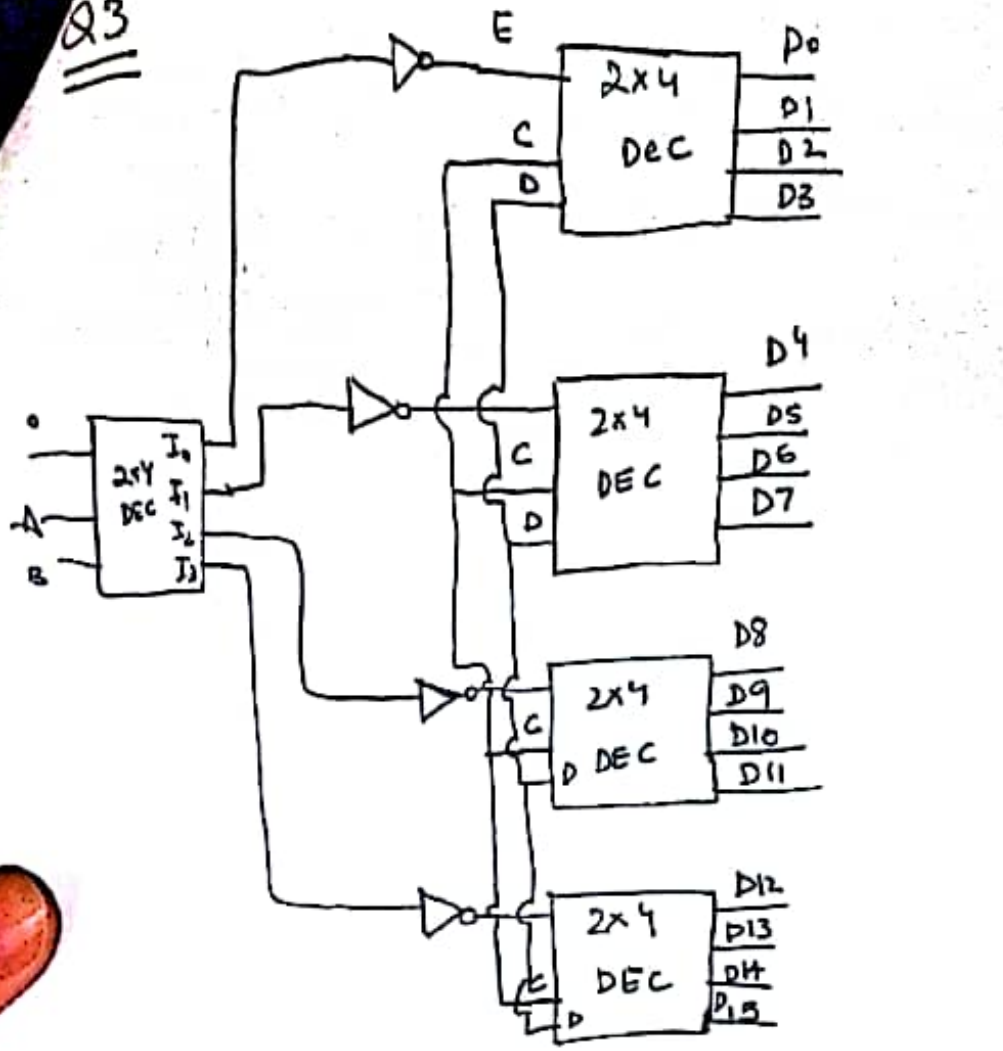
$D_2 = \bar{B}A + B\bar{A}$



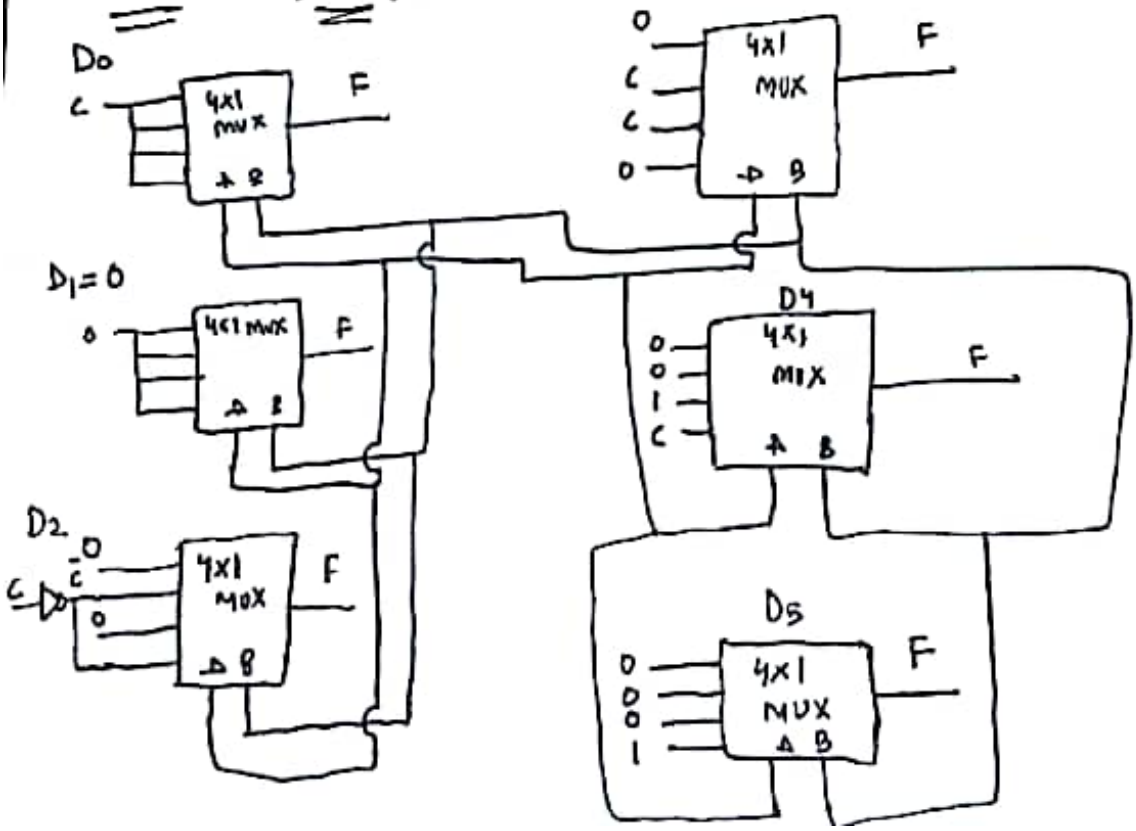
$D_5 = BA$

{⇒ Note : Circuit on end page}

Q3


E
2x4 DEC
C
D
D0
D1
D2
D3
D4
2x4 DEC
D5
D6
D7
D8
2x4 DEC
D9
D10
D11
D12
2x4 DEC
D13
D14
D15
2x4 DEC
A
B
D3

Q5 Design


D0
4x1 MUX
F
D1 = 0
D2
D4
D5
4x1 MUX

Q4 Construct 4-to-1 line MUX fixing input output variable A & D selection

$$F(A,B,C,D) = \sum m(2,4,6,9,10,11,15)$$

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

A & D	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0

$$I_0 = \bar{B}C + B\bar{C} + BC$$

A	D	B	C	F
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

$$I_1 = 0$$

A	D	B	C	F
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0

$$I_2 = \bar{B}C$$

A	D	B	C	F
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

$$I_3 = \bar{B}\bar{C} + \bar{B}C + BC$$

$$= \bar{B} + BC$$

$$= \bar{B}(1+C) + C$$

$$= \bar{B} + \bar{B}C + C$$

$$= \bar{B} + C(\bar{B}+1)$$

$$I_3 = \bar{B} + C$$

$$I_0 = \bar{B}C + B\bar{C} + BC$$

$$= \bar{B}C + B(\bar{C}+C)$$

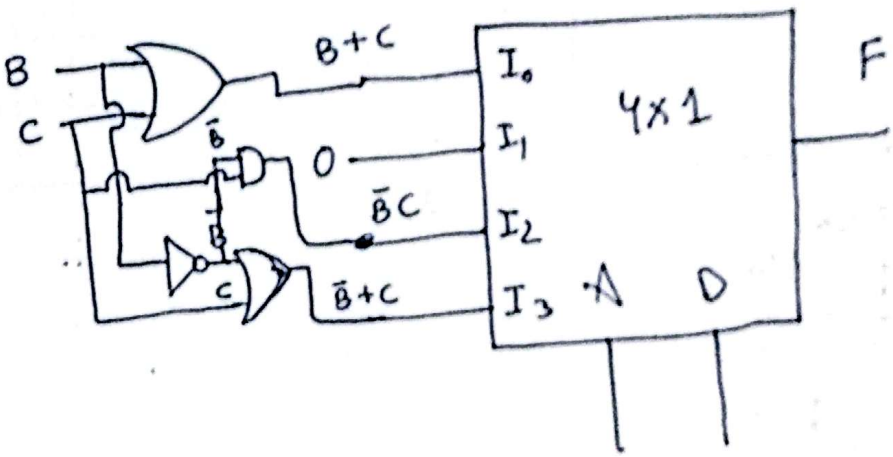
$$= \bar{B}C + B$$

$$= \bar{B}C + B(1+C)$$

$$= \bar{B}C + B + BC$$

$$= C(\bar{B}+B) + B$$

$$= C + B$$



Q8 Design logic circuit that performs the following operations on A(3-bit number) according to Status of selection bit S.

S	operation	F(output)
0	Increment	A+1
1	Tripler	3*A

S	A_0	A_1	A_2	D_0	D_1	D_2	D_3	D_4	D_5
0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	1	1	0	0	0	1	0	0
0	1	0	0	0	0	0	1	0	1
0	1	0	1	0	0	0	1	1	0
0	1	1	0	0	0	0	1	1	1
0	1	1	1	0	1	0	0	0	0
1	0	0	0	0	1	1	0	0	0
1	0	0	1	0	1	1	0	1	1
1	0	1	0	0	1	1	1	1	0
1	0	1	1	1	0	0	0	0	1
1	1	0	0	1	0	0	1	0	0
1	1	0	1	1	0	0	1	1	1
1	1	1	0	1	0	1	0	1	0
1	1	1	1	1	0	1	1	0	1

For D0:

00: 0

01: 0

10: $A_1 A_2$

11: $\bar{A}_1 \bar{A}_2 + \bar{A}_1 A_2 + A_1 \bar{A}_2 + A_1 A_2$

$\bar{A}_1 + A_1 = 1$

For D1:

00: 0

01: $A_1 A_2$

10: $\bar{A}_1 \bar{A}_2 + \bar{A}_1 A_2 + A_1 \bar{A}_2$

$\bar{A}_1 + A_1 \bar{A}_2$

$\bar{A}_1 + \bar{A}_1 \bar{A}_2 + A_1 \bar{A}_2$

$\bar{A}_1 + \bar{A}_2$

11: 0

For D2:

00: 0

01: 0

10: $\bar{A}_1 \bar{A}_2 + \bar{A}_1 A + A_1 \bar{A}_2$

$\bar{A}_1 + \bar{A}_2$

11: $A_1 \bar{A}_2 + A_1 A_2 = A_1$

For D3:

00: $A_1 A_2$

01: $\bar{A}_1 + \bar{A}_2$

10: $A_1 \bar{A}_2$

11: $\bar{A}_1 \bar{A}_2 + \bar{A}_1 A_2 + A_1 A_2$

$\bar{A}_1 + A_1 A_2$

$\bar{A}_1 + \bar{A}_1 A_2 + A_1 A_2$

$\bar{A}_1 + A_2$

For D4:

00: $\bar{A}_1 A_2 + A_1 \bar{A}_2$

01: $\bar{A}_1 A_2 + A_1 \bar{A}_2$

10: $\bar{A}_1 A_2 + A_1 \bar{A}_2$

11: $\bar{A}_1 A_2 + A_1 \bar{A}_2$

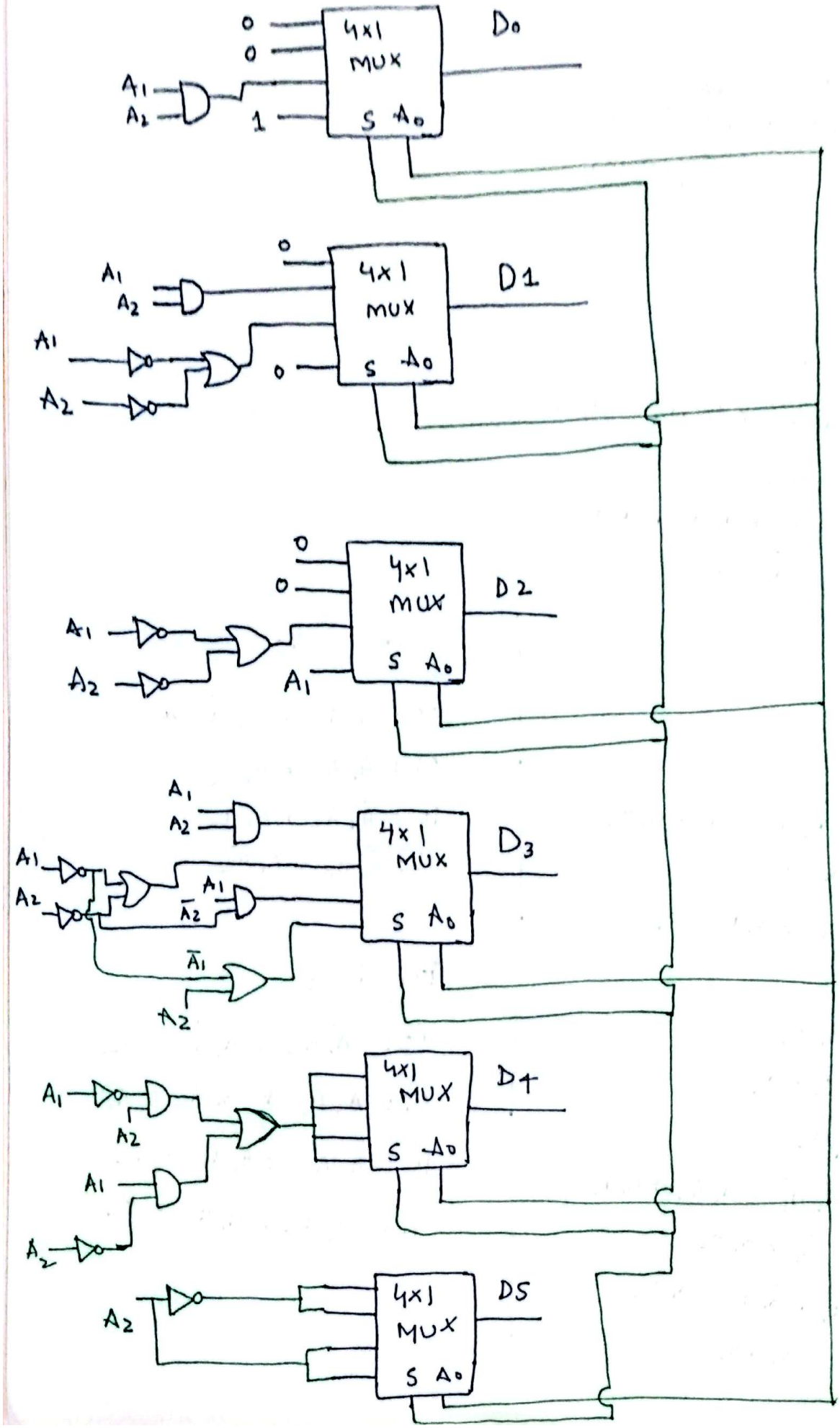
For D5:

00: $\bar{A}_1 \bar{A}_2 + A_1 \bar{A}_2 = \bar{A}_2$

01: $\bar{A}_1 \bar{A}_2 + A_1 \bar{A}_2 = \bar{A}_2$

10: $\bar{A}_1 A_2 + A_1 A_2 = A_2$

11: $\bar{A}_1 A_2 + A_1 A_2 = A_2$


0
0
A1
A2
1
4x1
MUX
S A0
D0
A1
A2
0
A1
A2
0
4x1
MUX
S A0
D1
0
0
A1
A2
A1
4x1
MUX
S A0
D2
A1
A2
A1
A2
A1
A2
4x1
MUX
S A0
D3
A1
A2
A1
A2
A2
A1
A2
4x1
MUX
S A0
D4
A2
4x1
MUX
S A0
D5