National University of Computer and Emerging Sciences 0086

Lahore Campus

# Digital Logic Design (EE1005)

## Final Exam

**Total Time (Hrs):** 3
**Total Marks:** 120
**Total Questions:** 6

Date: 27th May, 2025

**Course Instructor(s)**

Ms. Tamania Javaid

Mr. Ahmad Hamza

Roll No _____ Section _____ Student Signature _____

- **Attempt all the questions.**
- **Show complete working of each question.**
- **Multiple solutions of the same question will carry zero credit.**
- **State your valid assumptions clearly if you have to take any.**

***CLO #2: Apply Boolean Algebra and K-map methods to optimize logic circuits***

**Q1:** **[20 marks]**

a. **Use** K-Map method to minimize the following function in Sum of Product form

$F(W,X,Y,Z) = \Sigma m(0, 2, 4, 5, 8, 14, 15)$, $d(W,X,Y,Z) = \Sigma m(7, 10, 13)$

b. Implement two Input XNOR gate using two input NOR Gates only and **apply** gate reduction to reduce the circuit.

***CLO #3: Design combinational circuits using functional blocks***

**Q2:** **[20 marks]**

**Design** a combinational circuit with two data inputs A and B (each of two bits) i.e. A= A1 A0 and B=B1 B0 and two selection inputs, S1, S0.The system should implement the following functions based on selection inputs

| S1 | S0 | Operation |
|---|---|---|
| 0 | 0 | F=0 |
| 0 | 1 | $F = \begin{cases} 1, & if\ (A+B) < 2 \\ 0, & Otherwise \end{cases}$ |
| 1 | 0 | $F = \begin{cases} 1, & if\ total\ number\ of\ 1s\ in\ both\ A\ and\ B\ are\ odd \\ 0, & Otherwise \end{cases}$ |
| 1 | 1 | F=1 |

a. **Construct** the truth table of the functions and use decoders of appropriate size (if required) to implement the functions.
b. Then use a Multiplexer to generate the output. **Construct** a complete circuit diagram.

Use of at least two Decoders and one Multiplexer is mandatory in your design

Available resources are:

- Decoders and Multiplexers of all sizes
- Two, three and four input AND, OR, NAND and NOR gates
- 2 input XOR and XNOR gates
- NOT gates

***CLO #4: Analyze elements of sequential circuits***

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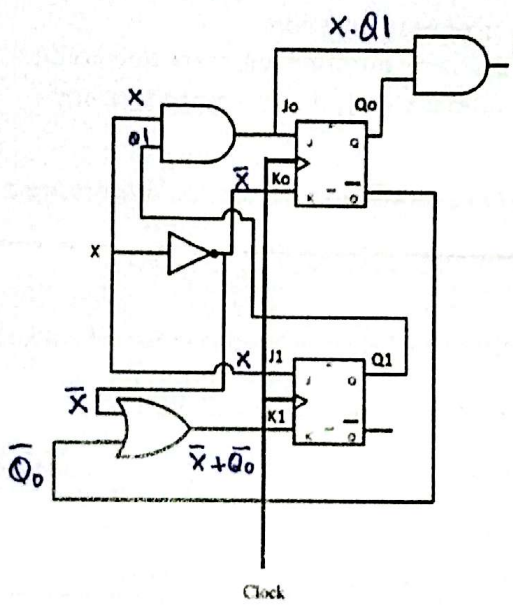
**Q3:** **[20 marks]**

**Analyze** the logic circuit given below




$Z = (X \cdot Q1 \cdot \bar{Q}o)$

$J_o = X \cdot Q1$

$K_o = \bar{X}$

$J_1 = X$

$K_1 = \bar{X} + \bar{Q}_o$

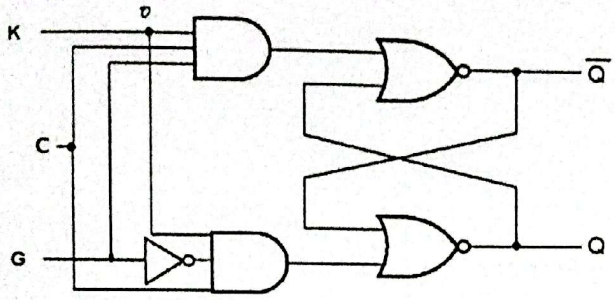
$\Rightarrow Q_o\bar{K} + \bar{Q}_oJ$

a. Find the Boolean expression for $J0, K0, J1, and\ K1$
b. Construct the state table and state diagram.
c. State if it is a Mealy or Moore Model circuit.

***CLO #4: Analyze elements of sequential circuits***

**Q4:** **[20 marks]**

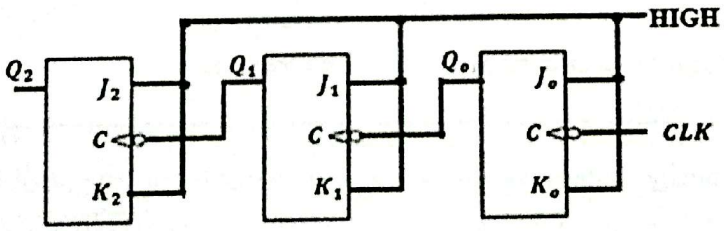
a. Circuit diagram of a new type of latch called KG latch is shown in the figure below.

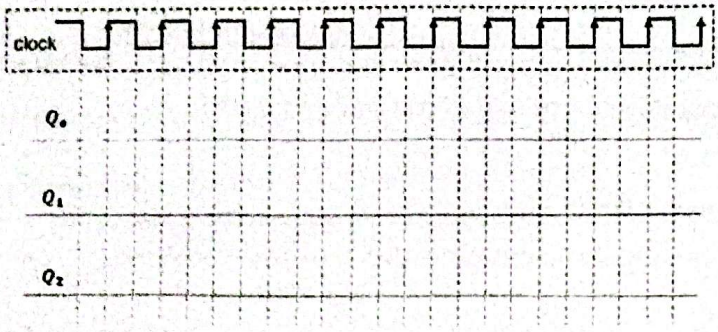



**Analyze** the circuit and fill-in the Next State Column of the function table of KG Latch. Identify if it is set, reset, hold or undefined (if applicable) state. Derive the expression $Q\ (t+1)$ as a function of $Q(t), K, and\ G$.

| Latch Inputs | | Next State |
|---|---|---|
| K | G | Q(t+1) |
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

**b.** **Analyze** the circuit to generate the timing diagram of the circuit. Assume all flip-flops have zero initial value. Show the contents of $Q_0, Q_1\ and\ Q_2$ for at least 6 clock cycles in the given timing diagram.

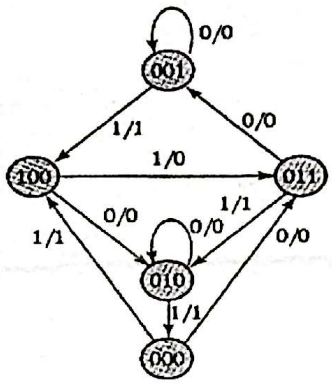





***CLO #5: Design of sequential circuits for various applications***

**Q5:** **[20 marks]**

**Design** a sequential circuit using D Flip flop that implements the following state diagram.




a. Construct the state table. Take unused states as don't care.
b. Find the expressions for flip-flop inputs and construct the logic circuit.
c. Construct the state diagram corresponding to your circuit including the unused states.

***CLO #5: Design of sequential circuits for various applications***

**Q6:** **[20 marks]**

**Design** a synchronous binary arbitrary counter with an input R that follows the sequence given below

i. $2 \longrightarrow 4 \longrightarrow 6 \longrightarrow 0 \longrightarrow 7$ and repeat when $R = 0$

ii. $0 \longrightarrow 2 \longrightarrow 6 \longrightarrow 4 \longrightarrow 7$ and repeat when $R = 1$

a) **Construct** the state diagram and state table.
b) **Construct** the logic diagram of your design using T- flip flops and logic gates of your choice.