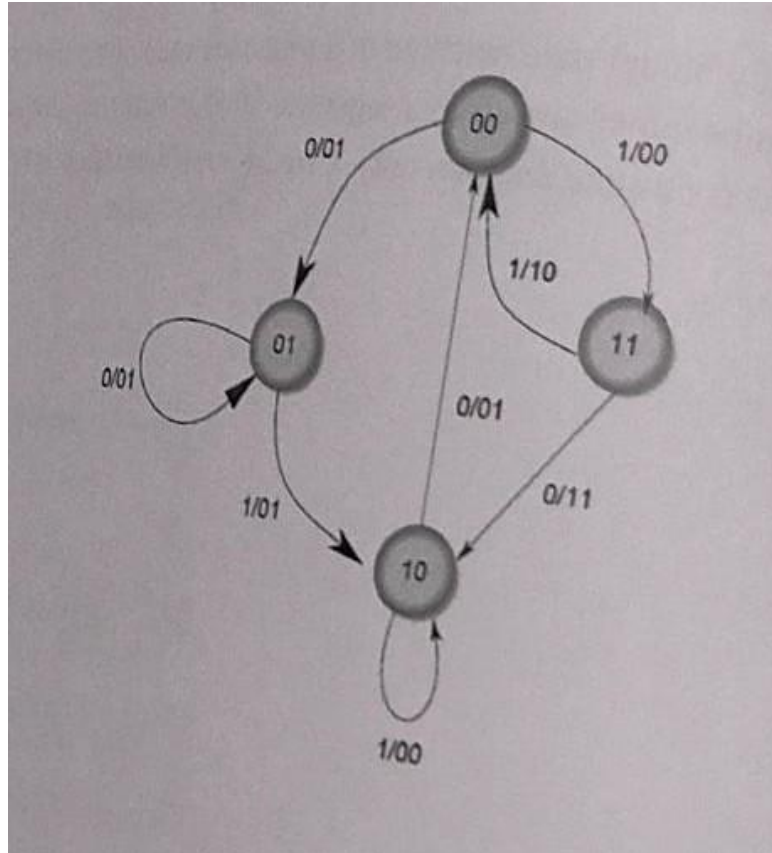**Q1:** Convert the following state diagram into state table and implement the circuit using JK Flip Flops

Q3: Tables in a restaurant are labeled A to D. Where customers are settled, they ring a bell placed on center of table to call waiter. Waiter gets to know when bulb indicating specific table gets **ON.** If more than two tables are ON simultaneously then priority is given in the following order to serve the customer.

Priority of table **D** > Priority of table **A** > Priority of table **C** > Priority of table **B**

You are required to design a circuit for the restaurant that helps them decide which customer to serve currently. The circuit must have three outputs **(E, F, G).** If the customer is not to be served then **E=0,** otherwise **E=1. F & G** indicates the table to be served.

Codes are:

Table	Code
A	00
B	01
C	10
D	11

a. Show Truth Table for outputs E, F, and G.
b. Find minimal SOP and POS expression for each output using **K-maps.**

Q4: Design a digital circuit to check whether the inequalities 3x+2>24 and 3x+6>37 are true or not. Here, x is unsigned 4-bit number.

a. Implement using 8×1 mux when x1, x2 and x4 are selection bits.
b. Implement using 4×1 mux when x1 and x3 are selection bits.

Q5: Design a MN flip flop with following characteristics:

If **MN 00**, the next state of the flip-flop is **0**.

If **MN 01**, the next state of the flip-flop is same as present state.

If **MN 10**, the next state of the flip-flop is the complement of the present state.

If **MN 11**, the next state of the flip-flop is **1**.

a. Write State Table
b. Compute following excitation table for MN flip flop (use don't cares where necessary)

Present State Q(t)	Next State Q(t+1)	M	N
0	0		
0	1		
1	0		
1	1		

c. Derive the characteristic equation/ next State equation
d. Draw state diagram
e. Draw circuit diagram using JK-flip-flop and logic gates.

Q6: Design the following circuit that performs the following operations on A (3-bit number) according to the status of selection bit S:

S	Operation	F (Output)
0	Incrementor	A+1
1	Tripler	3*A