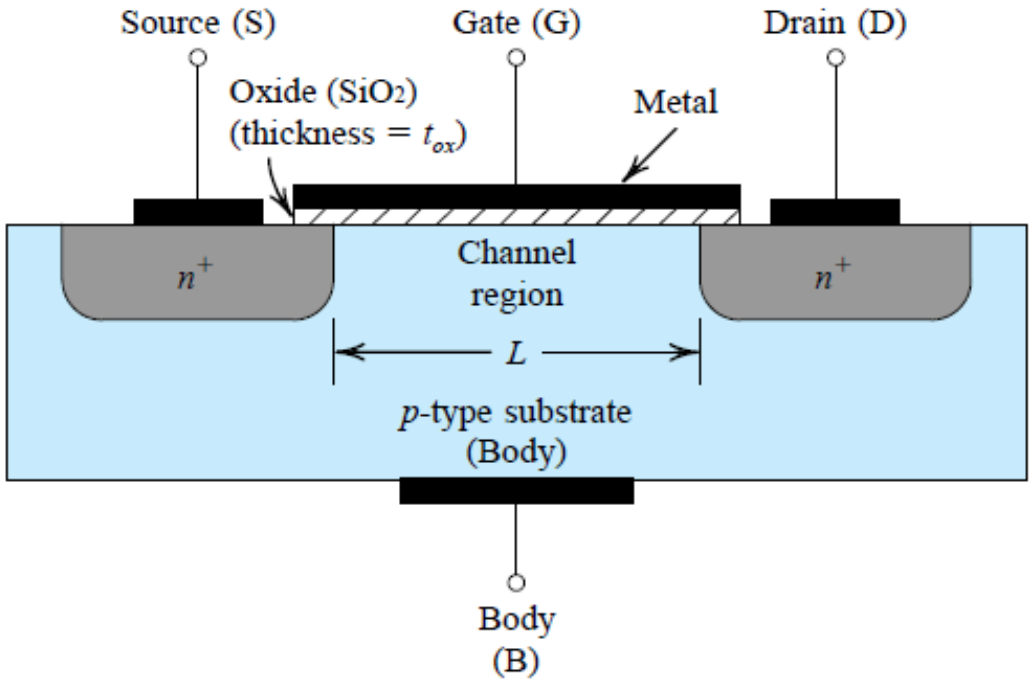
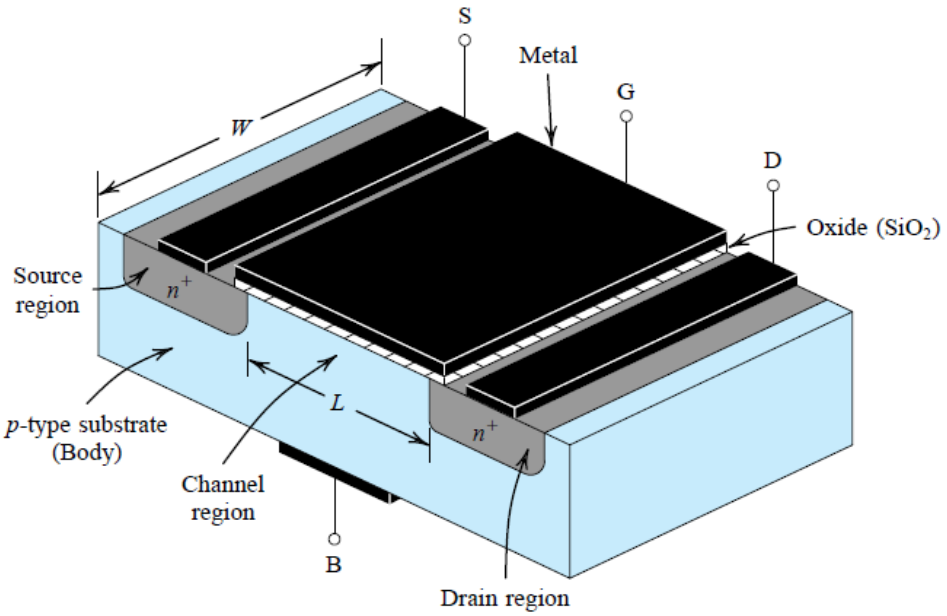
Electronic Devices and Circuits

Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

- Three terminal device
- Source, Drain, Gate
- Basic Operation:
- Voltage between two terminals controls the flow of current in the third terminal
- Applications:
- Amplification, Digital Logic, Memory
- Smaller in size
- Easy to manufacture
- Less power consumption
- MOSFET technology allows the placement of billions of transistor on a single IC
- As compared to BJT, it is more widely used in electronic circuits
- We will study enhancement type MOSFET
- Two types
- N-channel or NMOS
- P-channel or PMOS

N-Channel Enhancement MOSFET Physical Structure




S
Metal
G
D
W
Oxide (SiO_2)
Source region
n^+
p-type substrate (Body)
L
n^+
Channel region
B
Drain region

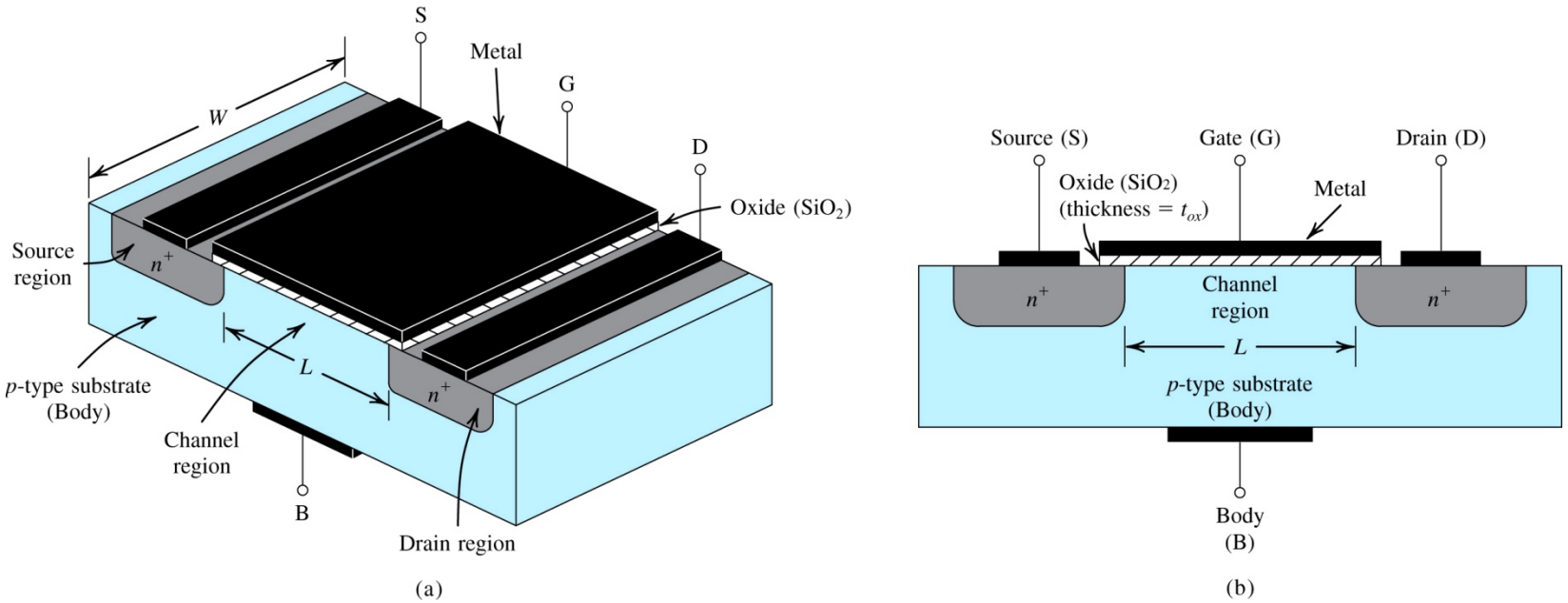
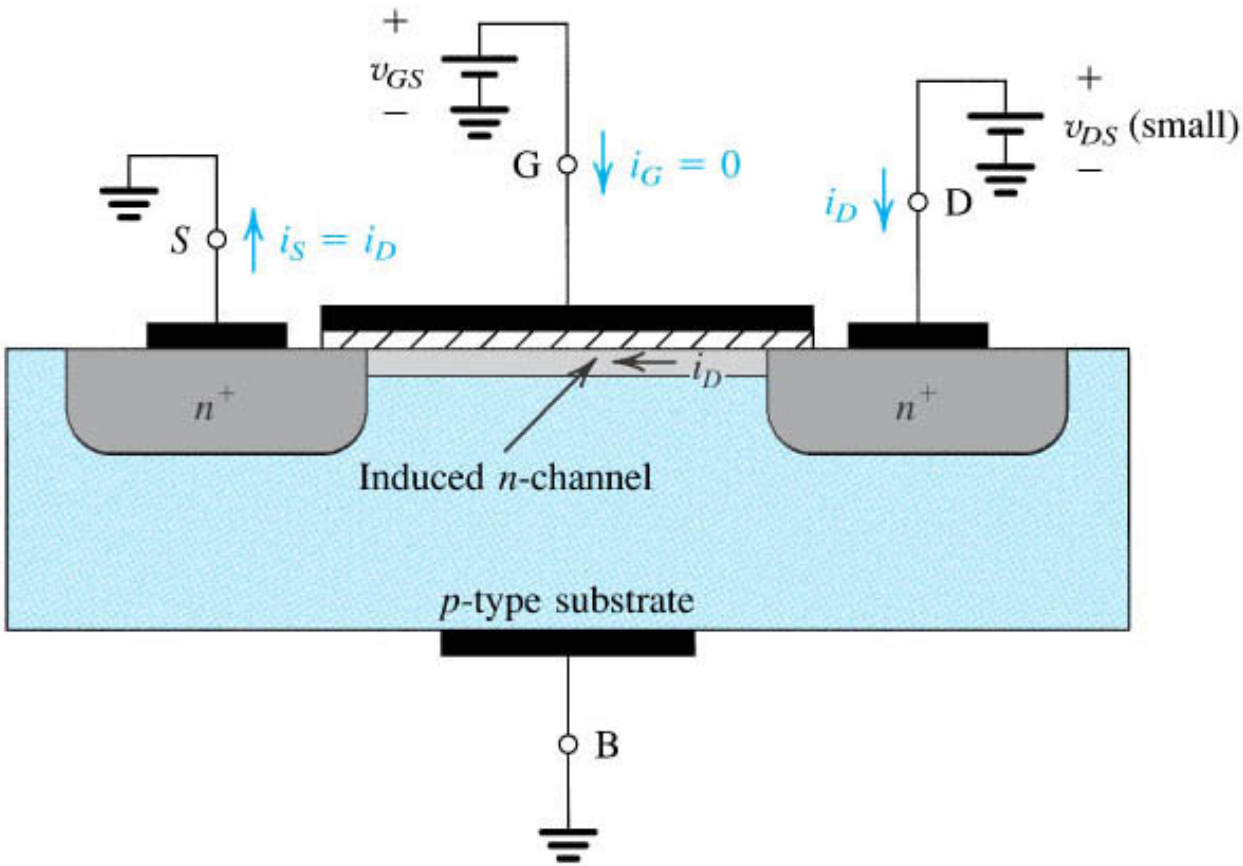
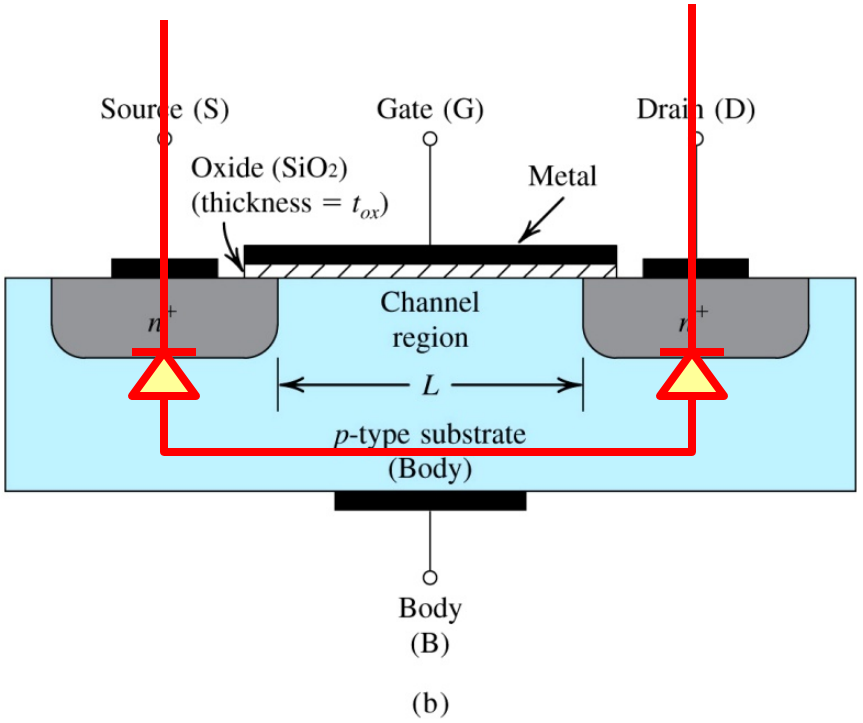


Figure 5.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically L = 0.03 μm to 1 μm, W = 0.1 μm to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm.


+
v_{GS}
−
G
$i_G = 0$
+
v_{DS} (small)
−
i_D
D
S
$i_S = i_D$
i_D
n^+
n^+
Induced n-channel
p-type substrate
B

Operation with Zero Gate Voltage

- With zero voltage applied to gate, two back-to-back diodes exist in series between drain and source.
- "They" prevent current conduction from drain to source when a voltage v_{DS} is applied.
  - yielding very high resistance (10^{12} *ohms*)



(b)

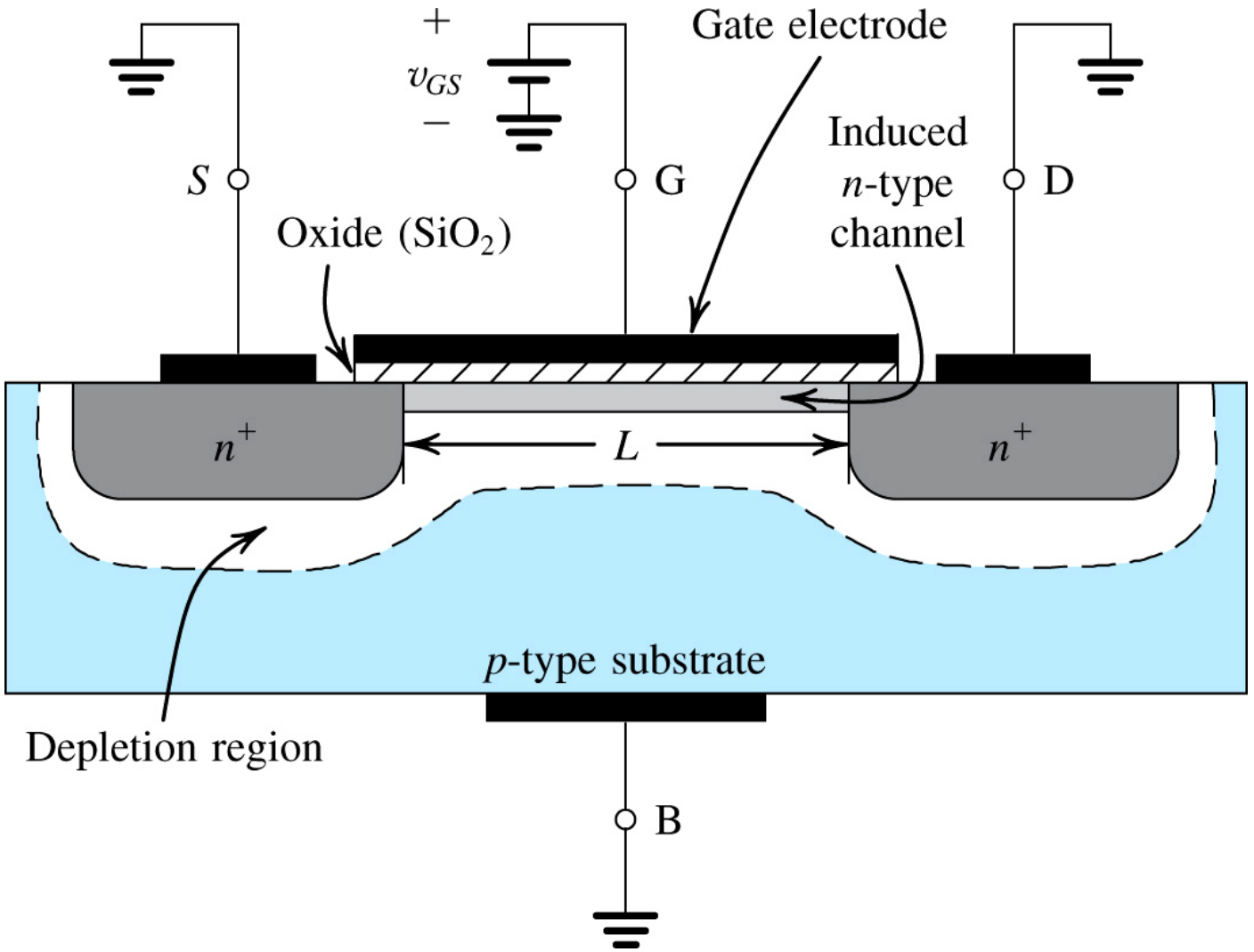


Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

Creating a Channel for Current Flow

- **Q:** What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate? Refer to figure to right.
  - **step #1:** v_{GS} is applied to the gate terminal, causing a positive build up of positive charge along metal electrode.
  - **step #2:** This "build up" causes free holes to be repelled from region of *p*-type substrate under gate.

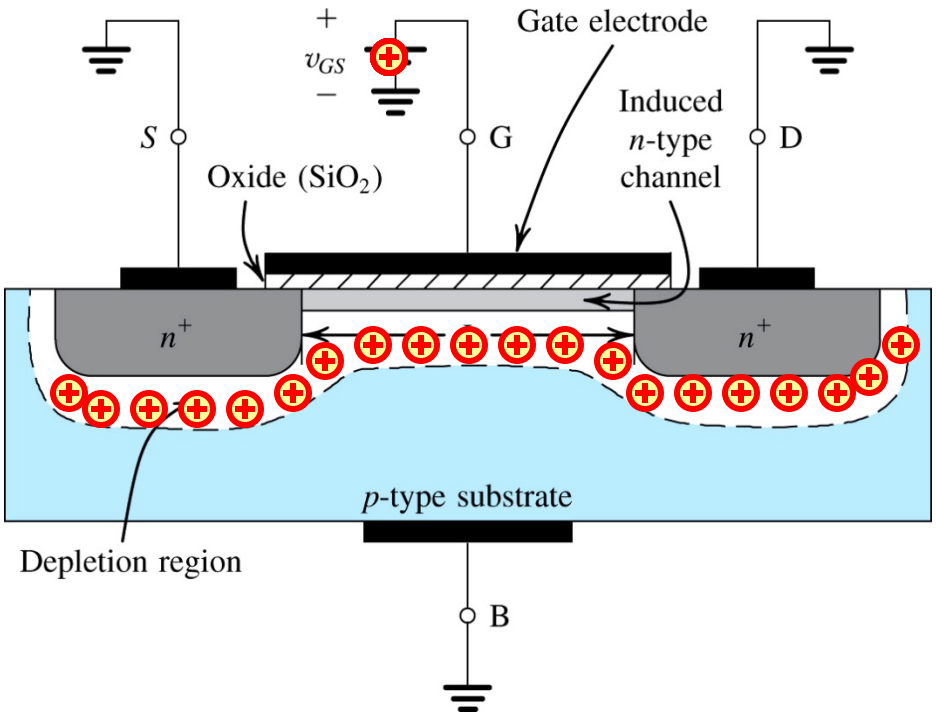


Figure : The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate

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Q: What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate? Refer to figure to right.

- **step #3:** This "migration" results in the uncovering of negative bound charges, originally neutralized by the free holes
- **step #4:** The positive gate voltage also attracts electrons from the n^+ source and drain regions into the channel.

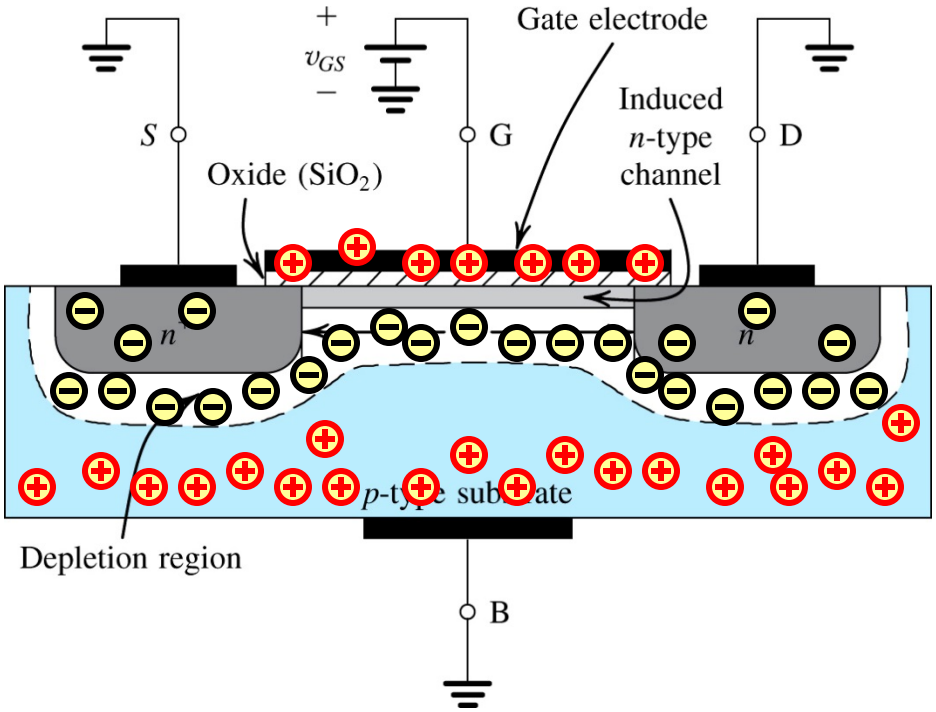

Figure : The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate

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Q: What happens if (1) source and drain are grounded a
is applied to gate? Refer to figure to right.

this induced channel is also known as an **inversion layer**

- **step #5:** Once a sufficient number of "these" electrons accumulate, an *n*-region is created…
  - …connecting the source and drain regions
- **step #6:** This provides path for current flow between *D* and *S*.

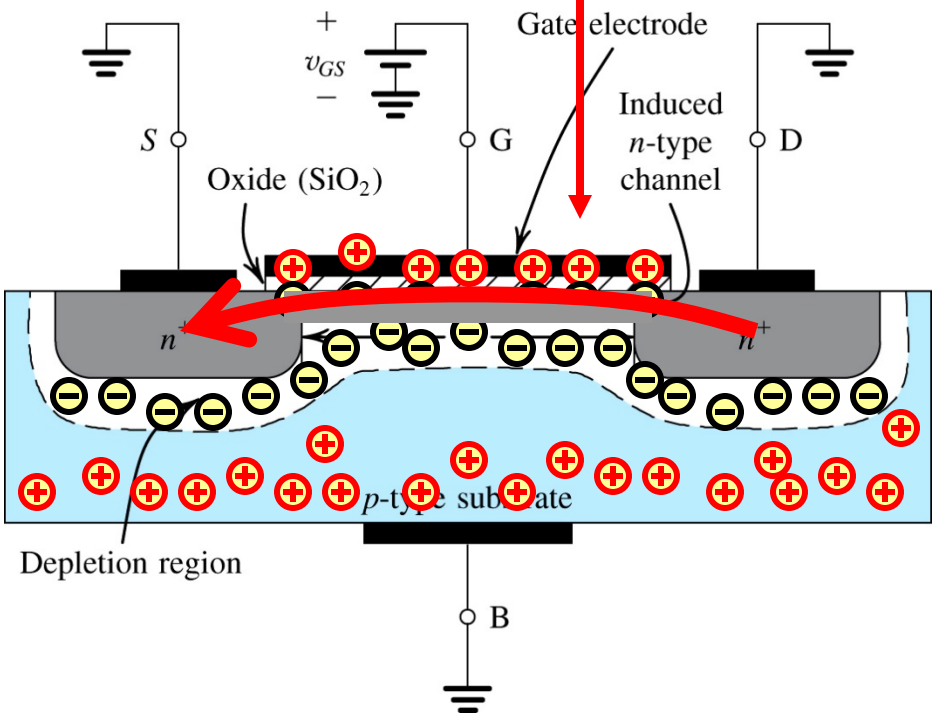

Figure: The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate

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Threshold Voltage

- Represented by V_t
- Data sheet parameter
- minimum value of v_{GS} required to form a conducting channel between drain and source
- V_{tn} is used for *n*-channel MOSFET, V_{tp} is used for *p*-channel

Overdrive Voltage (V_{ov})

- The excess of v_{GS} over V_t is called overdrive voltage
- $V_{ov} = V_{GS} - V_t$
- Also called effective voltage

Applying V_{DS} in the presence of V_{GS}

- If $V_{GS} < V_t$,
- No current would flow, cut off
- If $V_{GS} > V_t$
- V_{DS} is small, less than 50mV
- $V_{DS} > 50mV$ but less than V_{ov}
- $V_{DS} > V_{ov}$

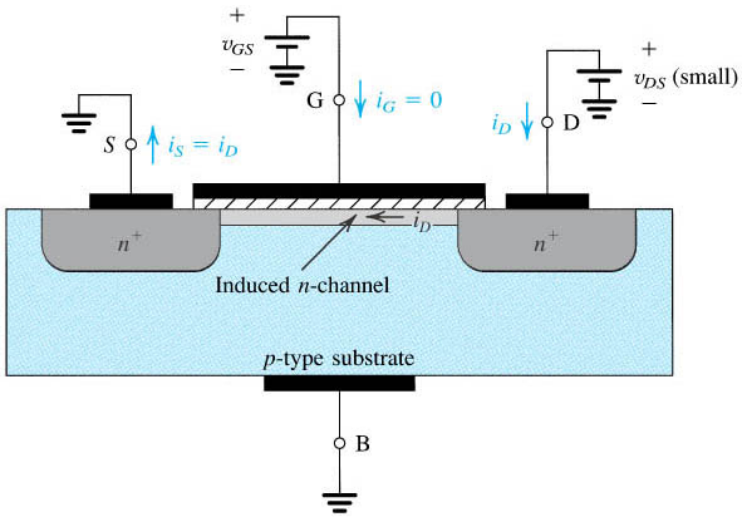
MOS Capacitance

- when positive v_{GS} is applied, an electric field develops between the gate electrode and induced *n*-channel – the conductivity of this channel is affected by the strength of field
  - SiO_2 layer acts as dielectric
- **oxide capacitance** (C_{ox}) – is the capacitance of the parallel plate capacitor per unit gate area (F/m^2)

ε_{ox} is permittivity of $SiO_2 = 3.45\mathbf{E}-11 (F/m)$

t_{ox} is thickness of SiO_2 layer

- $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \text{ in } F/m^2$$



Applying small V_{DS}

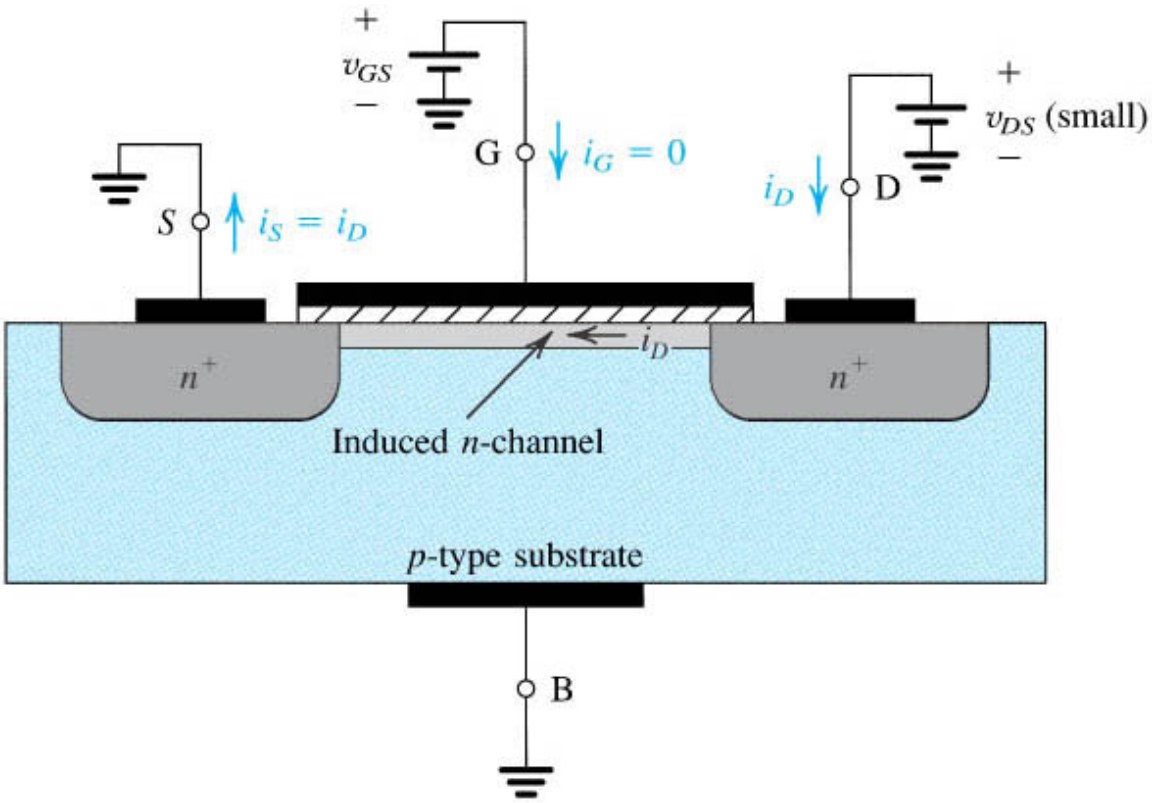


Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

Applying small V_{DS}

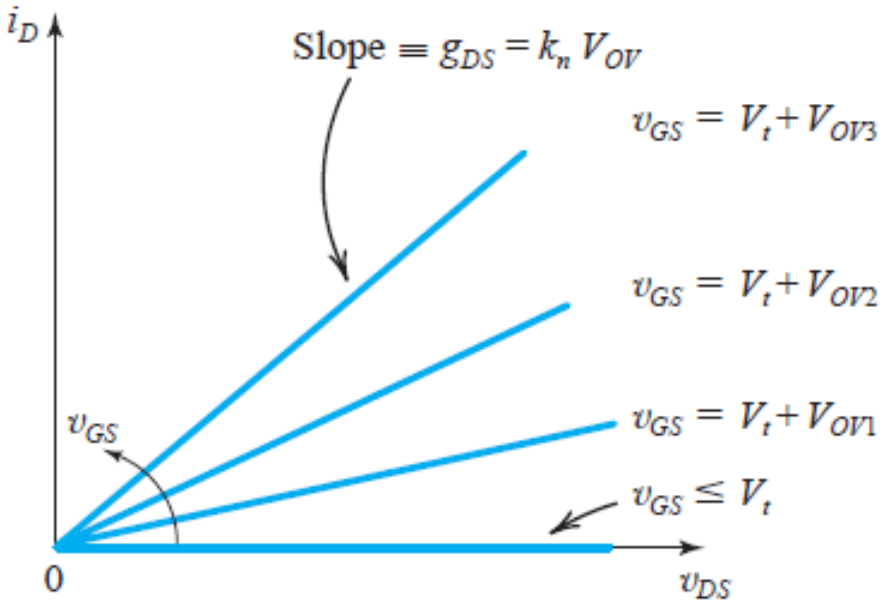
- Electrons are emitted from the source and move to drain.
- Direction of conventional current is from drain to source.
- Device acts like a linear resistor whose value is controlled by v_{GS}
- Linear relationship between current and voltage

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)v_{OV}\right]v_{DS}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}}$$

$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right)v_{OV}$$

$$r_{DS} = \frac{1}{g_{DS}}$$



Applying small V_{DS}

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)v_{OV}\right]v_{DS}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}}$$

$$r_{DS} = \frac{1}{g_{DS}}$$

$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right)v_{OV}$$

$$k_n' = \mu_n C_{ox}$$

$$k_n = k_n'(W/L)$$

$$k_n = (\mu_n C_{ox})(W/L)$$

- $\mu_n = mobility\ of\ electrons$
- $C_{ox} = oxide\ capacitance$
- $\frac{W}{L} = aspect\ ratio$
- $k_n' = process\ transconductance\ parameter$
- $k_n = MOSFET\ transconductance\ parameter$

Applying small v_{DS}

- r_{DS} is dependent on three factors
  - **process transconductance parameter for NMOS** ($\mu_n C_{ox}$) – which is determined by the manufacturing process
  - **aspect ratio** (W/L) – which is dependent on size requirements / allocations
  - **overdrive voltage** (v_{OV}) – which is applied by the user

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}}$$

k_n is known as **NMOS-FET transconductance parameter** and is defined as $\mu_n C_{ox} W/L$

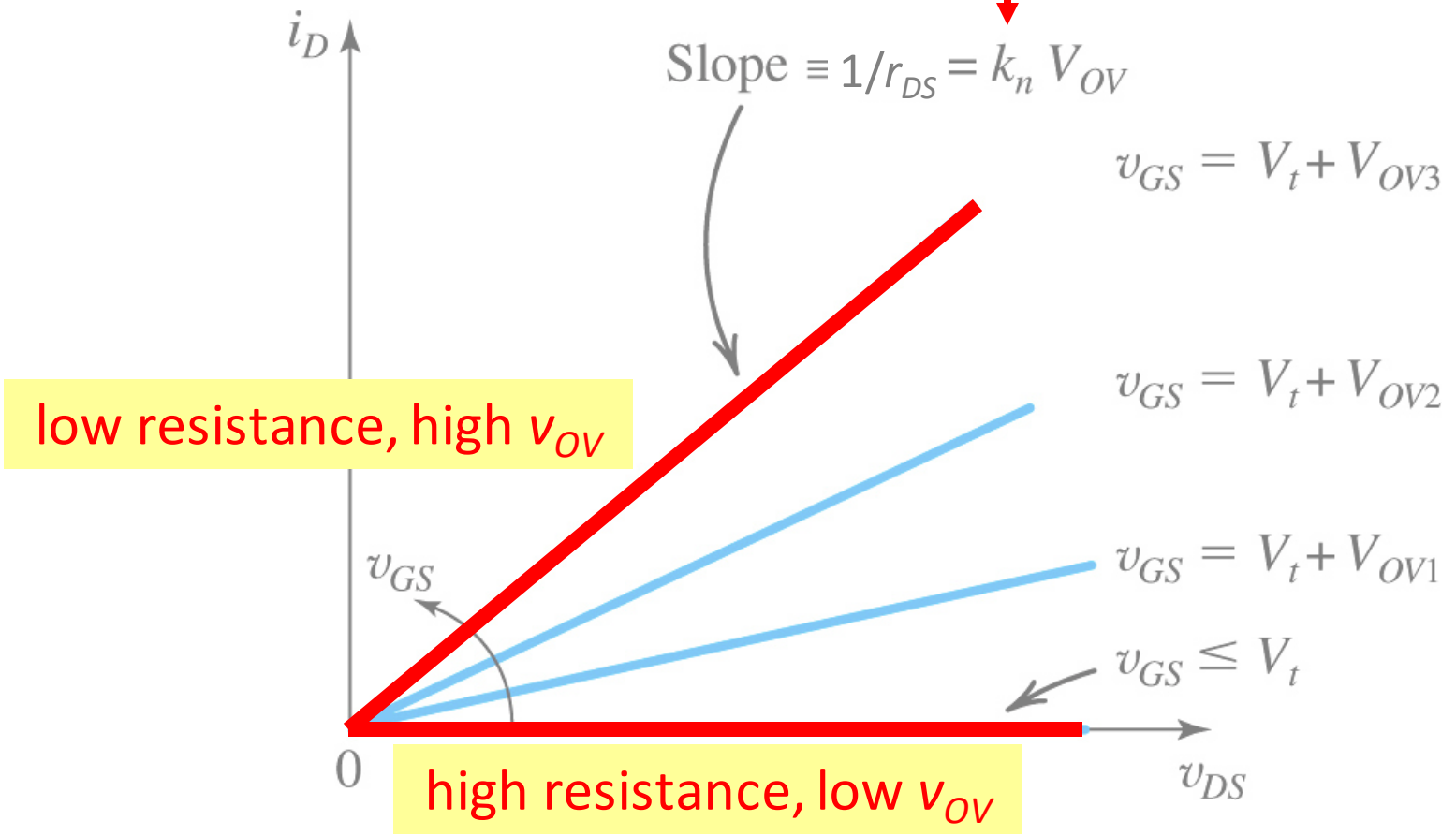
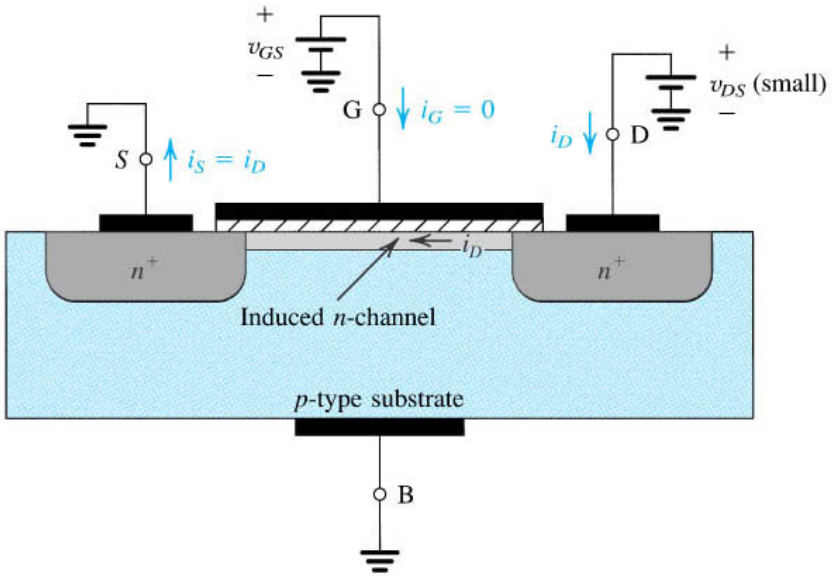


Figure : The i_D-v_{DS} characteristics of the MOSFET. when the voltage applied between drain and source V_{DS} is kept small.

The description above indicates that for the MOSFET to conduct, a channel has to be induced. Then, increasing v_{GS} above the threshold voltage V_t enhances the channel, hence the names **enhancement-mode operation** and **enhancement-type MOSFET**. Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$.

Effect of V_{ov} on channel

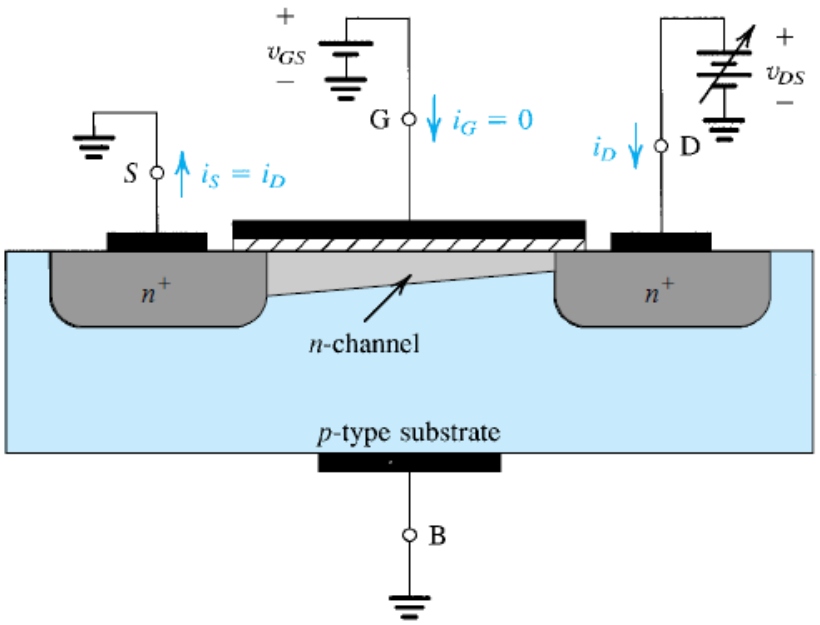
- As v_{OV} grows, so does the depth of the *n*-channel as well as its conductivity



Operation as v_{DS} is increased

$v_{DS} < V_{ov}$

- Current voltage relationship is no longer linear
- Triode region



$$i_D = k'_n\left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

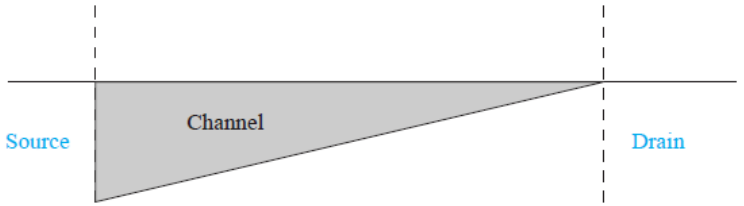
$$i_D = k'_n\left(\frac{W}{L}\right)\left(V_{OV}\ v_{DS} - \frac{1}{2}v_{DS}^2\right)$$

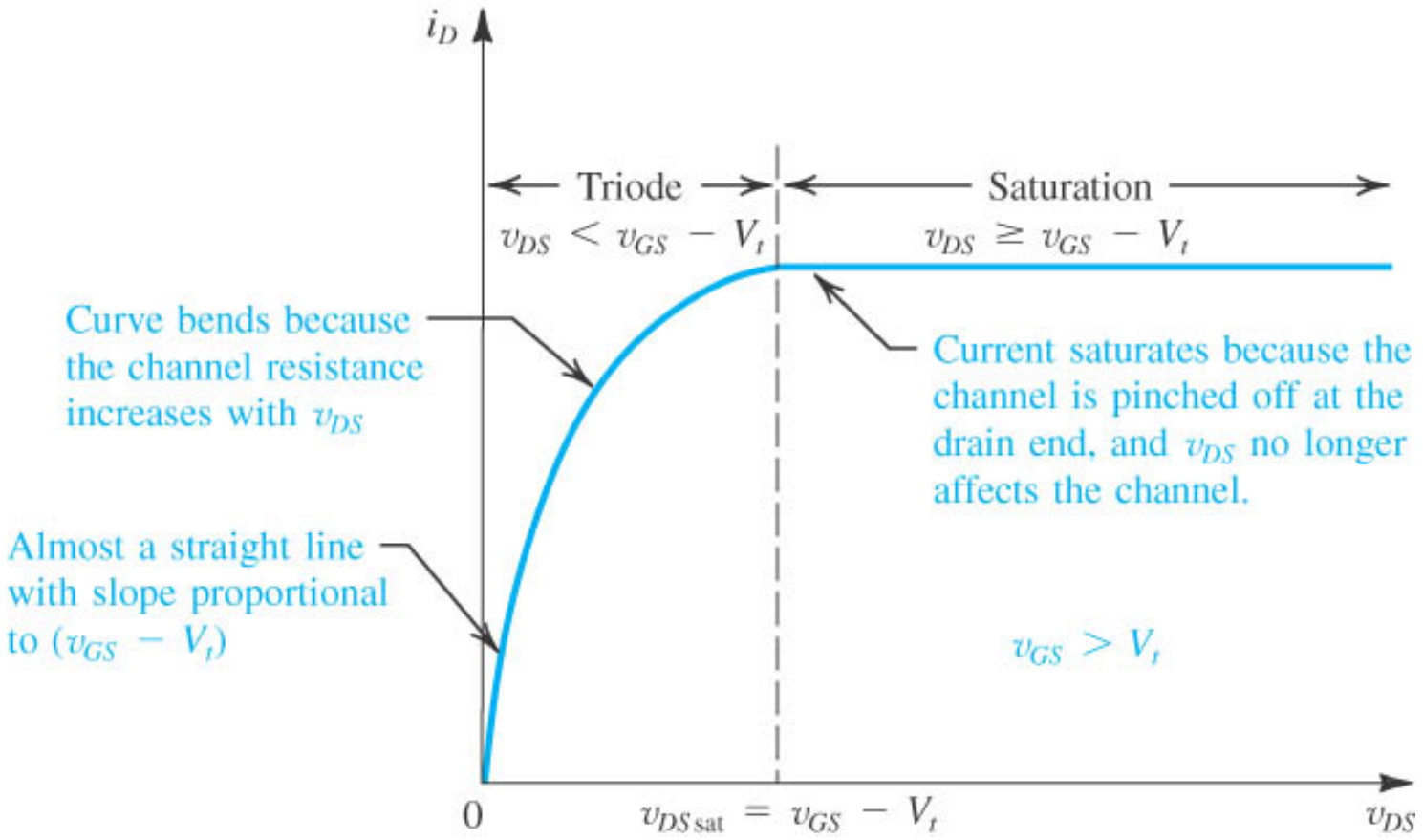
Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t; $v_{GS} = V_t + V_{OV}$.

Operation as $v_{DS} \geq V_{ov}$

- Current becomes constant
- Channel pinch off occurs
- MOSFET enters the saturation region
- Used as a voltage controlled current source.
- MOS is used as an amplifier
- Drain current is dependent on VGS and independent of VDS

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)V_{OV}^2$$

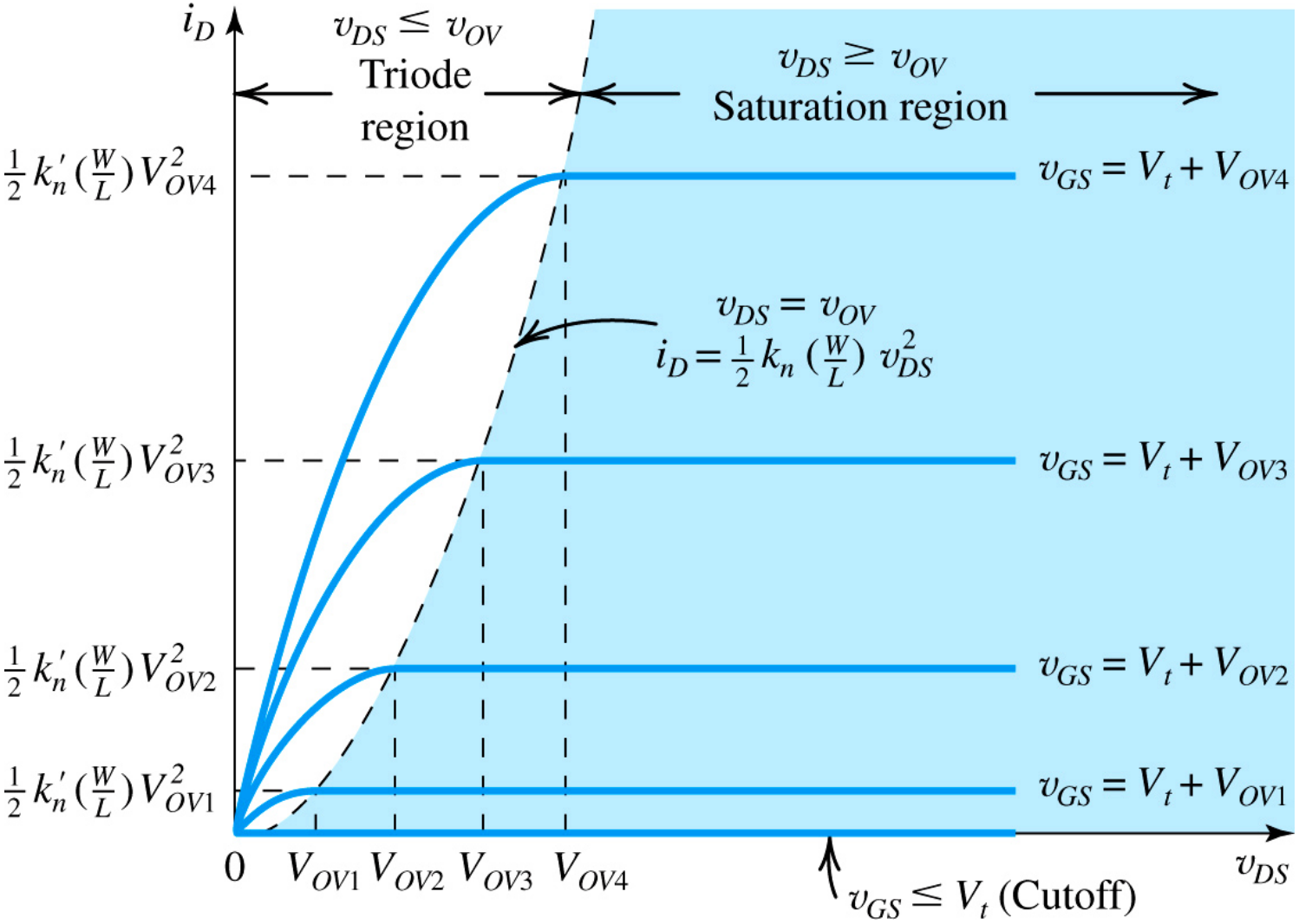




$$i_D = \begin{cases} \text{triode: } (\mu_n C_{ox})\dfrac{W}{L}\left(v_{OV} - \dfrac{1}{2}v_{DS}\right)v_{DS} & \text{if } v_{DS} < v_{OV} \\ \text{saturation: } \dfrac{1}{2}(\mu_n C_{ox})\dfrac{W}{L}v_{OV}^2 & \text{otherwise} \end{cases}$$

Figure 4.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

The i_D-v_{DS} Characteristics



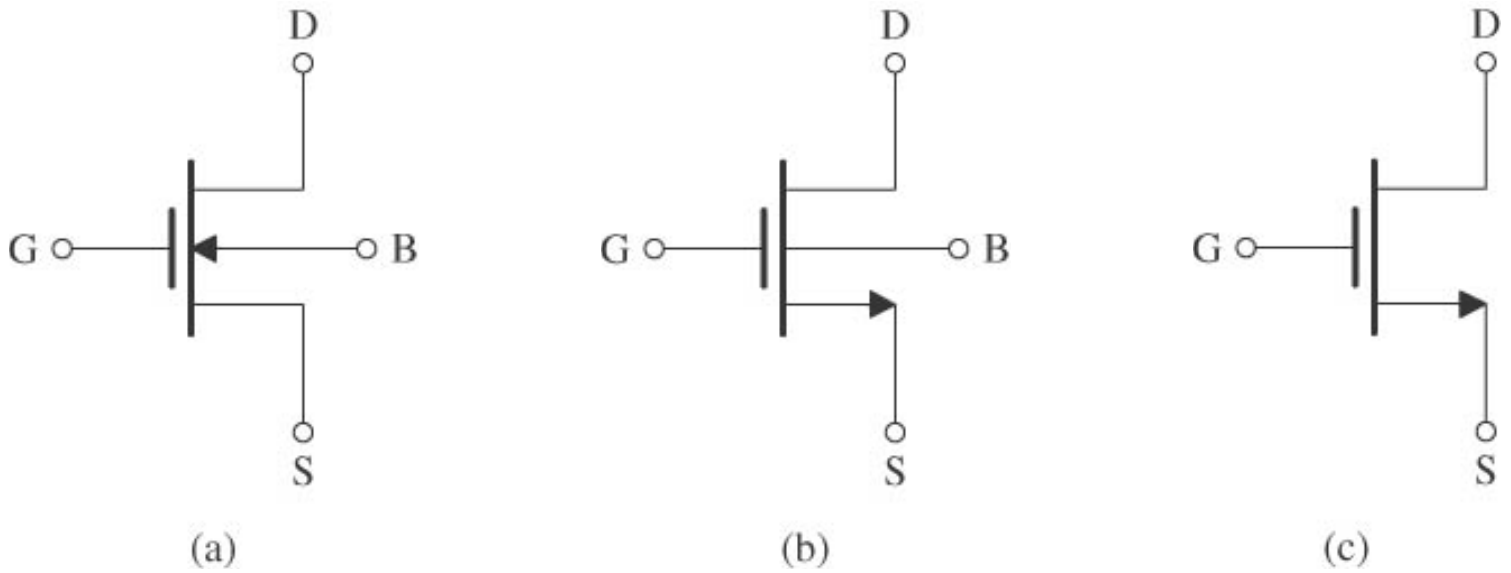


Figure 4.10 **(a)** Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

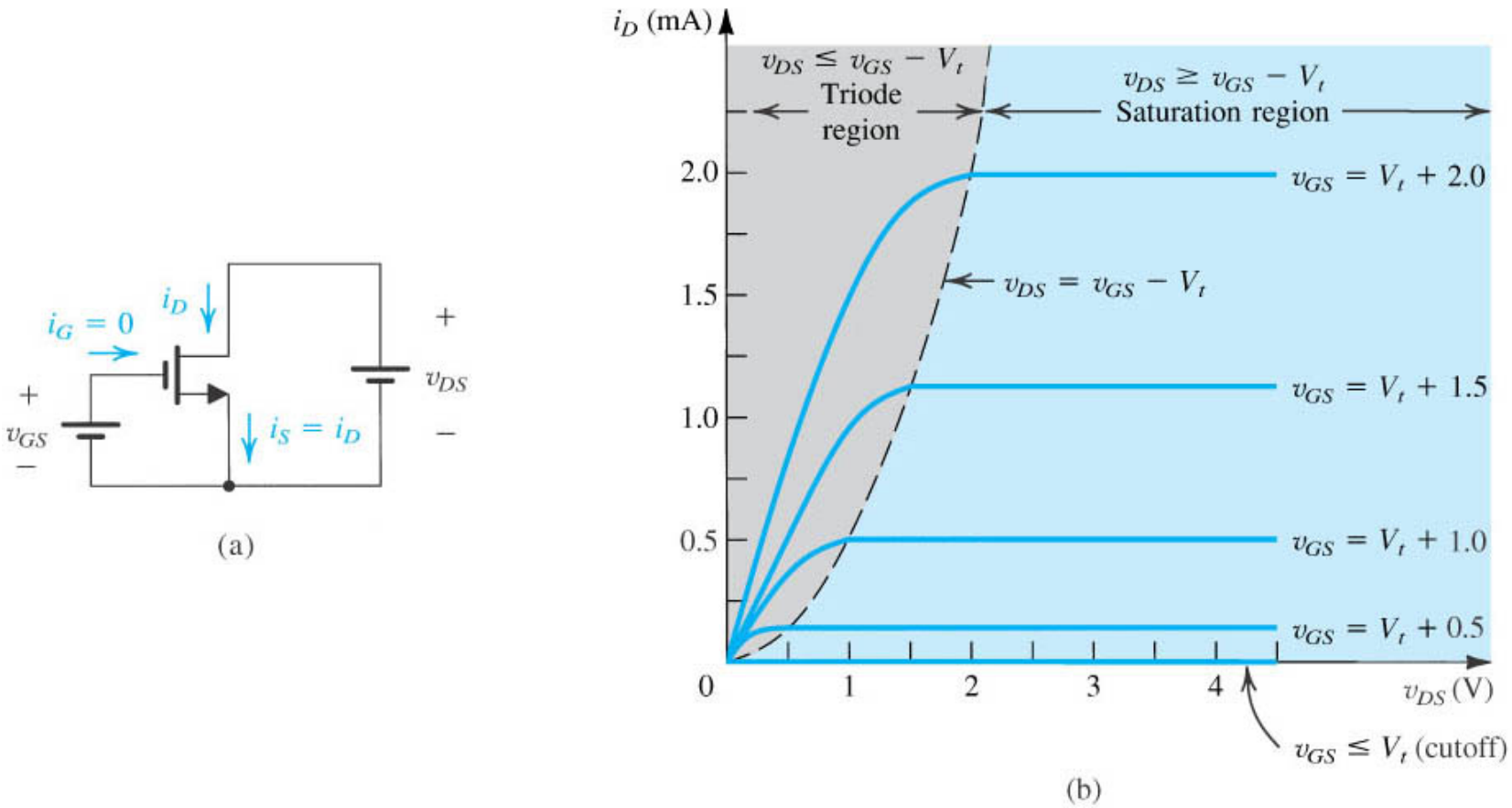
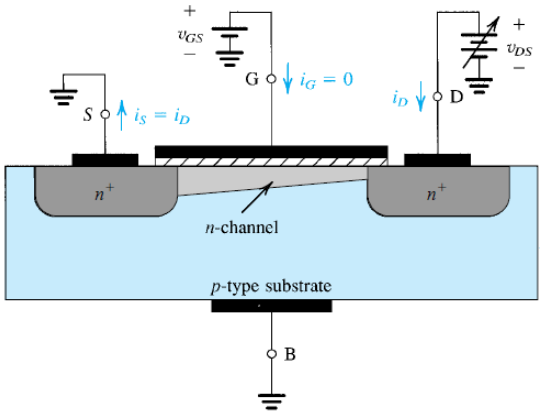
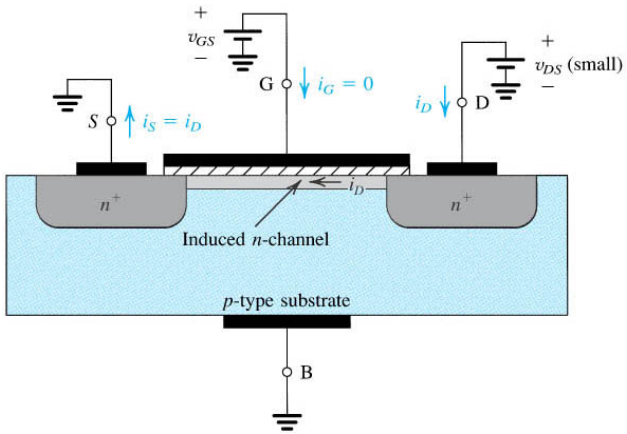


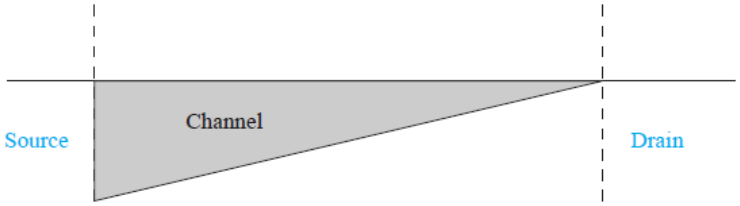
Figure 4.11 **(a)** An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)** The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V².

Effect of v_{DS} on the shape of channel

- v_{DS} is small
- channel is uniform
- $v_{DS} < V_{ov}$
- Channel is tapered
- $v_{DS} \geq V_{ov}$
- Channel is pinched off







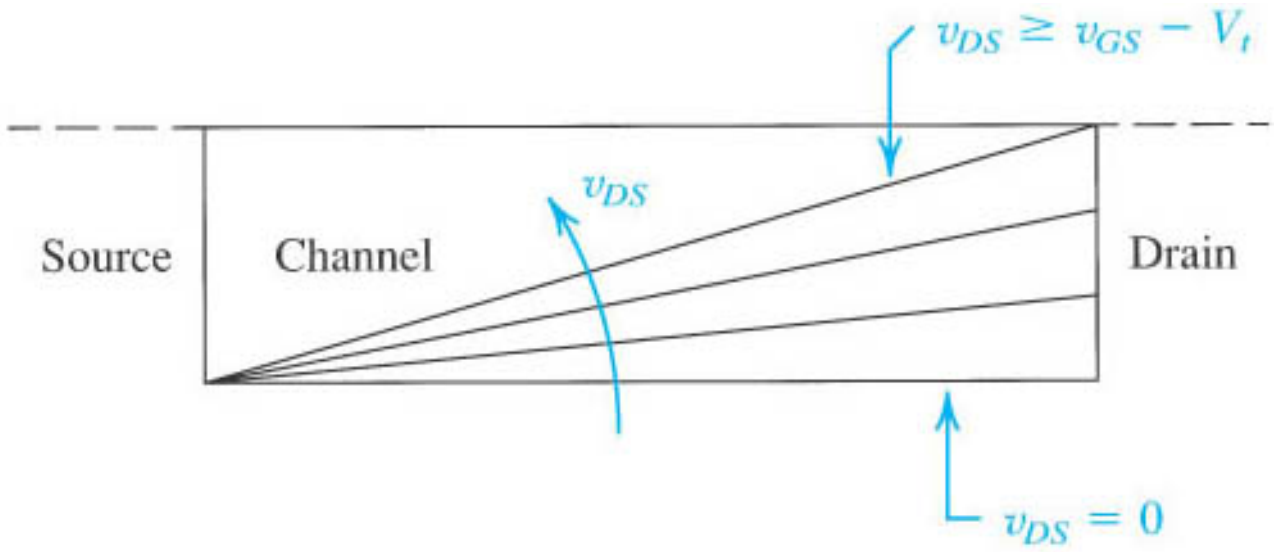
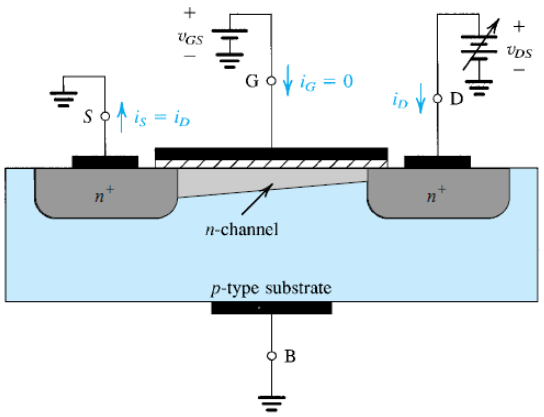


Figure 4.7 Increasing v_{DS} causes the channel to acquire a tapered shape. Eventually, as v_{DS} reaches $v_{GS} - V_t$, the channel is pinched off at the drain end. Increasing v_{DS} above $v_{GS} - V_t$ has little effect (theoretically, no effect) on the channel's shape.

Reason for non uniform channel

- Understand two parameters

1. Voltage drop across channel from drain to source v_{DS}
2. Voltage difference between gate and channel v_{GD}



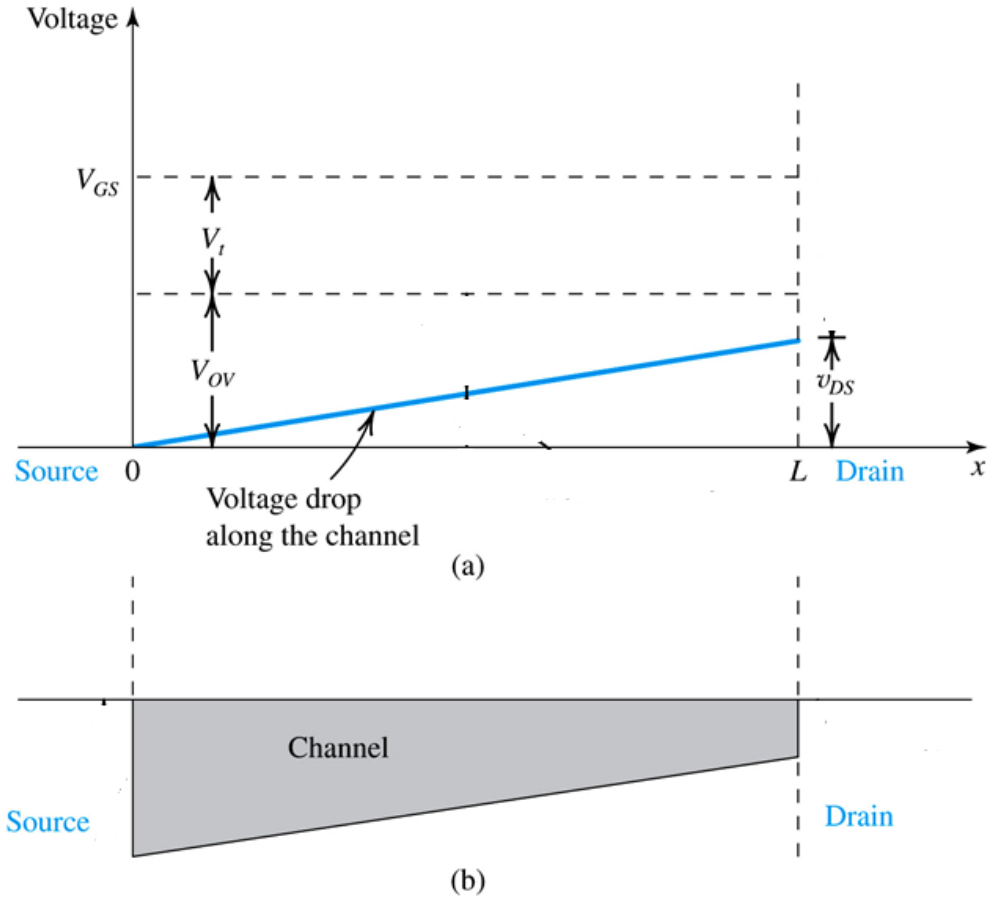
Reason for non uniform channel

- $v_{GD} = v_{GS} - v_{DS}$
- $v_{DS} > v_{GS} - V_t$ ← Condition for saturation
- $v_D - v_S > v_G - v_S - V_t$
- $v_D > v_G - V_t$
- $v_D - v_G > -V_t$
- $v_{DG} > -V_t$
- $-v_{GD} > -V_t$
- $v_{GD} < V_t$
- $v_{GD} > V_t$ ← Triode Region
- $v_{GD} = v_{GS} - (v_{GS} - V_t) = V_t$ ← Edge of saturation

Reason for non uniform channel

- v_{GS} is held constant at value greater than V_t.
- v_{DS} is applied and appears as voltage drop across the length of the *n*-channel.
- At the source end:
- $V_{GD} = V_{GS}$
- At the drain end:
- $V_{GD} = V_{GS} - V_{DS}$
- Going from drain to source, voltage drop at each point with respect to source decreases linearly.

- For small values of v_{DS}, one can still assume that voltage between gate and *n*-channel is constant


Voltage
V_{GS}
V_t
V_{OV}
v_{DS}
Source
0
L
Drain
x
Voltage drop
along the channel
(a)
Channel
Source
Drain
(b)

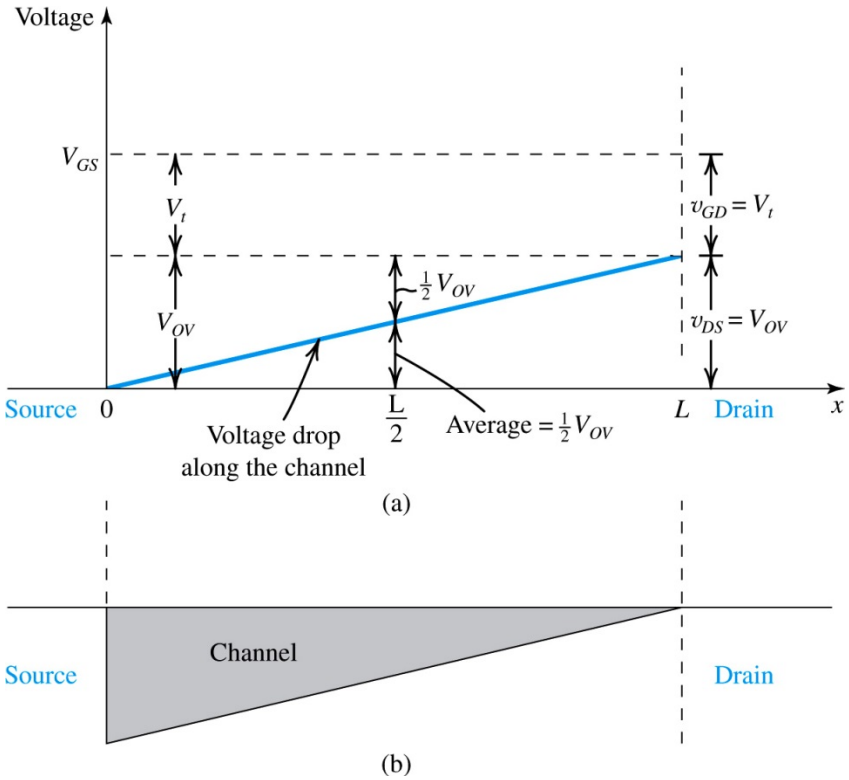
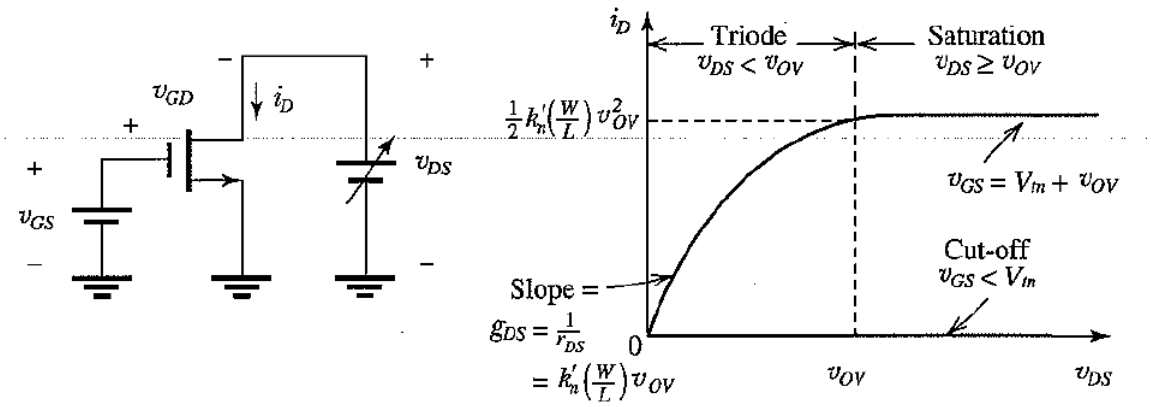


Figure : Operation of MOSFET with $v_{GS} = V_t + v_{OV}$ as v_{DS} is increased to v_{OV}. At the drain end, v_{GD} decreases to V_t and the channel depth at the drain-end reduces to zero (pinch-off). At this point, the MOSFET enters saturation mode of operation. Further increasing v_{DS} (beyond v_{OV}) has no effect on the channel shape and i_D remains constant.

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor



- $v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Consider a process technology for which $L_{min} = 0.4\ \mu m$, $t_{ox} = 8$ nm, $\mu_n = 450\ cm^2/V \cdot s$, and $V_t = 0.7$ V.

(a) Find C_{ox} and k'_n.

(b) For a MOSFET with $W/L = 8\ \mu m/0.8\ \mu m$, calculate the values of V_{OV}, V_{GS}, and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\ \mu A$.

(c) For the device in (b), find the values of V_{OV} and V_{GS} required to cause the device to operate as a 1000-Ω resistor for very small v_{DS}.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.32 \times 10^{-3}\ F/m^2 = 4.32\ fF/\mu m^2$$

$$k'_n = \mu_n C_{ox} = 450\ (cm^2/V \cdot s) \times 4.32\ (fF/\mu m^2)$$

$$= 450 \times 10^8\ (\mu m^2/V \cdot s) \times 4.32 \times 10^{-15}\ (F/\mu m^2)$$

$$= 194 \times 10^{-6}\ (F/V \cdot s)$$

$$= 194\ \mu A/V^2$$

(b) For operation in the saturation region,

$$i_D = \frac{1}{2} k'_n \frac{W}{L} v_{OV}^2$$

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8} V_{OV}^2$$

$$V_{OV} = 0.32\ V$$

$$V_{GS} = V_t + V_{OV} = 1.02\ V$$

$$V_{DSmin} = V_{OV} = 0.32\ V$$

(c) For the MOSFET in the triode region with v_{DS} very small,

$$r_{DS} = \frac{1}{k'_n \frac{W}{L} V_{OV}}$$

$$1000 = \frac{1}{194 \times 10^{-6} \times 10 \times V_{OV}}$$

$$V_{OV} = 0.52\ V$$

$$V_{GS} = 1.22\ V$$

Consider an NMOS transistor fabricated in a 0.18-µm process with $L = 0.18$ µm and $W = 2$ µm. The process technology is specified to have $C_{ox} = 8.6$ fF/µm^2, $\mu_n = 450$ cm^2/V·s, and $V_{tn} = 0.5$ V.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100$ µA.

(b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50$ µA.

(c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3$ V. Find the change in i_D resulting from v_{GS} changing from 0.7 V by +0.01 V and by –0.01 V.

$$k_n' = \mu_n C_{ox}$$
$$= 450 \times 10^{-4} \times 8.6 \times 10^{-15} \times 10^{12} \text{ A/V}^2$$
$$= 387 \text{ µA/V}^2$$

$$k_n = k_n'\left(\frac{W}{L}\right)$$
$$= 387\left(\frac{2}{0.18}\right) = 4.3 \text{ mA/V}^2$$

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{OV}^2$$

$$V_{OV} = 0.22 \text{ V}$$

$$V_{GS} = V_{tn} + V_{OV} = 0.5 + 0.22 = 0.72 \text{ V}$$

$$V_{DS} = V_{OV} = 0.22 \text{ V}$$

$$I_D = k_n\left[V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2\right]$$

$$50 = 4.3 \times 10^3\left[0.22 V_{DS} - \frac{1}{2} V_{DS}^2\right]$$

$$V_{DS}^2 - 0.44 V_{DS} + 0.023 = 0$$

$$V_{DS} = 0.06 \text{ V} \quad \text{and} \quad V_{DS} = 0.39 \text{ V}$$

$$V_{DS} = 0.06 \text{ V}$$

For $v_{GS} = 0.7$ V, $V_{OV} = 0.2$ V,

since $V_{DS} = 0.3$ V, the transistor is operating in saturation and

$$I_D = \frac{1}{2} k_n V_{OV}^2$$
$$= \frac{1}{2} \times 4300 \times 0.04$$
$$= 86 \text{ µA}$$

Now for $v_{GS} = 0.710$ V, $v_{OV} = 0.21$ V

$$i_D = \frac{1}{2} \times 4300 \times 0.21^2 = 94.8 \text{ µA}$$

for $v_{GS} = 0.690$ V, $v_{OV} = 0.19$ V,

$$i_D = \frac{1}{2} \times 4300 \times 0.19^2 = 77.6 \text{ µA}$$

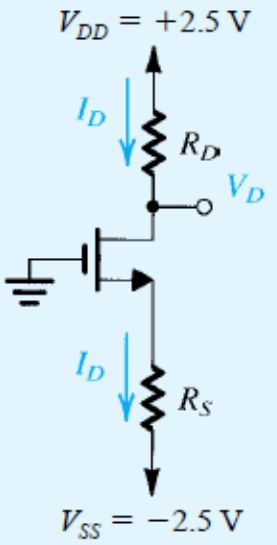
$\Delta V_{GS} = +0.01$ V, $\Delta i_D = 8.8$ µA;

$\Delta V_{GS} = -0.01$ V, $\Delta i_D = -8.4$ µA.

We conclude that the two changes are almost equal, an indication of almost-linear operation when the changes in v_{GS} are kept small. This is just a preview of the "small-signal operation" of the MOSFET stud-

Design the circuit of Fig. 5.21, that is, determine the values of R_D and R_S, so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, $L = 1\ \mu m$, and $W = 32\ \mu m$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5\ k\Omega$$



$$V_G = 0$$

$$V_{GD} = 0 - 0.5$$

$$V_{GD} < V_t$$

Device in saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

substituting $I_D = 0.4$ mA $= 400\ \mu$A, $\mu_n C_{ox} = 100\ \mu A/V^2$, and $W/L = 32/1$

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

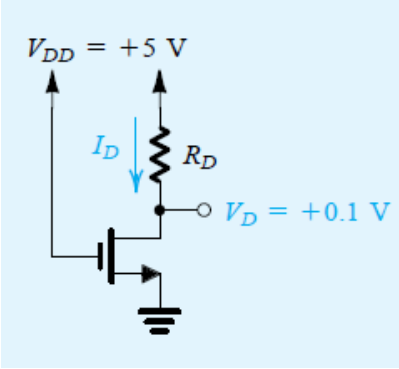
$$V_{OV} = 0.5\ V$$

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2\ V$$

the source must be at –1.2 V

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25\ k\Omega$$

Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2.



$V_G = +5V$

$V_D = 0.1V$

$V_{GD} = 5 - 0.1$

$V_{GD} > V_t$

Device in triode region

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = 1 \times \left[(5-1) \times 0.1 - \frac{1}{2} \times 0.01\right]$$
$$= 0.395 \text{ mA}$$

$$R_D = \frac{V_{DD} - V_D}{I_D}$$
$$= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega$$

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1}{0.395} = 253 \ \Omega$$

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

$$V_G = V_{DD}\frac{R_{G2}}{R_{G2}+R_{G1}} = 10 \times \frac{10}{10+10} = +5 \text{ V}$$

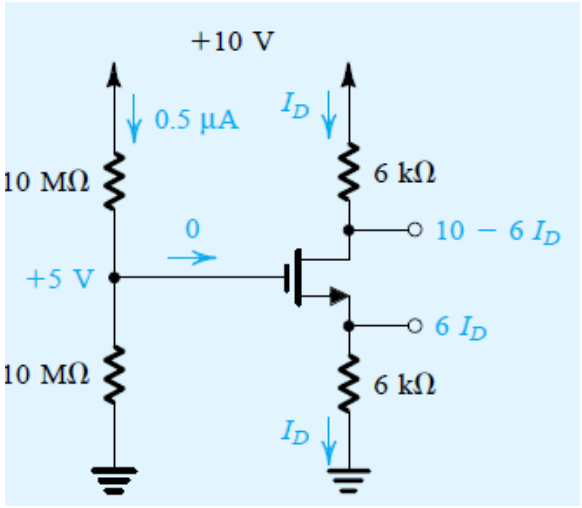
$$I_G = 0$$

Assume the device in saturation mode

$$V_D = V_{DD} - I_D R_D$$

$$I_D = I_S$$

$$V_S = I_D R_S$$



$$V_{GS} = 5 - 6I_D$$

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_{tn})^2$$

$$= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

$$18I_D^2 - 25I_D + 8 = 0$$

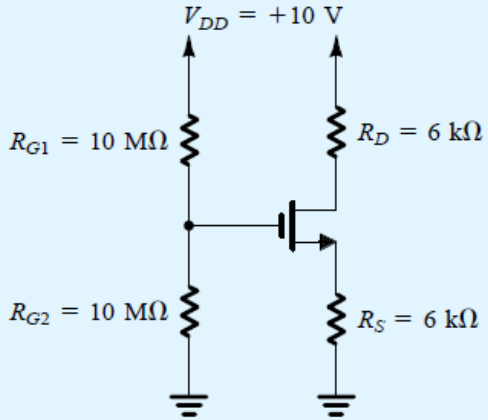
I_D: 0.89 mA and 0.5 mA.

$$V_S = 0.89 \times 6$$

$$V_S = 5.34V$$

$$V_{GS} = 5 - 5.34$$

Negative VGS is not valid for NMOS



$I_D = 0.5$ mA

$V_S = 0.5 \times 6 = +3$ V

$V_{GS} = 5 - 3 = 2$ V

$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

$$V_{GD} = 5 - 7$$

the transistor is operating in saturation, as initially assumed.