Digital Design Verification

UVM based VIP development for AMBA AXI-Lite protocol

Release: 1.0

Date: 04-Nov-2025

NUST Chip Design Centre (NCDC), Islamabad, Pakistan

Total Project Duration: 2 Weeks
Total Marks: 100

About the AXI4-Lite Protocol

The AMBA AXI protocol supports high-performance, high-frequency system designs.
The AXI protocol:

- is suitable for high-bandwidth and low-latency designs
- provides high-frequency operation without using complex bridges
- meets the interface requirements of a wide range of components
- is suitable for memory controllers with high initial access latency
- provides flexibility in the implementation of interconnect architectures
- is backward-compatible with existing AHB and APB interfaces.

The key features of the AXI protocol are:

- separate address/control and data phases
- support for unaligned data transfers, using byte strobes
- uses burst-based transactions with only the start address issued
- separate read and write data channels, that can provide low-cost Direct Memory Access (DMA)
- support for issuing multiple outstanding addresses
- support for out-of-order transaction completion
- permits easy addition of register stages to provide timing closure.

1. Understanding the AXI-Lite Specification
Description: Deep dive into the AMBA AXI-Lite protocol, covering all its features and requirements.
Deadline: Day 2 (by end of the day)
Marks and Deliverables:

- No deliverables for this milestone but understanding of the AMBA AXI-Lite specification will be indirectly evaluated during the final viva and through the quality of the final deliverables.

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2. Verification Plan Creation
Description: Develop and finalize the verification plan, outlining the testing strategy, functional coverage goals, and testbench architecture based on the given specifications.
Deadline: Day 3
Marks: 15
Deliverables:

- Complete verification plan document with test scenarios, coverage goals, and high-level testbench architecture.

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3. Environment and UVC Development
Description: Build the UVM environment based on the finalized architecture, including interface, UVCs (Universal Verification Components) for Master and Slave.
Deadline: Day 6
Marks: 20
Deliverables:

- UVM environment with working Master and Slave UVCs.
- Verification environment connected and configured.

4. Testbench Architecture Implementation

Description: Build the testbench architecture including the top module, connections between UVCs, and basic simulation control.
Deadline: Day 7
Marks: 15
Deliverables:

- Fully integrated testbench.

5. Test Sequences and Testcases Development

Description: Develop test sequences and specific testcases for various AXI-Lite transactions, ensuring coverage of edge cases.
Deadline: Day 9
Marks: 20
Deliverables:

- Collection of directed and random testcases.
- Test sequence files.

6. Coverage and Assertions

Description: Implement functional coverage, code coverage, assertions, and measure the coverage achieved by the testcases.
Deadline: Day 11
Marks: 10
Deliverables:

- Functional coverage model, code coverage model and assertion files.
- Coverage report indicating the percentage of coverage achieved.

7. Use your VIP to verify a simple AXI slave.

Description: Integrate all components, run full regression, and debug any remaining issues.
Deadline: Day 13
Marks: 10
Deliverables:

- Logs and results.

8. Final Integration and Regression Testing

Description: Integrate all components, run full regression, and debug any remaining issues.
Deadline: Day 13
Marks: 10
Deliverables:

- Complete regression run with logs and results.
- Debugged and optimized code.

9. Final Report and Review

- **Description**: Compile a final report summarizing the work done, coverage achieved, and project outcomes.
- **Deadline**: Day 14
- **Marks**: 10
- **Deliverables**:
  - In the end, Final project and its report to be submitted on Git and Viva will be taken.

Document Link:

https://archive.alvb.in/bsc/TCC/correlatos/amba_axi4.pdf