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## **Integrated Circuits**

**By**

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### **Integrated Circuits (EC : Sem-5)**

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11<sup>th</sup> Edition : 2020-21 (*Thoroughly Revised Edition*)

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## KEC-501 : INTEGRATED CIRCUITS

### UNIT-1 : THE 741 IC OP-AMP

(1-1 A to 1-20 A)

General operational amplifier stages (bias circuit, the input stage, the second stage, the output stage, short circuit protection circuitry), device parameters, DC and AC analysis of input stage, second stage and output stage, gain, frequency response of 741, a simplified model, slew rate, relationship between  $f_t$  and slew rate.

### UNIT-2 : LINEAR APPLICATIONS OF IC OP-AMPS (2-1 A to 2-36 A)

Linear Applications of IC Op-Amps: Op-Amp based V-I and I-V converters, instrumentation amplifier, generalized impedance converter, simulation of inductors.

Active Analog filters: Sallen Key second order filter, Designing of second order low pass and high pass Butterworth filter, Introduction to band pass and band stop filter, all pass active filters, KHN Filters. Introduction to design of higher order filters.

### UNIT-3 : FREQUENCY COMPENSATION

(3-1 A to 3-43 A)

Frequency Compensation & Nonlinearity: Frequency Compensation, Compensation of two stage Op-Amps, Slewing in two stage Op-Amp. Nonlinearity of Differential Circuits, Effect of Negative feedback on Nonlinearity.

Non-Linear Applications of IC Op-Amps: Basic Log-Anti Log amplifiers using diode and BJT, temperature compensated Log Anti Log amplifiers using diode, peak detectors, sample and hold circuits. Op-Amp as a comparator and zero crossing detector, astable multivibrator & monostable multivibrator. Generation of triangular waveforms, analog multipliers and their applications.

### UNIT-4 : DIGITAL INTEGRATED CIRCUIT DESIGN

(4-1 A to 4-24 A)

Digital Integrated Circuit Design: An overview, CMOS logic gate circuits basic structure, CMOS realization of inverters, AND, OR, NAND and NOR gates.

Latches and Flip flops: the latch, CMOS implementation of SR flip-flops, a simpler CMOS implementation of the clocked SR flip flop, CMOS implementation of J-K flip-flops, D flip-flop circuits.

### UNIT-5 : INTEGRATED CIRCUIT TIMER

(5-1 A to 5-22 A)

Integrated Circuit Timer: Timer IC 555 pin and functional block diagram, Monostable and Astable multivibrator using the 555 IC. Voltage Controlled Oscillator: VCO IC 566 pin and functional block diagram and applications.

Phase Locked Loop (PLL): Basic principle of PLL, block diagram, working, Ex-OR gates & multipliers as phase detectors, applications of PLL.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

<b>KEC-501</b>	<b>INTEGRATED CIRCUITS</b>	<b>3L:1T:0P</b>	<b>4 Credits</b>
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<b>Unit</b>	<b>Topics</b>	<b>Lectures</b>
I	<b>The 741 IC Op-Amp:</b> General operational amplifier stages (bias circuit, the input stage, the second stage, the output stage, short circuit protection circuitry), device parameters, DC and AC analysis of input stage, second stage and output stage, gain, frequency response of 741, a simplified model, slew rate, relationship between $f_t$ and slew rate.	8
II	<b>Linear Applications of IC Op-Amps:</b> Op-Amp based V-I and I-V converters, instrumentation amplifier, generalized impedance converter, simulation of inductors. <b>Active Analog filters:</b> Sallen Key second order filter, Designing of second order low pass and high pass Butterworth filter, Introduction to band pass and band stop filter, all pass active filters, KHN Filters. Introduction to design of higher order filters.	8
III	<b>Frequency Compensation &amp; Nonlinearity:</b> Frequency Compensation, Compensation of two stage Op-Amps, Slewing in two stage Op-Amp. Nonlinearity of Differential Circuits, Effect of Negative feedback on Nonlinearity. <b>Non-Linear Applications of IC Op-Amps:</b> Basic Log-Anti Log amplifiers using diode and BJT, temperature compensated Log-Anti Log amplifiers using diode, peak detectors, sample and hold circuits. Op-amp as a comparator and zero crossing detector, astable multivibrator & monostable multivibrator. Generation of triangular waveforms, analog multipliers and their applications.	4
IV	<b>Digital Integrated Circuit Design:</b> An overview, CMOS logic gate circuits basic structure, CMOS realization of inverters, AND, OR, NAND and NOR gates. <b>Latches and Flip flops:</b> the latch, CMOS implementation of SR flip-flops, a simpler CMOS implementation of the clocked SR flip-flop, CMOS implementation of J-K flip-flops, D flip-flop circuits.	6
V	<b>Integrated Circuit Timer:</b> Timer IC 555 pin and functional block diagram, Monostable and Astable multivibrator using the 555 IC. <b>Voltage Controlled Oscillator:</b> VCO IC 566 pin and functional block diagram and applications. <b>Phase Locked Loop (PLL):</b> Basic principle of PLL, block diagram, working, Ex-OR gates and multipliers as phase detectors, applications of PLL.	6

**Text Book:**

1. Microelectronic Circuits, Sedra and Smith, 7th Edition, Oxford, 2017.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill
3. Gayakwad, "Op-Amps and Linear Integrated Circuits, 4th Edition, Pearson Education.
4. Sergio Franco, Design of Operational Amplifier and Analog Integrated Circuit, McGraw Hill
5. David A. Bell, "Operational Amplifiers and Linear IC's", Pearson Education,

**Reference Books:**

1. Franco, Analog Circuit Design: Discrete & Integrated, McGraw Hill, 1st Edition.
2. D. Roy Choudhary and Shail B. Jain, "Linear Integrated Circuits", New Age Publication
3. International Publications TB1 L.K. Maheshwari, Analog Electronics, PHI, 2005
4. Salivahanan, Electronics Devices and Circuits, McGraw Hill , 3rd Edition, 2015
5. Millman and Halkias: Integrated Electronics, McGraw Hill, 2nd Edition, 2010.
6. TB2 L.K. Maheshwari and M.M.S. Anand, Laboratory Experiments & PSPICE Simulation in Analog Electronics Experiments, PHI, 2005.

**Course Outcomes: At the end of this course students will demonstrate the ability to:**

1. Explain complete internal analysis of Op-Amp 741-IC.
2. Examine and design Op-Amp based circuits and basic components of ICs such as various types of filter.
3. Implement the concept of Op-Amp to design Op-Amp based non-linear applications and wave-shaping circuits.
4. Analyse and design basic digital IC circuits using CMOS technology.
5. Describe the functioning of application specific ICs such as 555 timer, VCO IC 566 and PLL.

# 1

UNIT

## The 741 IC Op-Amp

### CONTENTS

- Part-1 :** The 741 IC Op-Amp : ..... **1-2A to 1-15A**  
General Operational  
Amplifier Stages (Bias  
Circuit, the Input Stage,  
The Second Stage, The Output  
Stage, Short Circuit Protection  
Circuitry), Device Parameters,  
DC and AC Analysis of Input State,  
Second Stage and Output Stage
- Part-2 :** Frequency Response of 741, ..... **1-15A to 1-19A**  
a Simplified Model, Gain,  
Slew Rate, Relationship Between  $f_t$   
and Slew Rate

**PART- 1**

*The 741 IC Op-Amp : General Operational Amplifier Stages (Bias Circuit, the Input Stage, The Second Stage, The Output Stage, Short Circuit Protection Circuitry), Device Parameters, DC and AC Analysis of Input State, Second Stage and Output Stage.*

**CONCEPT OUTLINE**

- The IC-741 is a widely used as general purpose Op-Amp. It is divided into 3 stages :
  - i. Input differential amplifier
  - ii. The gain stage
  - iii. The output stage
- The Op-Amp is supplied with positive and negative supply voltages of value  $\pm 15$  V.

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

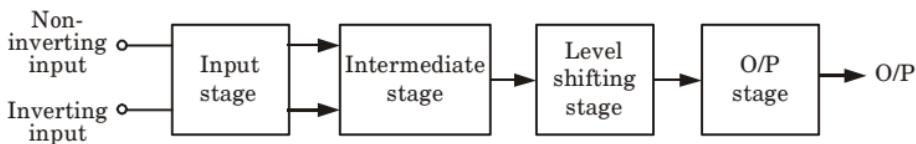
**Que 1.1.** Write a short note on 741 Op-Amp circuit and discuss the bias circuit.

**OR**

Write the characteristics of ideal Op-Amp.

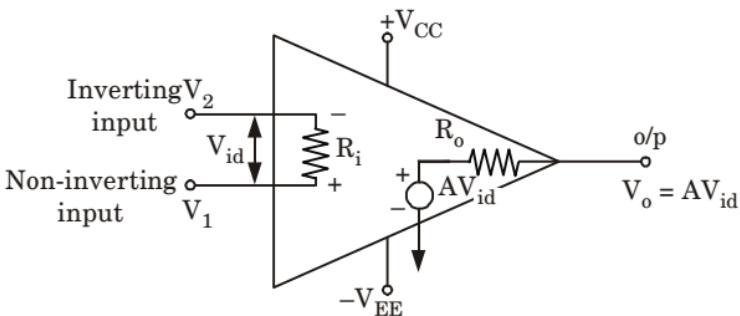
**Answer****A. Op-Amp circuit :**

1. Generally BJT based Op-Amp is focused on 741 Op-Amp circuit. If we use IC design, the circuits use large number of transistors but relatively few resistors and only one capacitor.
2. The block diagram of typical Op-Amp is shown in Fig. 1.1.1



**Fig. 1.1.1.** Block diagram of Op-Amp.

3. The equivalent circuit of Op-Amp is shown in Fig. 1.1.2.



**Fig. 1.1.2.** Equivalent circuit of Op-Amp.

### B. Characteristics of ideal Op-Amp :

1. Infinite voltage gain,  $A_v = \infty$ .
2. Infinite input resistance,  $R_i = \infty$ .
3. Zero output resistance,  $R_o = 0$ .
4. Zero output voltage when input voltage is zero.
5. Infinite bandwidth.

### C. Bias circuit :

1. The bias circuit is used to provide proportional current in the collector of transistor.
2. Some transistors form the current mirror, in which transistor collector provides bias current for other output stage of Op-Amp.
3. Finally some transistors works to provide the  $V_{BE}$  drop between the bases of output transistors for proper functioning of the device.

**Que 1.2.** Explain the three stages of Op-Amp, i.e., input differential stage, an intermediate single-ended high gain stage and an output buffering stage. Mention device parameters for the *npn* and *pnp* transistors.

### Answer

#### A. Stages of Op-Amp :

##### i. Input stage :

1. The input stage consists of transistors for biasing purpose, transistor also acts as emitter followers, causing the input resistance to be high and delivering the differential input signal to the differential common base amplifier.
2. The input stage is the differential version of the common-collector common-base configuration.
3. The combination of transistors and resistors form the current mirror (load circuit). It provide not only high-resistance load but also converts the signal from differential to single-ended form with no loss in gain or common-mode-rejection.

4. Op-Amp circuit includes a level shifter whose function is to shift the DC level of the signal so that signal at output can swing positive and negative.

### **ii. Second stage :**

1. The second or intermediate stage composed of some transistors and two resistors. Transistor act as emitter follower and provide high input resistance. They also minimize loss of gain.
2. The output of second stage is taken at the collector of transistor. Capacitor is also connected in the feedback path of second stage to provide frequency compensation.

### **iii. Output stage :**

1. The output stage is to provide the amplifier with a low output resistance. The output stage also supplies relatively large load currents without dissipating large amount of power.
2. The output circuit is a class *AB* output stage. To keep emitter-follower transistor conducting at all times to ensure the low output resistance. When bias current  $I$  is greater than load current  $i_L$ , this is called class *A* operation.
3. The power dissipation in output stage is reduced by arranging transistors to turn ON only when an input signal is applied. Such arrangement is known as class *B* operation.

## **B. Device Parameters :**

- i. For standard *npn* and *pnp* transistors.

***npn* :**  $I_s = 10^{-14}$  A,  $\beta = 200$

and  $V_A = 125$  V.

***pnp* :**  $I_s = 10^{-14}$  A,  $\beta = 50$

and  $V_A = 50$  V.

- ii. For parallel base-emitter junction,

***npn* :**  $I_s = 0.25 \times 10^{-14}$  A

***pnp* :**  $I_s = 0.75 \times 10^{-14}$  A

**Que 1.3.** Describe what is mean by output short circuit protection and explain how it is achieved in the output stage of IC741.

**AKTU 2019-20, Marks 07**

**OR**

**How the short circuit protection is achieved in the output stage of 741 Op-Amp ?**

**AKTU 2018-19, Marks 3.5**

**OR**

**Find out the output resistance of 741 Op-Amp.**

**Answer**

1. The short-circuit protection circuitry is shown in the Fig. 1.3.1

2. The Op-Amp 741 contains a number of transistors that are normally in the OFF state.
3. When the output terminal gets shorted to the ground, while keeping a positive output voltage due to certain input signal, this will induce a large current in the output transistor  $Q_{14}$ .
4. This will result in producing heat and cause burn-out of the transistor. Therefore, when current flow in  $Q_{14}$  reaches 20 mA, voltage drop across  $R_6$  becomes  $27 \times 20 = 540, which bias the transistor  $Q_{15}$ .$
5. Similarly, the maximum current in  $Q_{20}$  is limited by  $R_7$ ,  $Q_{21}$  and  $Q_{24}$ .
6. When the current increases, the voltage drop across  $R_7$  becomes sufficient and the transistor  $Q_{21}$  becomes ON and  $Q_{21}$  and  $Q_{24}$  shunt the excess current away from the transistor  $Q_{20}$ , hence protects the output transistor.

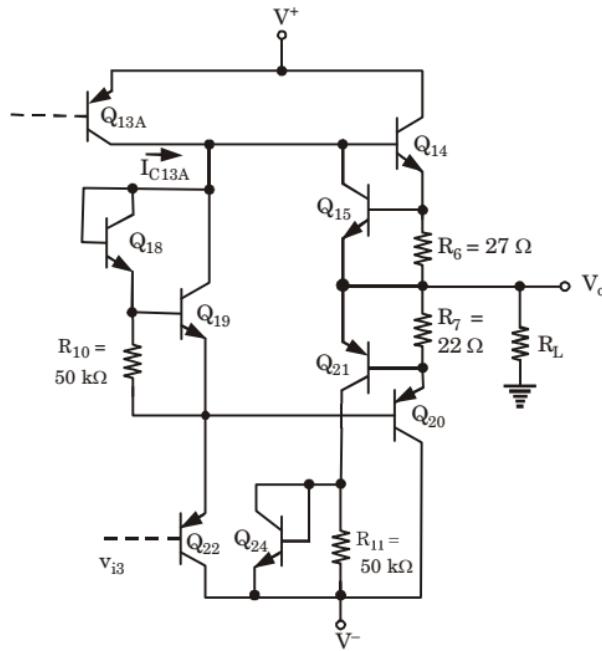


Fig. 1.3.1.

**Output resistance of 741 Op-Amp :**

1. The output resistance of the Op-Amp  $R_{out}$  is determined from the Fig. 1.3.2. In accordance with the definition of  $R_{out}$ , the input source feeding the output stage is grounded, but its resistance is included.
2. We have assumed that the output voltage  $v_o$  is negative and thus  $Q_{20}$  is conducting most of the current; transistor  $Q_{14}$  has therefore been eliminated. The exact value of the output resistance will depend on which transistor ( $Q_{14}$  or  $Q_{20}$ ) is conducting and on the value of load current.
3. The resistance of emitter of  $Q_{23}$  is

$$R_{o23} = \frac{R_{o2}}{\beta_{23} + 1} + r_{e23}$$

This resistance appears in parallel with the series combination of  $r_{o13A}$  and the resistance  $Q_{18}$ - $Q_{19}$  network.

4. Since  $r_{o13A}$  alone is larger than  $R_{o23}$ , the effective resistance between the base of  $Q_{20}$  and ground approximately to  $R_{o23}$ , the output resistance  $R_{out}$  as

$$R_{out} = \frac{R_{o23}}{\beta_{20} + 1} + r_{e20}$$

5. The output resistance of the 741 is specified to be typically  $75 \Omega$ .

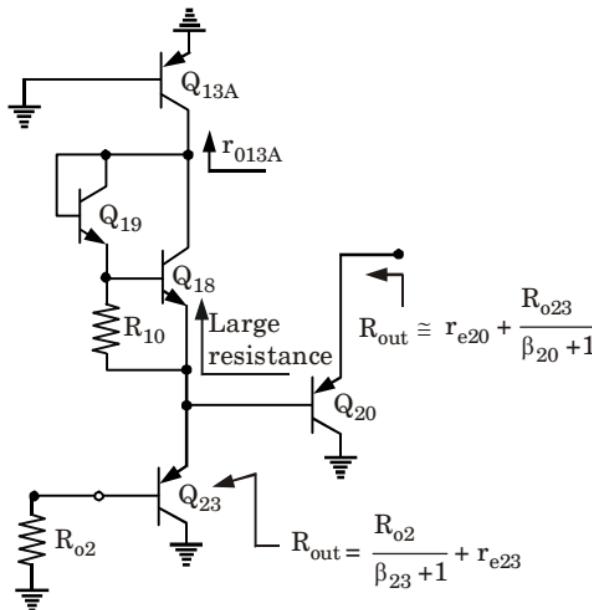


Fig. 1.3.2.

#### Que 1.4.

Discuss the DC analysis of input stage of 741 IC Op-Amp.

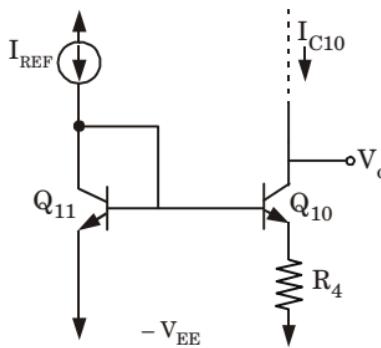
#### Answer

**Reference bias current :** The reference bias current  $I_{REF}$  is generated in the branch composed of the two diode-connected transistors  $Q_{11}$  and  $Q_{12}$  and resistor  $R_5$ .

$$I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}$$

For  $V_{CC} = V_{EE} = 15 \text{ V}$  and  $V_{BE11} = V_{EB12} \approx 0.7 \text{ V}$ , we have  $I_{REF} = 0.73 \text{ mA}$ .

1. Transistor  $Q_{11}$  is biased by  $I_{REF}$ , and the voltage developed across it is used to bias  $Q_{10}$ , which has a series emitter resistance  $R_4$ .



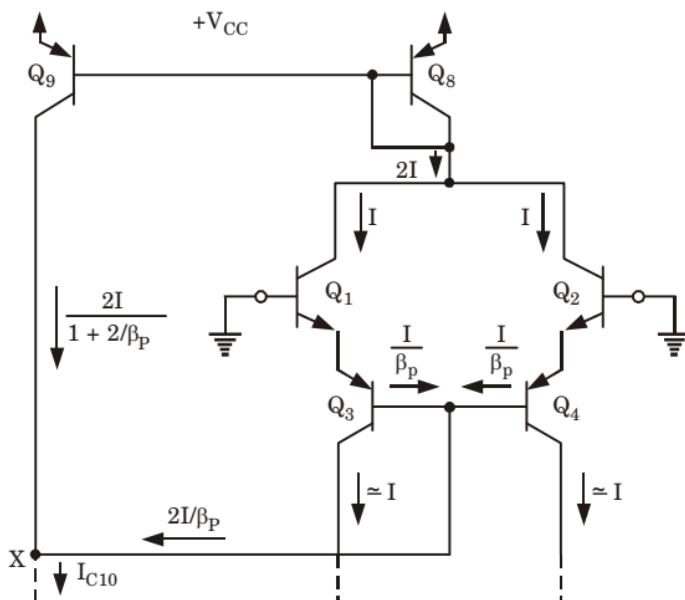
**Fig. 1.4.1.** The Widlar current source that biases the input stage.

2. This part of the circuit is redrawn in Fig. 1.4.2 and can be recognized as the Widlar current source.
3. From the circuit, and assuming  $\beta_{10}$  to be large, we have

$$V_{BE11} - V_{BE10} = I_{C10}R_4$$

Thus,

$$V_T = \ln \left( \frac{I_{REF}}{I_{C10}} \right) = I_{C10}R_4 \quad \dots(1.4.1)$$



**Fig. 1.4.2.** The DC analysis of the 741 input stage.

where it has been assumed that  $I_{S10} = I_{S11}$ .

4. Substituting the known values for  $I_{REF}$  and  $R_4$ , eq. (1.4.1) can be solved by trial and error to determine  $I_{C10}$ . For our case, the result is  $I_{C10} = 19 \mu\text{A}$ .

5. Having determined  $I_{C10}$ , we proceed to determine the DC current in each of the input-stage transistors. Part of the input stage is redrawn in Fig. 1.4.2. From symmetry, we see that

$$I_{C1} = I_{C2}$$

6. Denote this current by  $I$ . We see that if the *npn*  $\beta$  is high, then

$$I_{E3} = I_{E4} \approx I$$

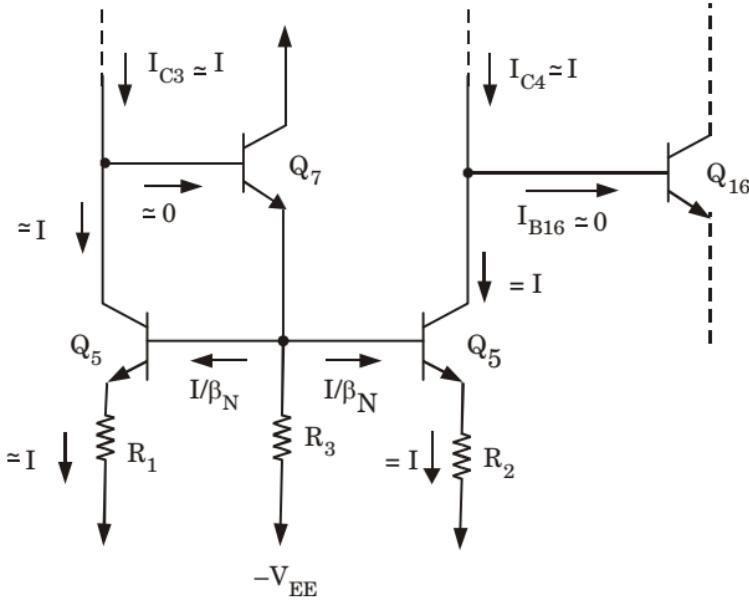
and the base currents of  $Q_3$  and  $Q_4$  are equal, with a value of  $I/(\beta_p + 1) \approx I/\beta_p$ , where  $\beta_p$  denotes  $\beta$  of the *pnp* devices.

7. The current mirror formed by  $Q_8$  and  $Q_9$  is fed by an input current of  $2I$ , we can express the output current of the mirror as

$$I_{C9} = \frac{2I}{1 + 2/\beta_p}$$

8. We can now write a node equation for node  $X$  in Fig. 1.4.3 and thus determine the value of  $I$ . If  $\beta_p > 1$ , then this node equation gives

$$2I = I_{C10}$$



**Fig. 1.4.3.**

9. For the 741,  $I_{C10} = 19 \mu\text{A}$ ; thus  $I = 9.5 \mu\text{A}$ . We have thus determined that

$$I_{C1} = I_{C2} \approx I_{C3} = I_{C4} = 9.5 \mu\text{A}$$

10. Fig. 1.4.3 shows the remainder of the 741 input stages. This part of the circuit is fed by  $I_{C3} = I_{C4} = I$ . Transistors  $Q_5$  and  $Q_6$  are identical and have equal resistances  $R_1$  and  $R_2$  in their emitters,

$$I_{C5} = I_{C6}$$

...(1.4.2)

Now if the base currents of  $Q_7$  and  $Q_{16}$  can be neglected, then

$$I_{C5} \approx I_{C3} = I \quad \dots(1.4.3)$$

and  $I_{C6} = I_{C4} = I \quad \dots(1.4.4)$

11. Thus both the symmetry of  $Q_5$  and  $Q_6$  and the node equations at their collectors force their currents to be equal and to equal  $I$ .

12. The bias current of  $Q_7$  can be determined from

$$I_{C7} \approx I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3} \quad \dots(1.4.5)$$

where  $\beta_N$  denote  $\beta$  of the  $npn$  transistors. To determine  $V_{BE6}$  we use the transistor exponential relationship and write

$$V_{BE6} = V_T \ln \frac{I}{I_S}$$

13. Substituting  $I_S = 10^{-14}$  A and  $I = 9.5$  mA results in  $V_{BE6} = 517$  mV. Then substituting in eq. (1.4.5) yields  $I_{C7} = 10.5$  mA.

**Que 1.5. Explain the DC analysis of second stage and output stage of 741 IC Op-Amp.**

**Answer**

**A. Second-Stage :**

- If we neglect the base current of  $Q_{23}$  from Op-Amp circuit then the collector current of  $Q_{17}$  is approximately equal to the current supplied by current source  $Q_{13B}$ .
- Because  $Q_{13B}$  has a scale current 0.75 times that of  $Q_{12}$ , its collector current will be  $I_{C13B} = 0.751 I_{REF}$ , where we have assumed that  $\beta_p > 1$ . Thus  $I_{C13B} = 550$   $\mu$ A and  $I_{C13} = 550$   $\mu$ A.
- At this current level the base-emitter voltage for  $Q_{17}$  is

$$V_{BE17} = V_T \ln \frac{I_{C17}}{I_S} = 618 \text{ mV}$$

4. The collector current of  $Q_{16}$  can be determined from

$$I_{C16} = I_{E16} = I_{B17} + \frac{I_{E17}R_8 + V_{BE17}}{R_9}$$

5. This calculation yields  $I_{C16} = 16.2$   $\mu$ A.

**B. Output-stage Bias :**

- Fig. 1.5.1 shows the output stage of the 741 with the short-circuit protection circuitry omitted.
- Current source  $Q_{12A}$  delivers a current of  $0.25I_{REF}$  (because  $I_S$  of  $Q_{13A}$  is 0.25 times the  $I_S$  of  $Q_{12}$ ) to the network composed of  $Q_{18}$ ,  $Q_{19}$  and  $R_{10}$ .
- If we neglect the base current of  $Q_{14}$  and  $Q_{20}$ , then the emitter current of  $Q_{23}$  will also be equal to  $0.25I_{REF}$ . Thus

$$I_{C23} \approx I_{E23} \approx 0.251 I_{REF} = 180 \mu\text{A}$$

4. Thus we see that the base current of  $Q_{23}$  is only  $180/50 = 3.6 \mu\text{A}$ , which is negligible compared to  $I_{C17}$ , as we have assumed.
5. We assume that  $V_{BE18}$  is approximately 0.6 V, we can determine the current in  $R_{10}$  as  $15 \mu\text{A}$ .
6. The emitter current of  $Q_{18}$  is therefore

$$I_{E18} = 180 - 15 = 165 \mu\text{A}$$

Also,  $I_{C18} \approx I_{E18} = 165 \mu\text{A}$

7. At this value of current we find the  $V_{BE18} = 588 \text{ mV}$ , which is quite close to the value assumed. The base current of  $Q_{18}$  is  $165/200 = 0.8 \text{ mA}$ , which can be added to the current in  $R_{10}$  to determine the  $Q_{19}$  current as

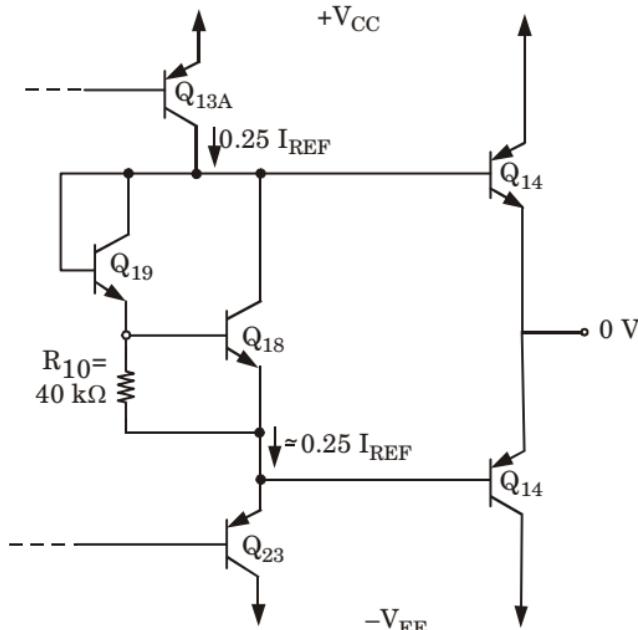
$$I_{C19} = I_{E19} = 15.8 \mu\text{A}$$

8. The voltage drop across the base-emitter junction of  $Q_{19}$  can now be determined as,

$$V_{BE19} = V_T \ln \frac{I_{C19}}{I_S} = 530 \text{ mV}$$

9. Voltage drop,  $V_{BB} = V_{BE18} + V_{BE19} = 588 + 530 = 1.118 \text{ V}$
10. Since  $V_{BB}$  appears across the series combination of the base-emitter junctions of  $Q_{14}$  and  $Q_{20}$ , we can write

$$V_{BB} = V_T \ln \frac{I_{C14}}{I_{S14}} + V_T \ln \frac{I_{C20}}{I_{S20}}$$



**Fig. 1.5.1.** The 741 output stage without the short-circuit protection devices.

11. Using calculated values of  $V_{BB}$  and substituting

$$I_{S14} = I_{S20} = 3 \times 10^{-14} \text{ A}$$

12. We determine the collector current as,

$$I_{C14} = I_{C20} = 154 \text{ mA}$$

13. This is the small current at which the class AB output stage is biased.

**Que 1.6.** Explain the input stage of small signal analysis.

**Answer**

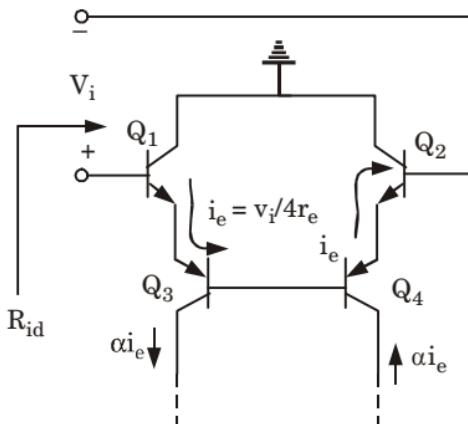
- Fig. 1.6.1 shows part of the 741 input stage for the purpose of performing small-signal analysis.
- The collector of  $Q_1$  and  $Q_2$  are connected to a constant DC voltage and are shown grounded. The input signal is applied between the input terminals of  $Q_1$ ,  $Q_2$ ,  $Q_3$  and  $Q_4$ .

$$i_e = \frac{v_i}{4r_e}$$

where  $i_e$  and  $r_e$  are the emitter current and resistance respectively.

$$r_e = \frac{V_T}{I}$$

- Four transistors  $Q_1$  through  $Q_4$  supply the load circuit with a pair of complementary current signals  $\alpha i_e$ .



**Fig. 1.6.1.** Small signal analysis of the 741 input stage.

$$R_{id} = 4(\beta + 1) r_e$$

where,  $R_{id}$  is input differential resistance.

- The output current  $i_o$  is

$$i_o = 2 \times \alpha i_e$$

- The transconductance of input stage,

$$G_{m1} = \frac{i_o}{v_i} = \frac{\alpha}{2r_e}$$

6. The output resistance is,  $R_o = r_o [1 + g_m (R_E \parallel r_\pi)]$

**Que 1.7.** Determine the small-signal model of the second stage of the 741 Op-Amp.

AKTU 2017-18, Marks 05

**Answer**

1. Fig. 1.7.1 shows the 741 second stage Op-Amp prepared for small-signal analysis. Now we analyze the second stage to determine the values of the parameters of the equivalent circuit shown in Fig. 1.7.2.

- a. **Input resistance :** The input resistance  $R_{i2}$  can be found by

$$R_{i2} = (\beta_{16} + 1) \{r_{e16} + [R_9 \parallel (\beta_{17} + 1)(r_{e17} + R_8)]\} \quad \dots(1.7.1)$$

Substituting the appropriate parameter values yields  $R_{i2} = 4 \text{ M}\Omega$ .

- b. **Transconductance :**

- i. From the equivalent circuit of Fig. 1.7.2, we see that the transconductance  $G_{m2}$  is the ratio of the short-circuit output current to the input voltage.

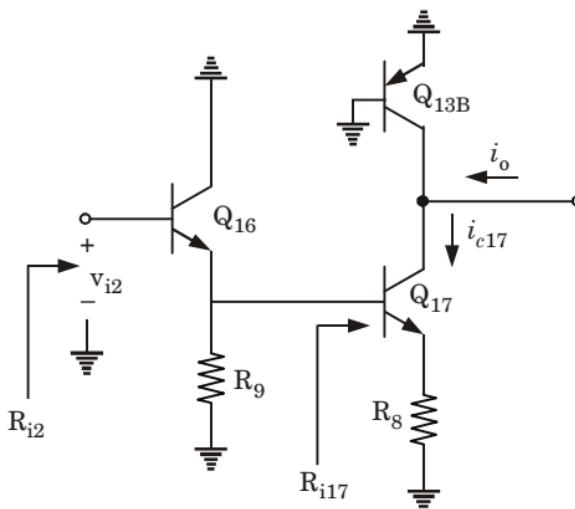
- ii. Short-circuiting the output terminal of the second stage to ground makes the signal current through the output resistance of  $Q_{13B}$  zero, and the output short-circuit current becomes equal to the collector signal current of  $Q_{17}(i_{c17})$ . This can be easily related to  $v_{i2}$  as follows :

$$i_{c17} = \frac{\alpha v_{b17}}{r_{e17} + R_8} \quad \dots(1.7.2)$$

$$v_{b17} = v_{i2} \frac{(R_9 \parallel R_{i17})}{(R_9 \parallel R_{i17}) + r_{e16}} \quad \dots(1.7.3)$$

$$R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8) \quad \dots(1.7.4)$$

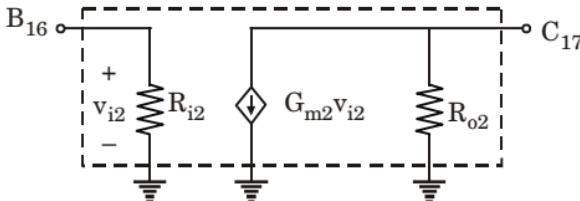
where we have neglected  $r_{o16}$  because  $r_{o16} \gg R_9$ .



**Fig. 1.7.1.** The 741 second stage prepared for small-signal analysis.

- iii. These equations can be combined to obtain

$$G_{m2} \equiv \frac{i_{c17}}{v_{i2}} \quad \dots(1.7.5)$$



**Fig. 1.7.2.** Small-signal equivalent-circuit model of the second stage.

**c. Output resistance :**

- i. To determine the output resistance  $R_{o2}$  of the second stage in Fig. 1.7.1 we ground the input terminal and find the resistance looking back into the output terminal.
- ii. So,  $R_{o2}$  is given by

$$R_{o2} = (R_{o13B} \parallel R_{o17})$$

where  $R_{o13B}$  is the resistance looking into the collector  $Q_{13B}$  while its base and emitter are connected to ground and  $R_{o17}$  is the resistance looking into the collector of  $Q_{17}$ .

**Que 1.8.** Describe the all stages of small signal analysis of the 741 Op-Amp.

**Answer**

- A. **Input Stage :** Refer Q. 1.6, Page 1-11A, Unit-1.
- B. **Second Stage :** Refer Q. 1.7, Page 1-12A, Unit-1.
- C. **Output Stage :** The 741 output stage without short circuit protection circuit is shown in Fig. 1.8.1.

**Output voltage limits :**

1. The maximum positive output voltage is limited by the saturation of current-source transistor  $Q_{13A}$ .

Thus,  $V_{o \max} = V_{CC} - |V_{CE \text{ sat}}| - V_{BE14} \quad \dots(1.8.1)$

$$V_{o \min} = -V_{EE} + V_{CE \text{ sat}} + V_{EB23} + V_{EB20} \quad \dots(1.8.2)$$

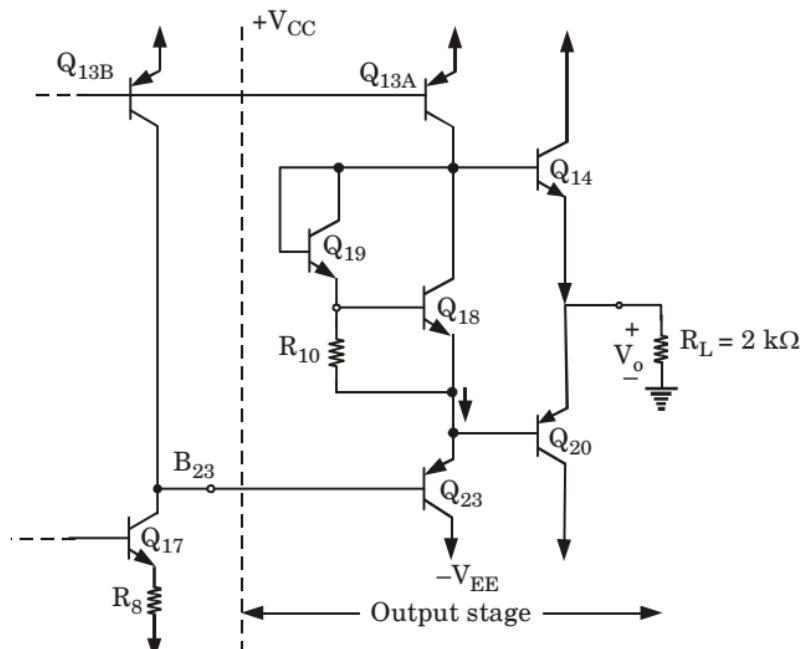


Fig. 1.8.1.

2. Small signal model is shown in Fig. 1.8.1.

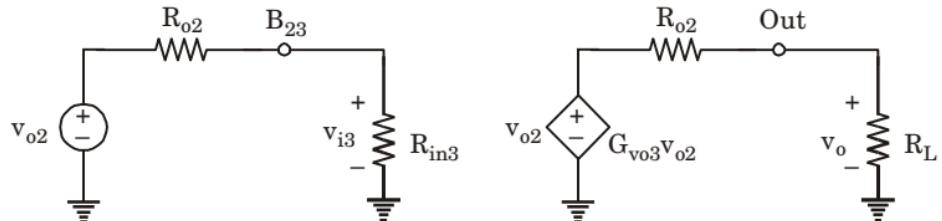


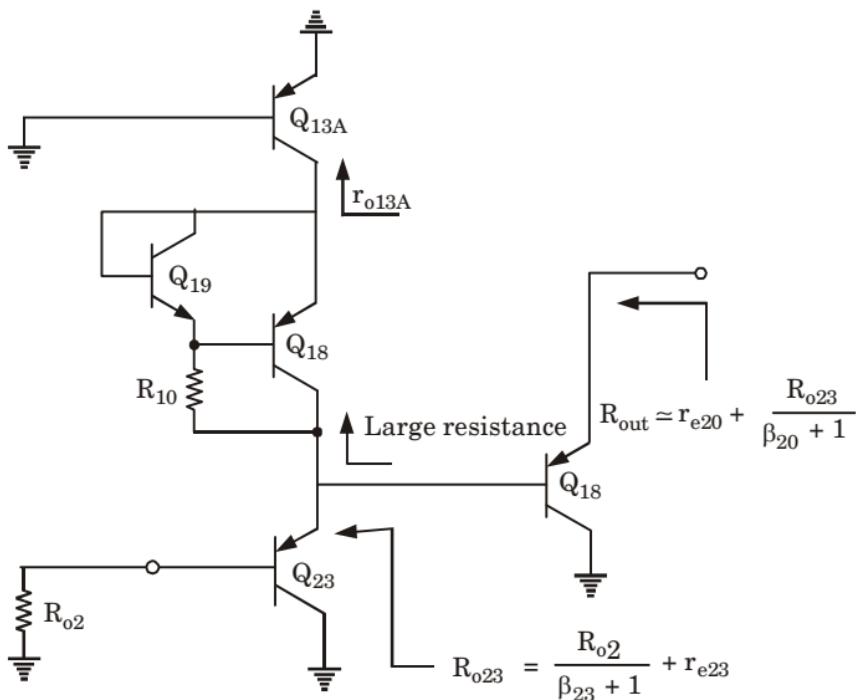
Fig. 1.8.2. Small signal model for the 741 output stage.

3. Open circuit voltage gain  $G_{vo3} = \frac{v_o}{v_{o2}} \Big|_{R_L=\infty}$
4. Circuit for finding out the output resistance is shown in Fig. 1.8.3.
5. Resistance seen looking into emitter of  $Q_{23}$  is

$$R_{o23} = \frac{R_{o2}}{\beta_{23} + 1} + r_{e23}$$

6. Since  $r_{o13A}$  alone is much larger than  $R_{o23}$  so effective resistance between the base of  $Q_{20}$  and ground is equal to  $R_{o23}$ .
7. Now, output resistance ( $R_{out}$ ) is

$$R_{out} = \frac{R_{o23}}{\beta_{20} + 1} + r_{e20}$$



**Fig. 1.8.3.** Circuit for finding the output resistance  $R_{out}$ .

## PART-2

*Frequency Response of 741, a Simplified Model, Gain, Slew Rate, Relationship Between  $f_t$  and Slew Rate.*

### Questions-Answers

### Long Answer Type and Medium Answer Type Questions

**Que 1.9.** Draw and explain the frequency response of IC 741.

**AKTU 2018-19, Marks 3.5**

### Answer

1. The system employs the Miller compensation technique.
2. A capacitor ( $C_c$ ) of about 30 pF is connected in the negative feedback path of the second stage.
3. An estimation of frequency of poles can be obtained as,

$$C_{in} = C_c(1 + |A_2|)$$

$A_2$  = Gain of second stage

4. Let  $A_2 = -515$   
 then  $C_{in} = 15480 \text{ pF}$

Since, this value of capacitor is large so we neglect all other capacitances between the base and ground of transistor.

5. The total resistance,

$$\begin{aligned} R_t &= (R_{o1} \parallel R_{i2}) \\ &= (6.7 \text{ M}\Omega \parallel 4 \text{ M}\Omega) \\ &= 2.5 \text{ M}\Omega \end{aligned}$$

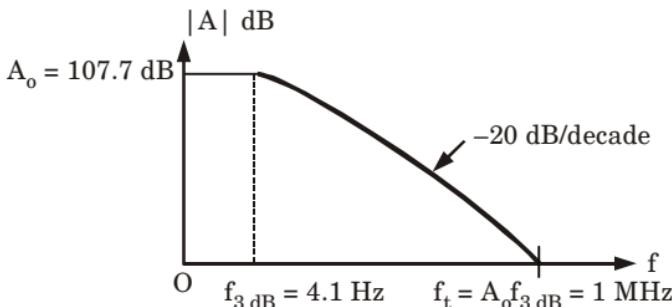
6. The dominant pole has a frequency  $f_p$ ,

$$f_p = \frac{1}{2\pi C_{in} R_t} = 4.1 \text{ Hz}$$

7. Calculate all the values of poles and a bode plot is shown in Fig. 1.9.1

$$f_t = A_o f_{3 \text{ dB}} = 243147 \times 4.1 \approx 1 \text{ MHz}$$

where,  $f_t$  is unity-gain bandwidth.



**Fig. 1.9.1.** Bode plot for the IC 741 gain.

9. Bode plot signifies that the phase shift at  $f_t$  is  $-90^\circ$  and thus phase margin is  $90^\circ$ . This phase margin is sufficient to provide stable operation of closed-loop amplifiers with any value of feedback factor  $\beta$ .

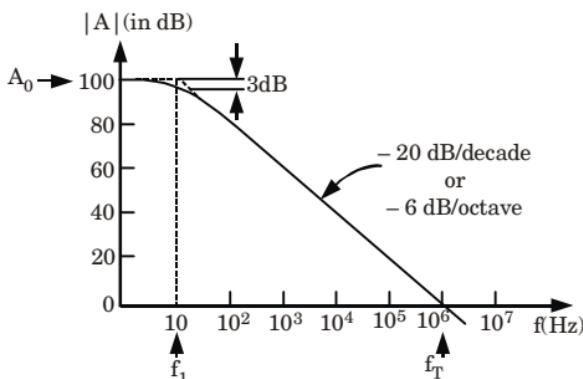
**Que 1.10.** Draw the frequency response of IC 741. Give the upper and lower 3-dB frequency of same.

**Answer**

- A. **Frequency response :** Refer Q. 1.9, Page 1-15A, Unit-1.  
 B. **Upper and lower 3-dB frequency :** The magnitude of open loop gain of Op-Amp is given by,

$$|A| = \frac{A_0}{\sqrt{1 + (f/f_1)^2}}$$

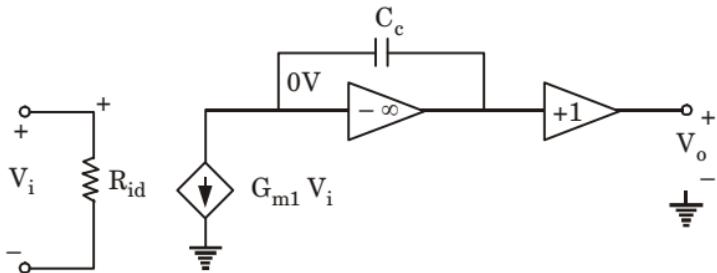
- i. The open-loop gain  $A$  is approximately constant from 0 Hz to break frequency  $f_1$ .

**Fig. 1.10.1.** Frequency response of IC 741 Op-Amp.

- ii. When  $f = f_1$ , the gain  $A$  is 3-dB down from its value at 0 Hz. Hence, the break frequency is called 3-dB frequency or corner frequency or lower 3-dB frequency.
- iii. For  $f > f_1$ , the open-loop gain rolls-off at a rate of  $-20 \text{ dB/decade}$  or  $-6 \text{ dB/octave}$ .
- iv. At a particular input frequency  $f_T$  shown, the open-loop gain  $A$  is unity, or gain in dB is zero. This is called the unity gain-bandwidth, small-signal bandwidth and unity gain cross-over frequency.

**Que 1.11.** Draw and explain the simplified model of 741 Op-Amp.**Answer**

1. Fig. 1.11.1 shows a simplified model of the 741 Op-Amp. The gain of 2<sup>nd</sup> stage is assumed sufficiently large. The output stage is assumed to be ideal unity-gain follower.

**Fig. 1.11.1.** A simple model for the 741 based on modeling the second stage as an integrator.

2. From the Fig. 1.11.1,

$$A(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_{m1}}{sC_c}$$

Thus, 
$$A(j\omega) = \frac{G_{m1}}{j\omega C_c}$$

3. At  $\omega = \omega_t$ ,  $G_{m1} = 1/5.26$  mA/V and  $C_c = 30$  pF

$$f_t = \frac{\omega_t}{2\pi} = 1 \text{ MHz}$$

where,  $\omega_t = \frac{G_{m1}}{C_c}$

4. This model is only valid at frequencies  $f >> f_{3 \text{ dB}}$

**Que 1.12.** Find out the overall gain of an Op-Amp IC-741 giving its cascaded equivalent circuit derived for its three stages. Also derive the relationship between  $f_t$  and slew rate for IC-741.

AKTU 2019-20, Marks 07

OR

Define the slew rate. Also derive the relationship between  $f_t$  and slew rate for the IC-741.

AKTU 2015-16, Marks 10

### Answer

**A. Overall gain of an Op-Amp IC-741 :**

The overall voltage gain  $A_v$  of the Op-Amp is the product of voltage gains of each stage as given by,

$$A_v = |A_d| |A_2| |A_3|$$

where,  $A_d$  = Gain of differential amplifier stage

$A_2$  = Gain of the second stage

$A_3$  = Gain of the output stage

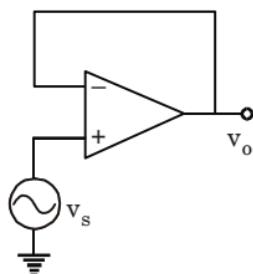
**B. Slew rate :** The slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per microsecond, i.e.,

$$SR = \left. \frac{dv_o}{dt} \right|_{\max} \text{ V/}\mu\text{s}$$

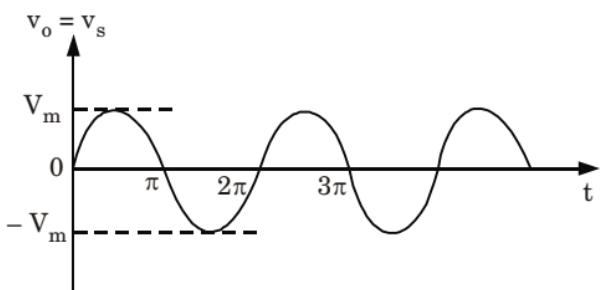
**C. Relationship between  $f_t$  and SR :**

- Consider a voltage follower shown in Fig. 1.12.1(a). The input is large amplitude, high frequency sine wave.
- If  $v_s = V_m \sin \omega t$   
Then, output  $v_o = V_m \sin \omega t$
- Fig. 1.12.1(b) shows the input-output waveform.
- The rate of change of the output is given by,

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$



(a) Voltage follower



(b) Input/output waveform

**Fig. 1.12.1.**

5. The maximum rate of change of the output occurs when  $\cos \omega t = 1$ . That is,  $SR = \left. \frac{dv_o}{dt} \right|_{\max} = \omega V_m$

6. Therefore, slew rate  $= 2\pi f V_m$  V/s

$$= \frac{2\pi f V_m}{10^6} \text{ V}/\mu\text{s}$$

where,

$f$  = Input frequency (Hz)

$V_m$  = Peak output amplitude.

**Que 1.13.** A 741 IC Op-Amp whose slew rate is 0.5 V/ $\mu$ s is used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve of 741 IC is flat upto 20 KHz. What maximum peak to peak input signal can be applied without distorting the output ?

### Answer

**Given :** Slew rate,  $SR = 0.5 \text{ V}/\mu\text{s}$ , Gain = 50,  $f = 20 \text{ KHz}$

**To Find :** Maximum peak to peak input signal.

1. We know,  $SR = \frac{2\pi f V_p}{10^6} \text{ V}/\mu\text{s}$  ... (1.13.1)

where  $V_p$  is peak value of output sine wave (V).

2. Putting all given values in eq. (1.13.1), we get,

$$0.5 = \frac{2\pi (20 \times 10^3) V_p}{10^6}$$

$$V_p = \frac{0.5 \times 10^3}{2\pi (20)} = 3.98 \text{ V (undistorted)}$$

3. Maximum peak to peak input signal that can be applied without distorting output is  $2 \times 3.98 = 7.96 \text{ V}$

**V ERY IMPORTANT QUESTIONS**

***Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.***

- Q. 1. Describe what is mean by output short circuit protection and explain how it is achieved in the output stage of IC741.**

**Ans.** Refer Q. 1.3.

- Q. 2. Determine the small-signal model of the second stage of the 741 Op-Amp.**

**Ans.** Refer Q. 1.7.

- Q. 3. Describe the all stages of small signal analysis of the 741 Op-Amp.**

**Ans.** Refer Q. 1.8.

- Q. 4. Draw and explain the frequency response of IC 741.**

**Ans.** Refer Q. 1.9.

- Q. 5. Draw the frequency response of IC 741. Give the upper and lower 3-dB frequency of same.**

**Ans.** Refer Q. 1.10.

- Q. 6. Find out the overall gain of an Op-Amp IC-741 giving its cascaded equivalent circuit derived for its three stages. Also derive the relationship between  $f_T$  and slew rate for IC-741.**

**Ans.** Refer Q. 1.12.



# 2

UNIT

## Linear Applications of IC Op-Amp

### CONTENTS

- Part-1 :** Linear Applications of ..... **2-2A to 2-9A**  
IC Op-Amps : Op-Amp  
Based V-I and I-V  
Converters, Instrumentation  
Amplifier, Generalized  
Impedance Converter, Simulation  
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- Part-2 :** Active Analog Filters : ..... **2-9A to 2-18A**  
Sallen Key Second Order  
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**PART - 1**

*Linear Applications of IC Op-Amps : Op-Amp Based V-I and I-V Converters, Instrumentation Amplifier, Generalized Impedance Coverter, Simulation of Inductors.*

**CONCEPT OUTLINE**

- The voltage to current converters accepts an input voltage  $V_1$  and gives an output current  $I_L$ .  
There are two circuits of  $V-I$  converter namely :
  - i. Voltage to current with floating load.
  - ii. Voltage to current with grounded load.
- A current to voltage converter or ideal current controlled voltage source, also called transresistance amplifier is the one, whose
  - i. Output voltage is equal to a constant  $k$  times the magnitude of an independent input current  $I_i$ ,  
*i.e.,* 
$$V_g = k I_i$$
  - ii. Output voltage is independent of the load connected to it. The constant  $k$  has the units of ohms.

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 2.1.** Draw  $V-I$  converter and derive its output equation for floating load.

**Answer**

1. The Fig. 2.1.1 shows an arrangement of voltage to current converter with load resistor  $R_L$ . Here  $R_L$  is in floating condition *i.e.*, not connected to ground.
2. The input is applied to non-inverting end and the feedback voltage across  $R_1$  drives the inverting input end.
3. The feedback voltage across  $R_1$  depends on the output current  $i_o$  and it is in series with the input difference voltage  $V_{id}$ .
4. Due to the concept of virtual ground, the voltage at node A will be  $V_{in}$ .  
Thus, 
$$i_o = V_{in} / R_1$$
  
*i.e.*, an input voltage  $V_{in}$  is converted into an output current of  $V_{in} / R_1$ .

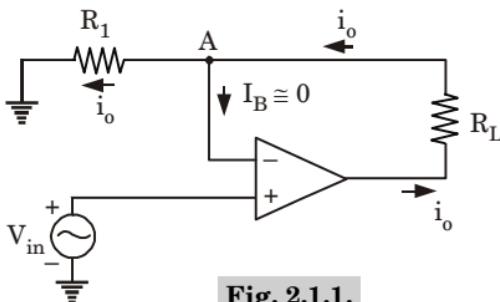


Fig. 2.1.1.

**Que 2.2.** Draw and explain  $I\text{-}V$  and  $V\text{-}I$  converters and derive its output.

AKTU 2018-19, Marks 07

### Answer

#### A. $I\text{-}V$ converter :

1. The current to voltage converter is shown in Fig. 2.2.1.
2. The open-loop gain  $A_v$  of the Op-Amp is very large, so due to virtual short concept,

$$V_1 \approx V_2$$

3. As the input impedance of Op-Amp is very high,

∴

$$I_{B1} = I_{B2} \approx 0$$

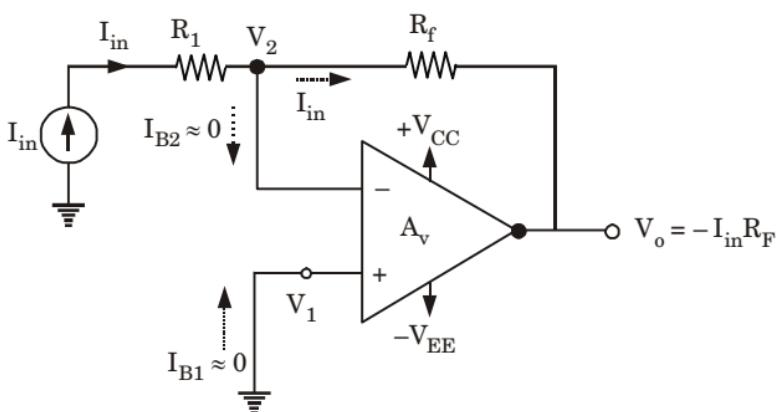


Fig. 2.2.1. Current to voltage converter.

4. Gain of inverting amplifier is given by

$$A_v = \frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

or

$$V_o = \frac{-R_f}{R_1} V_{in} \quad \dots(2.2.1)$$

4. But  $V_1 \approx V_2$  and

$$V_1 = 0$$

$$\therefore V_2 = 0$$

5. Thus the inverting terminal is also at ground potential and entire input voltage appears across  $R_1$

$$\therefore I_{\text{in}} = \frac{V_{\text{in}}}{R_1}$$

$$\text{or } V_{\text{in}} = I_{\text{in}} R_1 \quad \dots(2.2.2)$$

6. Substituting eq. (2.2.2) in eq. (2.2.1), we get

$$V_o = \frac{-R_f}{R_1} \times I_{\text{in}} R_1$$

$$V_o = -R_f I_{\text{in}} \quad \dots(2.2.3)$$

7. The eq. (2.2.3) shows how this circuit converts input current into a proportional voltage.

**B. V-I converter :** Refer Q. 2.1, Page 2-2A, Unit-2.

**Que 2.3.** Derive the expression of output voltage for instrumentation amplifier.

### Answer

- The instrumentation amplifier shown in Fig. 2.3.1 has high input impedance and a high gain.
- The Op-Amps  $A_1$  and  $A_2$  as shown in Fig. 2.3.1 are voltage follower or buffer circuits acting as the input stage for each of the input  $V_1$  and  $V_2$ .
- They have zero differential input voltage, i.e.,  $V_{id} = 0$ . Under such conditions with common mode signal = 0, and  $V_1 = V_2$ , the voltage across the resistor  $R$  is zero.
- The voltages at the inverting terminals of the buffers are equal to the input voltages. Since no current flows through the resistors  $R$  and  $R'$ , the output voltages are  $V_2' = V_2$  and  $V_1' = V_1$  respectively.
- The current flowing in the resistor  $R$  is  $I = \frac{(V_1 - V_2)}{R}$  and the same current  $I$  will flow through the resistors  $R'$  in the direction as shown in Fig. 2.3.1. The voltage at the non-inverting terminal of Op-Amp  $A_3$  is

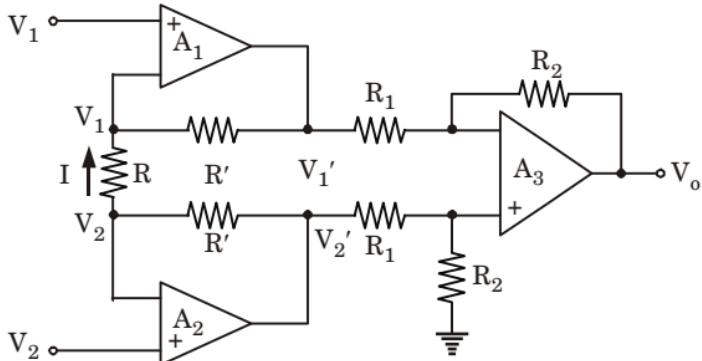
$$\frac{R_2 V_1'}{R_1 + R_2}.$$

6. By using superposition theorem, we get

$$V_o = -\frac{R_2}{R_1} V'_2 + \left(1 + \frac{R_2}{R_1}\right) \left(\frac{R_2 V'_1}{R_1 + V'_2}\right)$$

7. Simplifying, we get

$$V_o = \frac{R_2}{R_1} (V'_1 - V'_2) \quad \dots(2.3.1)$$



**Fig. 2.3.1.** Instrumentation amplifier.

8. Since there is no current entering the Op-Amp, the current

$$I = \frac{(V_1 - V_2)}{R}, \text{ which flows through the resistor } R'.$$

$$V'_1 = RI + V_1 = \frac{R'}{R} (V_1 - V_2) + V_1$$

$$\text{and} \quad V'_2 = RI + V_2 = \frac{R'}{R} (V_1 - V_2) + V_2$$

9. Substituting the values  $V'_1$  and  $V'_2$  in eq. (2.3.1), then we get

$$V_o = \frac{R_2}{R_1} \left[ \frac{2R'}{R} (V_2 - V_1) + (V_2 - V_1) \right]$$

$$\text{i.e.,} \quad V_o = \frac{R_2}{R_1} \left[ 1 + \frac{2R'}{R} \right] (V_2 - V_1)$$

10. By using a variable resistor  $R$ , the gain of this instrumentation amplifier can be varied.

**Que 2.4.** Describe the Antoniou inductance simulation circuit with properly labeled circuit diagram and give mathematical expressions in support of your answer. **AKTU 2015-16, Marks 10**

**Answer**

1. Fig. 2.4.1 shows the Antoniou inductance simulation circuit.

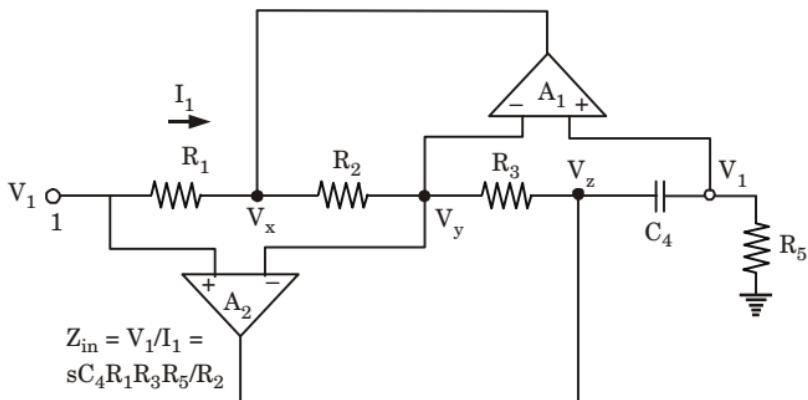


Fig. 2.4.1.

2. Applying KCL, we get

$$\frac{V_1 - V_z}{1/sC_4} + \frac{V_1}{R_5} = 0$$

$$V_z = V_1 \left[ 1 + \frac{1}{sC_4 R_5} \right]$$

3. Apply KCL, we get

$$\frac{V_y - V_x}{R_2} + \frac{V_y - V_z}{R_3} = 0 \quad \dots(2.4.1)$$

4. Substituting the value of  $V_z$  in eq. (2.4.1)

$$\frac{V_y - V_x}{R_2} + \frac{V_y - V_1 \left( 1 + \frac{1}{sC_4 R_5} \right)}{R_3} = 0$$

$$R_3(V_y - V_x) + R_2V_y - R_2V_1 \left( 1 + \frac{1}{sC_4 R_5} \right) = 0 \quad \dots(2.4.2)$$

5. Apply KCL, then we get

$$\frac{V_x - V_1}{R_1} + \frac{V_x - V_y}{R_2} = 0$$

$$R_2(V_x - V_1) + R_1(V_x - V_y) = 0$$

$$V_x(R_1 + R_2) = R_2V_1 + R_1V_y$$

$$V_y = \frac{V_x(R_1 + R_2)}{R_1} - \frac{R_2}{R_1}V_1 \quad \dots(2.4.3)$$

6. Now put the value of  $V_y$  in eq. (2.4.2),

then,

$$V_x = \left( V_1 + \frac{V_1 R_2}{sC_4 R_5 R_3} \right)$$

7. Current across resistance  $R_1$ ,

$$I_1 = \left[ V_1 - \left( V_1 + \frac{V_1 R_2}{s C_4 R_5 R_3} \right) \right] \times \frac{1}{R_1}$$

$$I_1 = \frac{V_1 R_2}{s C_4 R_5 R_3 R_1}$$

8. Then input impedance

$$Z_{in} = \frac{V_1}{I_1} = \frac{s C_4 R_1 R_3 R_5}{R_2}$$

which is that of an inductance  $L$  given by,

$$L = \frac{C_4 R_1 R_3 R_5}{R_2}$$

9. If  $R_1 = R_2 = R_3 = R_5 = R$  and  $C_4 = C$   
then,  $L = CR^2$ .

**Que 2.5.** Draw the generalized impedance converter and derive its impedance equation. Also simulate an inductor.

AKTU 2017-18, Marks 05

AKTU 2019-20, Marks 07

### Answer

#### A. General Impedance Converter (GIC) :

- Generalized impedance converters (GICs) are Op-Amp circuits that employ  $RC$  networks for simulating frequency-dependent impedance elements such as inductors. Fig. 2.5.1 shows the circuit of a GIC.
- From Fig. 2.5.1, at node 1,

$$I_C = \frac{V_1 - V_2}{Z_1} = \frac{V_{CC} - V_{01}}{Z_1} \quad \dots(2.5.1)$$

where  $V_1 = V_{CC}$  and  $V_2 = V_{01}$ . Now, between nodes 2 and 4, we obtain (using KCL)

$$\frac{V_2 - V_3}{Z_2} = \frac{V_3 - V_4}{Z_3} \quad \dots(2.5.2)$$

- From the Fig. 2.5.2, we observe that nodes 1 and 3 are virtually shorted, and hence using KCL

$$\frac{V_{01} - V_{CC}}{Z_2} = \frac{V_{CC} - V_{02}}{Z_3} \quad \dots(2.5.3)$$

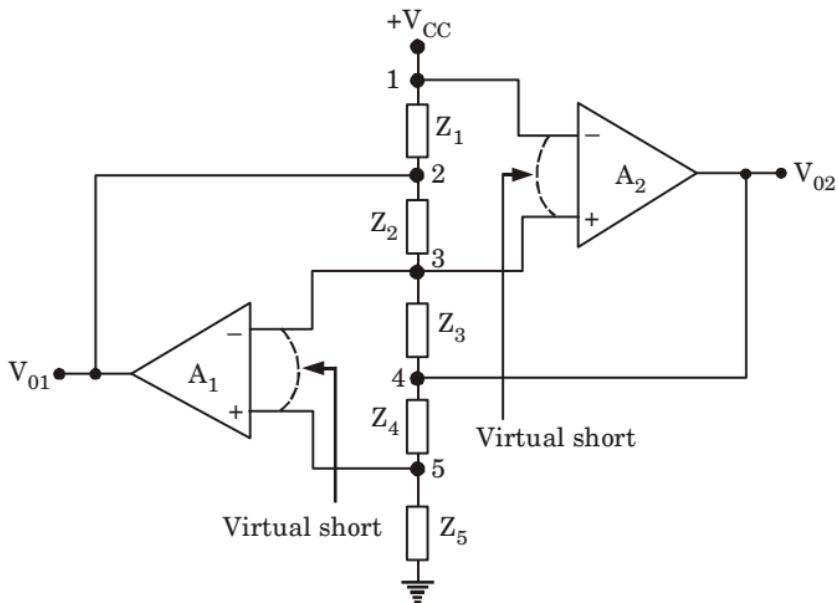
where  $V_{02} = V_4$ .

- Rearranging eq. (2.5.3) yields

$$(Z_2 + Z_3) V_{CC} = V_{02} Z_2 + V_{01} Z_3 \quad \dots(2.5.4)$$

- Now by using KCL between nodes 4 and 5, we have

$$\frac{V_{02} - V_5}{Z_4} = \frac{V_5}{Z_5} \quad \dots(2.5.5)$$



**Fig. 2.5.1.** Generalized impedance converter.

6. Substitution for  $V_5 = V_{CC}$  and rearrangements give

$$V_{02} = \frac{V_{CC}(Z_4 + Z_5)}{Z_5} \quad \dots(2.5.6)$$

7. Substituting for  $V_{02}$  from eq. (2.5.6) into eq. (2.5.4), we get

$$(Z_2 + Z_3)V_{CC} = \frac{V_{CC}(Z_4 + Z_5)}{Z_5} Z_2 + V_{01} Z_3 \quad \dots(2.5.7)$$

8. Rearranging eq. (2.5.7), we have

$$V_{CC} \left[ (Z_2 + Z_3) - \frac{(Z_4 + Z_5)}{Z_5} Z_2 \right] = V_{01} Z_3$$

$$V_{CC} \frac{[(Z_2 Z_5 + Z_3 Z_5) - (Z_4 Z_2 + Z_5 Z_2)]}{Z_3 Z_5} = V_{01}$$

$$\text{or, } V_{CC} \frac{Z_3 Z_5 - Z_4 Z_2}{Z_3 Z_5} = V_{01} \quad \dots(2.5.8)$$

9. Substituting for  $V_{01}$  from eq. (2.5.8) into (2.5.1) and simplifying, we obtain

$$I_C Z_1 = V_{CC} \left[ \frac{Z_3 Z_5 - (Z_3 Z_5 - Z_4 Z_2)}{Z_3 Z_5} \right] \quad \dots(2.5.9)$$

10. Rearrangement of eq. (2.5.9) yields the input impedance of the circuit

$$Z = \frac{V_{CC}}{I_C} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \quad \dots(2.5.10)$$

11. Eq. (2.5.10) shows that the circuit shown in Fig. 2.5.1 can be used as grounded impedance whose nature and value depends on the nature and values of impedance elements  $Z_1$  to  $Z_5$ .

**B. Simulation of Inductor :** Refer Q. 2.4, Page 2-5A, Unit-2.

**PART-2**

*Active Analog Filters : Sallen Key Second Order Filter, Designing of Second Order Low and High pass Butterworth Filter.*

**Questions-Answers**

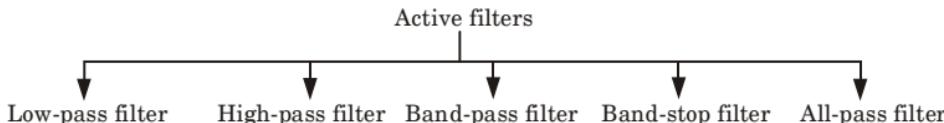
**Long Answer Type and Medium Answer Type Questions**

**Que 2.6.** Classify Active filters and write its advantages.

**Answer**

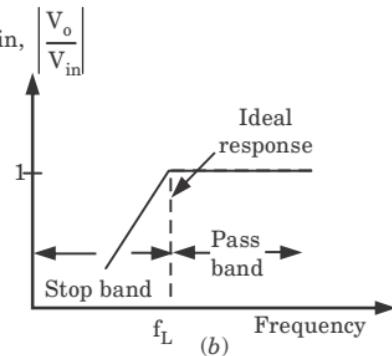
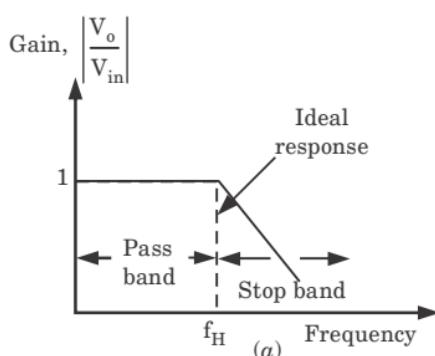
**A. Classification of active filters :**

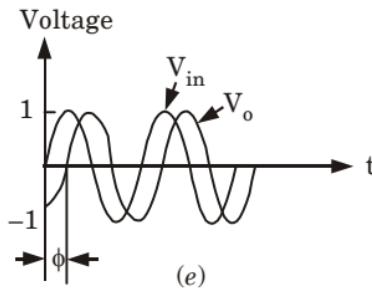
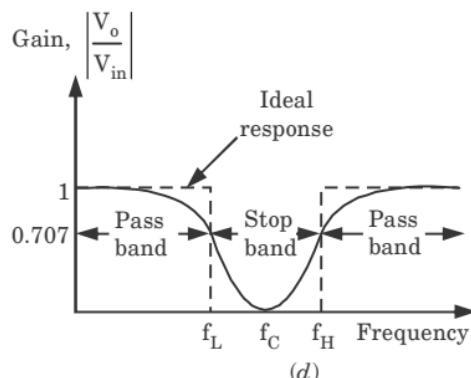
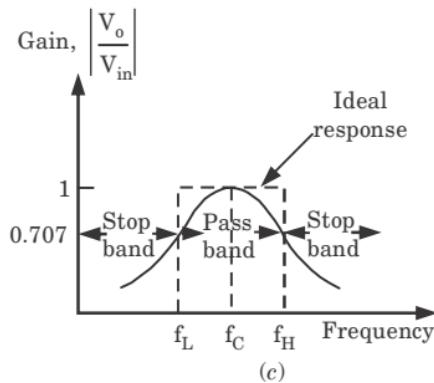
1. Active filters employ transistors or Op-Amps in addition to resistors and capacitors.
2. The type of element used dictates the operating frequency range of the filter. The classification of active filter is shown in Fig. 2.6.1.



**Fig. 2.6.1.**

3. Each of these filters uses an Op-Amp as the active element and resistors and capacitors as the passive elements.





**Fig. 2.6.2.** Frequency response of the major active filters :

(a) Low-pass ; (b) High-pass ; (c) Band-pass ; (d) Band-reject ;  
(e) Phase shift between input and output voltage of an all-pass filter.

4. Fig. 2.6.2 shows frequency response characteristics of the five types of filters. The ideal response is shown by dashed curves, while the solid lines indicate the practical filter response.

#### B. Advantages of active filters :

1. **No loading problem :** The Op-Amp provides a high input resistance and low output resistance. Therefore active filters using Op-Amp do not load the input source or load.
2. **Flexibility in gain and frequency adjustment :** In active filters, the input signal is not attenuated while passing through filter and thus provides flexibility in gain. In addition, the active filter is easy to tune, therefore easy frequency adjustment is possible.
3. **Small component size :** Active filters use components which are smaller in size.
4. **No insertion loss :** The active filters do not exhibit any insertion loss.
5. **Passband gain :** These filters provide some pass band gain.

**Que 2.7.** Compare active filters and passive filter.

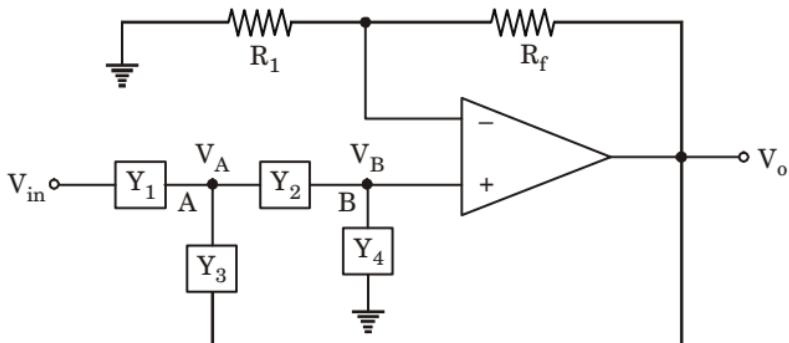
**Answer**

S. No.	<b>Active filter</b>	<b>Passive filter</b>
1.	Active filters have a power gain <i>i.e.</i> , can add energy into the circuit.	Passive filters cannot cause power gain, <i>i.e.</i> , they cannot bring energy into the circuit.
2.	Active filters require an external power supply.	Passive filters do not require any external power.
3.	Active filters have frequency limitation due to active elements.	Passive filters have no frequency limitations.
4.	It provides complex control system and therefore expensive than passive filters.	Passive filters are relatively cheaper than active filters.

**Que 2.8.** Write a short note on Sallen Key second order active filter.

**Answer**

1. A general Sallen-Key structure used for the second order active filters is shown in the Fig. 2.8.1.



**Fig. 2.8.1.**

2. The Op-Amp is used in the non-inverting amplifier mode hence we can write,

$$V_o = V_B \times [\text{Gain}] = V_B A_o$$

where  $A_o = 1 + \frac{R_f}{R_1}$  for non-inverting mode

and  $V_B$  = Voltage at node B

$Y_1, Y_2, Y_3$ , and  $Y_4$  are the admittances of the elements to be connected in the circuit.

## 3. Applying KCL at node A,

$$(V_{in} - V_A) Y_1 - (V_A - V_o) Y_3 - (V_A - V_B) Y_2 = 0$$

where,  $I_{in}$  = Current entering at A =  $(V_{in} - V_A)Y_1$

$I_3$  = Current through  $Y_3$  leaving A =  $(V_A - V_o)Y_3$

$I_2$  = Current through  $Y_2$  leaving A =  $(V_A - V_B)Y_2$

$$\therefore V_{in} Y_1 - V_A(Y_1 + Y_2 + Y_3) + V_B Y_2 + V_o Y_3 = 0 \quad \dots(2.8.1)$$

4. Now current entering at the Op-Amp terminals is zero hence current  $I_2$  flowing through  $Y_2$  flows through  $Y_4$  also.

$$\therefore (V_A - V_B)Y_2 = V_B Y_4$$

$$\therefore V_A = \frac{V_B(Y_2 + Y_4)}{Y_2} = \frac{V_o(Y_2 + Y_4)}{A_o Y_2} \quad \dots(2.8.2)$$

5. Substituting the values of  $V_A$  and  $V_B$  in terms of  $V_o$  in the eq. (2.8.1), we get

$$V_{in} Y_1 - \frac{V_o(Y_2 + Y_4)}{A_o Y_2} (Y_1 + Y_2 + Y_3) + \frac{V_o}{A_o} Y_2 + V_o Y_3 = 0$$

$$\therefore V_{in} Y_1 - V_o \left[ \frac{(Y_1 + Y_2 + Y_3)(Y_2 + Y_4)}{A_o Y_2} - \frac{Y_2}{A_o} - Y_3 \right] = 0$$

$$\therefore V_{in} Y_1 - \frac{V_o[Y_1 Y_2 + Y_2^2 + Y_2 Y_3 + Y_1 Y_4 + Y_2 Y_4 + Y_3 Y_4 - Y_2^2 - A_o Y_2 Y_3]}{A_o Y_2} = 0$$

$$\therefore V_{in} Y_1 = \frac{V_o[Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)]}{A_o Y_2}$$

$$\therefore \frac{V_o}{V_{in}} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)}$$

## 6. This is the voltage gain of a general Sallen-Key structure used for second order active filters.

**Que 2.9.** Write a short note on first order low-pass and high-pass filter.

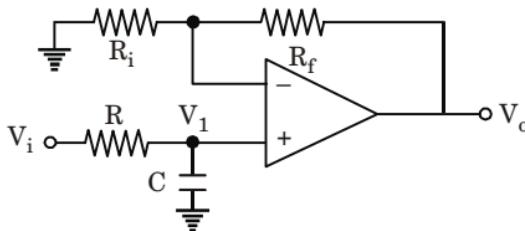
**Answer****A. First order low-pass filter :**

- Fig. 2.9.1 is an active low-pass filter with single  $RC$  network connected to the non-inverting terminal of Op-Amp.
- The input resistor  $R_i$  and feedback resistor  $R_f$  are used to determine the gain of the filter in the passband.
- Referring to Fig. 2.9.1, the voltage  $V_1$  across the capacitor is

$$V_1 = \frac{V_i}{1 + j2\pi f RC}$$

- The output voltage  $V_o$  for non-inverting amplifier is

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_1$$



**Fig. 2.9.1.** First order low-pass filter with variable gain.

5. By substituting  $V_1$  in the above equation, the output voltage  $V_o$  becomes

$$V_o = \left(1 + \frac{R_f}{R_i}\right) \frac{V_i}{1 + j2\pi f RC}$$

or

$$\frac{V_o}{V_i} = \frac{A}{1 + j\left(\frac{f}{f_H}\right)}$$

where  $\frac{V_o}{V_i}$  is the gain of the low-pass filter which is a function of frequency,  $A = 1 + \left(\frac{R_f}{R_i}\right)$  is the passband gain of the filter,  $f_H = \frac{1}{2\pi RC}$  is the high cut-off frequency of the filter.

6. The frequency response of the filter can be determined by using the magnitude of the gain of the low-pass filter, which is expressed as

$$\left| \frac{V_o}{V_i} \right| = \sqrt{\frac{A}{1 + \left(\frac{f}{f_H}\right)^2}}$$

### B. First order high-pass filter :

- The active high-pass filter with a single  $RC$  network connected to non-inverting terminal of the Op-Amps shown in Fig. 2.9.2.
- The input resistor  $R_i$  and feedback resistor  $R_f$  are used to determine the gain of the filter in the pass-band.
- The output voltage  $V_o$  of the first order active high-filter is

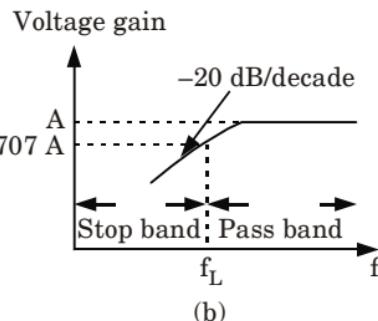
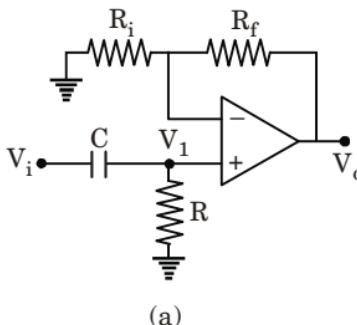
$$V_o = \left(1 + \frac{R_f}{R_i}\right) \frac{j2\pi f RC}{1 + j2\pi f RC} V_i$$

- Therefore, the gain of the filter becomes

$$\frac{V_o}{V_i} = A \left( \frac{j \left( \frac{f}{f_L} \right)}{1 + j \left( \frac{f}{f_L} \right)} \right) \quad \dots(2.9.1)$$

where pass-band gain of the filter is  $A = 1 + \left( \frac{R_f}{R_i} \right)$ ,  $f$  is the frequency of the input signal and the lower cut-off frequency of the filter is

$$f_L = \frac{1}{2\pi RC}$$



**Fig. 2.9.2.** (a) First order active high-pass filter with variable gain,  
(b) Frequency response of an active high-pass filter.

5. The frequency response of the filter is obtained from the magnitude of the filter,

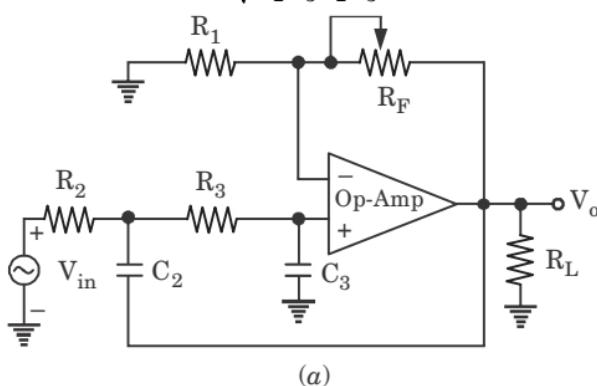
$$\text{That is, } |H(jf)| = \left| \frac{V_o}{V_i} \right| = \frac{A \left( \frac{f}{f_L} \right)}{\sqrt{1 + \left( \frac{f}{f_L} \right)^2}} = \frac{A}{\sqrt{1 + \left( \frac{f}{f_L} \right)^2}}$$

**Que 2.10.** Draw the circuit of second order low-pass filter and find the expression for its cut-off frequency.

### Answer

1. The second order low-pass filter can be obtained simply by inserting an additional  $RC$  network into the first order low pass filter.
2.  $R_2C_2$  is the additional  $RC$  network.
3. The frequency response is shown in Fig. 2.10.1(b). It shows that the response in the stop-band rolls off at a rate of  $-40$  dB/decade. This rate is double the rate of the first order filter. That means second order filters have a sharper frequency response.
4. The resistors  $R_F$  and  $R_1$  will decide the gain of the filter.
5. The cut-off frequency  $f_c$  is determined by  $R_2$ ,  $C_2$ ,  $R_3$  and  $C_3$  as follows :

$$f_c = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$



(a)

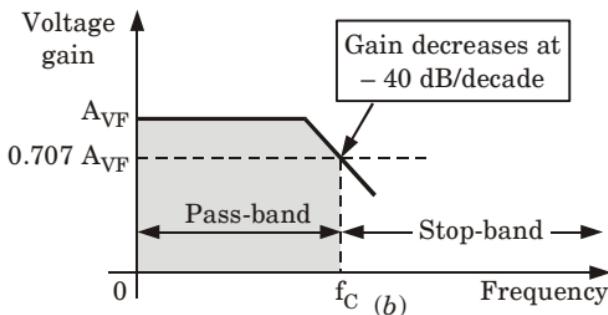


Fig. 2.10.1. (a) Second order low-pass filter (b) Frequency response.

**Que 2.11. Classify active filter. Design second order low pass filter with \$f\_H = 2\$ KHz and passband gain of 3. AKTU 2018-19, Marks 07**

**Answer**

**A. Active filter :** Refer Q. 2.6, Page 2-9A, Unit-2.

**B. Numerical :**

**Given :** Gain = 3, \$f\_H = 2\$ kHz

**To Design :** Second order low-pass filter.

1. Let,                      \$C\_2 = C\_3 = 0.0047 \mu F\$

Then,                      \$R\_2 = R\_3 = \frac{1}{2\pi f\_H C} = \frac{1}{2\pi(2 \times 10^3)(47 \times 10^{-10})}\$  
\$= 16.93 \text{ k}\Omega \approx 17 \text{ k}\Omega\$

2. Voltage gain,              \$A\_{vf} = 1 + \frac{R\_f}{R\_1}\$

$$3 = 1 + \frac{R_f}{R_1}$$

$$\begin{aligned} R_f &= 2R_1 \\ \text{Assuming, } R_1 &= 27 \text{ k}\Omega \end{aligned}$$

$$\therefore R_f = 2 \times 27 = 54 \text{ k}\Omega$$

3. The required circuit shown in Fig. 2.11.1.

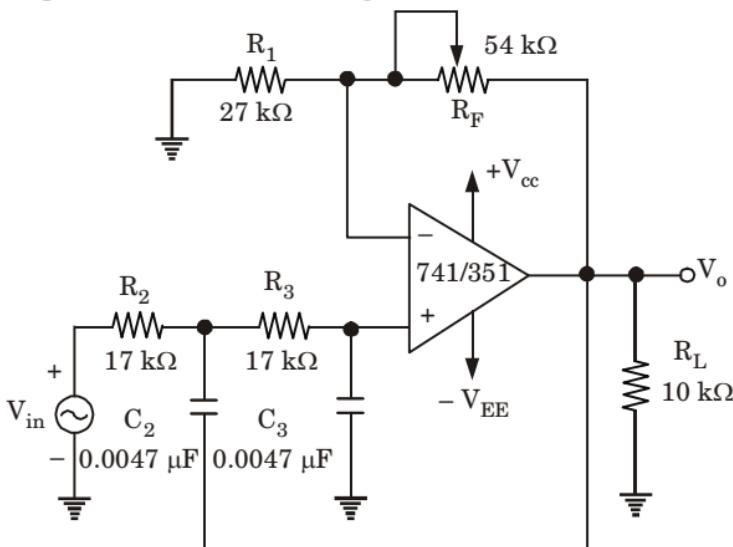


Fig. 2.11.1. Second order low-pass butterworth filter.

**Que 2.12.** Design a 2<sup>nd</sup> order Butterworth high-pass filter with overall passband gain of 3 having corner frequency 2 KHz. Also find and plot the frequency response at 100 Hz, 500 Hz, 1000 Hz, 1500 Hz, 2000 Hz, and 5000 Hz.

### Answer

**Given :** Pass-band gain = 3,  $f_c = 2 \text{ KHz}$

**To Design :** Second order Butterworth high-pass filter.

$$1. \text{ We know, } f_c = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} = \frac{1}{2\pi\sqrt{R^2 C^2}}$$

$$\begin{aligned} \text{Considering, } R_2 &= R_3 = R, C_2 = C_3 = C \text{ and assuming, } C = 0.01\mu\text{F} \\ R &= \frac{1}{2\pi f_c} = \frac{1}{2\pi \times 2000 \times 0.01 \times 10^{-6}} \\ R &= 7.95 \text{ k}\Omega \end{aligned}$$

$$2. \text{ Voltage gain, } A_{vf} = 1 + \frac{R_f}{R_1}$$

$$3 = 1 + \frac{R_f}{R_1} \Rightarrow R_f = 2R_1$$

$$\text{Choose } R_1 = 10 \text{ K}\Omega, R_f = 20 \text{ K}\Omega$$

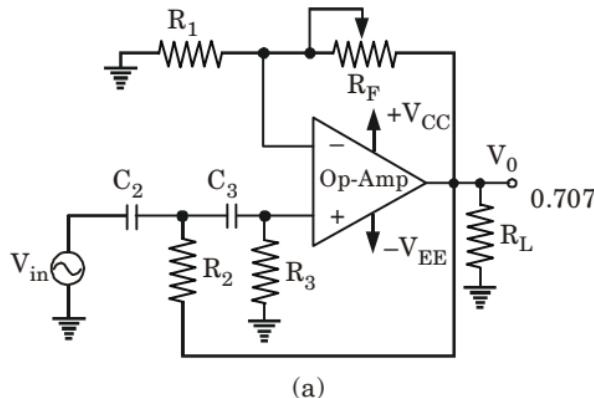
3. To plot frequency response

$$\left| \frac{v_0}{v_{in}} \right| = \frac{A_{vf}}{\sqrt{1 + \left( \frac{f_c}{f} \right)^4}} = \frac{3}{\sqrt{1 + \left( \frac{2000}{f} \right)^4}}$$

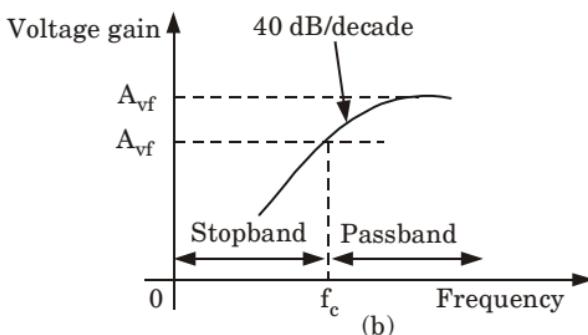
4. Table with  $\left| \frac{v_0}{v_{in}} \right|$  in dB i.e.,  $20 \log \left| \frac{v_0}{v_{in}} \right|$  and frequency with frequency response is shown in Fig. 2.12.1.

**Table 2.12.1.**

$f$ in Hz	$\left  \frac{v_0}{v_{in}} \right $ in dB
100	-42.49
500	-14.55
1000	-2.76
1500	3.25
2000	6.532
5000	9.432



(a)



**Fig. 2.12.1.** (a) Second order high-pass butterworth filter,  
(b) Frequency response.

**Que 2.13.** Compare and contrast active filters and passive filters.

**Design a second order low-pass Butterworth filter to have cut-off frequency of 1 KHz.**

**AKTU 2017-18, Marks 05**

**Answer**

**Comparison :** Refer Q. 2.7, Page 2-10A, Unit-2.

**Numerical :**

**Given :**  $f_H = 1\text{ KHz} = 1/2\pi RC$

**To Design :** Second order low-pass Butterworth filter.

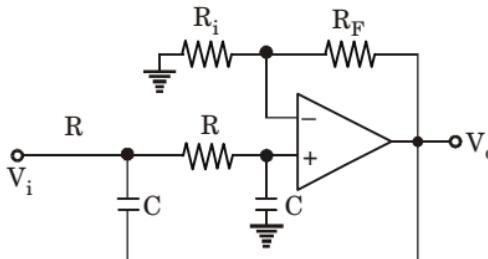
1. Let  $C = 0.1 \mu\text{F}$ , gives the choice of  $R = 1.6 \text{ K}\Omega$ .
2. For  $n = 2$ , the damping factor  $\alpha = 1.414$ . Then the passband gain,  

$$A_o = 3 - \alpha = 3 - 1.414 = 1.586.$$
3. The transfer function of the normalized second order low-pass Butterworth filter is

$$= \frac{1.586}{s_n^2 + 1.414 s_n + 1}$$

Now,

$$A_o = 1 + \frac{R_F}{R_i} = 1.586 = 1 + 0.586$$



**Fig. 2.13.1.** Second order low-pass butterworth filter.

4. Let,  $R_F = 5.86 \text{ K}\Omega$  and  $R_i = 10 \text{ K}\Omega$ . Then, we get  $A_o = 1.586$ .
5. The circuit realized in the Fig. 2.13.1 with component values as  $R = 1.6 \text{ K}\Omega$ ,  $C = 0.1 \mu\text{F}$ ,  $R_F = 5.86 \text{ K}\Omega$  and  $R_i = 10 \text{ K}\Omega$ .
6. For minimum DC offset,  $R_i \parallel R_F = 2R$ , which has not been taken into consideration here, otherwise, we would have to modify the values of  $R$  and  $C$  accordingly which comes out to be  $R = 1.85 \text{ K}\Omega$ ,  $C = 0.086 \mu\text{F}$ ,  $R_F = 5.86 \text{ K}\Omega$ ,  $R_i = 10 \text{ K}\Omega$ .

**PART-3**

*Introduction to Bandpass and Band Stop Filter, All Pass Active Filters, KHN Filters, Introduction to Design of Higher Order Filters.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 2.14.** Explain bandpass filters and its types.

**Answer****A. Bandpass filter :**

1. A bandpass filter passes a particular band of frequencies and attenuates any input frequency outside this pass-band.
2. This filter has a maximum gain at the resonant frequency ( $f_r$ ), which is defined as

$$f_r = \sqrt{f_H f_L}$$

3. The figure of merit or quality factor  $Q$ , is given by

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{B}$$

where  $B$  is bandwidth,  $f_H$  is higher cut-off frequency and  $f_L$  is lower cut-off frequency.

**B. Types :****i. Narrow bandpass filter :**

1. The narrow bandpass filter using one inverting mode Op-Amp with two feedback paths is shown in Fig. 2.14.1(a) and its frequency response is shown in Fig. 2.14.1(b).
2. The resonant frequency can be changed by adjusting  $R_f$  without changing the bandwidth or gain.
3. The bandwidth  $B$  is determined by resistor  $R$  and the two matched capacitors  $C$  as given by

$$B = \frac{0.1591}{RC}$$

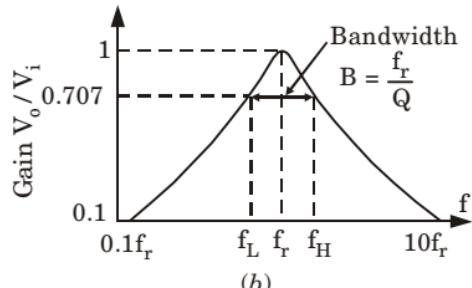
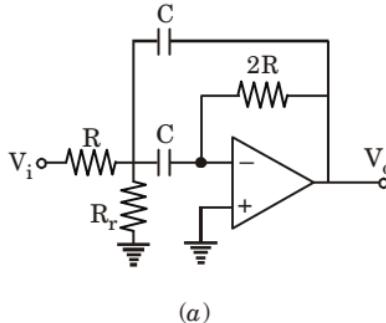
where  $B = f_r/Q$ .

4. The adjustable resistor  $R_r$  is determined by

$$R_r = \frac{R}{2Q^2 - 1}$$

5. Its resonant frequency  $f_r$  is determined from

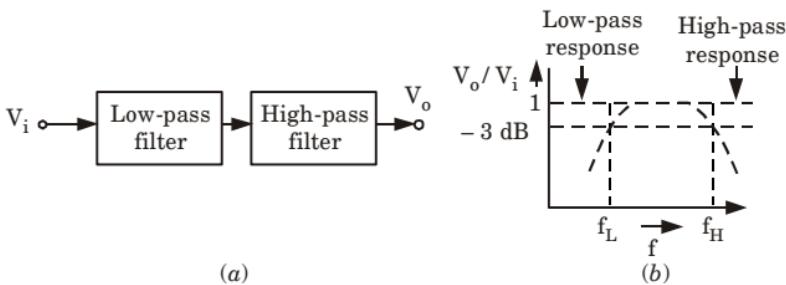
$$f_r = \frac{0.1125}{RC} \sqrt{1 + \frac{R}{R_r}}$$



**Fig. 2.14.1.** (a) Narrow bandpass filter circuit and  
(b) Its frequency response.

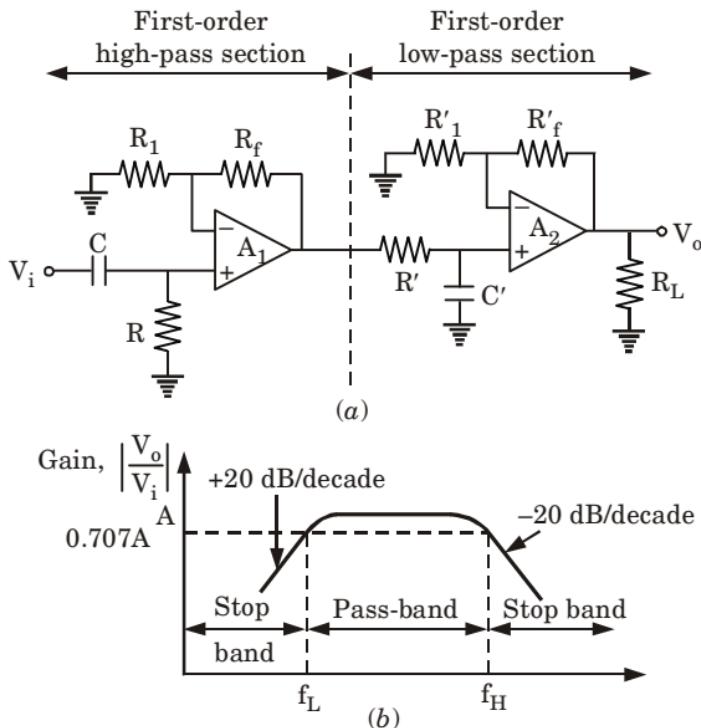
## ii. Wide bandpass filter :

1. A bandpass filter can be constructed simply by connecting low-pass and high-pass filters in cascade as shown in Fig. 2.14.2(a).
2. Here the low-pass circuit will pass all frequencies up to its cut-off frequency  $f_H$ , while the high-pass circuit will block all frequencies below its cut-off frequency  $f_L$  provided  $f_H > f_L$  i.e.,  $f_H$  must be at least 10 times  $f_L$ .
3. The cut-off frequencies of the low and high-pass sections must have the equal passband gain. Hence, the combination gives a filter with passband from  $f_L$  to  $f_H$  as shown in Fig. 2.14.2(b).



**Fig. 2.14.2.** (a) Cascaded low-pass and high-pass filters acting as bandpass filter (b) Frequency response of the bandpass filter.

4. For realizing a ±20 dB/decade bandpass filter, first order high-pass and first order low-pass sections are cascaded as shown in Fig. 2.14.3(a). Its frequency response is shown in Fig. 2.14.3(b).



**Fig. 2.14.3. (a)  $\pm 20$  dB/decade-wide bandpass filter and (b) its frequency response.**

**Que 2.15.** Design a wide bandpass filter with lower cut-off frequency  $f_L = 200$  Hz, higher cut-off frequency  $f_H = 1$  KHz and a pass-band gain = 4.

**AKTU 2016-17, Marks 10**

### Answer

**Given :**  $f_L = 200$  KHz;  $f_H = 1$  KHz;  $A = 4$

**To Design :** Wide bandpass filter.

#### A. Components of the low-pass filter :

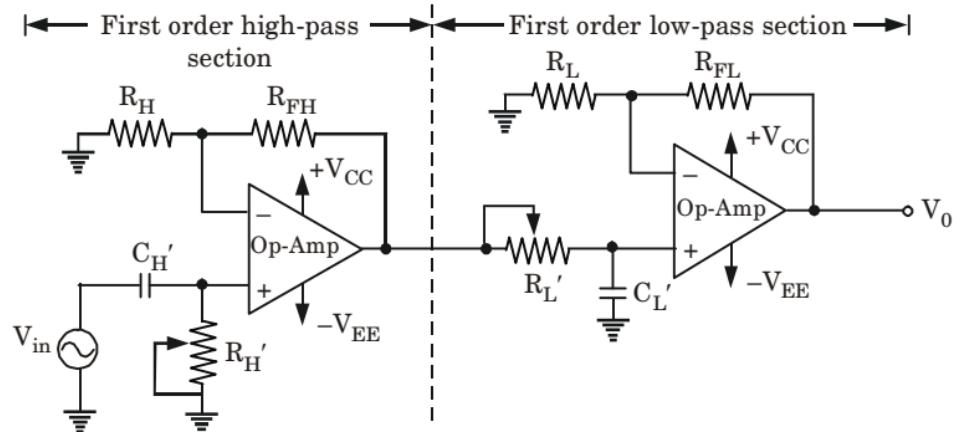
- Let  $C_{L'} = 0.01 \mu\text{F}$
- $R_{L'} = \frac{1}{2\pi f_H C_{L'}} = \frac{1}{2\pi \times 1000 \times 0.01 \times 10^{-6}} = 15.91 \text{ K}\Omega$
- The gain of the low-pass filter can be considered half,  
 $A_{LF} = 2$

$$2 = 1 + \frac{R_{FL}}{R_L}$$

$$R_{FL} = R_L = 10 \text{ K}\Omega \text{ (assume)}$$

**B. Components of the high-pass filter :**1. Let  $C_{H'} = 0.05 \mu\text{F}$ 

$$2. R_{H'} = \frac{1}{2\pi f_L C_{H'}} = \frac{1}{2\pi \times 200 \times 0.05 \times 10^{-6}} \\ R_{H'} = 15.91 \text{ K}\Omega$$

**Fig. 2.15.1**

3. The gain = 2

$$1 + \frac{R_{FH}}{R_H} = 2 \\ R_{FH} = R_H = 10 \text{ K}\Omega \text{ (assume)}$$

$$4. \text{ Quality factor, } Q = \frac{f_c}{f_H - f_L} = \frac{\sqrt{f_H f_L}}{f_H - f_L} \\ = \frac{\sqrt{200 \times 1000}}{800} = 0.56$$

**Que 2.16.** Design a wide bandpass filter with  $f_L = 500 \text{ Hz}$  and  $f_H = 1500 \text{ Hz}$  and passband gain of 5, draw frequency response of the filter and find value of  $Q$ .

**AKTU 2018-19, Marks 10****Answer****Given :**  $f_L = 500 \text{ Hz}$ ;  $f_H = 1500 \text{ Hz}$ ;  $A = 5$ **To Find :**  $Q$ .**A. Components of the low-pass filter :**1. Let  $C_{L'} = 0.01 \mu\text{F}$ 

$$2. R_{L'} = \frac{1}{2\pi f_H C_{L'}} = \frac{1}{2\pi \times 1500 \times 0.01 \times 10^{-6}} = 10.6 \text{ K}\Omega$$

3. The gain of the low-pass filter can be considered half,

$$A_{LF} = 2.5$$

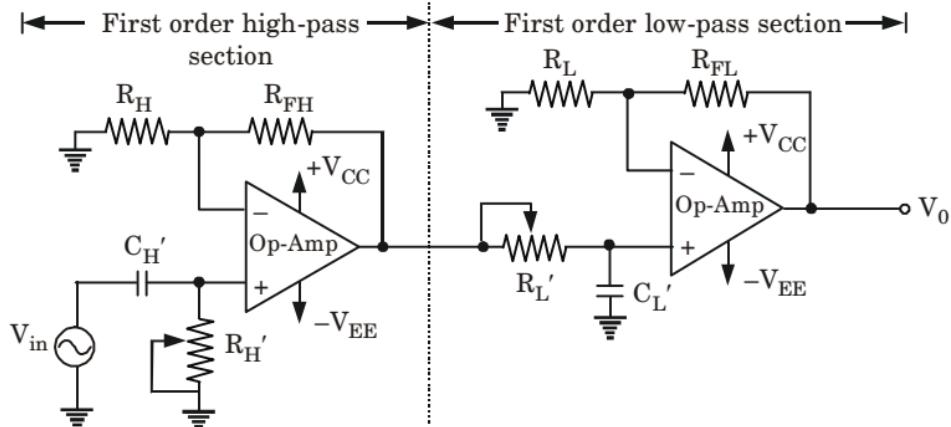
$$2.5 = 1 + \frac{R_{FL}}{R_L}$$

$$R_{FL} = 1.5 R_L$$

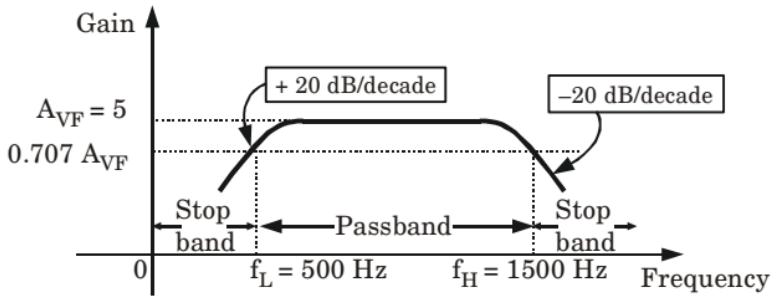
Let we choose  $R_L = 10 \text{ k}\Omega$

$$\therefore R_{FL} = 15 \text{ k}\Omega$$

### B. Components of the high-pass filter :



(a) Wide bandpass filter.



(b) Frequency response of a bandpass filter

**Fig. 2.16.1.**

1. Let

$$C_{H'} = 0.05 \mu\text{F}$$

2.  $\therefore$

$$R_{H'} = \frac{1}{2\pi f_L C_{H'}} = \frac{1}{2\pi \times 500 \times 0.05 \times 10^{-6}}$$

$$R_{H'} = 6.37 \text{ k}\Omega$$

3. The gain = 2.5

$$1 + \frac{R_{FH}}{R_{H'}} = 2.5$$

$$R_{FH} = 1.5 R_{H'}$$

Let we choose

$$R_{H'} = 10 \text{ k}\Omega$$

$$\therefore R_{FH} = 15 \text{ k}\Omega$$

4. Quality factor,  $Q = \frac{f_c}{f_H - f_L} = \frac{\sqrt{f_H f_L}}{f_H - f_L} = \frac{\sqrt{500 \times 1500}}{1000} = 0.866$

**Que 2.17.** Write a short note on band-reject filters.

**OR**

**Draw and explain narrow band-reject filter. Also, find its transfer function.**

**AKTU 2019-20, Marks 07**

**Answer**

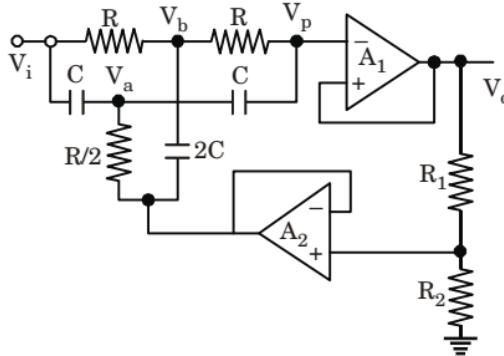
**A. Band-reject filter :**

Band-reject filter, also called as the band-elimination or band-stop filter, attenuates the frequencies in the stopband and passes them outside this band.

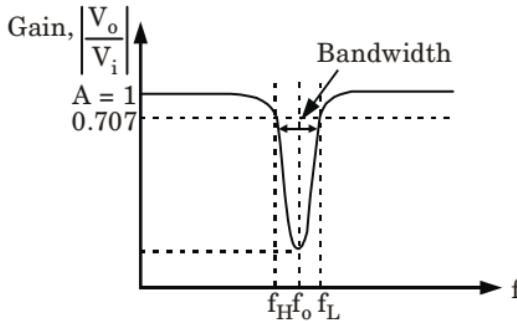
**B. Types :**

**i. Narrow band-reject filter :**

1. The narrow band-reject filter, often called the notch filter, is the twin T network cascaded with the voltage follower as shown in Fig. 2.17.1(a).



(a) Circuit of a narrow band-reject (notch) filter



(b) Its frequency response.

**Fig. 2.17.1.**

2. Applying Kirchhoff's current law at node  $V_a$ , we get  

$$(V_i - V_a)sC + (V_o - V_a)sC + (KV_o - V_a)2G = 0$$

$$sCV_i + (sC + 2KG)V_o = 2(sC + G)V_a$$

...(2.17.1)

where  $K = \frac{R_2}{(R_1 + R_2)}$  and  $G = \frac{1}{R}$

3. Applying Kirchhoff current law at node  $V_b$ , we get

$$(V_i - V_b)G + (V_o - V_b)G + 2(KV_o - V_b)sC = 0$$

$$GV_i + (G + 2KsC)V_o = 2(G + sC)V_b \quad \dots(2.17.2)$$

At node  $V_p$ ,

$$(V_a - V_o)sC + (V_b - V_o)G = 0$$

$$sCV_a + GV_b = (G + sC)V_o \quad \dots(2.17.3)$$

4. From the above three node voltage eq. (2.17.1), (2.17.2) and (2.17.3), the transfer function can be written as

$$\begin{aligned} H(s) &= \frac{V_o(s)}{V_i(s)} = \frac{G^2 + s^2 C^2}{G^2 + S^2 C^2 + 4(1-K)sCG} \\ &= \frac{s^2 + \left(\frac{G}{C}\right)^2}{s^2 + \left(\frac{G}{C}\right)^2 + 4(1-K)s\left(\frac{G}{C}\right)} \end{aligned}$$

5. In the steady-state, that is  $s = j\omega$ ,

$$H(j\omega) = \frac{\omega^2 - \omega_o^2}{\omega^2 - \omega_o^2 - j4(1-K)\omega\omega_o}$$

where  $\omega_o = \frac{G}{C} = \frac{1}{RC}$  or  $f_o = \frac{1}{2\pi RC}$

6. At 3 dB cut-off frequency,

$$|H| = \frac{1}{\sqrt{2}}$$

7. Therefore,  $\omega^2 - \omega_o^2 = \pm 4(1-K)\omega\omega_o$

$$\left(\frac{\omega}{\omega_o}\right)^2 \pm 4(1-K)\left(\frac{\omega}{\omega_o}\right) - 1 = 0$$

8. Upon solving the above quadratic equation, we obtain the upper and lower half power frequencies as,

$$f_H = f_o [\sqrt{1 + 4(1-K)^2} + 2(1-K)]$$

and  $f_L = f_o [\sqrt{1 + 4(1-K)^2} - 2(1-K)]$

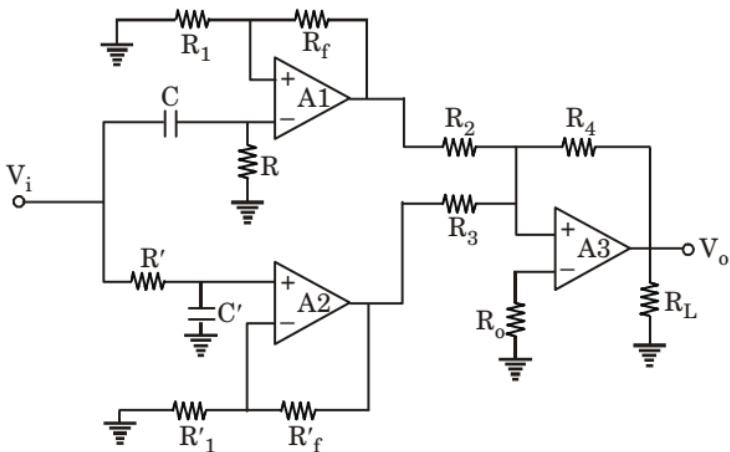
9. The 3 dB bandwidth is

$$B = f_H - f_L = 4(1-K)f_o$$

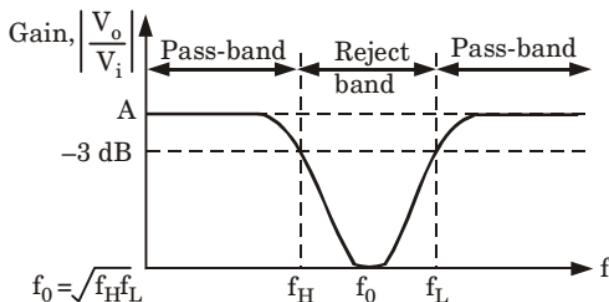
$$Q = \frac{f_o}{B} = \frac{1}{4(1-K)}$$

## ii. Wide band-reject filter :

1. Fig. 2.17.2(a) shows a wide band-reject filter that is obtained by paralleling a high-pass filter with a cut-off frequency of  $f_L$  with a low-pass filter.



(a) Circuit of a wide band-reject filter



(b) Its frequency response

**Fig. 2.17.2.**

- With cut-off frequency of  $f_H$ , provided  $f_L > f_H$  and a summing amplifier connected in series to add the filtered individual passband components.
- The passband gains of both the high-pass and low-pass sections must be equal.
- The frequency response characteristic of the wide band-reject filter is shown in Fig. 2.17.2 (b).

**Que 2.18.** Discuss all-pass filter in brief.

**Answer**

- An all-pass filter passes all frequency components of the input signal without attenuation, while providing predictable phase shifts for different frequencies of the input signal.
- When signals are transmitted over transmission lines, such as telephone wires, they undergo change in phase. To compensate for these phase changes, all-pass filters are required.
- The all-pass filters are also called delay equalizers or phase correctors.
- Fig. 2.18.1(a) shows an all-pass filter wherein  $R_F = R_1$ .

5. The output voltage  $v_o$  of the filter can be obtained by using the superposition theorem,

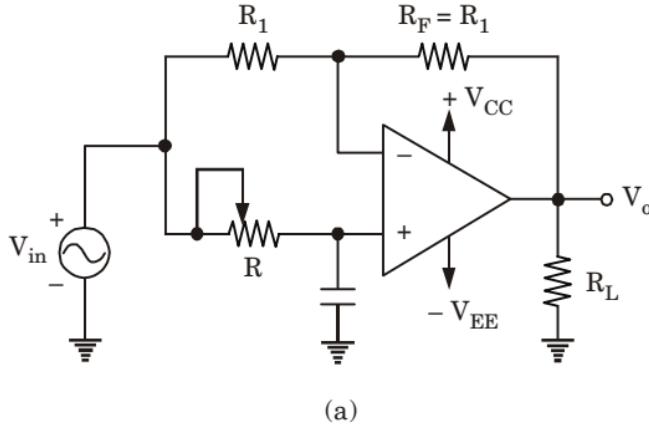
$$v_o = -v_{in} + \frac{-jX_C}{R - jX_C} v_{in} \quad (2) \quad \dots(2.18.1)$$

7. But  $-j = 1/j$  and  $X_C = 1/2\pi fC$ . Therefore, substituting for  $X_C$  and simplifying, we get

$$v_o = v_{in} \left( -1 + \frac{2}{j2\pi fRC + 1} \right)$$

or  $\frac{v_o}{v_{in}} = \frac{1 - j2\pi fRC}{1 + j2\pi fRC} \quad \dots(2.18.2)$

where  $f$  is the frequency of the input signal in hertz.



(a)

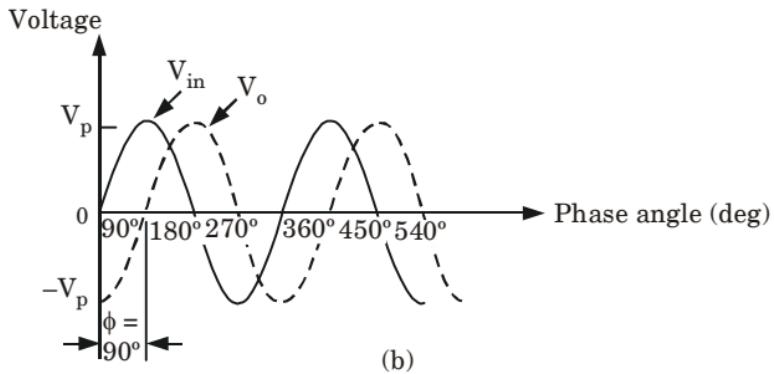


Fig. 2.18.1.

8. Eq. (2.18.2) indicates that the amplitude of  $v_o / v_{in}$  is unity; that is,  $|v_o| = |v_{in}|$  throughout the useful frequency range, and the phase shift between  $v_o$  and  $v_{in}$  is a function of input frequency  $f$ .
9. The phase angle  $\phi$  is given by,

$$\phi = -2 \tan^{-1} \left( \frac{2\pi fRC}{1} \right) \quad \dots(2.18.3)$$

where  $\phi$  in degrees,  $f$  in hertz,  $R$  in ohms, and  $C$  in farads.

10. Eq. (2.18.3) is used to find the phase angle  $\phi$  if  $f$ ,  $R$  and  $C$  are known.
11. Figure 2.18.1(b) shows a phase shift of  $90^\circ$  between the input  $v_{in}$  and output  $v_o$ . That is,  $v_o$  lags  $v_{in}$  by  $90^\circ$ . For fixed values of  $R$  and  $C$ , the phase angle  $\phi$  changes from 0 to  $-180^\circ$  as the frequency  $f$  is varied from 0 to  $\infty$ .
12. In Fig. 2.18.1(b), if the positions of  $R$  and  $C$  are interchanged, the phase shift between input and output becomes positive. That is, output  $v_o$  leads input  $v_{in}$ .

**Que 2.19.** Draw the circuit of KHN filter and derive the expression for its voltage gain.

AKTU 2016-17, Marks 10

**OR**

Derived the expression of voltage gain in KHN Biquad filter. Draw the KHN Biquad filter and derive transfer function of the BPF and LPF from that.

AKTU 2017-18, Marks 10

AKTU 2019-20, Marks 07

### Answer

1. The second order high-pass transfer function is

$$\frac{V_{hp}}{V_i} = \frac{Ks^2}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2} = T_{hp} \quad \dots(2.19.1)$$

where  $K$  is high frequency gain

2. Simplify eq. (2.19.1) and we get,

$$V_{hp} + \frac{1}{Q} \left( \frac{\omega_o}{s} V_{hp} \right) + \left( \frac{\omega_o^2}{s^2} V_{hp} \right) = KV_i \quad \dots(2.19.2)$$

3. The signal  $(\omega_o/s) V_{hp}$  can be obtained by passing  $V_{hp}$  through an integrator with time constant equal to  $1/\omega_o$ .
4. Passing resulting signal through another identical integrator results in the third signal involving  $V_{hp}$  in eq. (2.19.2) and rearranging eq. (2.19.2), we get

$$V_{hp} = KV_i - \frac{1}{Q} \frac{\omega_o}{s} V_{hp} - \frac{\omega_o^2}{s^2} V_{hp} \quad \dots(2.19.3)$$

5. Biquad means the circuit is capable of realizing a biquadratic transfer function.
6. Eq. (2.19.3) can be transfer to block diagram as shown in Fig. 2.19.1.

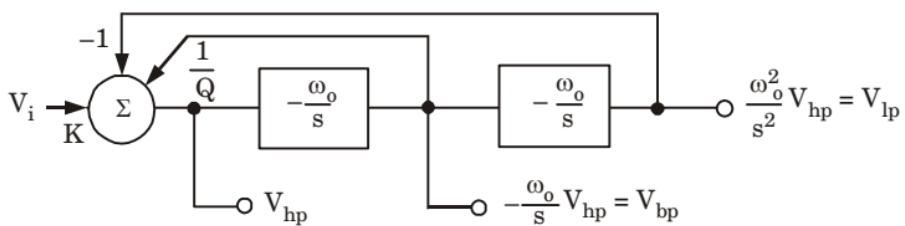


Fig. 2.19.1.

7. The output of second integrator is labeled as  $V_{lp}$  while  $V_{bp}$  for first integrator.

8. Bandpass filter transfer function is given by

$$T_{bp} = \frac{\left(-\frac{\omega_0}{s}\right) V_{hp}}{V_i} \quad \dots(2.19.4)$$

9. Using eq. (2.19.1),  $T_{bp} = \frac{-K\omega_0 s}{s^2 + s(\omega_0/Q) + \omega_0^2}$   $\dots(2.19.5)$

10. Low-pass filter transfer function is given by (using eq. (2.19.1))

$$T_{lp} = \frac{\omega_0^2}{s^2} \frac{V_{hp}}{V_i} = \frac{K\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad \dots(2.19.6)$$

11. To obtain Op-Amp circuit in Fig. 2.19.2, we replace each integrator with Miller integrator circuit having  $CR = 1/\omega$ , also replace summer block with Op-Amp summing circuit.

12. The resulting circuit is known as Kerwin-Huelsman-Newcomb or KHN biquad as shown in Fig. 2.19.2.

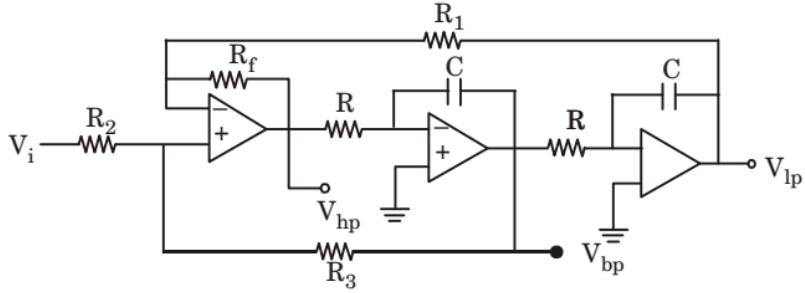


Fig. 2.19.2. KHN biquad filter.

13. Select suitable values of  $C$  and  $R$  of integrator so  $CR = 1/\omega_L$ . For resistors, we use superposition to express the output of summer  $V_{hp}$  in terms of its inputs,

$$V_{bp} = -\left(\frac{\omega_0}{s}\right) V_{hp} \text{ and } V_{lp} = \left(\frac{\omega_0^2}{s^2}\right) V_{hp}$$

as,

$$V_{hp} = \frac{R_3}{R_2 + R_3} \left( 1 + \frac{R_f}{R_1} \right) V_i + \frac{R_2}{R_2 + R_3} \left( 1 + \frac{R_f}{R_1} \right) \left( -\frac{\omega_o}{s} V_{hp} \right) - \frac{R_f}{R_1} \left( \frac{\omega_o^2}{s^2} V_{hp} \right) \quad \dots(2.19.7)$$

14. Equating the last RHS term of eq. (2.19.3) and (2.19.7) gives

$$\frac{R_f}{R_1} = 1$$

15. Now equating second to last terms on RHS of eq. (2.19.3) and (2.19.4) and let  $R_1 = R_f$

$$\frac{R_3}{R_2} = 2Q - 1$$

16. Finally equating coefficients of  $V_i$  in eq. (2.19.3) and (2.19.7) and substituting  $R_f = R_1$  and  $R_2/R_3$

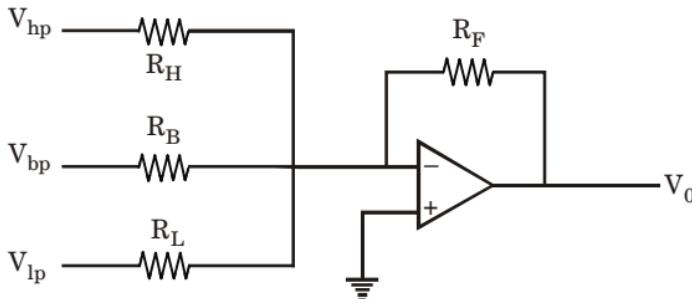
Then,  $K = 2 - \left( \frac{1}{Q} \right)$

17. The KHN biquad can be used to realize notch and all-pass functions by summing weighted versions of the three outputs LP, BP, and HP. Such an Op-Amp summer is shown in Fig. 2.19.3.

18. From Fig. 2.19.3, we can write

$$V_0 = - \left( \frac{R_F}{R_H} V_{hp} + \frac{R_F}{R_B} V_{bp} + \frac{R_F}{R_L} V_{lp} \right) \quad \dots(2.19.8)$$

$$= -V_i \left( \frac{R_F}{R_H} T_{hp} + \frac{R_F}{R_B} T_{bp} + \frac{R_F}{R_L} T_{lp} \right)$$



**Fig. 2.19.3.** Notch and all pass filter using KHN filter.

19. Substituting for  $T_{hp}$ ,  $T_{bp}$ , and  $T_{lp}$  from eq. (2.19.1), (2.19.5) and (2.19.6) give the overall transfer function

$$\frac{V_0}{V_i} = -K \frac{(R_F / R_H)s^2 - s(R_F / R_B)\omega_0 + (R_F / R_L)\omega_0^2}{s^2 + s(\omega_0 / Q) + \omega_0^2}$$

20. To obtain notch function by selecting  $R_B = \infty$

$$\frac{R_H}{R_L} = \left( \frac{\omega_n}{\omega_0} \right)^2$$

**Que 2.20.** Describe the circuit for the KHN filter using three Op-Amp. Design a second order Butterworth low-pass filter having upper cut-off frequency 1 KHz. Determine its frequency response.

AKTU 2015-16, Marks 15

### Answer

**A. KHN filter :** Refer Q. 2.19, Page 2-28A, Unit-2.

**B. Numerical :** Refer Q. 2.13, Page, 2-18A, Unit-2.

**C. Frequency response :**

1. The gain of second order Butterworth filter is given by

$$|T(j\omega)| = \frac{1.586}{\sqrt{1 + \left(\frac{f}{1 \times 10^3}\right)^4}}$$

$$|T(j\omega)|_{dB} = 20 \log \frac{1.586}{\sqrt{1 + \left(\frac{f}{1 \times 10^3}\right)^4}}$$

Input frequency (Hz)	$ T(j\omega) $ dB
10	4.34
100	4.005
1000	0.99 $\approx$ 1
2000	-8.298

2. Frequency response is shown in Fig. 2.20.1.

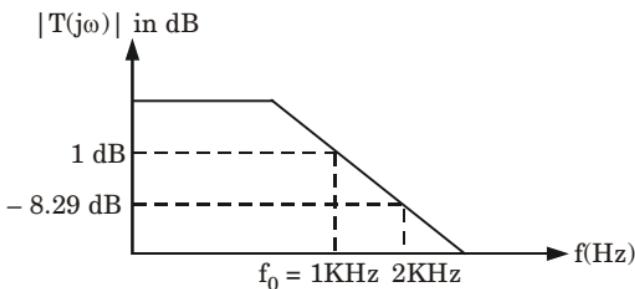


Fig. 2.20.1.

**Que 2.21.** Write a short note on higher-order filter.

**Answer**

1. In the stopband the gain of the filter changes at the rate of 20 dB / decade for first-order filters and at 40 dB/decade for second-order filters. This means that, as the order of the filter is increased, the actual stopband response of the filter approaches its ideal stopband characteristic.

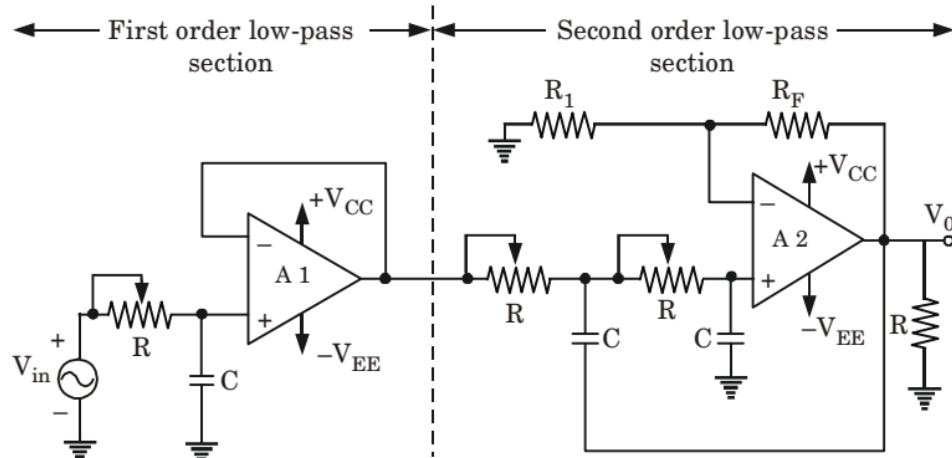


Fig. 2.21.1

2. Higher-order filters, such as third, fourth, fifth, and so on, are formed simply by using the first and second-order filters.

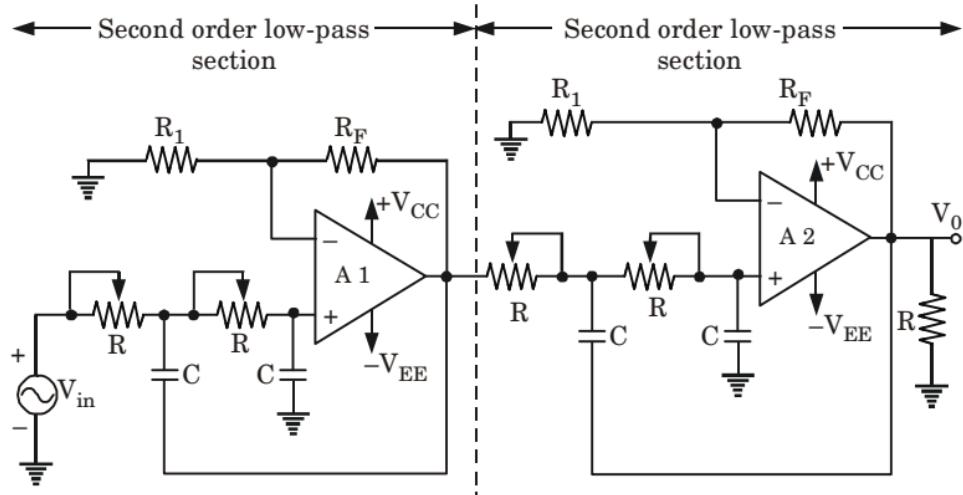


Fig. 2.21.2

For example, a third-order low-pass filter is formed by connecting in series or cascading first-and second-order low-pass filters; a fourth-order low-pass filter is composed of two cascaded second-order low-pass sections, and so on.

3. Although there is no limit to the order of the filter that can be formed, as the order of the filter increases, so does its size.
4. Also, its accuracy declines, in that the difference between the actual stopband response and the theoretical stopband response increases with an increase in the order of the filter.
5. Fig. 2.21.1 shows third and fourth-order low-pass Butterworth filters. In the third-order filter the voltage gain of the first-order section is one and that of the second-order section is two.
6. In the fourth-order the gain of the first section is 1.152 while that of the second section is 2.235. These gain values are necessary to guarantee Butterworth response and must remain the same regardless of the filter's cut-off frequency.
7. Furthermore, the overall gain of the filter is equal to the product of the individual voltage gains of the filter sections.
8. Thus the overall gain of the third-order filters is 2.0, and that of the fourth order filters is  $(1.152)(2.235) = 2.57$ .

**Que 2.22. Derive the output expression for *RC* phase shift oscillator.**

**AKTU 2017-18, Marks 05**

**Answer**

1. The circuit of an *RC* phase shift oscillator is shown in Fig. 2.22.1. The Op-Amp is used in the inverting mode and therefore provides  $180^\circ$  phase shift. The additional phase of  $180^\circ$  is provided by the *RC* feedback network to obtain a total phase shift of  $360^\circ$ .
2. The feedback network consists of three identical *RC* stages. Each of the *RC* stage provides a  $60^\circ$  phase shift so that the total phase shift due to feedback network is  $180^\circ$ .
3. The feedback factor  $\beta$  of the *RC* network can be calculated by writing the KVL equations from Fig. 2.22.2.

$$I_1 \left( R + \frac{1}{sC} \right) - I_2 R = V_0 \quad \dots(2.22.1)$$

$$-I_1 R + I_2 \left( 2R + \frac{1}{sC} \right) - I_3 R = 0 \quad \dots(2.22.2)$$

$$0 - I_2 R + I_3 \left( 2R + \frac{1}{sC} \right) = 6 \quad \dots(2.22.3)$$

and

$$V_f = I_3 R$$

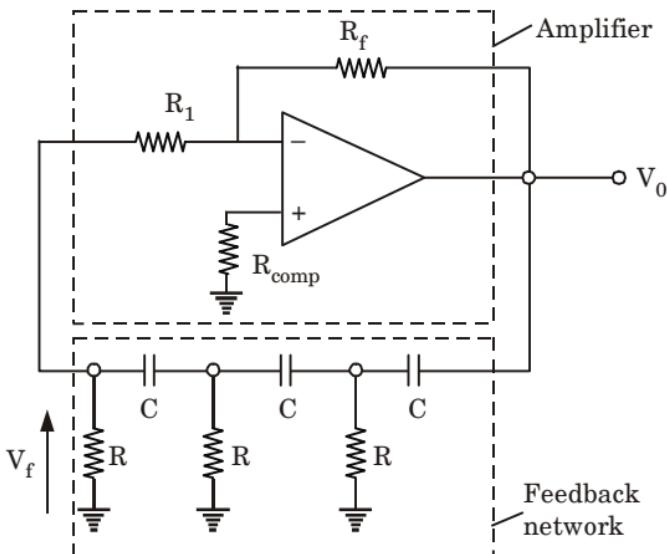
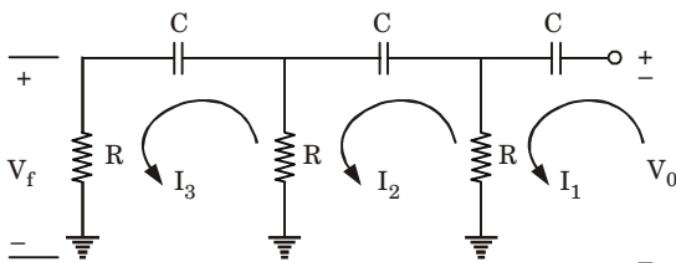


Fig. 2.22.1. Phase shift oscillator.

Fig. 2.22.2. Calculating  $\beta$  from phase shift network.

4. Solving eq. (2.22.1), (2.22.2) and (2.22.3) for  $I_3$ , we get

$$I_3 = \frac{V_0 R^2 s^3 C^3}{1 + 5sRC + 6s^2 C^2 R^2 + s^3 C^3 R^3}$$

and

$$V_f = I_3 R = \frac{V_0 R^3 s^3 C^3}{1 + 5sRC + 6s^2 C^2 R^2 + s^3 C^3 R^3}$$

$$= \frac{1}{1 + \frac{6}{sRC} + \frac{5}{s^2 C^2 R^2} + \frac{1}{s^3 C^3 R^3}}$$

5. Replacing  $s = j\omega$ ,  $s^2 = -\omega^2$  and  $s^3 = -j\omega^3$ , we get

$$\begin{aligned} \beta &= \frac{1}{1 + \frac{6}{j\omega RC} - \frac{5}{\omega^2 R^2 C^2} - \frac{1}{j\omega^3 R^3 C^3}} \\ &= \frac{1}{(1 - 5\alpha^2) + j\alpha(6 - \alpha^2)} \end{aligned} \quad \dots(2.22.4)$$

where,  $\alpha = \frac{1}{\omega RC}$

6. For  $A\beta = 1$ ,  $\beta$  should be real, that is the imaginary term in eq. (2.22.4) must be zero, thus

$$\alpha(6 - \alpha^2) = 0$$

or,  $\alpha^2 = 6$

$$\alpha = \sqrt{6}$$

That is,  $\frac{1}{\omega RC} = \sqrt{6}$

7. The expression for frequency of oscillation,  $f_o$ , is therefore given by

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

8. Putting  $\alpha^2 = 6$  in eq. (2.23.4), we get

$$\beta = -\frac{1}{29}$$

The negative sign indicates that the feedback network produces a phase shift of  $180^\circ$ .

9. So,  $|\beta| = \frac{1}{29}$

Since  $|A\beta| \geq 1$

Therefore, for sustained oscillations,

$$|A| \geq 29$$

10. The gain  $A_v$  is kept greater than 29 to ensure that variations in circuit parameters will not make  $|A_v\beta| < 1$ , otherwise oscillations will die out.

### VERY IMPORTANT QUESTIONS

***Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.***

- Q. 1. Draw and explain I-V and V-I converters and derive its output.**

**Ans.** Refer Q. 2.2.

- Q. 2. Describe the Antoniou inductance simulation circuit with properly labeled circuit diagram and give mathematical expressions in support of your answer.**

**Ans.** Refer Q. 2.4.

**Q. 3. Draw the generalized impedance converter and derive its impedance equation. Also simulate an inductor.**

**Ans.** Refer Q. 2.5.

**Q. 4. Classify active filter. Design second order low pass filter with  $f_H = 2$  KHz and passband gain of 3.**

**Ans.** Refer Q. 2.11.

**Q. 5. Compare and contrast active filters and passive filters. Design a second order Low-Pass Butterworth filter to have cut-off frequency of 1 KHz.**

**Ans.** Refer Q. 2.13.

**Q. 6. Design a Wide Bandpass filter with lower cut-off frequency  $f_L = 200$  Hz, higher cut-off frequency  $f_H = 1$  KHz and a Pass-band gain = 4.**

**Ans.** Refer Q. 2.15.

**Q. 7. Draw and explain narrow band-reject filter. Also, find its transfer function.**

**Ans.** Refer Q. 2.17.

**Q. 8. Derived the expression of voltage gain in KHN Biquad filter. Draw the KHN Biquad filter and derive transfer function of the BPF and LPF from that.**

**Ans.** Refer Q. 2.19.



# 3

UNIT

# Frequency Compensation and Non-Linearity

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- Part-1 :** Frequency Compensation, ..... **3-2A to 3-13A**  
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- Part-2 :** Non-linear Applications of ..... **3-13A to 3-23A**  
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**PART- 1**

*Frequency Compensation, Compensation of Two Stage Op-Amps,  
Slewing in Two Stage Op-Amp, Non-linearity of Differential  
Circuits, Effect of Negative Feedback on Non-linearity.*

**CONCEPT OUTLINE**

- The two types of compensation techniques used in practice are :
  - External frequency compensation
  - Internal frequency compensation.

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 3.1.** What are types of frequency compensation ? Explain any one.

**Answer****Types of Frequency compensation :**

- Internal frequency compensation.

**ii. External frequency compensation :**

- The compensating network is connected externally to the Op-Amp for modifying the response suiting the requirements.

- The compensating network alters the response so that – 20 dB/decade of roll-off rate is achieved over a broad range of frequency.

- The commonly used external compensation methods are :

- Pole-Zero (lag) compensation
- Miller effect compensation

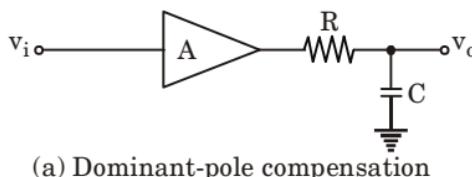
**c. Dominant-Pole compensation :**

- Assume  $A$  is the uncompensated transfer function of an open-loop Op-Amp, whose transfer function is given by

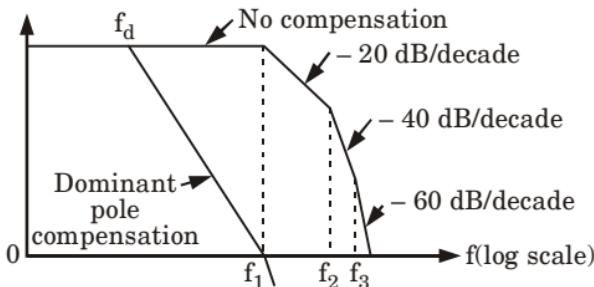
$$A = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)} \quad \dots(3.1.1)$$

where  $0 < \omega_1 < \omega_2 < \omega_3$ .

2. Figure 3.1.1(a) shows a dominant-pole compensation network by adding an  $RC$  network in series with an Op-Amp, or it can be achieved by connecting a capacitor  $C$  at a suitable high resistance node with respect to ground.



(a) Dominant-pole compensation



(b) Gain Vs frequency characteristics for dominant pole compensation.

**Fig. 3.1.1.**

3. Then, the compensated transfer function  $A'$  after compensation is given by

$$A' = \frac{v_o}{v_i} = A_0 \left( \frac{j / j\omega C}{R + \frac{1}{j\omega C}} \right) = \frac{A_0}{1 + j(f / f_d)}$$

where  $f_d = 1/2\pi RC$  is the break frequency of the compensating network.

4. Using eq. (3.1.1), we get the compensated transfer function as

$$A' = \frac{A_0}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

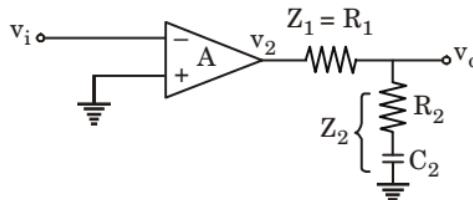
where  $f_d < f_1 < f_2 < f_3$ .

5. The capacitance  $C$  is selected such that, the modified loop gain drops down to 0 dB with a roll-off rate as given by 20 dB/decade at a frequency, where the poles of the uncompensated system transfer function  $A$  contributes negligible phase shift.
6. Normally, the break frequency  $f_d = \omega_d / 2\pi$  is selected so that, the transfer function  $A'$  passes through 0 dB at the pole  $f_1$  of  $A$ . The uncompensated and compensated magnitude plots are shown in Fig. (3.1.1(b)).

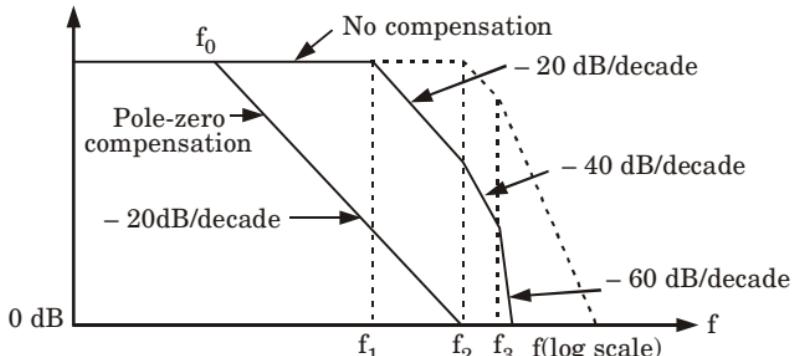
**Que 3.2.** Explain pole-zero compensation method.

**Answer**

1. In this method, both pole and zero are added to the uncompensated transfer function  $A$ .
2. Figure 3.2.1(a) shows the circuit arrangement of the pole-zero compensation method. The zero is added at a higher frequency than the pole.



(a) Pole-zero compensation



(a) Its open-loop Vs frequency response

**Fig. 3.2.1.**

3. The transfer function of the compensation network is given by,

$$\frac{v_o}{v_2} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2 + \frac{1}{jX_{C_2}}}{R_1 + R_2 + \frac{1}{jX_{C_2}}}$$

where,

$$Z_1 = R_1 \text{ and}$$

$$Z_2 = R_2 + \frac{1}{j\omega C_2}$$

i.e.,

$$\frac{v_o}{v_2} = \frac{1 + j\omega R_2 C_2}{1 + j\omega(R_1 + R_2)C_2} = \frac{1 + \left(j\frac{f}{f_1}\right)}{1 + \left(j\frac{f}{f_0}\right)}$$

where,

$$f_1 = \frac{1}{2\pi R_2 C_2} \text{ and}$$

$$f_0 = \frac{1}{2\pi(R_1 + R_2)C_2}$$

4. The compensating network introduces a zero at the first corner frequency  $f_1$  of uncompensated transfer function represented by  $A'$ , which cancels the effect of pole at  $f_1$ .
5. The pole of the compensation network at  $f_0$  given as  $\omega_0/2\pi$  is selected such that the compensated transfer function  $A'$  passes through 0 dB at the second corner frequency  $f_2$ . This is shown in Fig. 3.2.1(b) graphically by having  $A'$  passing through 0 dB at frequency  $f_2$  with a slope of -20 dB/decade.
6. The overall transfer function of the amplifier with compensation network is given by

$$\begin{aligned} A' &= \frac{v_o}{v_i} = \frac{v_o}{v_2} \times \frac{v_2}{v_i} \\ &= \frac{\left(1 + j\frac{f}{f_1}\right)}{\left(1 + j\frac{f}{f_0}\right)} \times \frac{A_0}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \end{aligned}$$

Therefore,

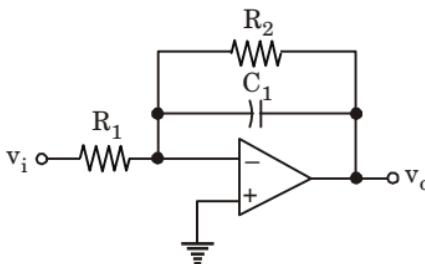
$$A' = \frac{A_0}{\left(1 + j\frac{f}{f_0}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

where  $0 < f_0 < f_2 < f_3$ .

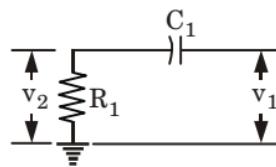
### Que 3.3. | Discuss Miller effect compensation method in brief.

#### Answer

1. Figure 3.3.1(a) shows the Op-Amp inverting amplifier with capacitor  $C_1$  connected in parallel with the feedback resistor  $R_2$ .



(a) Inverting amplifier with miller capacitor.



(b) Phase lead network of the compensated Op-Amp

**Fig. 3.3.1.**

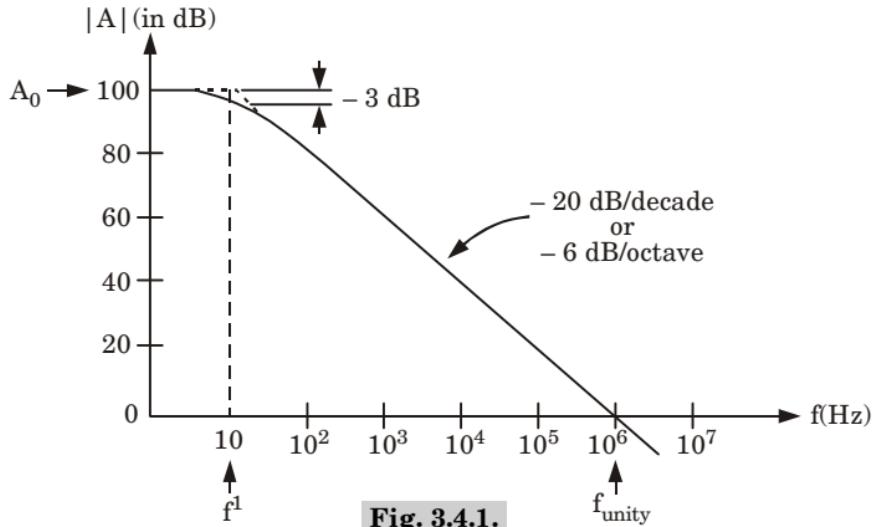
2. The combination of  $C_1$  and  $R_1$  behaves as phase-lead network in the feedback loop of Op-Amp as shown in Fig. 3.3.1(b).

3. Thus,  $C_1$  and  $R_1$  introduce a phase lead to cancel some amount of phase lag in the loop.

**Que 3.4.** Write a short note on internal frequency compensation.

**Answer**

1. Broad bandwidth may not be the only criterion required in some applications like instrumentation. In such cases, internally compensated Op-Amps called compensated Op-Amps can be employed. They are found to be stable regardless of the value of closed-loop gain and without any external compensation methods.
2. The frequency response of  $\mu$ A741 Op-Amp which is internally compensated is reproduced in Fig. 3.4.1.



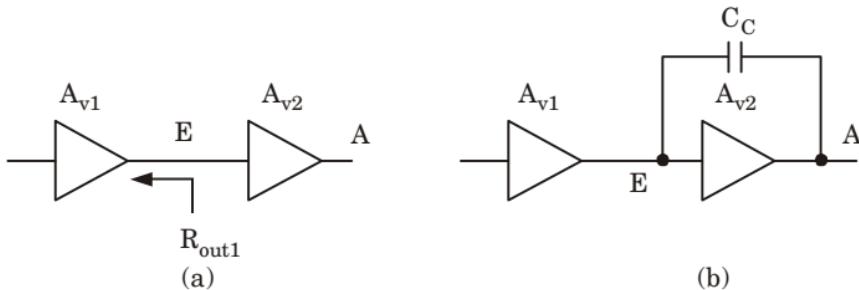
**Fig. 3.4.1.**

3. The Op-Amp 741 internally contains a capacitance of 30 pF that shunts OFF the signal current at higher frequencies, leading to decrease in output signal.
4. This internal compensating capacitor causes the open-loop gain to roll-off at  $-20 \text{ dB/decade}$  rate that assures a stable characteristic for the circuit.
5. The Op-Amp 741 has a gain-bandwidth (GBW) product of 1 MHz. This represents that the product of gain and frequency at any point on the open loop gain Vs frequency curve is 1 MHz.
6. If the Op-Amp is connected for a gain of 60 dB, or  $10^3$ , then the bandwidth obtainable is 1 KHz. For a gain of 10, the bandwidth increases to 100 KHz.

**Que 3.5.** Explain miller compensation of two stage Op-Amp.

## Answer

1. In Fig. 3.5.1(a), the first stage exhibits high output impedance and the second stage provides a moderate gain, thereby providing a suitable environment for Miller multiplication of capacitors.
  2. As shown in Fig. 3.5.1(b), the idea is to create a large capacitance at node  $E$ , equal to  $(1 + A_{v2}) C_C$ , moving the corresponding pole to  $R_{out1}^{-1} [C_E + (1 + A_{v2})C_C]^{-1}$ , where  $C_E$  denotes the capacitance at node  $E$  before  $C_C$  is added.
  3. As a result, a low frequency pole can be established with a moderate capacitor value, saving considerable chip area. This technique is called “Miller compensation”.



**Fig. 3.5.1.** Miller compensation of a two-stage Op-Amp.

4. In addition to lowering the required capacitor value, Miller compensation entails a very important property : it moves the output pole away from the origin.

### Que 3.6.

**Write a short note on slewing in two stage Op-Amp.**

## Answer

1. In Fig. 3.6.1(a)  $V_{in}$  experiences a large positive step at  $t = 0$ , turning OFF  $M_2$ ,  $M_4$ , and  $M_3$ .
  2. The circuit can be simplified to that in Fig. 3.6.1(b), revealing that  $C_C$  is charged by a constant current  $I_{SS}$  if parasitic capacitances at node  $X$  are negligible.
  3. Recognizing that the gain of the output stage makes node  $X$  a virtual ground, we write :  $V_{out} \approx I_{SS}t/C_C$ .
  4. Thus, the positive slew rate equals  $I_{SS}/C_C$ . During slewing,  $M_5$  must provide two currents :  $I_{SS}$  and  $I_1$ .
  5. If  $M_5$  is not wide enough to sustain  $I_{SS} + I_1$  in saturation, then  $V_X$  drops significantly, possibly driving  $M_1$  into the triode region.
  6. For the negative slew rate, we simplify the circuit as shown in Fig. 3.6.1(c). Here  $I_1$  must support both  $I_{SS}$  and  $I_{D5}$ . For example, if  $I_1 = I_{SS}$ , then  $V_X$  rises so as to turn OFF  $M_5$ . If  $I_1 < I_{SS}$ , then  $M_3$  enters the triode region and the slew rate is given by  $I_{D3}/C_C$ .

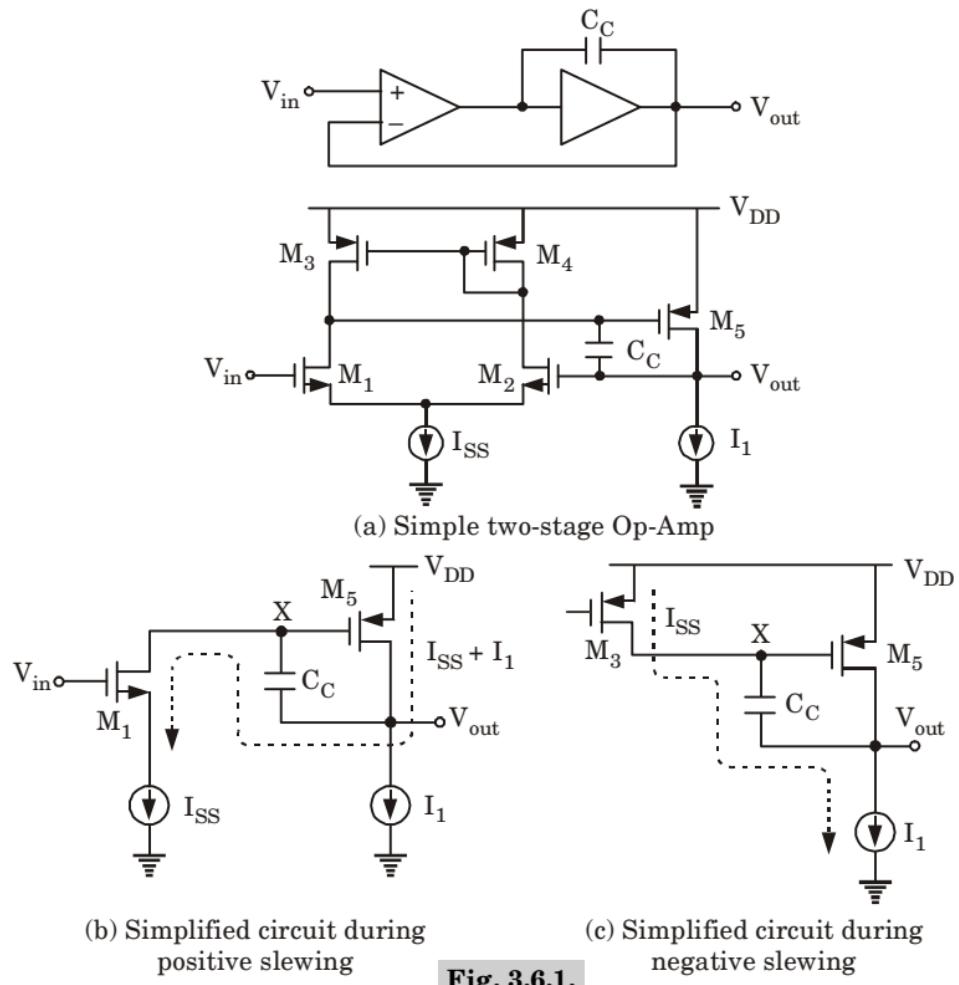


Fig. 3.6.1.

**Que 3.7.** The input/output characteristic of a differential amplifier is approximated as  $y(t) = \alpha_1 x(t) + \alpha_3 x^3(t)$ . Calculate the maximum non-linearity if the input range is from  $-x_{max}$  to  $x_{max}$ .

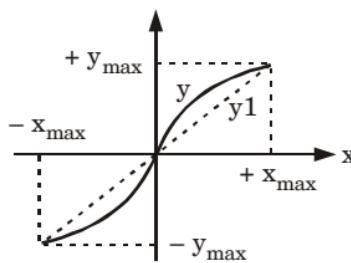


Fig. 3.7.1.

**Answer**

1. The polynomial equation is

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \dots \quad \dots(3.7.1)$$

2. As shown in Fig. 3.7.1, we can express the straight line passing through the end points as

$$\begin{aligned} y_1 &= \frac{\alpha_1 x_{\max} + \alpha_3 x_{\max}^3}{x_{\max}} x \\ &= (\alpha_1 + \alpha_3 x_{\max}^2) x \end{aligned}$$

3. The difference between  $y$  and  $y_1$  is therefore equal to

$$\Delta y = y - y_1$$

$$= \alpha_1 x + \alpha_3 x^3 - (\alpha_1 + \alpha_3 x_{\max}^2) x$$

$$\Delta y = \alpha_3 x^3 - \alpha_3 x_{\max}^2 x$$

4. Taking derivative with respect to  $x$  then we get

$$\frac{d \Delta y}{dx} = 3\alpha_3 x^2 - \alpha_3 x_{\max}^2$$

5. Putting  $\frac{d \Delta y}{dx} = 0$  then we get,

$$x = x_{\max} / \sqrt{3}$$

6. The maximum deviation is equal to  $2\alpha_3 x_{\max}^3 / (3\sqrt{3})$ . Normalized to the maximum output, the non-linearity is obtained as

$$\frac{\Delta y}{y_{\max}} = \frac{2\alpha_3 x_{\max}^3}{3\sqrt{3} \times 2(\alpha_1 x_{\max} + \alpha_3 x_{\max}^3)}$$

7. The maximum peak-to-peak output swing is equal to  $2(\alpha_1 x_{\max} + \alpha_3 x_{\max}^3)$ .

For small non-linearities, we can neglect  $\alpha_3 x_{\max}^3$  with respect to  $\alpha_1 x_{\max}$ , arriving at

$$\frac{\Delta y}{y_{\max}} \approx \frac{\alpha_3}{3\sqrt{3}\alpha_1} x_{\max}^2$$

8. The relative non-linearity is proportional to the square of the maximum input.

9. The non-linearity of a circuit can also be characterized by applying a sinusoid at the input and measuring the harmonic content of the output.

10. If  $x(t) = A \cos \omega t$ , then eq. (3.7.1) becomes,

$$y(t) = \alpha_1 A \cos \omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 \cos^3 \omega t + \dots$$

$$= \alpha_1 A \cos \omega t + \frac{\alpha_2 A^2}{2} [1 + \cos(2\omega t)] + \frac{\alpha_3 A^3}{4} [3 \cos \omega t + \cos(3\omega t)] + \dots$$

11. We observe that higher-order terms yield higher harmonics. In particular, even-order terms and odd-order terms result in even and odd harmonics, respectively. The magnitude of the  $n^{\text{th}}$  harmonic grows roughly in proportion to the  $n^{\text{th}}$  power of the input amplitude.

**Que 3.8.** Write a short note on non-linearity of differential circuits.

**Answer**

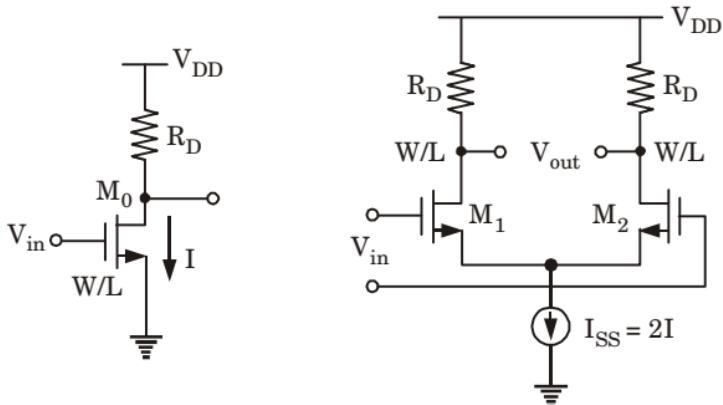
- Differential circuits exhibit an “odd-symmetric” input/output characteristic, i.e.,  $f(-x) = -f(x)$ . And the polynomial equation is

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \dots \quad \dots(3.8.1)$$

- For the polynomial of eq.(3.8.1) to be an odd function, all of the even-order terms, must be zero :

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) + \alpha_5 x^5(t) + \dots \quad \dots(3.8.2)$$

- Eq.(3.8.2) indicating that a differential circuit driven by a differential signal produces no even harmonics. This is another very important property of differential operation.



**Fig. 3.8.1.** Single ended and differential amplifiers providing the same voltage gain.

- In order to appreciate the reduction of non-linearity obtained by differential operation, let us consider the two amplifiers shown in Fig. 3.8.1, each of which is designed to provide a small-signal voltage gain of

$$|A_v| \approx g_m R_D \quad \dots(3.8.3)$$

$$= \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) R_D \quad \dots(3.8.4)$$

- Suppose a signal  $V_m \cos \omega t$  is applied to each circuit. Examining only the drain currents for simplicity, we can write for the common-source stage :

$$\begin{aligned}
 I_{D0} &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH} + V_m \cos \omega t)^2 \\
 &= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 + \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_m \cos \omega t \\
 &\quad + \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_m^2 \cos^2 \omega t \\
 &= I + \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_m \cos \omega t + \frac{1}{4} \mu_n C_{ox} \frac{W}{L} V_m^2 [1 + \cos(2\omega t)]
 \end{aligned} \quad \dots(3.8.5)$$

6. Thus, the amplitude of the second harmonic,  $A_{HD2}$ , normalized to that of the fundamental,  $A_F$ , is

$$\frac{A_{HD2}}{A_F} = \frac{V_m}{4(V_{GS} - V_{TH})} \quad \dots(3.8.6)$$

7. On the other hand, for  $M_1$  and  $M_2$  in Fig. 3.8.1, we have

$$I_{D1} - I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{in} \sqrt{\frac{4I_{SS}}{W} - V_{in}^2} \quad \dots(3.8.7)$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{in} \sqrt{4(V_{GS} - V_{TH})^2 - V_{in}^2} \quad \dots(3.8.8)$$

8. If  $|V_{in}| \ll V_{GS} - V_{TH}$ , then

$$I_{D1} - I_{D2} = \mu_n C_{ox} \frac{W}{L} V_{in} (V_{GS} - V_{TH}) \sqrt{1 - \frac{V_{in}^2}{4(V_{GS} - V_{TH})^2}} \quad \dots(3.8.9)$$

$$\approx \mu_n C_{ox} \frac{W}{L} V_{in} (V_{GS} - V_{TH}) \left[ 1 - \frac{V_{in}^2}{8(V_{GS} - V_{TH})^2} \right] \quad \dots(3.8.10)$$

$$= \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \left[ V_m \cos \omega t - \frac{V_m^3 \cos^3 \omega t}{8(V_{GS} - V_{TH})^2} \right] \quad \dots(3.8.11)$$

9. Since  $\cos^3 \omega t = [3 \cos \omega t + \cos(3\omega t)]/4$ , we obtain

$$I_{D1} - I_{D2} = \left[ V_m - \frac{3V_m^3}{32(V_{GS} - V_{TH})^2} \right] \cos \omega t - g_m \frac{V_m^3 \cos(3\omega t)}{32(V_{GS} - V_{TH})^2} \quad \dots(3.8.10)$$

10. If  $V_m \gg 3V_m^3/[8(V_{GS} - V_{TH})^2]$ , then

$$\frac{A_{HD3}}{A_F} \approx \frac{V_m^2}{32(V_{GS} - V_{TH})^2} \quad \dots(3.8.11)$$

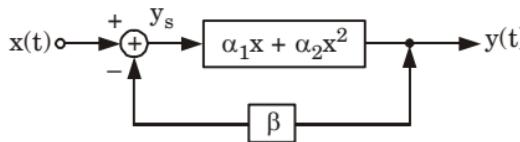
11. Comparison of eq. (3.8.8) and eq. (3.8.9) indicates that the differential circuit exhibits much less distortion than its single-ended counterpart while providing the same voltage gain and output swing.

For example, if  $V_m = 0.2(V_{GS} - V_{TH})$ , eq. (3.8.10) and eq. (3.8.11) yield a distortion of 5% and 0.125 %, respectively.

**Que 3.9. What is the effect of negative feedback on non-linearity ?**

**Answer**

1. We observed that negative feedback makes the closed-loop gain relatively independent of the Op-Amp's open-loop gain.
2. Since non-linearity can be viewed as variation of the small-signal gain with the input level, we expect that negative feedback suppresses this variation as well, yielding higher linearity for the closed-loop system.



**Fig. 3.9.1.** Feedback system incorporating a non-linear feedforward amplifier.

3. Let us assume that the core amplifier in the system of Fig. 3.9.1 has an input-output characteristic  $y \approx \alpha_1x + \alpha_2x^2$ .
4. We apply a sinusoidal input  $x(t) = V_m \cos \omega t$ , postulating that the output contains a fundamental component and a second harmonic and hence can be approximated as  $y \approx a \cos \omega t + b \cos 2\omega t$ .
5. The output of the subtractor can be written as,

$$y_s = x(t) - \beta y(t) \quad \dots(3.9.1)$$

$$= V_m \cos \omega t - \beta(a \cos \omega t + b \cos 2\omega t) \quad \dots(3.9.2)$$

$$= (V_m - \beta a) \cos \omega t - \beta b \cos 2\omega t \quad \dots(3.9.3)$$

6. This signal experiences the non-linearity of the feed forward amplifier, thereby producing an output given by

$$y(t) = \alpha_1[(V_m - \beta a) \cos \omega t - \beta b \cos 2\omega t] + \alpha_2[(V_m - \beta a) \cos \omega t - \beta b \cos 2\omega t]^2 \quad \dots(3.9.4)$$

$$= [\alpha_1(V_m - \beta a) - \alpha_2(V_m - \beta a)\beta b] \cos \omega t$$

$$+ \left[ -\alpha_1\beta b + \frac{\alpha_2(V_m - \beta a)^2}{2} \right] \cos 2\omega t + \dots \quad \dots(3.9.5)$$

7. The coefficients of  $\cos \omega t$  and  $\cos 2\omega t$  in eq. (3.9.5) must be equal to  $a$  and  $b$ , respectively :

$$a = (\alpha_1 - \alpha_2\beta b)(V_m - \beta a) \quad \dots(3.9.6)$$

$$b = -\alpha_1\beta b + \frac{\alpha_2(V_m - \beta a)^2}{2} \quad \dots(3.9.7)$$

8. The assumption of small non-linearity implies that both  $\alpha_2$  and  $b$  are small quantities, yielding  $a \approx \alpha_1(V_m - \beta a)$  and hence

$$a = \frac{\alpha_1}{1 + \beta\alpha_1} V_m \quad \dots(3.9.8)$$

which is to be expected because  $\beta\alpha_1$  is the loop gain. To calculate  $b$ , we write

$$V_m - \beta a \approx \frac{a}{\alpha_1} \quad \dots(3.9.9)$$

thus expressing (3.9.7) as

$$b = -\alpha_1 \beta b + \frac{1}{2} \alpha_2 \left( \frac{a}{\alpha_1} \right)^2$$

That is  $b(1 + \alpha_1 \beta) = \frac{\alpha_2}{2} \left( \frac{a}{\alpha_1} \right)^2$

$$= \frac{\alpha_2}{2\alpha_1^2} \frac{\alpha_1^2}{(1 + \beta\alpha_1)^2} V_m^2$$

It follows that  $b = \frac{\alpha_2 V_m^2}{2} \frac{1}{(1 + \beta\alpha_1)^3}$

9. For a meaningful comparison, we normalize the amplitude of the second harmonic to that of the fundamental :

$$\frac{b}{a} = \frac{\alpha_2 V_m}{2} \frac{1}{\alpha_1} \frac{1}{(1 + \beta\alpha_1)^2}$$

10. Without feedback, on the other hand, such a ratio would be equal to  $(\alpha_2 V_m^2/2)/\alpha_1 V_m = \alpha_2 V_m/(2\alpha_1)$ . Thus, the relative magnitude of the second harmonic has dropped by a factor of  $(1 + \beta\alpha_1)^2$ .
11. Negative feedback therefore reduces the relative second harmonic by a factor of  $(1 + \beta\alpha_1)^2$  and the gain by  $1 + \beta\alpha_1$ .

## PART-2

*Non-linear Applications of IC Op-Amps : Basic Log-Antilog Amplifiers using Diode and BJT, Temperature Compensated Log-Antilog Amplifier using Diode, Peak Detector, Sample and Hold Circuits.*

### Questions-Answers

### Long Answer Type and Medium Answer Type Questions

**Que 3.10.** Write a short note on logarithmic amplifier with its mathematical expression.

**Answer**

1. A fundamental log amplifier is formed by placing a transistor in negative feedback path of Op-Amp as shown in Fig. 3.10.1.

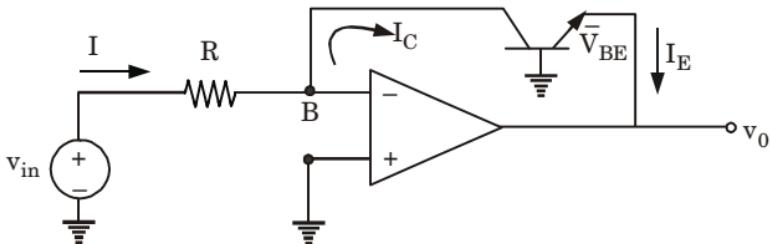


Fig. 3.10.1.

2. The node  $B$  is at virtual ground hence  $V_B = 0$ . The current through resistor  $R$  can be written as

$$I = \frac{v_{in} - V_B}{R} = \frac{v_{in}}{R} \quad \dots(3.10.1)$$

$$I = I_C = I_E = \frac{v_{in}}{R} \quad \dots(3.10.2)$$

3. At the Op-Amp input current is zero

$$I = I_C = \text{Collector current} \quad \dots(3.10.3)$$

4. The voltage  $V_{CB} = 0$  as the collector is at virtual ground and base is grounded. Hence, we can write the equation of  $I_C$  as,

$$I_C = I_E = I_S (e^{V_{BE}/V_T}) \quad \dots(3.10.4)$$

5. Take natural log on both sides of eq. (3.10.4)

$$V_{BE} = V_T \ln \left( \frac{I_E}{I_S} \right) \quad \dots(3.10.5)$$

6. Substitute the eq. (3.10.2) in eq. (3.10.5), we get

$$V_{BE} = V_T \ln \left( \frac{v_{in}}{I_S R} \right) = V_T \ln \left( \frac{v_{in}}{v_{REF}} \right) \quad \dots(3.10.6)$$

where  $v_{ref} = I_s R$  and the output is same as  $V_{BE}$

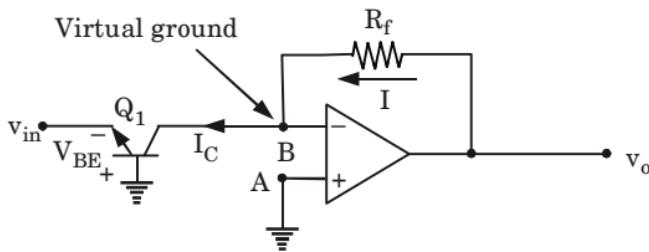
$$\therefore v_0 = -V_{BE}$$

$$v_0 = -V_T \ln \left( \frac{v_{in}}{v_{REF}} \right) \quad \dots(3.10.7)$$

**Que 3.11.** Draw the circuit for anti-log amplifier and derive the expression.

**Answer**

1. Fig. 3.11.1, shows the anti-log amplifier using transistor,

**Fig. 3.11.1.** Basic Anti-log amplifier circuit.

2. The node  $B$  is at a virtual ground hence  $V_B = 0$ . Thus both collector and base of the transistor are at ground potential and  $V_{CB} = 0$ . Hence the voltage across the transistor is  $V_{BE}$  and  $I_C$  can be written as

$$I_C = I_S e^{V_{BE}/V_T} \quad \dots(3.11.1)$$

3. From Fig. 3.11.1,  $V_{BE} = v_{in}$

$$\therefore I_C = I_S e^{v_{in}/V_T} \quad \dots(3.11.2)$$

4. Now the current  $I_C$  and current  $I$  are same as Op-Amp input current is zero,

$$I = I_C = \frac{V_B - v_o}{R_f} = \frac{-v_o}{R_f} \quad \dots(3.11.3)$$

5. Substitute eq. (3.11.3) in eq. (3.11.2) we get,

$$-\frac{v_o}{R_f} = I_S e^{v_{in}/V_T}$$

$$v_o = -I_S R_f e^{v_{in}/V_T} \quad \dots(3.11.4)$$

6. Assume  $I_S R_f = v_{ref}$ , we can write the equation,

$$v_o = -v_{ref} e^{v_{in}/V_T}$$

7. Thus the output voltage  $v_o$  is proportional to the exponential of  $v_{in}$  i.e., anti-log of  $v_{in}$ . Thus the circuit works as basic anti-log amplifier.

**Que 3.12.** Describe temperature compensated log amplifier using two Op-Amp and explain its operation. AKTU 2017-18, Marks 05

### Answer

- The logarithmic amplifier is very sensitive to temperature. To minimize the temperature effects, the circuit called temperature-compensated logarithmic amplifier is used, in which two matched diodes are used to cancel the temperature-dependent offset term ' $\log I_S$ '.
- Similarly, a thermistor, which is a temperature-sensitive resistor can be used to cancel the temperature-dependent scaling factor ' $\eta V_T$ '.
- The output voltage of Op-Amp  $A_1$  is negative of the voltage across diode  $D_1$  and is given by

$$v_{01} = -V_{f1} = -\eta V_T \left[ \log \frac{v_1}{R_1} - \log I_S \right] \quad \dots(3.12.1)$$

4. Similarly, the voltage across diode  $D_2$  is given by

$$V_{f2} = \eta V_T (\log I - \log I_S) \quad \dots(3.12.2)$$

where  $I$  is the forward current and  $I_S$  is the reverse saturation current of diode  $D_2$ .

5. As both diodes are matched, their reverse saturation currents are same. The voltage at the non-inverting terminal of Op-Amp  $A_2$  is given by

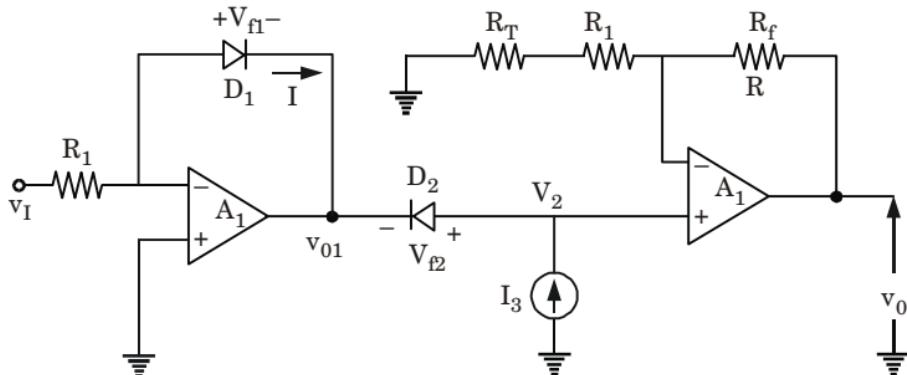
$$V_2 = v_{01} + V_{f2} = -\eta V_T \log \left( \frac{v_I}{IR_1} \right) \quad \dots(3.12.3)$$

6. Thus, the temperature-dependent offset term is eliminated from the output of  $A_1$ . The Op-Amp  $A_2$  is a non-inverting amplifier and its output is given by

$$v_0 = \left( 1 + \frac{R_f}{R_1 + R_T} \right) V_2 \quad \dots(3.12.4)$$

$$v_0 = - \left( \frac{R_1 + R_T + R_f}{R_1 + R_T} \right) \eta V_T \log \frac{v_I}{IR_1} \quad \dots(3.12.5)$$

7. Thus the circuit shown in Fig. 3.12.1 cancels the temperature-dependent terms present at the output of the log amplifier and provides a temperature-independent logarithmic output.

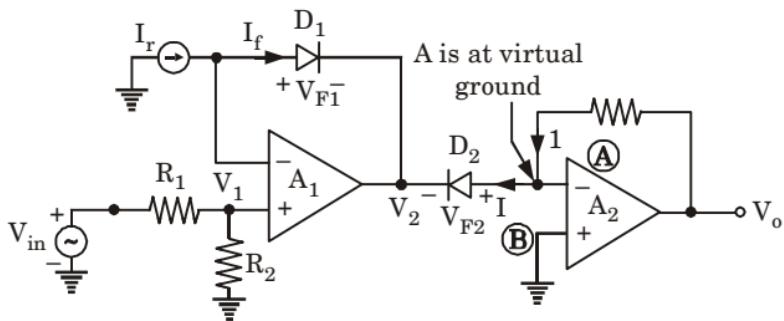


**Fig. 3.12.1.** Circuit for a temperature-compensated logarithmic amplifier.

**Que 3.13.** Derive the expression for output voltage of temperature compensated anti-log amplifier.

**Answer**

1. The temperature compensated anti-log amplifier is shown in Fig. 3.13.1. This circuit uses a constant current source ' $I_r$ ' as shown in Fig. 3.13.1.



**Fig. 3.13.1.** Temperature compensated antilog amplifier.

2. The voltage at non-inverting terminal of Op-Amp is given by,

$$V_1 = \frac{R_2}{(R_1 + R_2)} \cdot V_{\text{in}} \quad \dots(3.13.1)$$

3. Output voltage of first Op-Amp which is acting as a subtractor is given by,

$$V_2 = V_1 - V_{F1}$$

$$= \frac{R_2}{(R_1 + R_2)} \cdot V_{\text{in}} - V_{F1} \quad \dots(3.13.2)$$

4. The expression for the forward voltage across the diode 1 is given by

$$V_{F1} = -\eta V_T [\log_e(I_f) - \log_e(I_o)]$$

5. Substituting the value of  $V_{F1}$  in eq. (3.13.2) we get,

$$V_2 = \frac{R_2}{(R_1 + R_2)} \cdot V_{\text{in}} - \eta V_T [\log_e(I_f) - \log_e(I_o)] \quad \dots(3.13.3)$$

6. Applying the concept of virtual ground to the second amplifier in Fig. 3.13.1 we get,

$$V_2 = -V_{F2} = -\eta V_T [\log_e(I) - \log_e(I_o)] \quad \dots(3.13.4)$$

where  $I = \frac{V_o}{R_f}$  and  $I_f = I_r$

7. Equating eq. (3.13.3) and (3.13.4) we get,

$$V_{\text{in}} \frac{R_2}{R_1 + R_2} - \eta V_T [\log_e(I_r) - \log_e I_o] = -\eta V_T [\log_e(V_o/V_F) - \log_e(I_o)]$$

$$\therefore V_{\text{in}} \frac{R_2}{R_1 + R_2} - \eta V_T \log_e(I_r) = -\eta V_T \log_e(V_o/V_F)$$

$$\therefore V_{\text{in}} \frac{R_2}{R_1 + R_2} = \eta V_T [\log_e(I_r) - \log_e(V_o/V_F)]$$

$$V_{in} \frac{R_2}{R_1 + R_2} = \eta V_T \log_e \left[ \frac{I_r R_f}{V_o} \right]$$

∴

$$V_o = R_f I_r e^{\left[ \frac{V_{in}}{\eta V_T} \left( \frac{R_2}{R_1 + R_2} \right) \right]}$$

**Que 3.14.** What do you understand by precision rectifier? Explain the working of half wave precision rectifier.

### Answer

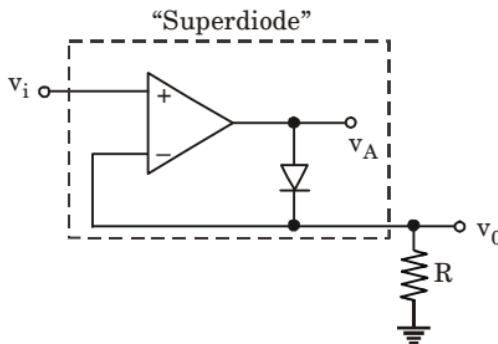
- A. **Precision rectifier :** A circuit which can act as an ideal diode for rectifying voltages which are below the level of cut-in voltage of the diode are called precision rectifier circuit.
- B. **Half wave precision rectifier :** Fig. 3.14.1 shows a precision half wave rectifier circuit consisting of a diode placed in the negative-feedback path of an Op-Amp, with  $R$  being the rectifier load resistance.

### C. Operation :

1. If  $v_i$  goes positive, the output voltage  $v_A$  of the Op-Amp will go positive and the diode will conduct, thus establishing a closed feedback path between the Op-Amp's output terminal and the negative input terminal.
2. The negative-feedback path will cause a virtual short circuit to appear between the two input terminals.
3. Thus the voltage at the negative input terminal, which is also the output voltage  $v_0$ , will equal (to within a few millivolts) that at the positive input terminal, which is the input voltage  $v_i$ ,

$$v_0 = v_i \quad v_i \geq 0$$

4. Consider now the case when  $v_i$  goes negative. The Op-Amp's output voltage  $v_A$  will tend to follow and go negative.
5. This will reverse-bias the diode, and no current will flow through resistance  $R$ , causing  $v_0$  to remain equal to 0 V. Thus, for  $v_i < 0$ ,  $v_0 = 0$ .



**Fig. 3.14.1.** Half wave precision rectifier.

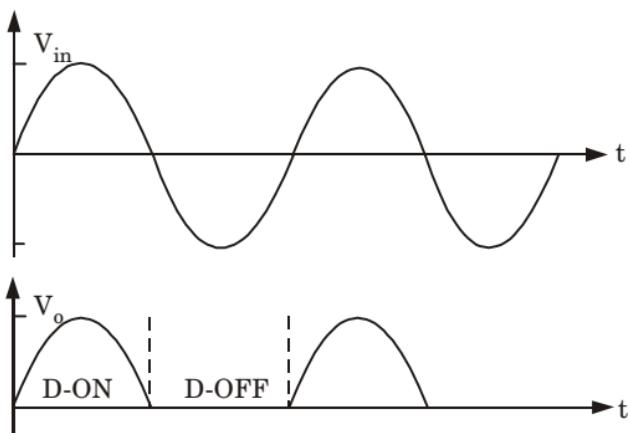


Fig. 3.14.2. Waveform of Half wave precision rectifier.

**Que 3.15.** Draw the circuit diagram of full wave precision rectifier and find expression for output voltage for both positive and negative half cycle of input sinusoidal waveform.

AKTU 2018-19, Marks 07

OR

Explain working of precision full wave rectifier with necessary waveform.

AKTU 2016-17, Marks 10

OR

What are precision rectifiers ? Describe the working of single Op-Amp based full wave precision rectifier.

AKTU 2019-20, Marks 07

### Answer

- A. **Precision rectifier :** Refer Q. 3.14, Page 3-18A, Unit-3.  
 B. **Full wave precision rectifier :**
- For positive half cycle of  $V_{in}$ , diode  $D_1$  will be ON and  $D_2$  will be OFF. Both the Op-Amps will act like inverter and thus,  $V_o$  will follow the input  $V_{in}$ . From Fig. 3.15.2,

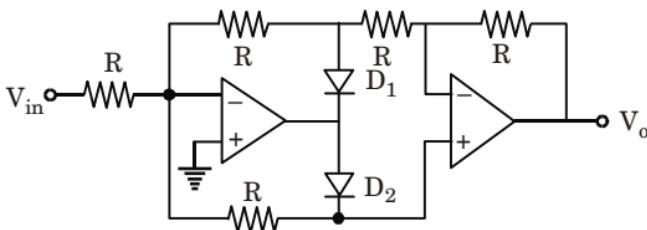


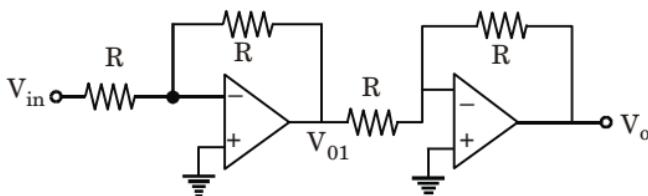
Fig. 3.15.1.

Hence,

$$V_{01} = \frac{-R}{R} V_{in} = -V_{in}$$

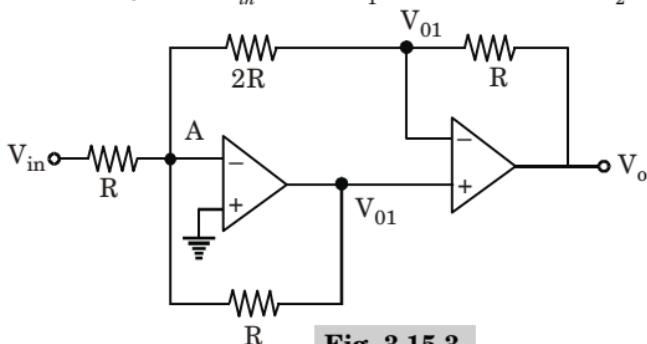
and

$$V_0 = \frac{-R}{R} (-V_{in}) = V_{in}$$



**Fig. 3.15.2.**

2. In negative half cycle of  $V_{in}$ , diode  $D_1$  will be OFF and  $D_2$  will be ON.



**Fig. 3.15.3.**

- i. Applying KCL at node A,

$$\frac{V_A - V_{in}}{R} + \frac{V_A - V_{01}}{R} + \frac{V_A - V_{01}}{2R} = 0$$

- ii. Now,  $V_A = 0$  [Virtual ground concept]

$$-\frac{V_{in}}{R} - \frac{V_{01}}{R} - \frac{V_{01}}{2R} = 0$$

$$V_{in} = -\frac{3}{2}V_{01}$$

$$V_{01} = -\frac{2}{3}V_{in}$$

- iii. Also,

$$V_o = \left(1 + \frac{R}{2R}\right) V_{01} = \left(1 + \frac{R}{2R}\right) \left(-\frac{2}{3}V_{in}\right)$$

Hence, for

$$\begin{aligned} V_o &= -V_{in} \\ V_{in} &< 0, \\ V_0 &= V_{in} \end{aligned}$$

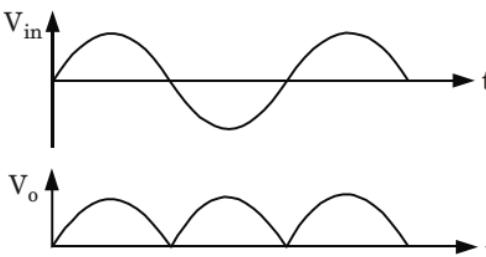


Fig. 3.15.4. Input and output waveforms of full wave rectifier.

**Que 3.16.** Explain the working of peak detectors.**AKTU 2018-19, Marks 3.5****Answer**

- Fig. 3.16.1 shows a peak detector that measures the positive peak values of square wave input.
- For positive half-cycle of  $V_{in}$ , the diode  $D_1$  conducts and charge capacitor  $C$  to positive peak value  $V_p$  of the input  $V_{in}$ , i.e. the Op-Amp acts as a voltage follower.
- During negative half cycle of  $V_{in}$ , diode  $D_1$  is reversed biased and open-circuit. Here voltage across  $C$  is retained.
- For proper operation of the circuit, the charging time constant ( $CR_d$ ) and discharging time constant ( $CR_L$ ) must satisfy,

$$CR_d \leq T / 10$$

Here,

 $R_d$  = Resistance of forward bias diode $T$  = Time period of input waveform

and,

$$CR_L \geq 10T$$

Here,  $R_L$  is load resistor.

- If  $R_L$  is very small, then use of buffer is needed between  $C$  and  $R_L$ .

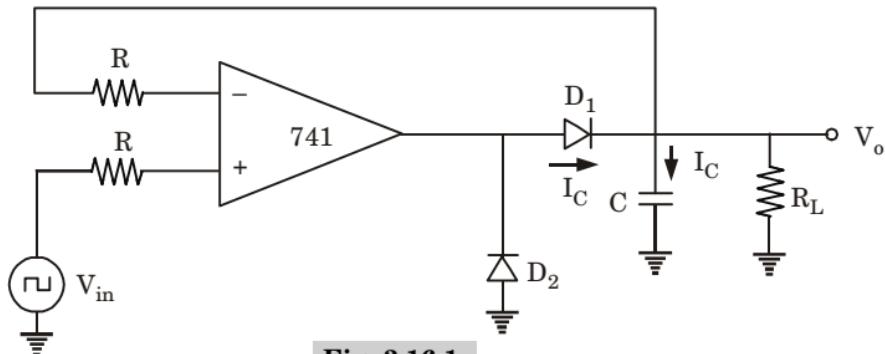


Fig. 3.16.1.

- Resistance  $R$  is used to protect the Op-Amp against the excessive discharge currents, when power supply is switched OFF.  $D_2$  conducts during negative half cycle to prevent Op-Amp from going into negative saturation and helps to reduce recovery time of Op-Amp.

7. The input and output waveforms is shown in Fig. 3.16.2.

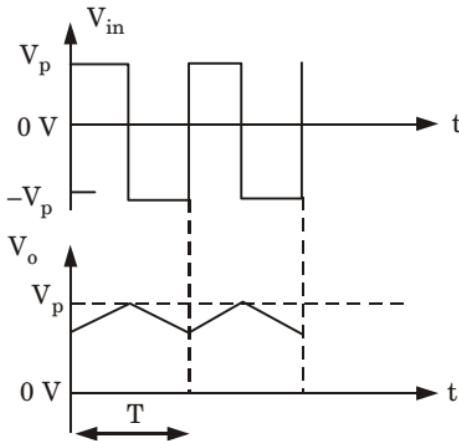


Fig. 3.16.2.

**Que 3.17.** Describe the sample and hold circuit with the help of an Op-Amp. What are the applications of sample and hold circuit ?

AKTU 2015-16, Marks 10

### Answer

#### A. Sample and hold circuit :

- Fig. 3.17.1 shows the circuit for sample and hold using Op-Amp. It samples an input signal and holds on to its last sampled value until the input is sampled again.

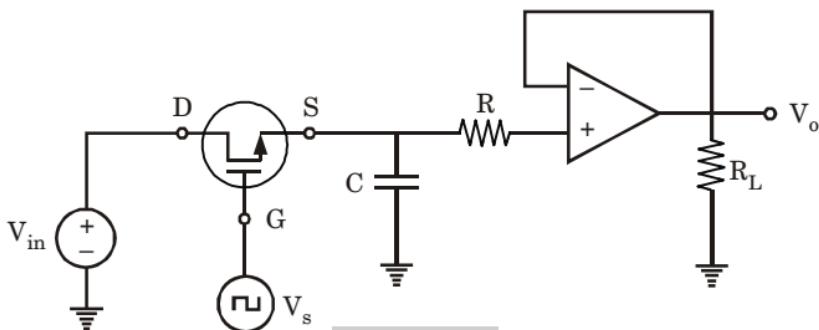
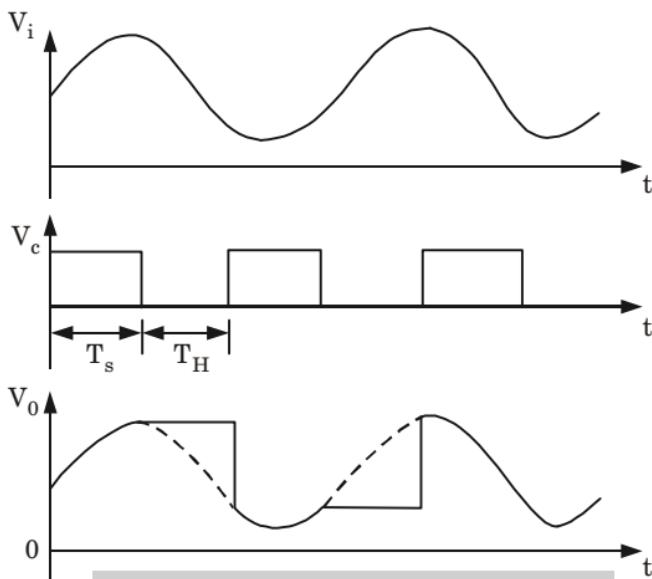


Fig. 3.17.1.

- Op-Amp and enhancement MOSFET is used in the circuit. MOSFET acts as switch to control  $V_s$  while  $C$  serves as a storage element.  $V_{in}$  to be sampled is applied to drain and  $V_s$  across the gate of MOSFET.
- During positive portion of  $V_s$ , the MOSFET conducts and allow input voltage to charge capacitor  $C$ .

**Fig. 3.17.2.** Input and output waveforms.

4. When  $V_s$  is zero, the MOSFET is OFF and the discharge path for capacitor  $C$  is through the Op-Amp.
5. However, the input resistance of the Op-Amp voltage follower is also very high; hence the voltage across  $C$  is retained. Fig. 3.17.2 shows the input and output waveforms.
6. The time period  $T_s$  of voltage  $V_s$  during which the voltage across the  $C$  is equal to the input voltage are called sample periods.
7. The time period  $T_H$  of  $V_s$  during which the voltage across the capacitor  $C$  is constant are called hold periods as shown in Fig. 3.17.2.

#### **B. Applications :**

- i. PAM demodulator.
- ii. PCM.
- iii. Analog to digital converters.

#### **PART-3**

*Op-Amp as a Comparator and Zero Crossing Detector, Astable Multivibrator and Monostable Multivibrator, Generation of Triangular Waveforms, Analog Multipliers and Their Applications.*

#### **Questions-Answers**

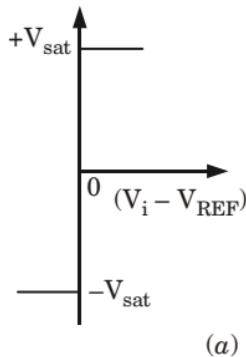
#### **Long Answer Type and Medium Answer Type Questions**

**Que 3.18.** Write a short note on comparator and enlist its applications.

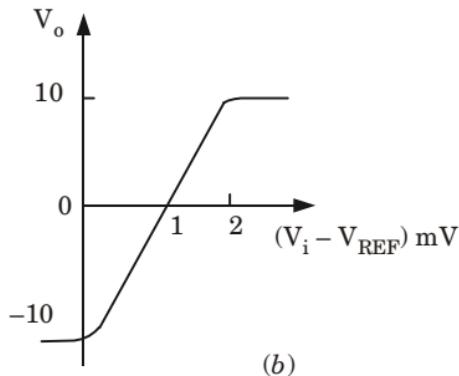
**Answer**

**A. Comparator :**

1. A comparator is a circuit that is used for comparing a signal voltage applied at one input of Op-Amp with a known reference voltage at other input.



(a)



(b)

**Fig. 3.18.1.** The transfer characteristics (a) ideal comparator  
(b) Practical comparator.

2. It is basically an open-loop Op-Amp with output  $\pm V_{\text{sat}}$  ( $= V_{CC}$ ) as shown in ideal transfer characteristics of Fig. 3.18.1(a).
3. There are basically two types of comparator :
  - a. **Non-inverting comparator :**
    1. The circuit of Fig. 3.18.2(a) is called a non-inverting comparator. A fixed reference voltage  $V_{\text{ref}}$  is applied to (-ve) input and a time varying signal  $v_i$  is applied to (+ve) input.
    2. The output voltage is at  $-V_{\text{sat}}$  for  $v_i < V_{\text{ref}}$ . And  $v_o$  goes to  $+V_{\text{sat}}$  for  $v_i > V_{\text{ref}}$ .
    3. The output waveform for a sinusoidal input signal applied to the (+ve) input is shown in Fig. 3.18.2(b) and (c) for positive and negative  $V_{\text{ref}}$  respectively.

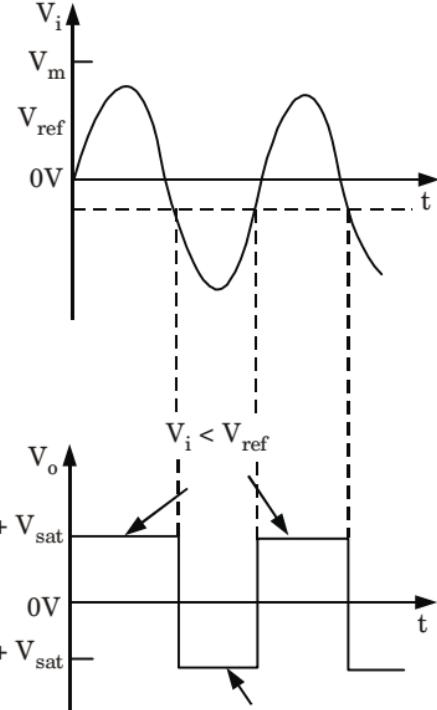
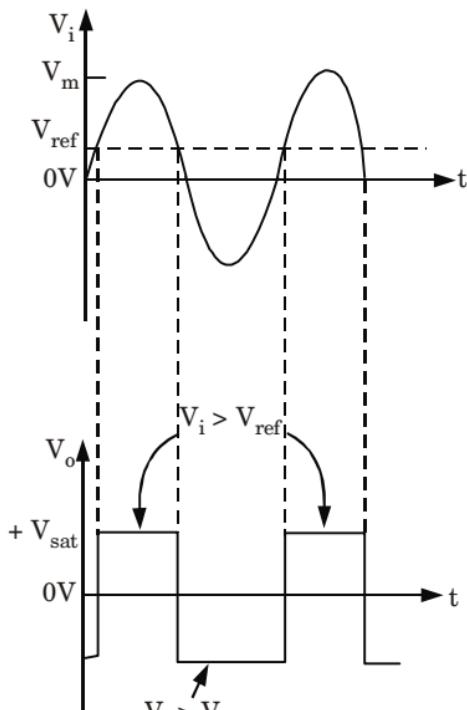
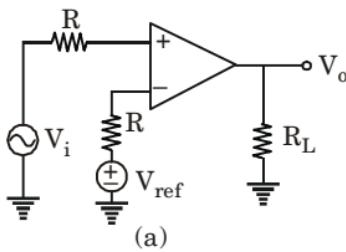
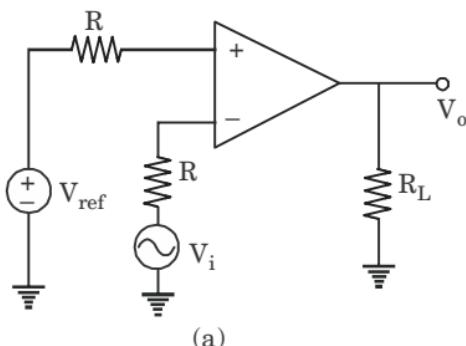
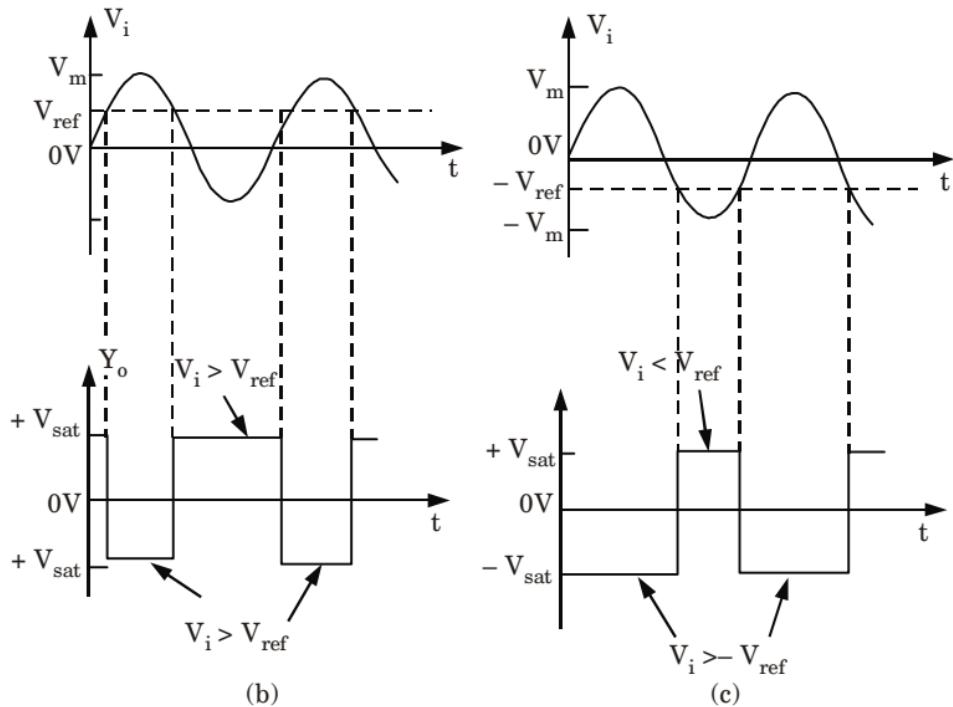


Fig. 3.18.2.

### b. Inverting comparator :

In inverting comparator, fixed reference voltage  $V_{ref}$  is applied to (+ve) input and a time varying signal  $v_i$  is applied to (-ve) input.





**Fig. 3.18.3. (a) Inverting comparator. Input and output waveforms for (b)  $V_{ref} > 0$  (c)  $V_{ref} < 0$ .**

## B. Applications :

- i. Zero crossing detector
- ii. Window detector
- iii. Phase meter.

**Que 3.19.** Write short notes on zero crossing detection.

### Answer

1. The basic comparators can be used as zero crossing detector by making  $V_{REF} = 0$ .
2. Whenever the input voltage crosses the  $x$ -axis,  $V_o$  changes from  $+V_{sat}$  to  $-V_{sat}$  or  $-V_{sat}$  to  $+V_{sat}$  as shown in Fig. 3.19.1.

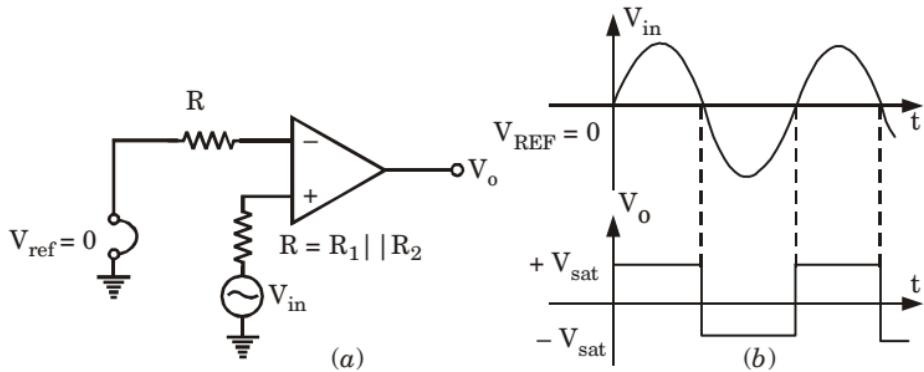


Fig. 3.19.1.

3. Zero crossing detector is also called sine to square wave generator. There are two types of zero crossing detectors :

**a. Non-inverting zero crossing detector :**

1. In a non-inverting zero crossing detector, the Op-Amp is used in open loop configuration. Inverting terminal of the Op-Amp is grounded and input is applied to the non-inverting terminal. The circuit is shown in Fig. 3.19.2.

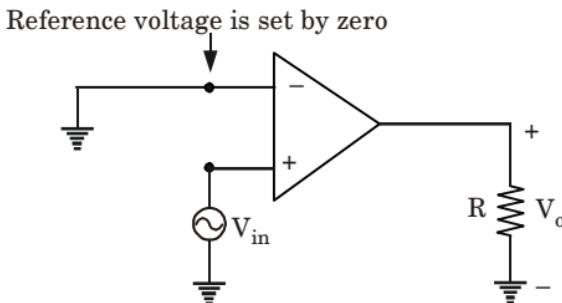


Fig. 3.19.2. Non-inverting zero crossing detector.

2. During the positive half cycle, the input voltage is positive *i.e.*, above the reference voltage (0 V). Hence the output voltage is  $+V_{sat}$ .
3. During negative half cycle, the input voltage  $V_{in}$  is negative, *i.e.*, below the reference voltage. The output voltage is then  $-V_{sat}$ .
4. Thus the output voltage switches between  $+V_{sat}$  and  $-V_{sat}$  whenever the input signal crosses the zero level. This is shown in Fig. 3.19.3.

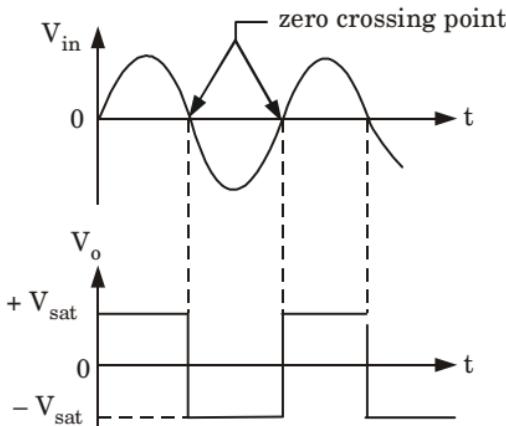


Fig. 3.19.3. Input is sinusoidal.

**b. Inverting zero crossing detector :**

1. In the inverting zero crossing detector, input is directly applied to the inverting input terminal while the non-inverting terminal is grounded. The circuit is shown in Fig. 3.19.4.

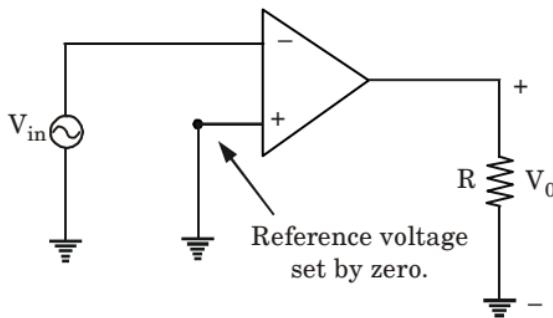


Fig. 3.19.4. Inverting zero crossing detector.

2. During positive half cycle, inverting terminal is more positive than non-inverting terminal, so output is  $-V_{sat}$  while for negative half cycle, the output is  $+V_{sat}$ . This circuit is called an inverter. The waveforms are shown in Fig. 3.19.5.

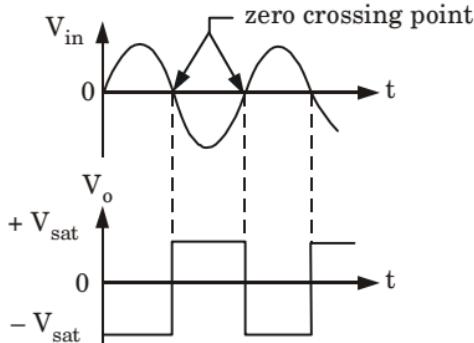
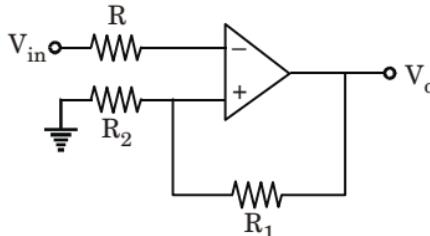


Fig. 3.19.5. Input is sinusoidal.

**Que 3.20.** Describe the Schmitt trigger with help of proper circuit diagram and transfer characteristics. AKTU 2018-19, Marks 3.5

**Answer**

- If positive feedback is added to the comparator circuit, gain can be increased greatly. This circuit is called Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback.



**Fig. 3.20.1.** Schmitt trigger.

- Schmitt trigger also exhibits the phenomenon of hysteresis. The input voltage is applied to the (-ve) input terminal and feedback voltage to the (+ve) input terminal.
- Input voltage  $V_{in}$  triggers output  $V_o$ , every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage ( $V_{UT}$ ) and lower threshold voltage ( $V_{LT}$ ).
- Now, suppose the output  $V_o = +V_{sat}$ . The voltage at (+) input terminal will be

$$V_{UT} = \frac{R_2}{R_1 + R_2} (+V_{sat}) \quad \dots(3.20.1)$$

This voltage is upper threshold voltage. As long as  $V_{in}$  is less than  $V_{UT}$ , the output  $V_o$  remains constant at  $+V_{sat}$ .

- When  $V_{in}$  is just greater than  $V_{UT}$ , the output then switches to  $-V_{sat}$  and remains at this level as long as  $V_{in} > V_{UT}$ .
- For  $V_o = -V_{sat}$ , the voltage at (+ve) input terminal will be

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{sat}) \quad \dots(3.20.2)$$

This voltage is called lower threshold voltage.

- The output voltage is  $-V_{sat}$  as long as  $V_{in}$  is above or positive with respect to  $V_{LT}$ . The output voltage  $V_o$  changes to  $+V_{sat}$  if  $V_{in}$  goes more negative than or below  $V_{LT}$ . Resistor  $R$  is shown as  $R_1 \parallel R_2$  to compensate for input bias current,
- Input and output voltage waveforms are shown in Fig. 3.20.2.

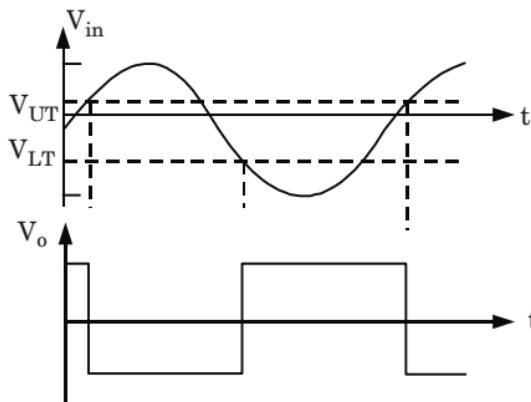


Fig. 3.20.2.

## 9. Hysteresis curve (Transfer characteristics) :

- From eq. (3.20.1) and (3.20.2),

$$V_{UT} > V_{LT}$$

$$\therefore V_{UT} - V_{LT} = \frac{2R_2}{R_1 + R_2} V_{sat}$$

This difference is called hysteresis width.

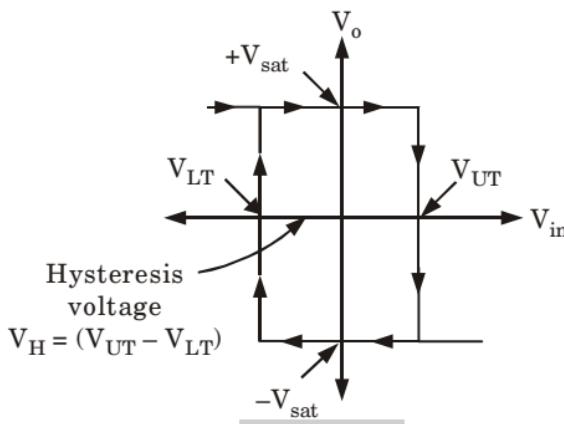


Fig. 3.20.3.

- $V_H$  is also called dead band because change in  $V_{in}$  do not change the output voltage. That is when the input exceeds  $V_{UT}$ , out switches from  $+V_{sat}$  to  $-V_{sat}$  and reverts back to its original state,  $+V_{sat}$ , when the input goes below  $V_{LT}$ .

- Uses : Schmitt trigger is used to convert any wave into a square wave.

**Que 3.21.** Describe the Schmitt trigger with the help of proper circuit diagram and transfer characteristics. A Schmitt trigger with the upper threshold level  $V_{UT} = 0 \text{ V}$  and hysteresis width is 0.2 V converts 1 KHz sine wave of amplitude 4 V<sub>PP</sub> into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

AKTU 2015-16, Marks 15

### Answer

- A. Schmitt trigger and its transfer characteristics : Refer Q. 3.20, Page 3-29A, Unit-3.  
 B. Numerical :

**Given:**  $V_{UT} = 0 \text{ V}$ ,  $V_H = 0.2 \text{ V}$ ,  $f = 1 \text{ KHz}$

**To Find :** Time duration.

1.  $V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$   
 So,  $V_{LT} = -0.2 \text{ V}$

2. In Fig. 3.21.1 the angle  $\theta$  can be calculated as

$$\begin{aligned} -0.2 &= V_m \sin(\pi + \theta) = -V_m \sin \theta = -2 \sin \theta \\ \theta &= \arcsin 0.1 = 0.1 \text{ radian} \end{aligned}$$

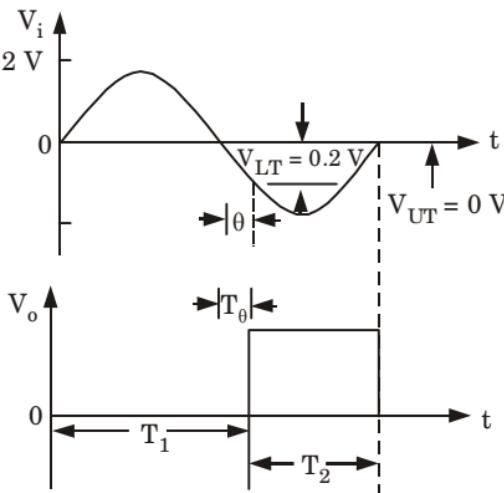


Fig. 3.21.1.

3. The period,  $T = 1/f = 1/1000 = 1 \text{ ms}$   
 $\omega T_0 = 2\pi (1000) T_0 = 0.1$   
 $T_0 = (0.1/2 \pi) \text{ ms} = 0.016 \text{ ms}$
4. So,  
 and  $T_1 = T/2 + T_0 = 0.516 \text{ ms}$   
 $T_2 = T/2 - T_0 = 0.484 \text{ ms}$

**Que 3.22.** Explain how a Schmitt trigger circuit works with a neat diagram. Design a Schmitt trigger with  $V_{UT} = 2 \text{ V}$ ,  $V_{LT} = -2 \text{ V}$ . Assume  $\pm V_{\text{sat}} = \pm 13 \text{ V}$ .

AKTU 2017-18, Marks 05

**Answer**

**A. Schmitt trigger :** Refer Q. 3.20, Page 3-29A, Unit-3.

**B. Numerical :**

Given :  $V_{UT} = 2 \text{ V}$ ,  $V_{LT} = -2 \text{ V}$ ,  $\pm V_{\text{sat}} = \pm 13 \text{ V}$

To Design : Schmitt trigger.

- We know, 
$$V_{UT} = \frac{R_2}{R_1 + R_2} (+ V_{\text{sat}})$$

$$2 \text{ V} = \frac{R_2}{R_1 + R_2} (+ 13)$$

$$\frac{R_2}{R_1 + R_2} = \frac{2}{13} = 0.154 \quad \dots(3.22.1)$$

and 
$$V_{LT} = \frac{R_2}{R_1 + R_2} (- V_{\text{sat}})$$

$$-2 \text{ V} = \frac{R_2}{R_1 + R_2} (-13)$$

$$\frac{R_2}{R_1 + R_2} = \frac{-2}{-13} = 0.154 \quad \dots(3.22.2)$$

2. From eq. (3.22.1) and (3.22.2)

Let 
$$\frac{R_2}{R_1 + R_2} = 0.154$$
  

$$R_2 = 100 \Omega$$
  

$$\therefore \frac{100}{R_1 + 100} = 0.154$$
  

$$\Rightarrow R_1 = 549.35 \Omega$$

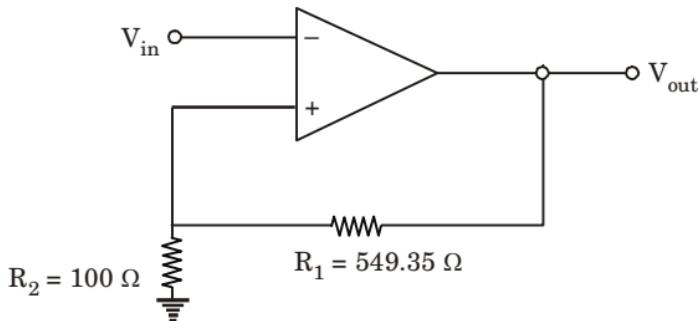


Fig. 3.22.1.

**Que 3.23.** Draw the circuit diagram for monostable multivibrator with operational amplifier. Explain its operation. Derive the expression for its time period.

**OR**

Draw and explain the working of monostable multivibrator using Op-Amp.

AKTU 2019-20, Marks 07

### Answer

#### A. Monostable multivibrator :

- Fig. 3.23.1 shows the circuit diagram of monostable multivibrator. A diode  $D_1$  clamps the capacitor voltage to 0.7 V when the output is at  $+V_{sat}$ .
- The negative going pulse signal of magnitude  $V_1$  (triggering signal) passing through the differentiator  $R_3C_1$  and diode  $D_2$  produces a negative going triggering pulse and is applied to the (+) input terminal.

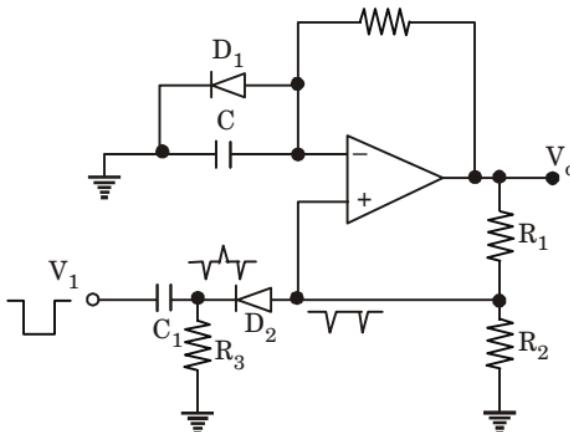


Fig. 3.23.1.

#### B. Operation :

- For monostable operation, the trigger pulse width  $T_p$  should be much less than  $T$ , the pulse width of the monostable multivibrator.
- The diode  $D_2$  is used to avoid malfunctioning by blocking the positive spikes that may be present at the differentiated trigger input.
- Fig. 3.23.2 shows the trigger and output waveform.
- When  $V_o$  is  $+V_{sat}$ , voltage divider  $R_1$  and  $R_2$  feedback  $V_{UT}$  to the (+ve) input. The diode  $D_1$  clamps the (-ve) input at approximately 0.7 V (because the diode is forward biased).
- The feedback voltage at (+ve) terminal is higher than (-ve) terminal therefore Op-Amp holds  $V_o$  at  $+V_{sat}$ . This output state is called as stable state.

6. If the negative spike (trigger signal) is applied to (+ ve) of Op-Amp which is higher than the voltage at (- ve) terminal. The combination of feedback voltage and negative trigger voltage will be pulled below the voltage at (- ve) input.
7. Once the (+ ve) input becomes negative with respect to the (- ve) input,  $V_o$  switches to  $-V_{sat}$ . With this change, the one-shot is now in its timing state. This state is an unstable state.
8. Due to  $V_o = -V_{sat}$ , the diode  $D_1$  is reverse biased and the capacitor  $C$  charges, the (- ve) input becomes more and more negative with respect to ground. When the capacitor voltage is more than (+ ve) terminal,  $V_o$  switches to  $+V_{sat}$ .

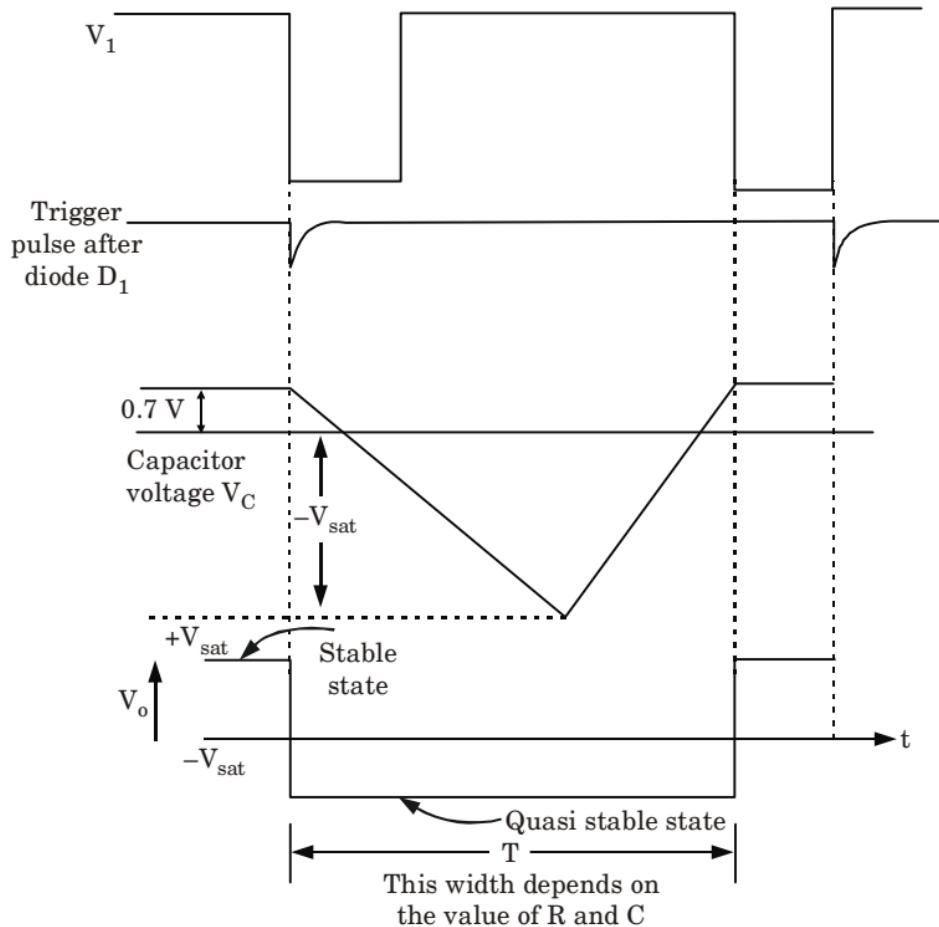


Fig. 3.23.2. Input and output waveform.

#### C. Expression for time period :

1. The general solution for a signal time constant low pass  $RC$  circuit with  $V_i$  and  $V_f$  as initial and final value is

$$V_o = V_f + (V_i - V_f) e^{-t/RC}$$

2. For the circuit,  $V_f = -V_{sat}$  and  $V_i = V_D$  (diode forward voltage)

The output  $V_C$  is

$$V_C = -V_{\text{sat}} + (V_D + V_{\text{sat}}) e^{-t/RC} \quad \dots(3.23.1)$$

If the time constant  $T = RC$  and when  $t = T$

$$V_C = -\beta V_{\text{sat}}$$

$$V_C = \frac{R_2}{R_1 + R_2} (-V_{\text{sat}})$$

where

$$\beta = \frac{R_2}{R_1 + R_2}$$

Therefore

$$-\beta V_{\text{sat}} = -V_{\text{sat}} + (V_D + V_{\text{sat}}) e^{-t/RC}$$

4. After simplification, the pulse widths is obtained as

$$T = RC \ln \frac{(1 + V_D / V_{\text{sat}})}{1 - \beta} \quad \dots(3.23.2)$$

If  $V_{\text{sat}} \gg V_D$  and  $R_1 = R_2$  so that  $\beta = 0.5$  then

$$T = 0.69RC$$

**Que 3.24.** A monostable multivibrator is to be used as divide-by-4 network. The frequency of input trigger is 12 KHz. If the value of  $C = 0.05 \mu\text{F}$ , what should be value of  $R$  ?

### Answer

Given :  $f = 12 \text{ KHz}$ ,  $C = 0.05 \mu\text{F}$

To Find :  $R$ .

1. For a divide-by-4 network,  $t_p$  should be slightly larger than thrice the period of the input trigger signal.

2. Let  $t_p = 3.2 T$

Therefore,  $t_p = (3.2) \frac{1}{12 \text{ KHz}} = 3.2 \times 8.33 \times 10^{-5}$   
 $= 26.656 \times 10^{-5} \text{ sec}$

3.  $t_p = 1.1RC = 26.656 \times 10^{-5}$

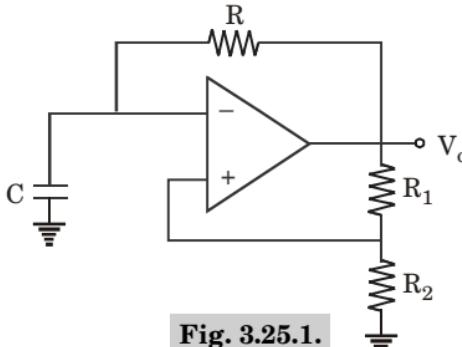
$$R = \frac{26.656 \times 10^{-5}}{1.1 \times 0.05 \times 10^{-6}} = 4.84 \text{ k } \Omega \approx 5 \text{ k } \Omega$$

**Que 3.25.** Explain astable multivibrator with its waveform.

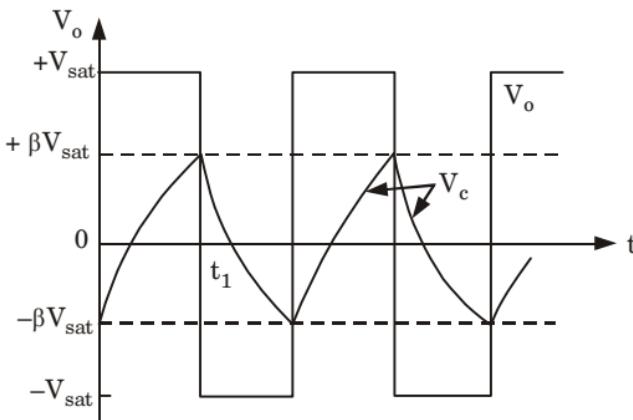
**Answer**

1. Square wave generator is also called as astable multivibrator or free running oscillator.
2. Circuit of square wave generator is as shown in Fig. 3.25.1. The principle of generation of square wave output is to force an Op-Amp to operate in the saturation region.
3. A fraction of output is fed back to the (+ ve) input terminal. This fraction is given by,

$$\beta = \frac{R_2}{R_1 + R_2}$$

**Fig. 3.25.1.**

4. Thus, the reference voltage is  $\beta V_o$  and may take values as  $+ \beta V_{sat}$  or  $- \beta V_{sat}$ . The output is also fed back to the (- ve) input terminal after integrating by  $RC$  combination. When (- ve) input terminal voltage exceeds  $V_{REF}$ , switching takes place resulting in square wave output.

**Fig. 3.25.2.**

5. Now, consider the waveform shown in Fig. 3.25.2. When the output is at  $+ V_{sat}$ , capacitor C starts charging through R. Voltage at (+ ve) input terminal is  $+ \beta V_{sat}$ . Now as the charge C rises above this reference voltage  $+ \beta V_{sat}$ , output switches to  $- V_{sat}$ .

6. At this instant, voltage on the capacitor is  $+ \beta V_{\text{sat}}$ , hence it starts discharging through  $R$  i.e., towards  $- \beta V_{\text{sat}}$ . When output voltage switches to  $- V_{\text{sat}}$ , the capacitor charges more negatively until its voltage just exceeds  $- \beta V_{\text{sat}}$ .
7. The output switches back to  $+ V_{\text{sat}}$  and hence the cycle repeats itself.
8. Now, voltage across the capacitor, as a function of time is given by

$$V_c(t) = V_{\text{final}} + (V_{\text{initial}} - V_{\text{final}}) e^{-t/RC}$$

As,

$$V_{\text{final}} = +V_{\text{sat}}$$

and

$$V_{\text{initial}} = - \beta V_{\text{sat}}$$

$$V_c(t) = V_{\text{sat}} + (- \beta V_{\text{sat}} - V_{\text{sat}}) e^{-t/RC}$$

$$V_c(t) = V_{\text{sat}} - V_{\text{sat}} (1 + \beta) e^{-t/RC}$$

9. At  $t = t_1$ , voltage across capacitor reaches to  $+ \beta V_{\text{sat}}$ , therefore,

$$V_c(t_1) = \beta V_{\text{sat}} = V_{\text{sat}} - V_{\text{sat}} (1 + \beta) e^{-t_1/RC}$$

After solving,

$$t_1 = RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

This is only half of the total period.

$$\therefore \text{Total time period} = 2t_1 = 2RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

**Que 3.26.** Explain the generation of square and triangular waveforms from astable multivibrator operation using Op-Amp. Also find expression of the time period for both cases.

AKTU 2016-17, Marks 15

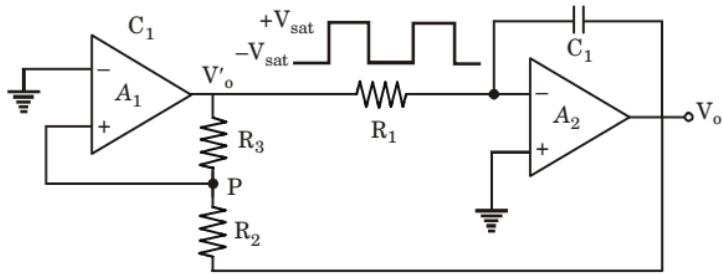
OR

Draw and explain the circuit of triangular wave generator. How square wave can be obtained using this triangular wave.

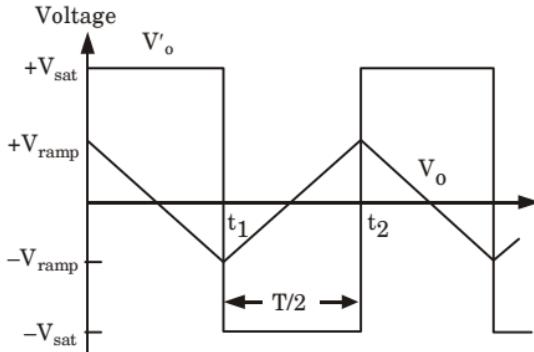
AKTU 2017-18, Marks 05

### Answer

- A. **Generation of square waveforms :** Refer Q. 3.25, Page 3-35A, Unit-3.
- B. **Generation of triangular waveforms :**
  1. A triangular wave can be simply obtained by integrating a square wave.
  2. Triangular wave generator along with waveforms is shown in Fig. 3.26.1 (a).



(a) Triangular waveform generator



(b) Waveforms.

**Fig. 3.26.1.****Working :**

1. Assume output of comparator  $A_1$  is at  $\pm V_{\text{sat}}$  so output of integrator will be a negative going ramp as shown in Fig. 3.26.1(b).
2. When the negative going ramp reaches to  $-V_{\text{ramp}}$ , the output of  $A_1$  switches from  $+V_{\text{sat}}$  to  $-V_{\text{sat}}$ . The sequence then repeats to give triangular wave at the output of  $A_2$ .
3. The frequency of triangular waveform can be calculated as follows :
  - i. The effective voltage at point  $P$  during the time when output of  $A_1$  is at  $+V_{\text{sat}}$  level is given by,

$$-V_{\text{ramp}} + \frac{R_2}{R_2 + R_3} [+V_{\text{sat}} - (V_{\text{ramp}})] \quad \dots(3.26.1)$$

- ii. At  $t = t_1$ , the voltage at point  $P$  becomes equal to zero. Therefore from eq. (3.26.1)

$$-V_{\text{ramp}} = -\frac{R_2}{R_3} (+V_{\text{sat}}) \quad \dots(3.26.2)$$

- iii. Similarly, at  $t = t_2$ , when the output of  $A_1$  switches from  $-V_{\text{sat}}$  to  $+V_{\text{sat}}$ ,

$$V_{\text{ramp}} = \frac{-R_2}{R_3} (-V_{\text{sat}}) = \frac{R_2}{R_3} (V_{\text{sat}})$$

- iv. Therefore, peak to peak amplitude of the triangular wave is

$$V_o(pp) = +V_{\text{ramp}} - (-V_{\text{ramp}}) = 2 \frac{R_2}{R_3} V_{\text{sat}} \quad \dots(3.26.3)$$

- v. The output switches from  $-V_{\text{ramp}}$  to  $+V_{\text{ramp}}$  in half the time period  $T/2$ . Putting the values in the basic integrator equation,

$$V_o = -\frac{1}{RC} \int v_i dt$$

$$V_o(pp) = -\frac{1}{R_1 C_1} \int_0^{T/2} (-V_{\text{sat}}) dt = \frac{V_{\text{sat}}}{R_1 C_1} \left( \frac{T}{2} \right)$$

$$\text{or, } T = 2R_1 C_1 \frac{V_o(pp)}{V_{\text{sat}}} \quad \dots(3.26.4)$$

- vi. Putting the value of  $V_o(pp)$  from eq. (3.26.4), we get

$$T = \frac{4R_1 C_1 R_2}{R_3}$$

Hence the frequency of oscillation  $f_o$  is,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1 C_1 R_2}$$

**Que 3.27.** Write a short note on analog multiplier also give its applications.

**OR**

Write short notes on the following :

i. Analog multiplier.

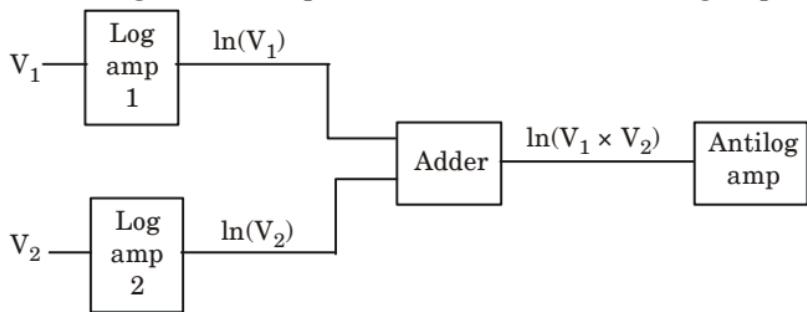
ii. Logarithmic amplifier.

**AKTU 2018-19, Marks 07**

### Answer

i. **Analog multiplier :**

1. A multiplier is an active network whose output is proportional to the product of two input signals.
2. Fig. 3.27.1 shows the basic block diagram of an analog multiplier, which uses two logarithmic amplifiers, an adder, and an antilog amplifier.



**Fig. 3.27.1.** Basic block diagram of an analog multiplier.

3. The input signals, which are to be multiplied, are applied to the input logarithmic amplifiers.

4. The logarithmic amplifiers produce the logarithm of the input signal and these outputs are applied to the adder circuit.
5. The output of the adder circuit, which is the logarithm of product of the two input signals, is fed to the anti-log amplifier.
5. The anti-log amplifier finally removes the logarithm of the terms and produces the multiplication of the input signals.

i.e.,  $V_1 \times V_2 = \text{Anti-log}(V_1 \times V_2)$

### **Applications of analog multiplier :**

#### **a. Squarer circuit :**

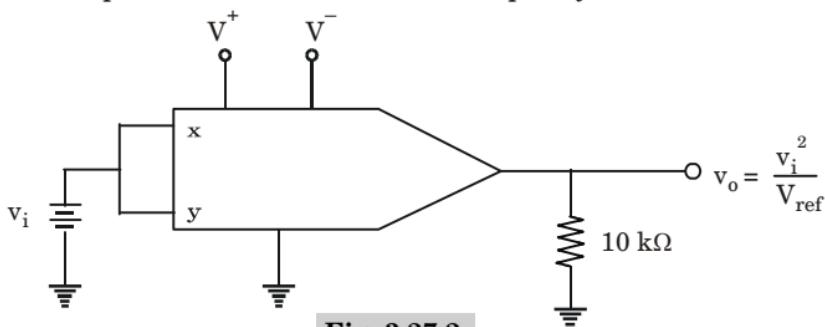
1. The squarer circuit is shown in Fig. 3.27.2. The basic multiplier can be used to square any positive or negative number provided the number can be represented by a voltage between 0 to  $V_{REF}$ .
2. The voltage  $V_i$  representing the number is connected to both the inputs. It is possible to square a sine wave voltage too.
3. In Fig. 3.27.2, if a sine wave voltage  $v_i = V_m \sin \omega t$  is applied to both the inputs, then the output voltage,  $v_o$  is given by

$$v_o = \frac{v_i^2}{V_{REF}}$$

4. For  $v_i = 5 \sin 2\pi \times 10^4 t$  and  $V_{REF} = 10 \text{ V}$ ,

$$v_o = \frac{5^2}{10} (\sin 2\pi \times 10^4 t)^2 = 2.5 \left[ \frac{1}{2} - \frac{1}{2} \cos 2\pi \times 2 \times 10^4 t \right] \\ = 1.25 - 1.25 \cos 2\pi \times 2 \times 10^4 t$$

The output contains a DC term and frequency is doubled.



**Fig. 3.27.2.**

#### **b. Phase angle detection :**

1. If the input signals applied to a multiplier are

$$v_x = V_{mx} \sin \omega t \\ v_y = V_{my} \sin(\omega t + \theta)$$

2. Then,  $v_o = \frac{V_{mx} V_{my}}{V_{REF}} \sin \omega t \sin(\omega t + \theta)$

$$= \frac{V_{mx} V_{my}}{V_{REF}} \times \frac{1}{2} [\cos \theta - \cos(2\omega t + \theta)]$$

3. The phase difference  $\theta$  between the two point signals can be calculated from the DC component in the output voltage  $V_o$ . That is,

$$V_{o,DC} = \frac{V_{mx} V_{my}}{2V_{REF}} \times \cos \theta$$

**ii. Logarithmic amplifier :** Refer Q. 3.10, Page 3-13A, Unit-3.

**Que 3.28.** What do you mean by the quadrant operation of multiplier? Draw and explain a GILBERT analog multiplier.

AKTU 2017-18, Marks 10

AKTU 2019-20, Marks 07

### Answer

#### A. Quadrant operation of multiplier :

1. The quadrant defines the applicability of the circuit for bipolar signals at its inputs.
2. First-quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four-quadrant device accepts two bipolar signals.

#### B. GILBERT analog multiplier :

1. The GILBERT multiplier cell is a modification of the emitter coupled cell and this allows four-quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced multipliers.

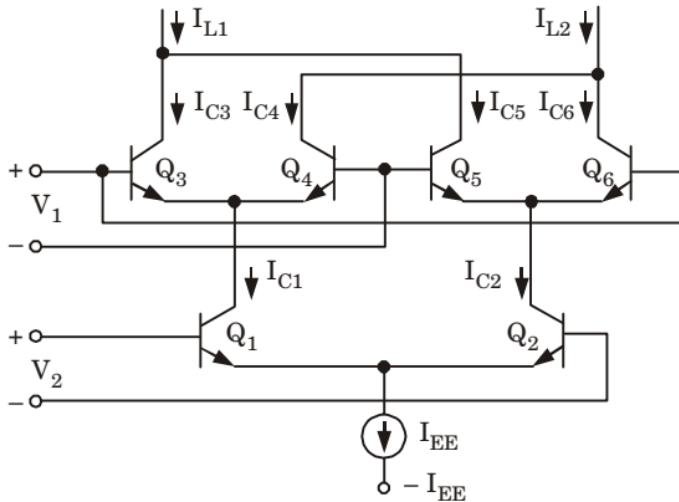


Fig. 3.28.1. GILBERT multiplier cell.

2. Two cross-coupled emitter-coupled pairs in series connection with an emitter coupled pair form the structure of the GILBERT multiplier cell.
3. The collector currents of  $Q_3$  and  $Q_4$  are given by

$$I_{C3} = \frac{I_{C1}}{1 + e^{-V_1/V_T}} \quad \dots(3.28.1)$$

and  $I_{C4} = \frac{I_{C1}}{1 + e^{V_1/V_T}}$  ... (3.28.2)

4. Similarly the collector currents of  $Q_5$  and  $Q_6$  are given by

$$I_{C5} = \frac{I_{C2}}{1 + e^{V_1/V_T}} \quad \dots(3.28.3)$$

and  $I_{C6} = \frac{I_{C2}}{1 + e^{-V_1/V_T}}$  ... (3.28.4)

5. The collector currents  $I_{C1}$  and  $I_{C2}$ , of transistors  $Q_1$  and  $Q_2$  can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_2/V_T}} \quad \dots(3.28.5)$$

and  $I_{C2} = \frac{I_{EE}}{1 + e^{V_2/V_T}}$  ... (3.28.6)

6. Substituting eq. (3.28.5) in eq. (3.28.1) and (3.28.2), we get

$$I_{C3} = \frac{I_{EE}}{[1 + e^{-V_1/V_T}][1 + e^{-V_2/V_T}]} \quad \dots(3.28.7)$$

and  $I_{C4} = \frac{I_{EE}}{[1 + e^{V_1/V_T}][1 + e^{-V_2/V_T}]}$  ... (3.28.8)

7. Similarly, substituting eq. (3.28.6) in eq. (3.28.3) and (3.28.4), we get

$$I_{C5} = \frac{I_{EE}}{[1 + e^{V_1/V_T}][1 + e^{V_2/V_T}]} \quad \dots(3.28.9)$$

and  $I_{C6} = \frac{I_{EE}}{[1 + e^{-V_1/V_T}][1 + e^{V_2/V_T}]}$  ... (3.28.10)

8. The differential output current  $\Delta I$  is given by

$$\Delta I = I_{L1} - I_{L2}$$

That is,  $\Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6})$

or  $\Delta I = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5})$  ... (3.28.11)

9. Substituting eq. (3.28.7) to (3.28.10) in eq. (3.28.11) and employing exponential formulae for hyperbolic functions, we get

$$\Delta I = I_{EE} \left[ \tanh\left(\frac{V_1}{2V_T}\right) \tanh\left(\frac{V_2}{2V_T}\right) \right] \quad \dots(3.28.12)$$

eq. (3.28.12) shows that when  $V_1$  and  $V_2$  are small, the GILBERT cell shown in Fig. 3.28.1 can be used as a four-quadrant analog multiplier with the use of current-to-voltage converters.

**VERY IMPORTANT QUESTIONS**

***Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.***

**Q. 1. What are types of frequency compensation ? Explain any one.**

**Ans.** Refer Q. 3.1.

**Q. 2. What is the effect of negative feedback on non-linearity ?**

**Ans.** Refer Q. 3.9.

**Q. 3. Describe temperature compensated log amplifier using two op-amp and explain its operation.**

**Ans.** Refer Q. 3.12.

**Q. 4. Draw the circuit diagram of full wave precision rectifier and find expression for output voltage for both positive and negative half cycle of input sinusoidal waveform.**

**Ans.** Refer Q. 3.15.

**Q. 5. Describe the sample and hold circuit with the help of an Op-Amp. What are the applications of sample and hold circuit ?**

**Ans.** Refer Q. 3.17.

**Q. 6. Describe the Schmitt trigger with help of proper circuit diagram and transfer characteristics.**

**Ans.** Refer Q. 3.20.

**Q. 7. Draw and explain the working of monostable multivibrator using Op-Amp.**

**Ans.** Refer Q. 3.23.

**Q. 8. Explain the generation of square and triangular waveforms from astable multivibrator operation using Op-Amp. Also find expression of the time period for both cases.**

**Ans.** Refer Q. 3.26.

**Q. 9. What do you mean by the quadrant operation of multiplier ? Draw and explain a GILBERT analog multiplier.**

**Ans.** Refer Q. 3.28.



**4****UNIT****Digital Integrated  
Circuit Design****CONTENTS**

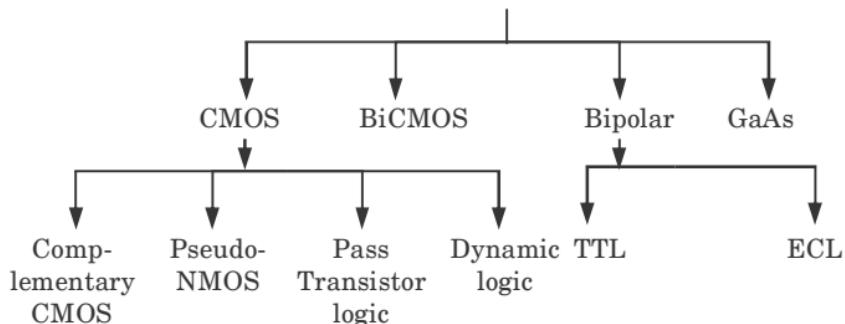
- 
- Part-1 :** An Overview, CMOS Logic Gate ..... **4-2A to 4-16A**  
Circuits, Basic Structure, CMOS  
Realization of Inverters, AND,  
OR, NAND and NOR Gates
- Part-2 :** Latches and Flip-Flops : ..... **4-16A to 4-23A**  
The Latch, CMOS  
Implementation of SR  
Flip-Flops, a Simpler CMOS  
Implementation of the Clocked  
SR Flip-Flop, CMOS Implementation  
of J-K Flip-Flops,  
D Flip-Flop Circuits

## PART- 1

*An Overview, CMOS Logic Gate Circuits, Basic Structure, CMOS Realization of Inverters, AND, OR, NAND and NOR Gates.*

### CONCEPT OUTLINE

- Digital IC technologies and logic-circuit families



- CMOS technology is the most dominant of all the IC technologies available for digital circuit design.

### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

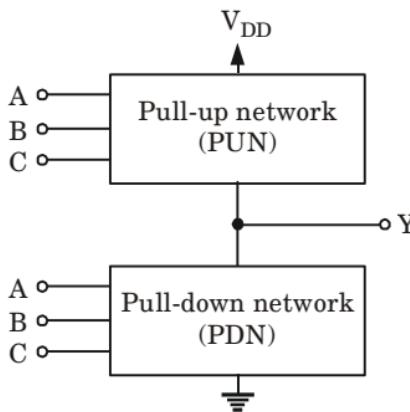
**Que 4.1. Discuss CMOS circuit and its features.**

#### **Answer**

**A. CMOS circuit :**

1. The CMOS logic gate consists of two networks.
- i. The pull-down network (PDN) constructed of NMOS transistor.
- ii. The pull-up network (PUN) constructed of PMOS transistors.
2. The two networks are operated by the input variables, in a complementary fashion.
3. Thus, for the three-input gate represented in Fig. 4.1.1, the PDN will conduct for all input combinations that require a low output ( $Y = 0$ ) and will then pull the output node down to ground, causing a zero voltage to appear at the output,  $v_y = 0$ .
4. Simultaneously, the PUN will be OFF, and no direct DC path will exist between  $V_{DD}$  and ground. On the other hand, all input combinations that call for a high output ( $Y = 1$ ) will cause the PUN to conduct, and the

PUN will then pull the output node up to  $V_{DD}$ , establishing an output voltage  $v_y = V_{DD}$ .



**Fig. 4.1.1.** Representation of a three-input CMOS logic gate.

The PUN comprises PMOS transistors, and the PDN comprises NMOS transistors.

- Simultaneously, the PDN will be cut-off, and again, no DC current path between  $V_{DD}$  and ground will exist in the circuit.

#### B. Features :

- The output is always connected to  $V_{DD}$  or GND and in steady state; it gives full logic swing (between 0 V and  $V_{DD}$ ) voltage transfer characteristics and large noise margins.
- Logic levels are not dependent upon the relative sizes of the devices.
- There is no direct path between  $V_{DD}$  and GND in steady state. Thus, static power dissipation of CMOS circuit is negligible.
- It has high input impedance and fast switching speed.

**Que 4.2.** Explain the effect of fan-in and fan-out on propagation delay in CMOS digital logic circuit.

#### Answer

- The fan-in of a gate is the number of its inputs. Each additional input to a CMOS gate requires two additional transistors, one NMOS and one PMOS.
- The additional transistor not only increases the chip area but also the total effective capacitance per gate and increases the propagation delay.
- By increasing device size, we are able to preserve the current-driving capability.
- However, the capacitance  $C$  increases because of both the increased number of inputs and increase in device size. Normally delay increases following a quadratic function of fan-in.

5. An increase in a gate's fan-out adds directly to its load capacitance and thus, increases its propagation delay.

**Que 4.3.** Explain the working operation of CMOS inverter with VTC characteristics.

**Answer**

**A. CMOS inverter circuit :**

- Fig. 4.3.1 shows the CMOS inverter. In the CMOS inverter, the PMOS and NMOS devices  $Q_P$  and  $Q_N$  are driven simultaneously by an input  $V_{in}$ .

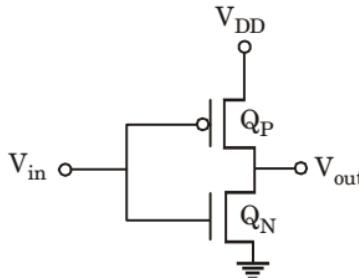


Fig. 4.3.1. CMOS inverter circuit.

**B. Working operation :**

- When input is high ( $\approx V_{DD}$ )  $Q_N$  is made to conduct, while  $Q_P$  is forced to cut-off. This causes the output becomes low ( $V_o = 0$ ) as shown in Fig. 4.3.2.

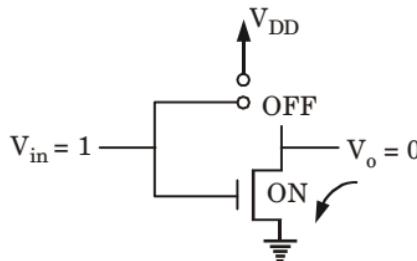


Fig. 4.3.2.

- When input is low ( $\approx 0$  V)  $Q_N$  becomes ON and  $Q_P$  becomes OFF, therefore the output becomes logic high ( $V_o = V_{DD}$ ) as shown in Fig. 4.3.3.

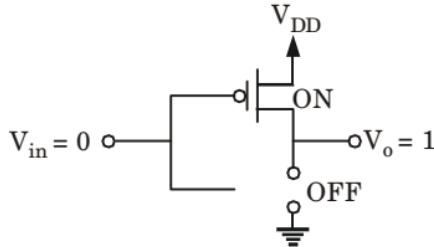


Fig. 4.3.3.

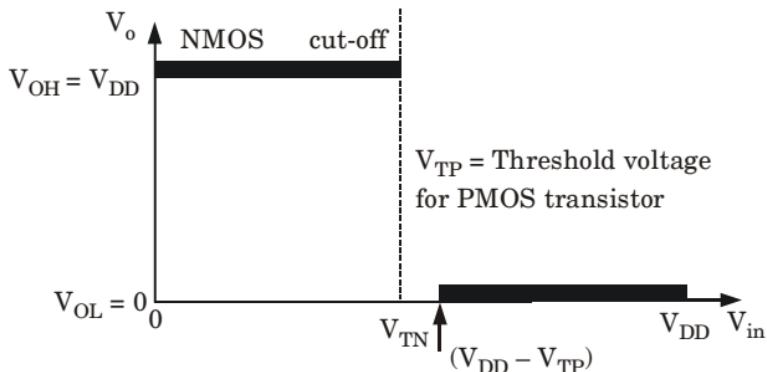
3. Table 4.3.1 shows the operation of COMS inverter circuit.

**Table 4.3.1.**

$V_{in}$	$Q_P$	$Q_N$	$V_o$
0	ON	OFF	1
1	OFF	ON	0

**C. Voltage transfer characteristics :**

- As shown in Fig. 4.3.4, the more positive output voltage corresponds to a logic 1 is  $V_{OH} = V_{DD}$ , and the more negative output voltage corresponds to a logic 0 is  $V_{OL} = 0$ .
- When output is in the logic 0 state, the PMOS transistor is cut-off and when the output is in the logic 1 state, the NMOS transistor is cut-off.



**Fig. 4.3.4.**

**Que 4.4.**

Derive the formula for  $V_{IL}$  and  $V_{IH}$  of CMOS inverter.

**AKTU 2016-17, Marks 7.5**

**AKTU 2018-19, Marks 07**

**OR**

Describe different regions of operation for CMOS inverter over its VTC characteristics.

**Answer**

- The NMOS transistor operates in saturation if  $V_{in} > V_{T0,N}$  and if the following condition is satisfied.

$$V_{DS,N} \geq V_{GS,N} - V_{T0,N} \Leftrightarrow V_{out} \geq V_{in} - V_{T0,N} \quad \dots(4.4.1)$$

- The PMOS transistor operates in saturation if  $V_{in} < (V_{DD} + V_{T0,P})$ , and if:

$$V_{DS,P} \leq V_{GS,P} - V_{T0,P} \Leftrightarrow V_{out} \leq V_{in} - V_{T0,P} \quad \dots(4.4.2)$$

- The table 4.4.1 lists these regions and the corresponding critical input and output voltage levels.

Table 4.4.1.

Region	$V_{in}$	$V_{out}$	NMOS	PMOS
A	$< V_{T0, N}$	$V_{OH}$	cut-off	linear
B	$V_{IL}$	high $\approx V_{OH}$	saturation	linear
C	$V_{th}$	$V_{th}$	saturation	saturation
D	$V_{IH}$	low $\approx V_{OL}$	linear	saturation
E	$> (V_{DD} + V_{T0, P})$	$V_{OL}$	linear	cut-off

- In region A, where  $V_{in} < V_{T0, N}$ , the NMOS transistor is cut-off and the output voltage is equal to  $V_{OH} = V_{DD}$ .
- As the input voltage is increased beyond  $V_{T0, N}$  (into region B), the NMOS transistor starts conducting in saturation mode and the output voltage begins to decrease. The critical voltage  $V_{IL}$  which corresponds to  $(d V_{out} / d V_{in}) = -1$  is located within region B.
- As the output voltage further decrease, the PMOS transistor enters saturation at the boundary of region C. It is seen from, Fig. 4.4.1 that the inverter threshold voltage, where  $V_{in} = V_{out}$ , is located in region.

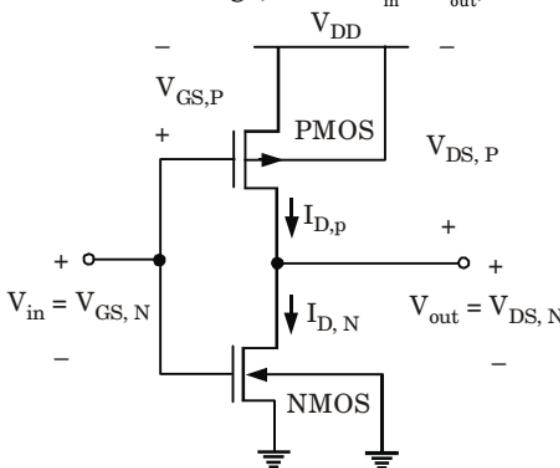
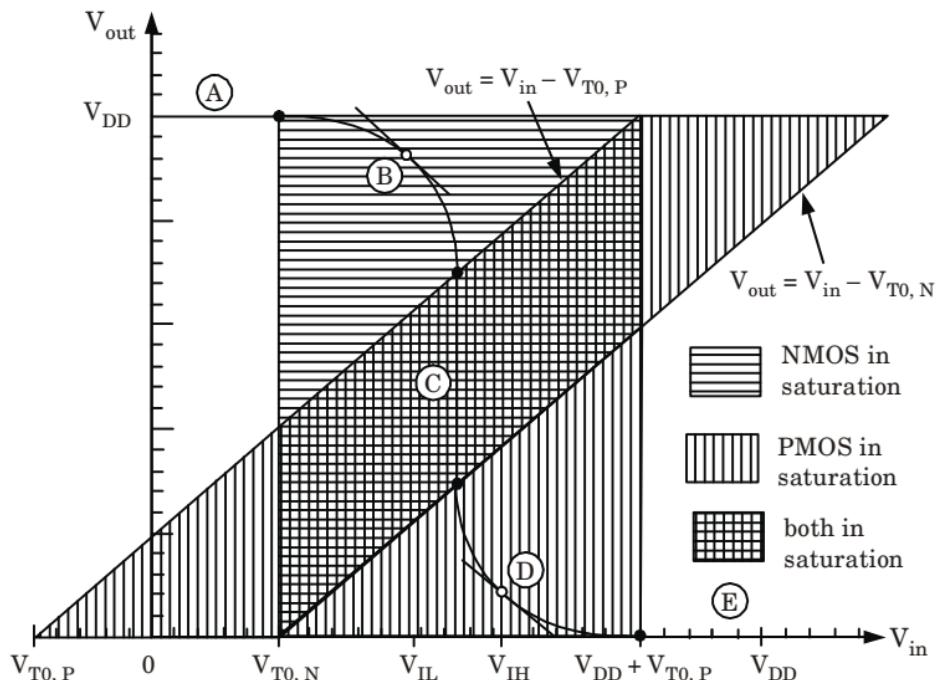


Fig. 4.4.1. CMOS inverter circuit.

- When the output voltage  $V_{out}$  falls below  $(V_{in} - V_{T0, N})$ , the NMOS transistor starts to operate in linear mode. This corresponds to region D in Fig. 4.4.2, where the critical voltage point  $V_{IH}$  with  $(d V_{out} / d V_{in}) = -1$  is also located.
- Finally, in region E, with the input voltage  $V_{in} > (V_{DD} + V_{T0, P})$ , the PMOS transistor is cut-off, and the output voltage is  $V_{OL} = 0$ .



**Fig. 4.4.2.** Operating regions of the NMOS and the PMOS transistors.

### Calculation of $V_{IL}$ :

1. By definition, the slope of the VTC is equal to  $(-1)$ , i.e.,  $dV_{out}/dV_{in} = -1$  when the input voltage is  $V_{in} = V_{IL}$ .
2. Note that in this case, the NMOS transistor operates in saturation while the PMOS transistor operates in the linear region.
3. From  $I_{D,N} = I_{D,P}$ , we obtain the following current equation :

$$\frac{k_n}{2} (V_{GS,N} - V_{T0,N})^2 = \frac{k_p}{2} [2(V_{GS,P} - V_{T0,P})V_{DS,P} - V_{DS,P}^2] \quad \dots(4.4.1)$$

$$\frac{k_n}{2} (V_{in} - V_{T0,N})^2 = \frac{k_p}{2} [2(V_{in} - V_{DD} - V_{T0,P})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2] \quad \dots(4.4.2)$$

4. To satisfy the derivative condition at  $V_{IL}$ , we differentiate both sides of eq. (4.4.2) with respect to  $V_{in}$ .

$$\begin{aligned} k_n (V_{in} - V_{T0,N}) &= k_p \left[ (V_{in} - V_{DD} - V_{T0,P}) \left( \frac{dV_{out}}{dV_{in}} \right) + (V_{out} - V_{DD}) \right. \\ &\quad \left. - (V_{out} - V_{DD}) \left( \frac{dV_{out}}{dV_{in}} \right) \right] \end{aligned} \quad \dots(4.4.3)$$

5. Substituting  $V_{in} = V_{IL}$  and  $(dV_{out}/dV_{in}) = -1$  in eq. (4.4.3), we obtain

$$k_n(V_{IL} - V_{T0,N}) = k_p(2V_{out} - V_{IL} + V_{T0,P} - V_{DD}) \quad \dots(4.4.4)$$

6. The critical voltage  $V_{IL}$  can now be found as a function of the output voltage  $V_{out}$ , as follows :

$$V_{IL} = \frac{2V_{out} + V_{T0,P} - V_{DD} + k_R V_{T0,N}}{1 + k_R} \quad \dots(4.4.5)$$

where  $k_R$  is defined as,

$$k_R = \frac{k_n}{k_p}$$

### Calculation of $V_{IH}$ :

- When the input is equal to  $V_{IH}$ , the NMOS transistor operates in the linear region and the PMOS transistor operates in saturation.
- From  $I_{D,N} = I_{D,P}$

$$\frac{k_n}{2} [2(V_{GS,N} - V_{T0,N})V_{DS,N} - V_{DS,N}^2] = \frac{k_p}{2} (V_{GS,P} - V_{T0,P})^2 \quad \dots(4.4.6)$$

$$\frac{k_n}{2} [2(V_{in} - V_{T0,N})V_{out} - V_{out}^2] = \frac{k_p}{2} (V_{in} - V_{DD} - V_{T0,P})^2 \quad \dots(4.4.7)$$

- Now, differentiate both sides of eq. (4.4.7) with respect to  $V_{in}$ .

$$\begin{aligned} k_n \left[ (V_{in} - V_{T0,N}) \left( \frac{dV_{out}}{dV_{in}} \right) + V_{out} - V_{out} \left( \frac{dV_{out}}{dV_{in}} \right) \right] \\ = k_p (V_{in} - V_{DD} - V_{T0,P}) \end{aligned} \quad \dots(4.4.8)$$

- Substituting  $V_{in} = V_{IH}$  and  $(dV_{out} / dV_{in}) = -1$  in eq. (4.4.8), we obtain  
 $k_n (-V_{IH} + V_{T0,N} + 2V_{out}) = k_p (V_{IH} - V_{DD} - V_{T0,P})$   $\dots(4.4.9)$
- The critical voltage  $V_{IH}$  can now be found as a function of  $V_{out}$  as follows :

$$V_{IH} = \frac{V_{DD} + V_{T0,P} + k_R (2V_{out} + V_{T0,N})}{1 + k_R} \quad \dots(4.4.10)$$

**Que 4.5.** Describe different regions of operation for CMOS inverter over its VTC characteristics.

Consider a CMOS inverter with following parameters :

$$V_{DD} = 3.3 \text{ V}, V_{T0,N} = 0.6 \text{ V}, V_{T0,P} = 0.7 \text{ V},$$

$$k_n = 200 \mu\text{A/V}^2, k_p = 80 \mu\text{A/V}^2$$

Calculate the noise margin of the CMOS inverter circuit.

**AKTU 2015-16, Marks 15**

**Answer**

A. Regions of operation for CMOS : Refer Q. 4.4, Page 4-5A, Unit-4.

**B. Numerical :**

**Given :**  $V_{DD} = 3.3 \text{ V}$ ,  $V_{T0,N} = 0.6 \text{ V}$ ,  $V_{T0,P} = 0.7 \text{ V}$ ,  $k_n = 200 \mu\text{A/V}^2$ ,  
 $k_p = 80 \mu\text{A/V}^2$

**To Find :** Noise margin.

1. We know,  $k_R = \frac{k_n}{k_p} = \frac{200}{80} = 2.5$
2. As  $V_{OL} = 0$  and  $V_{OH} = 3.3 \text{ V}$ , to calculate  $V_{IL}$  in terms of the output voltage, we use

$$\begin{aligned} V_{IL} &= \frac{2V_{out} + V_{T0,P} - V_{DD} + k_R V_{T0,N}}{1 + k_R} \\ &= \frac{2V_{out} - 0.7 - 3.3 + 1.5}{1 + 2.5} \\ &= 0.57 V_{out} - 0.71 \end{aligned} \quad \dots(4.5.1)$$

3. Also,  $k_n(V_{IL} - V_{T0,N}) = k_p(2V_{out} - V_{IL} + V_{T0,P} - V_{DD})$   $\dots(4.5.2)$
4. Putting value of  $V_{IL}$  in eq. (4.5.2), we get

$$\begin{aligned} 2.5(0.57 V_{out} - 0.71 - 0.6)^2 &= 2(0.57 V_{out} - 0.71 - 3.3 + 0.7) \\ (V_{out} - 3.3) - (V_{out} - 3.3)^2 &\quad \dots(4.5.3) \end{aligned}$$

5. This expression yields a second-order polynomial in  $V_{out}$ , as follows :

$$0.66 V_{out}^2 + 0.05 V_{out} - 6.65 = 0 \quad \dots(4.5.4)$$

$$V_{out} = 3.14 \text{ V} \quad \dots(4.5.5)$$

6. From eq. (4.5.1), we can calculate the critical voltage  $V_{IL}$  as :

$$V_{IL} = 0.57 \times 3.14 - 0.71 = 1.08 \text{ V}$$

7. To calculate  $V_{IH}$  in terms of the output voltage, use :

$$V_{IH} = \frac{V_{DD} + V_{T0,P} + k_R (2V_{out} + V_{T0,N})}{1 + k_R} \quad \dots(4.5.6)$$

$$= \frac{3.3 - 0.7 + 2.5(2V_{out} + 0.6)}{1 + 2.5} = 1.43 V_{out} + 1.17 \quad \dots(4.5.7)$$

8. Again,  $k_n(-V_{IH} + V_{T0,N} + 2V_{out}) = k_p(V_{IH} - V_{DD} - V_{T0,P})$   $\dots(4.5.8)$

9. Now, substitute the value of  $V_{IH}$  in eq. (4.5.8),

$$2.5[2(1.43 V_{out} + 1.17 - 0.6)V_{out} - V_{out}^2] = (1.43 V_{out} - 1.43)^2 \quad \dots(4.5.9)$$

$$2.61 V_{out}^2 + 6.94 V_{out} - 2.04 = 0$$

10. On solving, we get,

$$V_{out} = 0.27 \text{ V} \quad \dots(4.5.10)$$

11. From eq. (4.5.9) and (4.5.10) we can calculate the critical voltage  $V_{IH}$  as :

$$V_{IH} = 1.43 \times 0.27 + 1.17 = 1.55 \text{ V}$$

12. Finally, we find the noise margins for low voltage levels and for high voltage levels

$$NM_L = V_{IL} - V_{OL} = 1.08 \text{ V}$$

$$N_{MH} = V_{OH} - V_{IH} = 1.75 \text{ V}$$

**Que 4.6.** Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR-AND-INVERT (OAI) function using CMOS logic circuit.

AKTU 2017-18, Marks 10

AKTU 2019-20, Marks 07

### Answer

- Features of CMOS circuit :** Refer Q. 4.1, Page 4-2A, Unit-4.
- AOI and OAI functions :**
  - AOI and OAI functions can be implemented with just one gate level transistor. Both the complex gates have a propagation delay equivalent to that of a single NAND or NOR gate.
  - AOI and OAI gates are essentially representations of SOP and POS expressions of functions respectively.

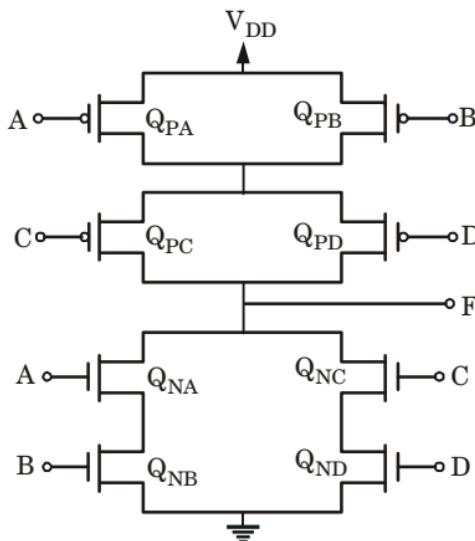


Fig. 4.6.1. AOI realisation using CMOS logic circuit.

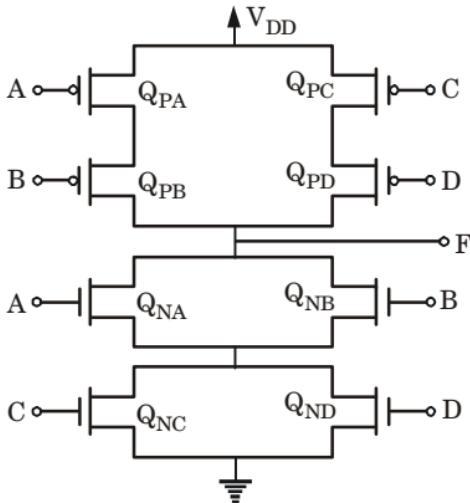
- Let us implement the function,  $F = \overline{AB + CD}$

Here,  $AB$  and  $CD$  are two AND functions and their sum is the OR function, which is finally inverted. Thus  $F$  can be implemented as an AOI gate.

- Fig. 4.6.1 shows the CMOS realization of an AOI gate.

5. The CMOS realization of the OR-AND-INVERT (OAI) gate is the dual of that for the AND-OR-INVERT gate and is easily obtained by flipping the latter end-for-end while interchanging all NMOS circuits with PMOS circuits and vice versa, as shown in Fig. 4.6.2.
6. The output expression for OAI gate is,

$$F = \overline{(A + B)(C + D)}$$



**Fig. 4.6.2.** CMOS realisation of an OAI gate.

**Que 4.7.** Sketch the CMOS logic circuit realization of the expression

$$Y = \overline{A(B + C) + DE}$$

**AKTU 2018-19, Marks 3.5**

**Answer**

CMOS logic circuit realization of

$$Y = \overline{A(B + C) + DE}$$

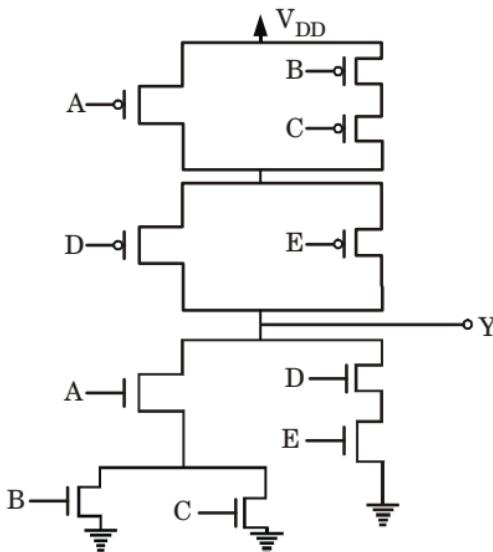


Fig. 4.7.1.

**Que 4.8.** Design a CMOS half adder circuit with inputs  $A$  and  $B$ .

AKTU 2016-17, Marks 7.5

**Answer**

- For CMOS half adder :

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = AB$$

- CMOS half-adder circuit is shown in Fig. 4.8.1.

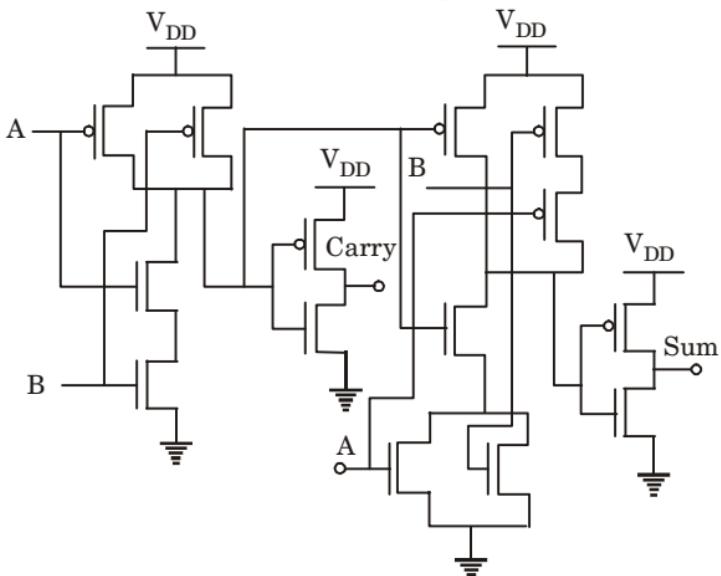


Fig. 4.8.1

**Que 4.9.** Design a CMOS full adder circuit with inputs  $A, B$ , and  $C$  and two outputs  $S$  and  $C_o$ .

**Answer**

1. The sum ( $S$ ) and carry ( $C_o$ ) of the full adder are defined by the following two combinational boolean functions of the three input variables,  $A, B$ , and  $C$ .

Sum,

$$S = A \oplus B \oplus C = ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}C\bar{B}$$

Carry,

$$C_o = AB + AC + BC$$

**CMOS implementation :**

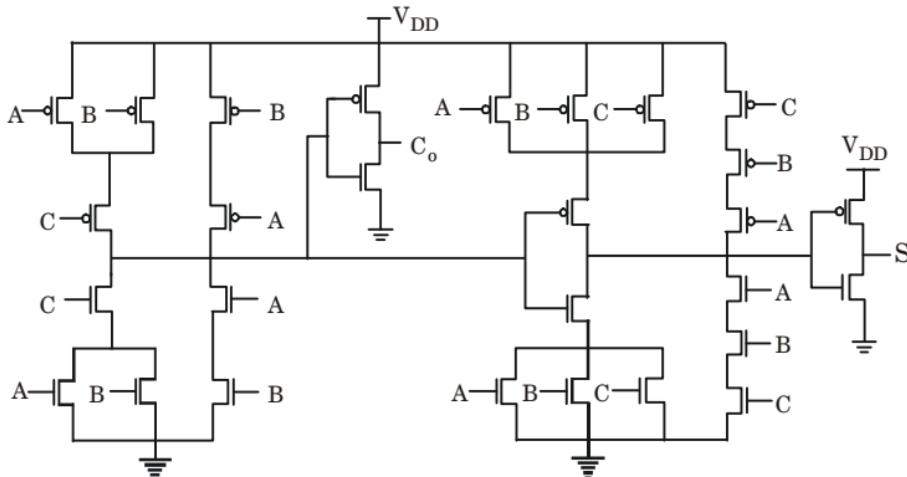


Fig. 4.9.1. Transistor-level schematic of the one-bit full-adder circuit.

**Que 4.10.** Realize the circuit of 2 input NOR gate and 2 input NAND gate using CMOS and explain the operation.

AKTU 2019-20, Marks 07

**Answer**

**A. 2 input NOR gate :**

Realization of 2 input NOR gate circuit is shown in Fig. 4.10.1.

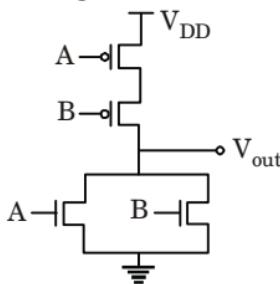


Fig. 4.10.1.

**Operation :** The logic operation of NOR gate is such that the output is HIGH only when all inputs are LOW for remaining all other conditions, the output is LOW.

### B. 2 input NAND gate :

Realization of 2 input NAND gate circuit is shown in Fig. 4.10.2.

**Operation :** A NAND gate produces a LOW output only when all the inputs are HIGH. When any of the inputs is LOW, the output will be HIGH.

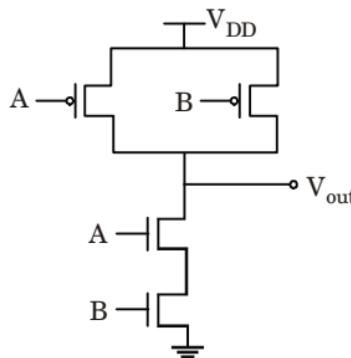


Fig. 4.10.2.

**Que 4.11.** Sketch a CMOS logic circuit that realizes the function :

$$\begin{aligned} F_1 &= ABC + DEF && \text{(use only CMOS NOR gate)} \\ F_2 &= (A + B + C)(D + E + F) && \text{(use only CMOS NAND gate)} \end{aligned}$$

### Answer

1. Given,  $F_1 = ABC + DEF = \overline{\overline{ABC} \cdot \overline{DEF}} = (\overline{A} + \overline{B} + \overline{C}) \cdot (\overline{D} + \overline{E} + \overline{F})$

**CMOS logic circuit :**

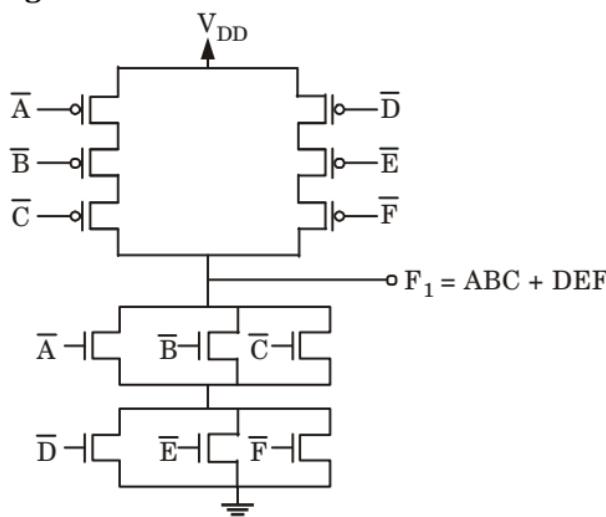


Fig. 4.11.1.

2. Given,

$$\begin{aligned} F_2 &= (A + B + C)(D + E + F) \\ &= \overline{(A + B + C)} + \overline{(D + E + F)} \\ &= (\overline{A}\ \overline{B}\ \overline{C}) + (\overline{D}\ \overline{E}\ \overline{F}) \end{aligned}$$

**CMOS logic circuit :**

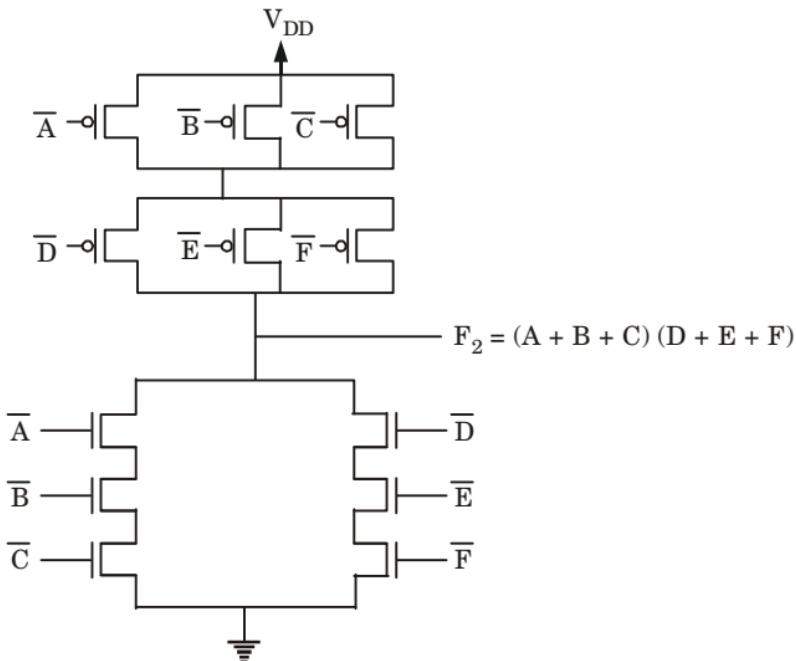


Fig. 4.11.2.

**Que 4.12.** Give two different CMOS realization of the Exclusive-OR gate function in which the PDN and PUN are dual network.

AKTU 2017-18, Marks 05

### Answer

1. For Exclusive - OR function we have,

$$Y = A\bar{B} + \bar{A}B$$

and

$$\begin{aligned} \bar{Y} &= \overline{A\bar{B} + \bar{A}B} = \overline{A\bar{B}} \cdot \overline{\bar{A}B} = (\bar{A} + B) \cdot (A + \bar{B}) \\ &= AB + \bar{A}\bar{B} \end{aligned}$$

#### Realization I :

- Note that Fig. 4.12.1(b) is drawn by converting parallel networks of Fig. 4.12.1(a) to serial networks.
- Now by connecting PUN of Fig. 4.12.1(a) with PDN of Fig. 4.12.1(b) we can realize Exclusive-OR function.

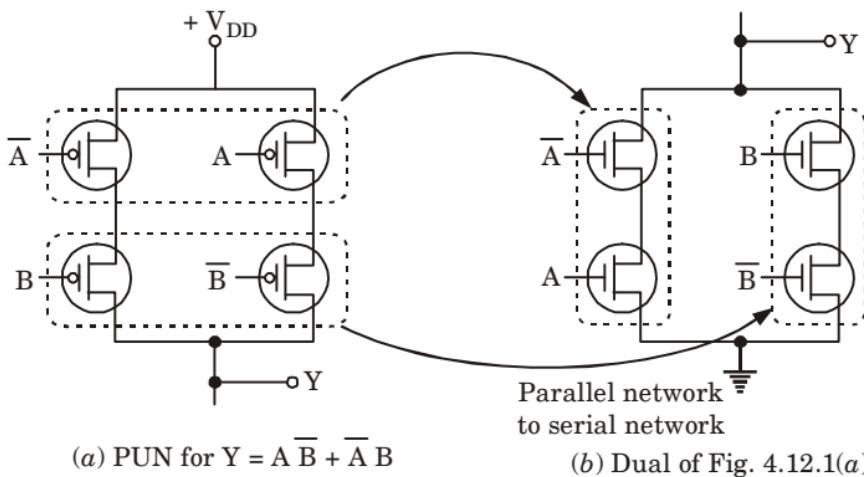


Fig. 4.12.1.

**Realization II :**

PDN for  $\bar{Y} = AB + \bar{A}\bar{B}$  is shown in Fig. 4.12.2(a).

4. Note that Fig. 4.12.2(b) is drawn by converting series networks into parallel networks.
5. Now by connecting PUN of Fig. 4.12.2(b) with PDN of Fig. 4.12.2(a) we can realize Exclusive-OR function.

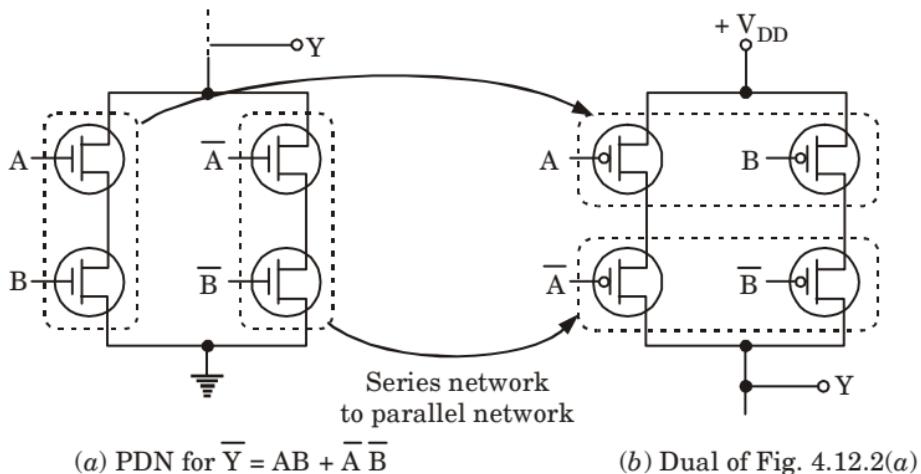


Fig. 4.12.2.

**PART-2**

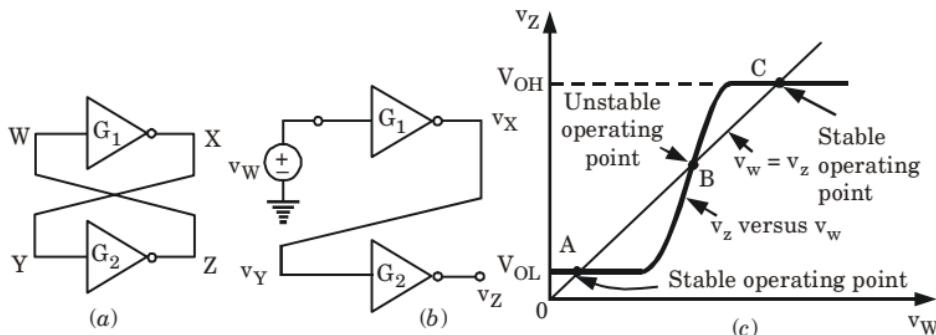
*Latches and Flip-Flops : The Latch, CMOS Implementation of SR Flip-Flops, a Simpler CMOS Implementation of the Clocked SR Flip-Flop, CMOS Implementation of J-K Flip-Flops, D Flip-Flop Circuits.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 4.13.** Write a short note on latch.

**Answer**

1. The basic memory element, the latch, is shown in Fig. 4.13.1(a). It consists of two cross-coupled logic inverters,  $G_1$  and  $G_2$ .
2. The inverters form a positive feedback loop. To investigate the operation of the latch we break the feedback loop at the input of one of the inverters, say  $G_1$  and apply an input signal,  $v_W$ , as shown in Fig. 4.13.1(b).
3. Assuming that the input impedance of  $G_1$  is large, breaking the feedback loop will not change the loop voltage transfer characteristic, which can be determined from the circuit of Fig. 4.13.1(b) by plotting  $v_Z$  versus  $v_W$ .
4. This is the voltage transfer characteristic of two cascaded inverters and thus takes the shape shown in Fig. 4.13.1(c).



**Fig. 4.13.1.** (a) Basic latch. (b) The latch with the feedback loop opened.  
(c) Determining the operating point(s) of the latch.

5. Observe that the transfer characteristic consists of three segments with the middle segment corresponding to the transition region of the inverters.
6. Also shown in Fig. 4.13.1(c) is a straight line with unity slope. This straight line represents the relationship  $v_W = v_Z$  that is realized by reconnecting  $Z$  to  $W$  to close the feedback loop.
7. As indicated the straight line intersects the loop transfer curve at three points,  $A$ ,  $B$  and  $C$ . Thus, any of these three points can serve as the operating point for the latch.
8. While points  $A$  and  $C$  are stable operating points in the sense that the circuit can remain at either indefinitely, point  $B$  is an unstable operating point, the latch cannot operate at  $B$  for any significant period of time.

**Que 4.14.** Realize a simpler CMOS implementation of clocked SR flip flop. Also explain the working of circuit.

AKTU 2016-17, Marks 10

**OR**

Give CMOS implementation of a SR flip-flop and explain its working.

AKTU 2017-18, Marks 05

AKTU 2019-20, Marks 07

**OR**

Give CMOS implementation of a clocked SR flip-flop and explain its working.

AKTU 2018-19, Marks 07

### Answer

**A. Clocked SR flip-flop using NAND gate :** Fig. 4.14.1 shows gate level schematic of clocked NAND based SR flip-flop circuit.

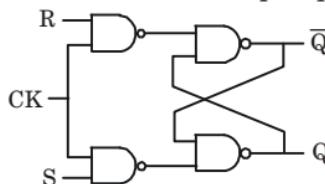


Fig. 4.14.1.

**B. CMOS Implementation :**

1. A simpler implementation of a clocked SR flip-flop is shown in Fig. 4.14.2. Here, pass transistor logic is employed to implement the clocked set-reset function.

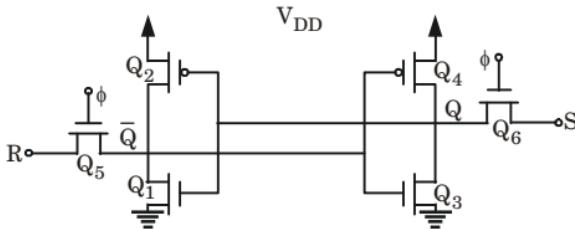


Fig. 4.14.2. A simpler CMOS implementation of the clocked SR flip-flop.

2. The SR flip-flop comprising two cross-coupled inverters and two pass transistors  $Q_5$  and  $Q_6$ . The pass transistors are turned ON when the clock ( $\phi$ ) is high, and they connect the flip-flop input S and R. The pass transistors act as transmission gates allowing the inputs S and R.

**C. Operation :**

1. Consider the flip-flop output has the initial state  $Q = 1$  and  $\bar{Q} = 0$ , and the input  $R = 1$  and  $S = 0$  is applied to the input of flip-flop.
2. When the clock  $\phi$  is high, the transistors  $Q_5$  and  $Q_6$  are turned ON.

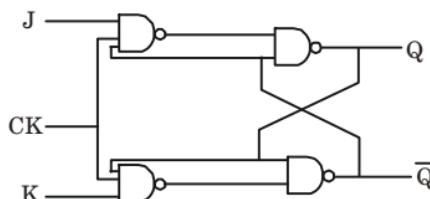
3. For this input  $R = 1$  and  $S = 0$ , the transistor  $Q_3$  is turned ON and pull down the output  $Q = 0$ .
4. These output  $Q$  is applied to the input of  $Q_2$  and  $Q_1$  transistors, this will make the transistor  $Q_2$  is turned ON and the output  $\bar{Q}$  becomes high.
5. Now consider the output has initial state  $Q = 0$  and  $\bar{Q} = 1$ , and the input  $R = 0$  and  $S = 1$ . When the clock  $\phi$  is high, the pass transistors  $Q_5$  and  $Q_6$  are turned ON. For this input  $R = 0$  and  $S = 1$ , the transistor  $Q_1$  turned ON and  $Q_2$  is turned OFF.
6. This causes the output  $\bar{Q} = 0$  and  $\bar{Q}$  is applied to the input of transistors  $Q_3$  and  $Q_4$ . Now the transistor  $Q_4$  turned ON and this make the output  $Q$  is high.

**Que 4.15.** Explain the mechanism of JK and Master-slave flip flop with its working.

### Answer

#### A. JK flip-flop :

1. The circuit diagram of JK flip-flop is shown in Fig. 4.15.1.



**Fig. 4.15.1.**

2. In SR flip-flop  $S = R = 1$  is not allowed so SR flip-flop has been overcome by JK flip-flop. The truth table of JK flip-flop is shown below :

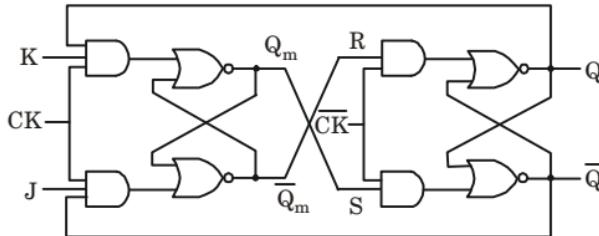
#### Truth Table :

J	K	Q	$Q_{t+1}$	Operation
0	0	0	0 }	No change i.e., $Q_n$
0	0	1	1 }	
0	1	0	0 }	Reset
0	1	1	0 }	
1	0	0	1 }	Set
1	0	1	1 }	
1	1	0	1 }	
1	1	1	0 }	$\bar{Q}$

3. The working of  $JK$  flip-flop is similar to  $SR$  flip-flop except that when  $J = K = 1$ , the output exists i.e., when  $J = K = 1$ , the output is 1, when its previous output is '0' and '0' if its previous output is 1.
4. The condition  $J = K = 1$  arises a major problem i.e., race-around condition. Consider  $J = K = 1$  and  $Q = 0$  and a pulse is applied at clock ( $CK$ ) input.
5. After a time interval  $\Delta t$  equal to propagation delay through two NAND gates in series, the output will change to  $Q = 1$ . In other case if we have  $J = K = 1$  and  $Q = 1$  after another  $\Delta t$  time the output will change back to  $Q = 0$  i.e., the output will oscillate between 0 and 1.
6. At the end of  $CK$ , the output is uncertain and the condition is race-around condition.
7. There are two methods to avoid race-around condition.
  - i.  $JK$  master slave flip-flop.
  - ii. Edge-triggered flip-flop.

#### B. Master-slave flip-flop :

1. This is the cascade network of two  $SR$  flip-flop with feedback from the output of the second to the inputs of the first.
2. The master-slave flip-flop is shown in Fig. 4.15.2.



**Fig. 4.15.2.**

3. When  $CK$  is 1, the master is enabled and the output  $Q_m$  and  $\bar{Q}_m$  responds to inputs ( $J$  and  $K$ ) as shown in truth table of  $JK$  flip-flop.
4. When  $CK$  is 0 then master is disable and slave is in active mode and the outputs  $Q$  and  $\bar{Q}$  follows  $Q_m$  and  $\bar{Q}_m$  respectively.
5. In this circuit, the inputs to the  $R$  and  $S$  AND gates do not change during the clock pulse ( $CK$ ), and therefore the race around condition does not exist.

**Que 4.16.** Sketch the properly labeled master slave  $D$  flip-flop circuit and explain its operation with the help of proper waveform of the clock signal.

**AKTU 2015-16, Marks 10**

**OR**

**Draw the  $D$  flip-flop using CMOS.**

**AKTU 2018-19, Marks 3.5**

**Answer**

#### A. $D$ flip-flop :

1. The  $D$  flip-flop has two inputs, data input  $D$  and a clock input  $\phi$ . The complementary outputs are labeled as  $Q$  and  $\bar{Q}$ .

2. When clock is low, the flip-flop is in the memory or reset state, and any changes on  $D$  input line have no effect on the state of flip-flop.
3. As clock goes high, flip-flop output is equal to  $D$  line just before the rising edge of the clock, such flip-flop is said to be edge triggered.
4. A CMOS based circuit implementation of  $D$  flip-flop is shown in Fig. 4.16.1.
5. The circuit consists of two inverters connected in positive feedback loop, and the loop is closed at particular time when the clock is low ( $\phi = 0$  and  $\bar{\phi} = 1$ ).
6. The input  $D$  is connected to the flip-flop through the switch that closes when the clock is high.

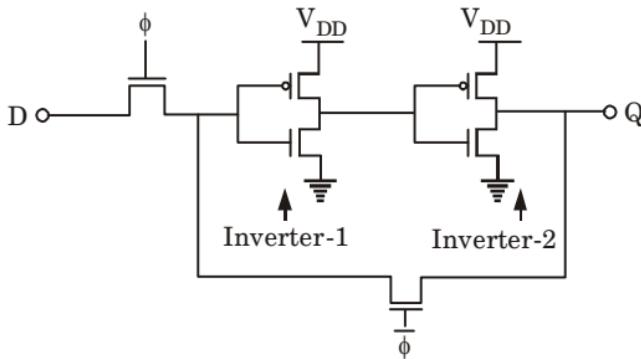


Fig. 4.16.1.

7. When  $\phi$  is high, the loop is opened, the  $D$  input connected to input of inverter 1.
8. The capacitance at input node of inverter 1 is charged to value of  $D$ , while capacitance at input node of inverter 2 is charged to value of  $\bar{D}$ .
9. When clock is low, the input line is isolated from flip-flop, the feedback loop is closed and the latch requires the state corresponding to the value of  $D$  just before  $\phi$  went down and providing an output  $Q = D$ .

#### B. Master-slave $D$ flip-flop :

1. The master-slave consists of pair of  $D$  flip-flop circuits as shown in Fig. 4.16.2. To emphasize that two clock phases must be non-overlapping, we denote them by  $\phi_1$  and  $\phi_2$ .

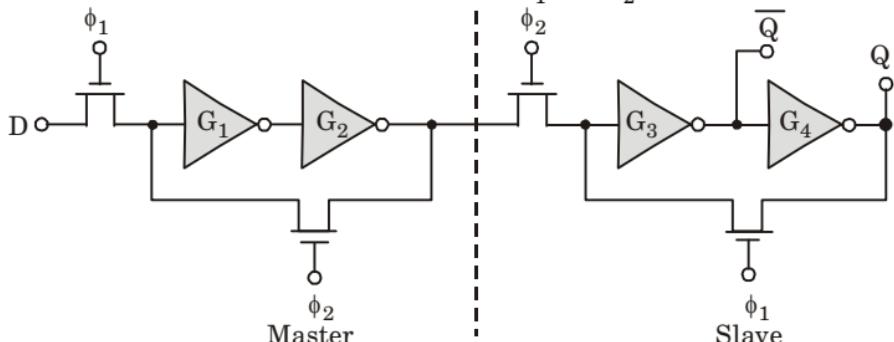
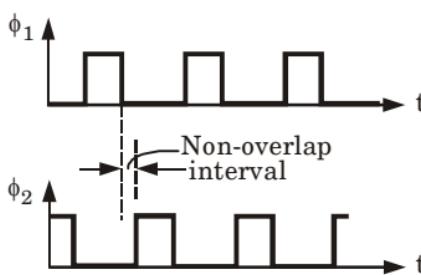


Fig. 4.16.2.

**Fig. 4.16.3** Waveforms of the two-phase non-overlapping clock required.

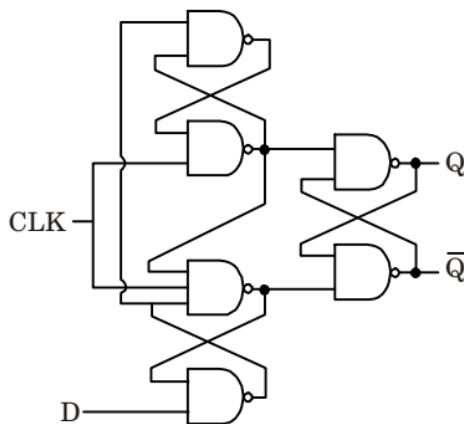
- When  $\phi_1$  is high and  $\phi_2$  is low, the input is connected to the master latch whose feedback loop is opened, while the slave latch is isolated.
- Thus, the output  $Q$  remains at the value stored previously in the slave latch whose loop is now closed. The node capacitances of master latch are charged to the appropriate voltages corresponding to the present value of  $D$ .
- When  $\phi_1$  goes low, the master latch is isolated from input data line  $D$ . When  $\phi_2$  goes high, the feedback loop of the master latch is closed, locking in the value of  $D$ . Further, its output is connected to the slave latch whose loop is now open.
- The node capacitances in the slave are appropriately charged so that, when  $\phi_1$  goes high again, the slave latch locks in the new value of  $D$  and provides the output  $Q = D$ . The  $D$  flip-flop has two inputs, data input  $D$  and a clock input  $\phi$ . The complementary outputs are labeled as  $Q$  and  $\bar{Q}$ .

**Que 4.17.** Discuss **D-F/F circuit using NAND CMOS gates.**

**AKTU 2017-18, Marks 05**

**Answer**

- Fig. 4.17.1 shows the circuit realization of  $D$  flip-flop with CMOS NAND gate. This circuit consists of two stages implemented by  $SR$  NAND latches.

**Fig. 4.17.1.** A positive edge triggered  $D$  flip-flop.

2. The input stage (the two latches on the left) processes the clock and data signals to ensure correct input signals for the output stage (the single latch on the right).
3. If the clock is low, both the output signals of the input stage are high regardless of the data input; the output latch is unaffected and it stores the previous state.
4. When the clock signal changes from low to high, only one of the output voltages (depending on the data signal) goes low and set/resets the output latch. If  $D = 0$ , the lower output becomes low; if  $D = 1$ , the upper output becomes low.
5. If the clock signal continues staying high, the outputs keep their states regardless of the data input and force the output latch to stay in the corresponding state as the input logical zero remains active while the clock is high.
6. Hence the role of the output latch is to store the data only while the clock is low.
7. The  $D$  latch is normally, implemented with transmission gate (TG) switches as shown in the Fig. 4.17.2.

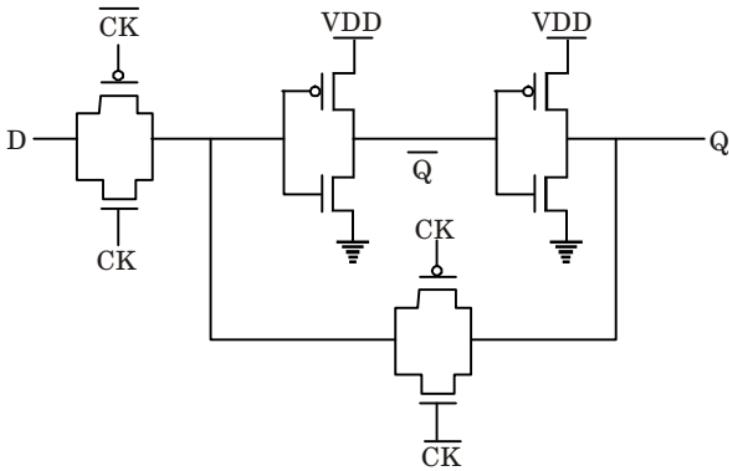


Fig. 4.17.2.

8. Input  $D$  is accepted when  $CK$  is high. When  $CK$  goes low, the input is open-circuited and the latch is set with the prior data  $D$ .

**VERY IMPORTANT QUESTIONS**

***Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.***

**Q. 1. Derive the formula for  $V_{IL}$  and  $V_{IH}$  of CMOS inverter.**

**Ans.** Refer Q. 4.4.

**Q. 2. Describe different regions of operation for CMOS inverter over its VTC characteristics.**

**Consider a CMOS inverter with following parameters :**

$$V_{DD} = 3.3 \text{ V}, V_{T0,N} = 0.6 \text{ V}, V_{T0,P} = 0.7 \text{ V},$$

$$k_n = 200 \mu\text{A/V}^2, k_p = 80 \mu\text{A/V}^2$$

**Calculate the noise margin of the CMOS inverter circuit.**

**Ans.** Refer Q. 4.5.

**Q. 3. Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR-AND-INVERT (OAI) function using CMOS logic circuit.**

**Ans.** Refer Q. 4.6.

**Q. 4. Design a CMOS half adder circuit with inputs A and B.**

**Ans.** Refer Q. 4.8.

**Q. 5. Realize the circuit of 2 input NOR gate and 2 input NAND gate using CMOS and explain the operation.**

**Ans.** Refer Q. 4.10.

**Q. 6. Give two different CMOS realization of the Exclusive-OR gate function in which the PDN and PUN are dual network.**

**Ans.** Refer Q. 4.12.

**Q. 7. Give CMOS implementation of a clocked SR flip-flop and explain its working.**

**Ans.** Refer Q. 4.14.



# 5

UNIT

## Integrated Circuit Timer

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- Part-1 :** Integrated Circuit Timer : ..... **5-2A to 5-11A**  
Timer IC 555 Pin and Functional  
Block Diagram, Monostable and  
Astable Multivibrator using the  
555 IC
- Part-2 :** Voltage Controlled Oscillator : ..... **5-12A to 5-14A**  
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- Part-3 :** Phase Locked Loop (PLL) : ..... **5-14A to 5-21A**  
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Diagram, Working, Ex-OR Gates  
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Applications of PLL

**PART- 1**

*Integrated Circuit Timer : Timer IC 555 Pin and Functional Block Diagram, Monostable and Astable Multivibrator using the 555 IC.*

**CONCEPT OUTLINE**

- The 555 timer is a highly stable device for generating accurate time delay or oscillation.
- Applications of 555 timers include pulse generator, ramp and square wave generator, monostable multivibrator, burglar alarm etc.

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 5.1.** Draw and explain the block diagram of IC 555.

**AKTU 2017-18, Marks 05**

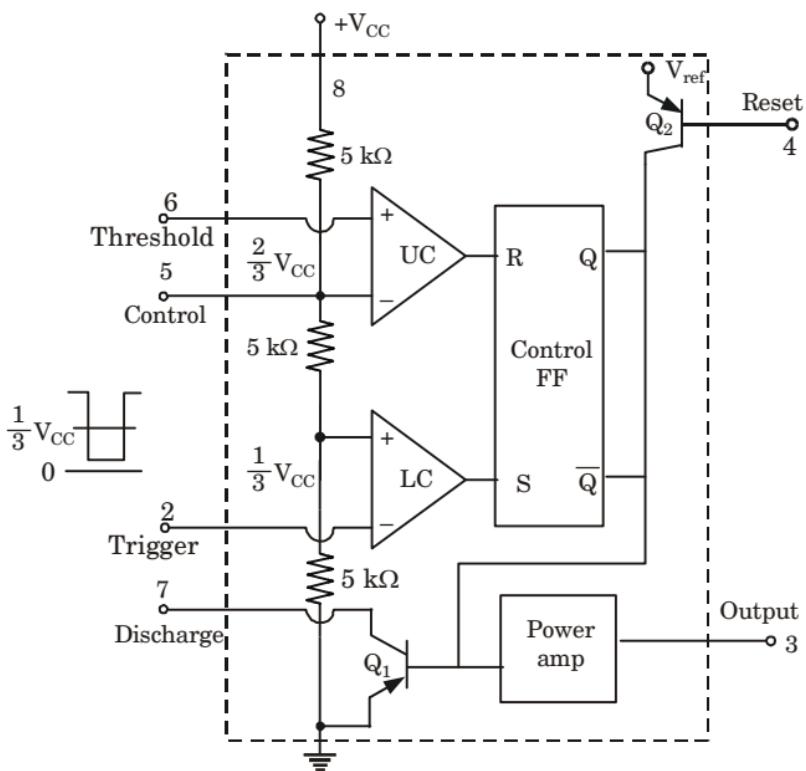
**OR**

**Draw the functional block diagram of IC 555 and explain its working.**

**AKTU 2018-19, Marks 3.5**

**Answer**

1. In the stable state, the output  $\bar{Q}$  of the flip-flop (FF) is high. This makes the output low because of power amplifier which is basically an inverter.
2. If negative going trigger pulse is applied to pin 2 and should have its DC level greater than the threshold level of the lower comparator (*i.e.*,  $V_{CC}/3$ ), now the trigger passes through  $(V_{CC}/3)$ , the output of the lower comparator goes high and sets the FF ( $Q = 1, \bar{Q} = 0$ ). Therefore the output of IC 555 becomes high.
3. When the threshold voltage at pin 6 passes through  $(2/3) V_{CC}$ , the output of the upper comparator goes high and resets the FF ( $Q = 0, \bar{Q} = 1$ ).
4. The reset input (pin 4) is used to reset the FF and the flip flop output  $\bar{Q}$  becomes high and the output of IC 555 becomes low because the output of FF is 1.

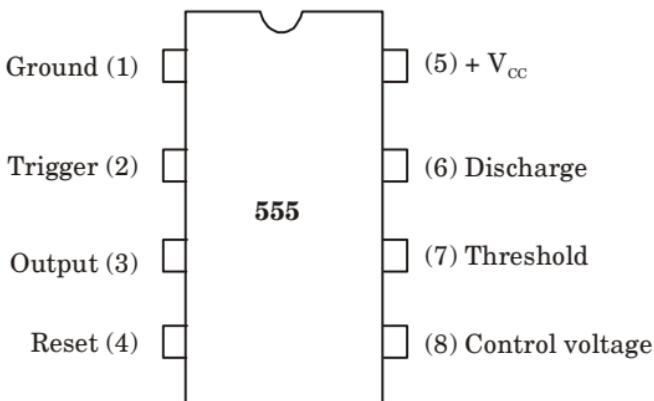


**Fig. 5.1.1.** Functional diagram of IC 555.

**Que 5.2.** Draw the pin-diagram of IC 555 and explain the function of each pin.

**Answer**

- Fig. 5.2.1 shows the pin-diagram of 8-pin DIP 555 timer.



**Fig. 5.2.1.**

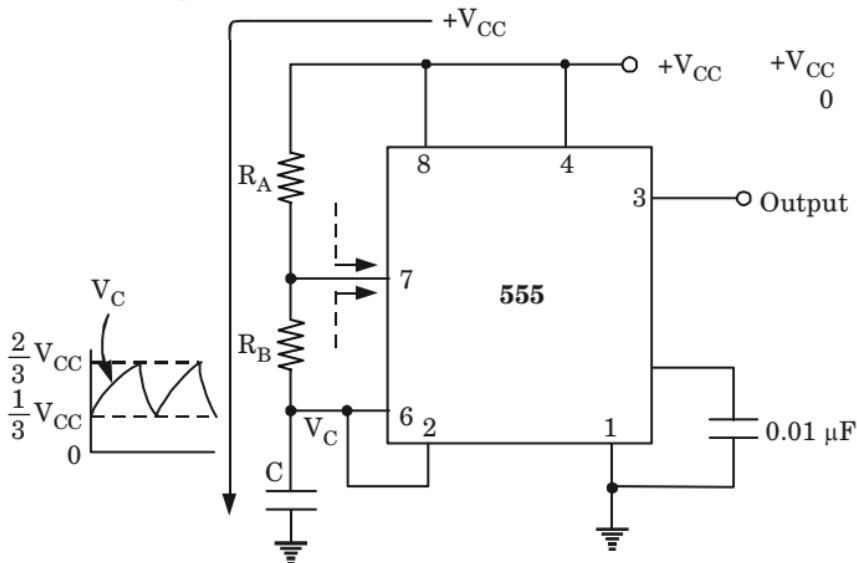
**Function :**

1. **Ground :** All the voltages are measured with respect to this terminal.
2. **Trigger :** The output of the timer is controlled by this pin. The output is low if the voltage is greater than  $2/3 V_{CC}$ . For negative going pulse of amplitude larger than  $1/3 V_{CC}$  is applied to this pin, the comparator II output goes high, which in turn makes the output high as long as the trigger terminal has a low voltage.
3. **Output :** The complementary signal out of the flip-flop goes through an output stage and becomes the output of the timer.
4. **Reset :** This pin is connected to supply *i.e.*,  $+V_{CC}$  in order to avoid any false triggering. Generally pin 4 is not used.
5. **Supply  $+V_{CC}$  :** The 555 times works with supply voltage  $+5\text{ V}$  to  $+18\text{ V}$  with respect to ground.
6. **Discharge :** A capacitor is connected externally to the ground at this pin. Internally the collector of the discharge transistor is coming at this pin. A high  $Q$  output from the flip-flop makes the transistor OFF, *i.e.* open circuit and external capacitor charges at a rate determined by external  $RC$  network. When output  $Q$  is low, transistor gets saturated and external capacitor discharges.
7. **Threshold :** When voltage is greater than or equal to  $2/3 V_{CC}$ , the output of comparator I goes high which makes the output of the timer low.
8. **Control voltage :** The pulse width of output waveform can be varied by imposing a voltage at this pin. In most applications this pin is not required and a capacitor is connected to this pin and ground to prevent noise introduction in the circuit.

**Que 5.3.** What are different modes of operation of IC 555 ? Draw the circuit diagram of a delay circuit using 555. What is maximum delay that can be provided with 555 with a capacitor of  $1000\text{ }\mu\text{F}$  ?

**Answer**

- A. **Modes of operation of IC 555 :** The timer (555) can operate in two modes :
- i. A monostable (one-shot) multivibrator
  - ii. An astable (free running) multivibrator.

**B. Circuit diagram :****Fig. 5.3.1** Astable multivibrator using 555 timer.**C. Numerical :****Given :**  $C = 1000 \mu\text{F}$ **To Find :** Maximum delay.

1. The total period of output waveform is

$$T = t_c + t_d = 0.69 (R_1 + 2R_2)C$$

2. For maximum delay, it is given that

$$C = 1000 \mu\text{F} \text{ and we assume } R_1 = R_2 = 1 \text{ k}\Omega$$

$$T = 0.69 (1 \text{ k}\Omega + 2 \times 1 \text{ k}\Omega) 1000 \times 10^{-6} = 0.69 (3 \text{ k}\Omega) \times 10^3 \times 10^{-6}$$

$$= 0.69 \times 3 = 2.07 \text{ sec}$$

So, the maximum delay is 2.07 seconds.

**Que 5.4.** Draw the functional block diagram of IC 555 and explain its working. Draw the circuit diagram of a monostable multivibrator using 555 and find expression for quasi state period.

**AKTU 2018-19, Marks 07****OR**

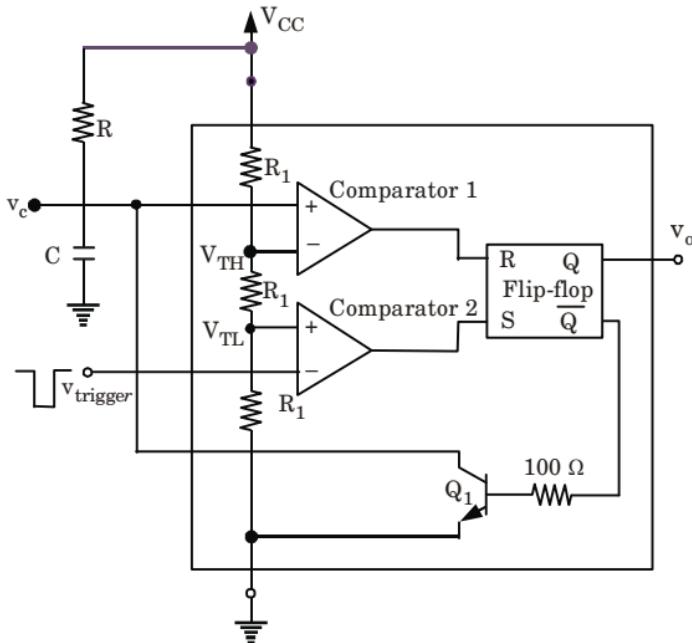
Explain the block diagram of IC 555. Derive the expression for time delay of a monostable multi-vibrator using 555.

**AKTU 2019-20, Marks 07****Answer**

- A. Functional block diagram IC 555 : Refer Q. 5.1, Page 5-2A, Unit-5.

## B. Monostable multivibrator using IC 555 :

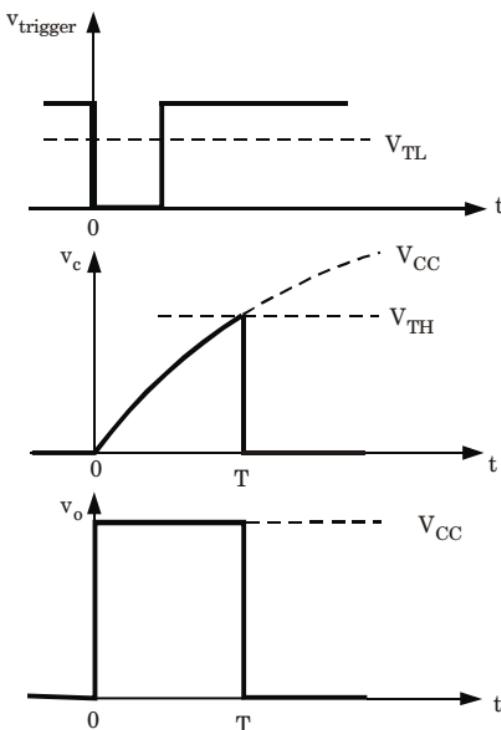
- Fig. 5.4.1 shows a monostable multivibrator implemented using the 555 IC together with an external resistor  $R$  and an external capacitor  $C$ .
- In the stable state the flip-flop will be in the reset state, and thus its  $\bar{Q}$  output will be high, turning ON transistor  $Q_1$ , transistor  $Q_1$  will be saturated, and thus  $v_c$  will be close to 0 V, resulting in a low level at the output of comparator 1.



**Fig. 5.4.1.** The 555 timer connected to implement a monostable multivibrator.

- The voltage at the trigger input terminal, labeled  $v_{trigger}$  is kept high (greater than  $V_{TL}$ ), and thus the output of comparator 2 also will be low.
- Since the flip-flop is in the reset state,  $Q$  will be low and thus  $v_o$  will be closed to 0 V.
- To trigger the monostable multivibrator, a negative input pulse is applied to the trigger input terminal. As  $v_{trigger}$  goes below  $V_{TL}$ , the output of comparator 2 goes high to level, thus setting the flip-flop. Output  $Q$  of the flip-flop goes high, and thus  $v_o$  goes high, and output  $\bar{Q}$  goes low, turning OFF transistor  $Q_1$ .
- Capacitor  $C$  now begins to charge up through resistor  $R$ , and its voltage  $v_c$  rises exponentially toward  $V_{CC}$ , as shown in Fig. 5.4.2 the monostable multivibrator is now in its quasi-stable state.

7. This state prevails until  $v_c$  reaches the threshold of comparator 1,  $V_{TH}$ , at that time the output of comparator 1 goes high, resetting the flip-flop.
8. Output  $Q$  of the flip-flop now goes high and turns ON transistor  $Q_1$ .



**Fig. 5.4.2.** Waveform of the circuit.

9. In turn, transistor  $Q_1$  rapidly discharges capacitor  $C$ , causing  $v_c$  to go to 0 V. Also, when the flip-flop resets its  $Q$ , output goes low and thus  $v_o$  goes back to 0 V. The monostable multivibrator is now back in its stable state and is ready to receive a new triggering pulse.
10. The width of the pulse,  $T$ , is the time interval that the monostable multivibrator spends in the quasi-stable state; it can be determined by reference to the waveforms in Fig. 5.4.2 at which the trigger pulse is applied as  $t = 0$ , the exponential waveform of  $v_c$  can be expressed as

$$v_c = V_{CC}(1 - e^{-t/CR})$$

Substituting  $v_c = V_{TH} = \frac{2}{3}V_{CC}$  at  $t = T$

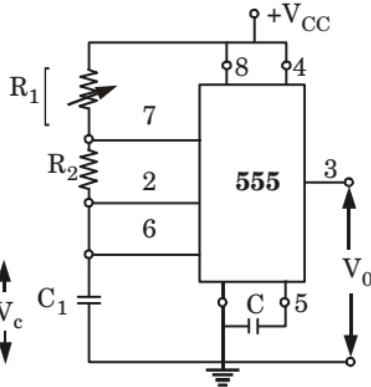
$$T = RC \ln 3 \approx 1.1 RC$$

where,  $T = \text{Time delay}$

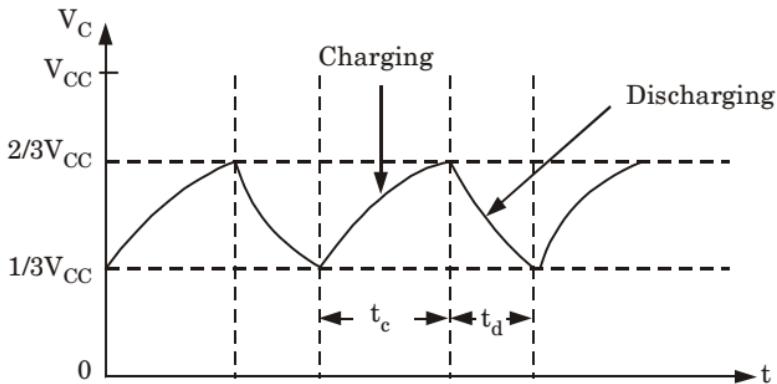
**Que 5.5.** Derive the expression for time delay, duty cycle and frequency of oscillation for astable multivibrator.

**Answer**

1. The circuit using 555 timer in astable mode or in free running is shown in Fig. 5.5.1.
2. The circuit does not require external trigger to change the state of the output and hence is also called free-running multivibrator.

**Fig. 5.5.1.**

3. Pin 2 to pin 6 of timer 555 are shorted, it to work as a free-running multivibrator. When the voltage across capacitor,  $V_C$  equals  $2/3 V_{CC}$ , comparator-1 trigger the flip-flop inside the timer and the output goes low as shown in Fig. 5.5.2.

**Fig. 5.5.2.**

4. At this point the  $C_1$  starts discharging through  $R_2$  and transistor inside the timer. As soon as voltage  $V_c$  equal  $1/3 V_{cc}$  comparator II output triggers the flip-flop and the output goes high. This cycle goes on repeating.
5. The external capacitor  $C_1$  charges through  $R_1$  and  $R_2$  and discharges through  $R_2$  only. So, the duty cycle is set by the ratio of these two resistances. The  $C_1$  charges and discharges between  $2/3 V_{cc}$  and  $1/3 V_{cc}$  respectively.

6. The time during which the capacitor charges from  $1/3 V_{cc}$  to  $2/3 V_{cc}$  is equal to the time the output is high and given by

$$t_c = 0.693 (R_1 + R_2) C_1$$

7. Similarly the time during which the capacitor discharges from  $2/3 V_{cc}$  to  $1/3 V_{cc}$  is equal to the time the output is low and is given by

$$t_d = 0.693 R_2 C_1$$

8. Hence the total period of output waveform is

$$T = t_c + t_d = 0.693 (R_1 + 2R_2) C_1$$

9. The duty cycle is the ratio of time in the high state to the total period  $T$  and is given by

$$\text{Duty cycle} = \frac{t_c}{T} = \frac{(R_1 + R_2)}{(R_1 + 2R_2)}$$

10. The frequency of oscillation is given by,

$$\begin{aligned} f &= \frac{1}{T} = \frac{1}{0.693(R_1 + 2R_2)C_1} \\ &= \frac{1.44}{(R_1 + 2R_2)C_1} \text{ Hz} \end{aligned}$$

**Que 5.6.** Draw the functional block diagram of IC-555 and explain its working. Design a 555 timer as an astable multivibrator with an output signal timer frequency of 700 Hz and 60 % duty cycle.

**AKTU 2015-16, Marks 10**

### Answer

- A. Functional block diagram and working of IC 555 :** Refer Q. 5.1, Page 5-2A, Unit-5.

- B. Numerical :**

**Given :** Duty cycle,  $D = 60\% = 0.6$ ; Frequency,  $f = 700 \text{ Hz}$

**To Design :** 555 timer as an astable multivibrator.

1. Assume,  $C = 0.01 \mu\text{F}$

2. We know,  $D = \frac{R_1 + R_2}{R_1 + 2R_2}$

$$0.6 = \frac{R_1 + R_2}{R_1 + 2R_2} \quad \dots(5.6.1)$$

3. Also,  $f = \frac{1.44}{(R_1 + 2R_2)C}$

$$0.01 \times 10^{-6} \times 700 = \frac{1.44}{R_1 + 2R_2}$$

$$R_1 + 2R_2 = \frac{1.44}{7} \times 10^6 = 2 \times 10^5 \Omega \quad \dots(5.6.2)$$

4. Substituting this value from eq. (5.6.2) in eq. (5.6.1)

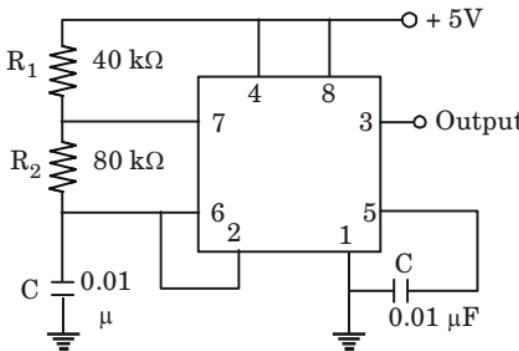
$$0.6 = \frac{R_1 + R_2}{2 \times 10^5}$$

$$12 \times 10^4 = R_1 + R_2 \quad \dots(5.6.3)$$

$$R_B = 80 \text{ k}\Omega$$

$$R_A = 40 \text{ k}\Omega$$

5. The circuit is shown in Fig. 5.6.1.



**Fig. 5.6.1.**

**Que 5.7.** Design a 555 timer as astable multivibrator giving its block diagram which provides an output signal frequency of 2 KHz and 75 % duty cycle.

**AKTU 2017-18, Marks 05**

### Answer

**Given :** Frequency,  $f_c = 2 \text{ KHz}$ , Duty cycle,  $D = 75 \%$

**To Design :** 555 timer as an astable multivibrator.

1. We know,  $T = \frac{1}{f} = \frac{1}{2 \times 10^3} = 0.5 \text{ ms}$

$$D = \frac{T_{\text{ON}}}{T}$$

$$\text{i.e., } T_{\text{ON}} = 0.5 \times 0.75 = 3.75 \times 10^{-4} \text{ sec}$$

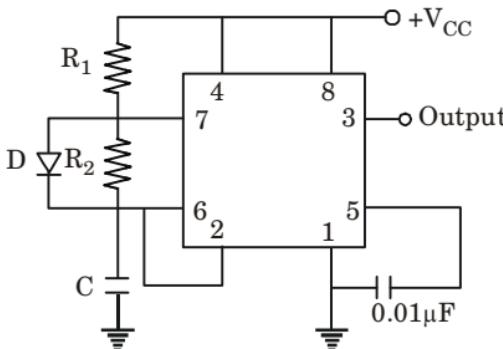
$$T_{\text{OFF}} = T - T_{\text{ON}} = 1.25 \times 10^{-4} \text{ sec}$$

2. Duty cycle is more than 50 % hence modified circuit must be used.  
 3. The modified circuit is shown in Fig. 5.7.1.  
 4. Let  $C = 0.01 \mu\text{F}$

The charging of  $C$  takes place through  $R_1$  and diode  $D$  while discharging takes place through  $R_2$  only

$$\therefore T_{\text{ON}} = 0.693 R_1 C$$

and  $T_{\text{OFF}} = 0.693 R_2 C$



**Fig. 5.7.1.**

5. Using values of  $T_{\text{ON}}$ ,  $T_{\text{OFF}}$  and  $C$ ,

$$R_1 = 8.658 \text{ k}\Omega$$

and  $R_2 = 20.202 \text{ k}\Omega$

**Que 5.8.** For 555 astable multivibrator  $R_A = 4.7 \text{ k}\Omega$ ,  $R_B = 1 \text{ k}\Omega$  and  $C = 1 \mu\text{F}$ . Determine the positive pulse width, the negative pulse width, and the free-running frequency. What is the duty cycle of output waveform ?

**AKTU 2016-17, Marks 10**

### Answer

**Given :**  $R_A = 4.7 \text{ K}\Omega$ ,  $R_B = 1 \text{ K}\Omega$ ,  $C = 1 \mu\text{F}$

**To Find :** Duty cycle,  $D$ .

1. Positive pulse width,

$$t_c = 0.69 (R_A + R_B)C \\ = 0.69 (4.7 \text{ K}\Omega + 1 \text{ K}\Omega) (10^{-6}) = 3.933 \text{ ms}$$

2. Negative pulse width,

$$t_d = 0.69 R_B C \\ = 0.69 (1 \text{ K}\Omega) (10^{-6}) = 0.69 \text{ ms}$$

3. Free-running frequency,

$$f_o = \frac{1}{t_c + t_d} = \frac{1}{(3.933 + 0.69)(10^{-3})} = 0.216 \text{ KHz}$$

4. % Duty cycle =  $\frac{t_c}{t_c + t_d} \times 100 = \frac{3.933}{(3.933 + 0.69)} \times 100 = 85.07 \%$

**PART-2**

*Voltage Controlled Oscillator : VCO IC 566 Pin and Functional Block Diagram and Applications.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

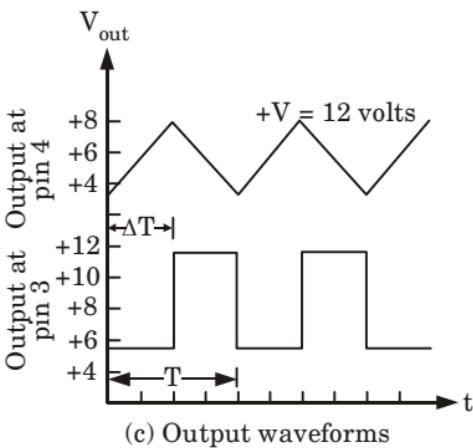
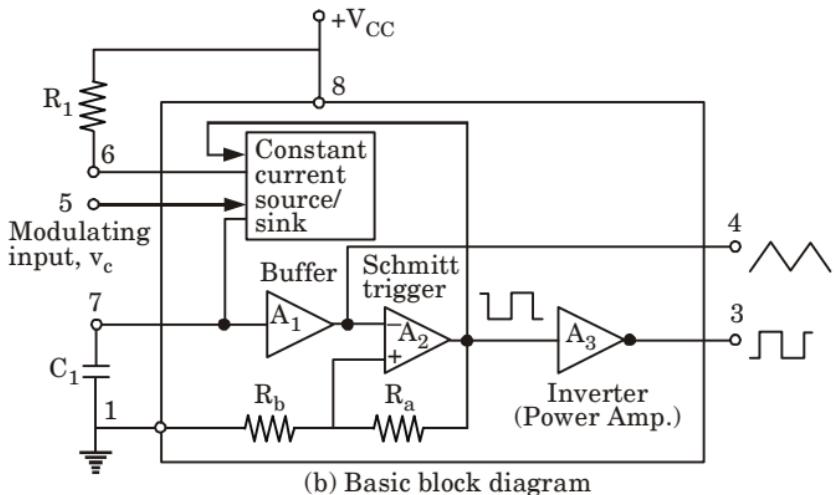
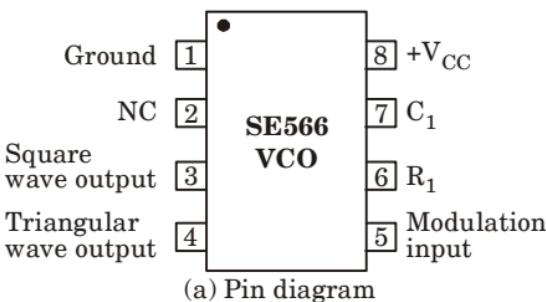
**Que 5.9.** Explain the operation of VCO with help of functional block diagram. Also show the pin-diagram of VCO.

**Answer**

1. The pin configuration and the basic block diagram of IC 566 VCO are shown in the Fig. 5.9.1(a) and (b) respectively. The frequency of oscillation is determined by an externally connected resistor  $R_1$  and a capacitor  $C_1$ .
2. The control voltage or the modulating input  $v_c$  is applied at the control terminal (pin 5).
3. The triangular voltage obtained at pin 4 is shown in Fig. 5.9.2(c). It is generated by alternately charging the capacitor  $C_1$  by one current source, and discharging it linearly through another current source. The amount of charge and discharge voltage swing is determined by the Schmitt trigger.
4. The Schmitt trigger also provides the square-wave output at pin 3 through the power amplifier  $A_3$  and the triangular output is available at pin 4 through the buffer amplifier  $A_1$ .

**Operation of VCO :**

1. The output voltage swing of the Schmitt trigger is set to the levels  $V_{CC}$  and  $0.5V_{CC}$ . In Fig. 5.9.2, if  $R_a = R_b$  in the positive feedback path, the voltage at the non-inverting terminal of Op-Amp  $A_2$  swings from  $0.5 V_{CC}$  to  $0.25 V_{CC}$ .
2. During charging of  $C_1$ , when the voltage across  $C_1$  just exceeds  $0.5 V_{CC}$ , the Schmitt trigger switches to LOW ( $0.5 V_{CC}$ ) and the capacitor starts discharging.
3. When the voltage across  $C_1$  reduces to  $0.25 V_{CC}$ , the Schmitt trigger switches to HIGH ( $V_{CC}$ ).
4. By maintaining the source current and sink current of the two current sources equal, a uniform triangular voltage with equal positive and negative slopes is obtained at pin 4.



**Fig. 5.9.1.** Voltage controlled oscillator.

5. The square-wave output of Schmitt trigger, inverted and buffered is available at pin 3.
6. The waveforms at the output pins 3 and 4 are shown in Fig. 5.9.1(c).

**Que 5.10.** Discuss voltage controlled oscillator in brief. Also write its applications.

**Answer**

- A. VCO :** Refer Q. 5.9, Page 5-12A, Unit-5.
- B. Applications :** The various application of VCO are :
1. Frequency modulation.
  2. Signal generation (Triangular or square wave)
  3. Function generation.
  4. Frequency shift keying i.e. FSK demodulator.
  5. In frequency multipliers.
  6. Tone generation.

**PART-3**

*Phase Locked Loop (PLL) : Basic Principle of PLL, Block Diagram, Working, Ex-OR Gates and Multiplier as Phase Detectors, Applications of PLL.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

- Que 5.11. Explain the types of phase detectors with suitable circuit diagrams and input-output waveforms.**

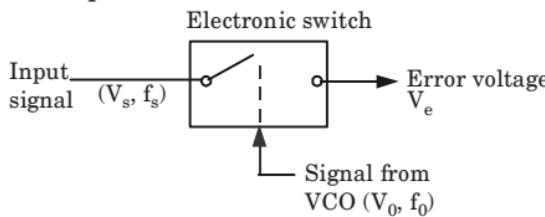
**AKTU 2016-17, Marks 10**

**Answer**

Phase detectors or comparators used in a PLL can be of two types :

**A. Analog phase detector :**

1. Fig. 5.11.1 shows a switch type phase detector. Here, switch is an electronic switch which is being opened and closed by the VCO output signal.
2. Switch is closed only when VCO output is positive and switch is open for negative VCO output.



**Fig. 5.11.1.**

3. Fig. 5.11.2 shows the input signal  $V_s$  at the same frequency  $f_o$  but at different phase shifts  $\phi = 0^\circ, 90^\circ$  and  $180^\circ$ .
4. For  $V_s$  having  $\phi = 0^\circ$ , a positive error voltage will be produced.

- When  $\phi = 90^\circ$ , the average value of error voltage produced at the switch is zero and when  $\phi = 180^\circ$ , only the negative half cycles of input appear across the output, thus error voltage is negative.
- Error voltage is zero for  $\phi = 90^\circ$ , hence perfect lock thus, VCO output and input signal  $V_s$  should be  $90^\circ$  out of phase.

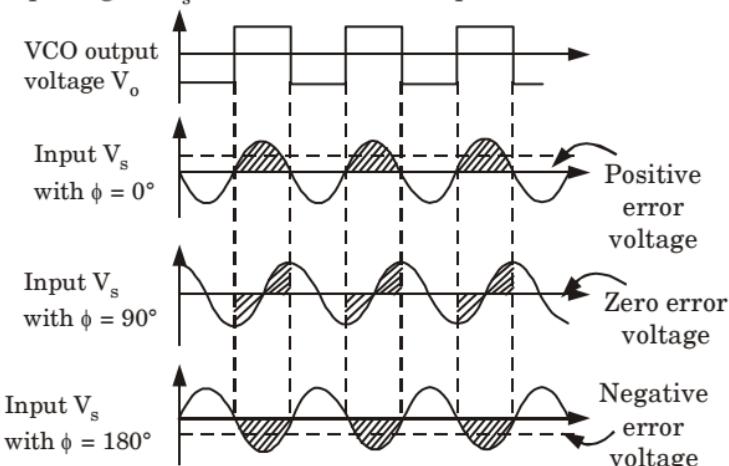


Fig. 5.11.2. I/O waveforms of phase detector.

### B. Digital phase detector :

- A digital phase detector is a simple XOR gate. XOR gate output is high only if one of its inputs is high.
- The two inputs of the gate are connected to the input signal ( $V_s, f_s$ ) and output signal ( $V_o, f_o$ ) respectively.

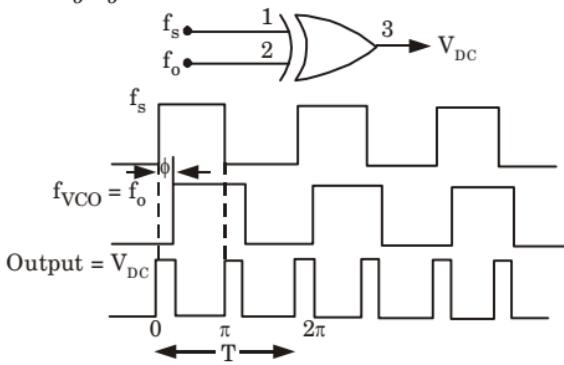


Fig. 5.11.3.

- Output will increase with increase in the phase difference  $\phi$ .
- For  $\phi = 0^\circ$  the waveforms at inputs  $f_s$  and  $f_o$  overlap and output is always zero. Therefore, the average error voltage will be zero. It will be maximum for  $\phi = 180^\circ$ .
- Thus, in this phase detector, phase  $\phi$  must be zero for zero error voltage i.e., for perfect lock condition.

**Que 5.12.** Write a note on Ex-OR as a phase detector.

**Answer**

1. The Exclusive-OR phase detector is shown in Fig. 5.12.1. The output of Ex-OR gate circuit is high only when any one of the two input signals, namely  $f_o$  or  $f_i$  is high.



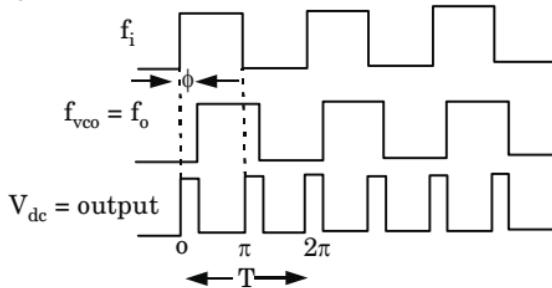
**Fig. 5.12.1.** Exclusive-OR phase detector.

2. The input and output waveform for  $f_i = f_o$  are shown in Fig. 5.12.2. In a digital phase detector, the phase error  $\phi$  is defined as

$$\phi = \frac{\tau}{T} 2\pi$$

where  $T$  is the period of input signals of same frequency and  $\tau$  is the time difference between the leading edges of the two signals.

3. Fig. 5.12.2 shows that  $f_o$  leads  $f_i$  by  $\phi$  degrees and the DC output voltage of the Ex-OR gate is a function of the phase error  $\phi$  between the two inputs.  
 4. Ex-OR phase detector can be realized using ICs such as CD4070. The output DC voltage depends on the duty cycle of the input waveforms. Therefore, this type of phase detector is employed when the waveforms of  $f_i$  and  $f_o$  are of square waveform with 50 % duty cycle.



**Fig. 5.12.2.** Input and output waveforms.

**Que 5.13.** Explain the working of PLL with suitable block diagram.

Write down the different applications of PLL.

**AKTU 2016-17, Marks 10**

**OR**

Draw the block diagram of PLL and explain its operation. Explain lock-in range, capture range and pull-in time of a PLL. List the applications of PLL.

**AKTU 2017-18, Marks 10**

**AKTU 2019-20, Marks 07**

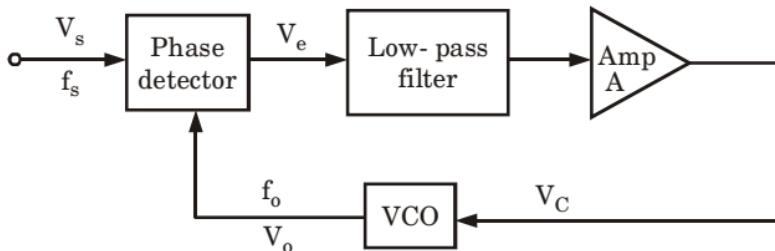
**OR**

Explain the working of PLL with suitable block diagram.

**AKTU 2018-19, Marks 3.5**

**Answer****A. Principle of operation of PLL :**

1. The two inputs of the phase detector or comparator are the input voltage  $V_s$  at frequency  $f_s$  and the feedback voltage from a voltage controlled oscillator (VCO) at frequency  $f_o$ .
2. The phase detector compares these two signals and produces a DC voltage  $V_e$  which is proportional to the phase difference between  $f_s$  and  $f_o$ .
3. The output voltage  $V_e$  of the phase detector is called as error voltage. This error voltage is then applied to low-pass filter.
4. Low-pass filter removes the high frequency noise present in the phase detector output and produces a ripple free DC level.
5. This DC level is amplified to an adequate level by the amplifier and applied to a VCO.
6. The DC amplifier output voltage is called as the control voltage  $V_C$ .

**Fig. 5.13.1. Block diagram of PLL.**

7. The control voltage  $V_C$  is applied at the input of a VCO. The output frequency of VCO is directly proportional to the DC control voltage  $V_C$ .
  8. The VCO frequency  $f_o$  is compared with the input frequency  $f_s$  by the phase detector and it is adjusted continuously until it is equal to the input frequency  $f_s$  i.e.,  $f_o = f_s$ .
  9. Once, the action of shifting VCO frequency in a direction to reduce the frequency difference between  $f_s$  and  $f_o$  starts, we say the signal is in the capture range.
  10. When the output frequency is exactly the same as the input frequency, PLL is then said to be locked.
  11. Once locked the output frequency  $f_o$  is identical to  $f_s$  except for a finite phase difference.
  12. This phase difference generates a control voltage  $V_C$  to shift VCO frequency from  $f_o$  to  $f_s$  thereby maintaining the lock. Once locked, PLL tracks the frequency changes of the input signal.
- B. Lock-in range :** Once the PLL is locked, it can track the frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called lock-in range or tracking range.
- C. Capture range :** The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range.

**D. Pull-in time :** The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the loop gain and loop filter characteristics.

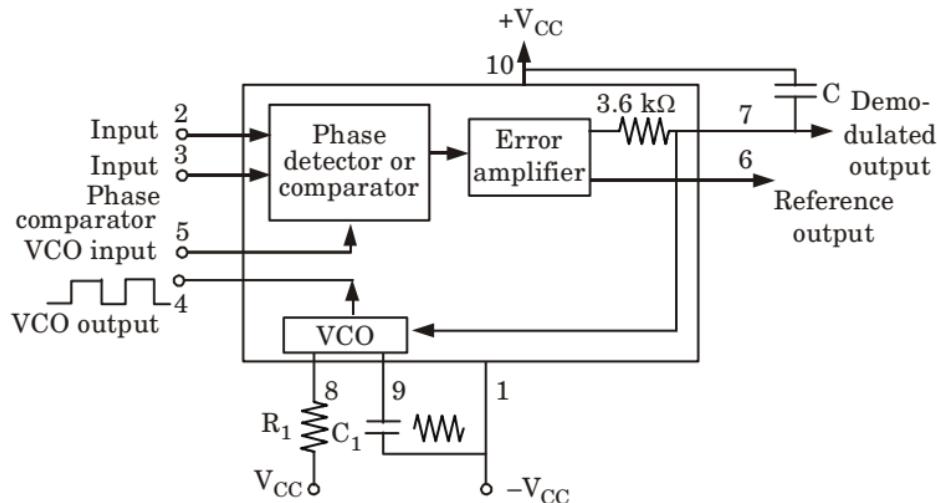
**E. Applications :**

- |                          |                         |
|--------------------------|-------------------------|
| 1. Frequency divider     | 2. Frequency multiplier |
| 3. Frequency synthesizer | 4. AM detector          |
| 5. FM detector           | 6. FSK demodulator.     |

**Que 5.14.** Draw the functional block diagram of PLL IC. Explain its working and deduce the expression for maximum frequency range of signal that can be locked.

**Answer**

**A. Functional block diagram :**



**Fig. 5.14.1.** Functional block diagram of PLL-565.

**Working :**

- It may be seen that phase locked loop is internally broken between the VCO output and the phase comparator input.
- A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare  $f_0$  with input signal  $f_{in}$ .
- A capacitor  $C$  is connected between pin 7 and pin 10 (supply terminal) to make a low-pass filter with the internal resistance of  $3.6 \text{ k}\Omega$ . This capacitor should be large enough to eliminate the variations in the demodulated output at pin 7.

**B. Derivation of lock-range :**

- Assume  $\phi$  radian is the phase difference between the input signal and the VCO voltage. Then the output voltage  $v_e$  of the analog phase detector is given by

$$v_e = K_d \left( \phi - \frac{\pi}{2} \right) \quad \dots(5.14.1)$$

where  $K_d$  is the phase angle-to-voltage transfer coefficient of the phase detector.

- Therefore, the control voltage to VCO is

$$v_c = AK_d \left( \phi - \frac{\pi}{2} \right) \quad \dots(5.14.2)$$

where  $A$  is the voltage gain of the amplifier.

- This control voltage  $v_c$  shifts VCO frequency from its free running frequency  $f_0$  to a frequency  $f$  represented by

$$f = f_0 + K_0 v_c \quad \dots(5.14.3)$$

where  $K_0$  is the voltage to frequency transfer coefficient of the VCO.

- When PLL achieves lock with signal frequency  $f_i$ , we have

$$f = f_i = f_0 + K_0 v_c$$

- From eq. (5.14.2) and eq. (5.14.3) we get

$$v_c = \frac{(f_i - f_0)}{K_0} = AK_d \left( \phi - \frac{\pi}{2} \right)$$

Therefore,  $\phi = \frac{\pi}{2} + \frac{(f_i - f_0)}{K_0 K_d A}$

- The maximum output voltage magnitude available from the phase detector occurs for  $\phi = \pi$  and 0 radian and

$$v_{e(\max)} = \pm K_d \frac{\pi}{2}$$

- Then, the corresponding value of the maximum control voltage available to drive the VCO is given by

$$v_{c(\max)} = \pm \left( \frac{\pi}{2} \right) K_d A$$

- The maximum VCO swing in frequency that can be achieved is given by

$$(f - f_0)_{\max} = K_0 v_{c(\max)} = K_d K_0 A \left( \frac{\pi}{2} \right) \quad \dots(5.14.4)$$

- Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be

$$f_i = f_0 \pm (f - f_0)_{\max} = f_0 \pm K_d K_0 A \left( \frac{\pi}{2} \right) = f_0 \pm \Delta f_L$$

- The lock-in frequency range is  $2\Delta f_L$  and from eq. (5.14.4) it is given by

$$\text{Lock-in range} = 2\Delta f_L = K_d K_0 A \pi = K_v \pi \quad \dots(5.14.5)$$

where  $K_d K_0 A = K_v$  is the loop bandwidth.

or,  $\Delta f_L = K_d K_0 A \left( \frac{\pi}{2} \right) = K_v \left( \frac{\pi}{2} \right)$

- The lock-in range is symmetrically located with respect to the free running frequency  $f_0$  of VCO. For IC PLL 565, we have

$$K_0 = \frac{8f_0}{V}$$

where

$$V = +V_{CC} - (-V_{CC})$$

12. For PLL,  $K_d = \frac{1.4}{\pi}$

and  $A = 1.4$

Hence, from eq. (5.14.5) the lock-in range becomes

$$\Delta f_L = \pm 7.8 f_0/V$$

**Que 5.15.** Explain the application of PLL as frequency multiplier with suitable circuit diagram.

**Answer**

1. A divide by  $N$  network is connected externally between VCO output and phase comparator input as shown in Fig. 5.15.1.
2. Since the output of the divider network is locked to input frequency  $f_s$ , VCO actually operates at a frequency which is  $N$  times higher than  $f_s$ .

$$\therefore f_s = f_o/N$$

$$f_o = Nf_s$$

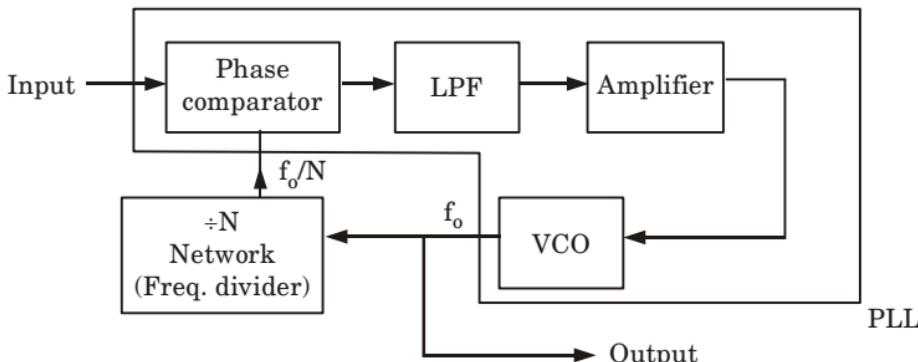


Fig. 5.15.1.

**Que 5.16.** Describe PLL application as frequency translator.

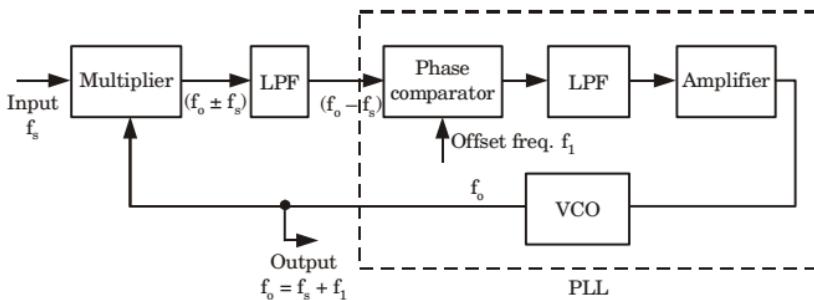
**Answer**

1. A schematic for shifting the frequency of an oscillator by a small factor is shown in Fig. 5.16.1.
2. The signal  $f_s$  which has to be shifted and the output frequency  $f_o$  of the VCO are applied as inputs to the mixer.
3. The output of the mixer contains the sum and difference of  $f_s$  and  $f_o$ . However, the output of LPF contains only the difference signal ( $f_o - f_s$ ). The translation or offset frequency  $f_1$  ( $f_1 \ll f_s$ ) is applied to the phase comparator.
4. When PLL is in locked state,

$$f_o - f_s = f_1$$

or  $f_o = f_s + f_1$

Thus, it is possible to shift the incoming frequency  $f_s$  by  $f_1$ .



5.16.1. PLL used as a frequency translator.

**Que 5.17.** Determine the free running frequency  $f_o$  and the lock range,  $f_L$  and the capture range,  $f_c$  for PLL 565 having  $R_1 = 12 \text{ K}\Omega$ ,  $C_1 = 0.001 \mu\text{F}$ ,  $C_2 = 10 \mu\text{F}$ ,  $C_3 = 0.001 \mu\text{F}$ ,  $V_{CC} = \pm 10 \text{ V}$ . Show the graphical representation of relationship between lock frequency, capture frequency and free running frequency.

### Answer

Given :  $R_1 = 12 \text{ K}\Omega$ ,  $C_1 = 0.001 \mu\text{F}$ ,  $C_2 = 10 \mu\text{F}$ ,  $C_3 = 0.001 \mu\text{F}$ ,  $V_{CC} = \pm 10 \text{ V}$ .

To Find :  $f_o, f_L, f_c$ .

- Free running frequency,  $f_o = \frac{1.2}{4 R_1 C_1}$ 

$$= \frac{1.2}{4 \times 12 \times 10^3 \times 0.001 \times 10^{-6}} = 25 \text{ KHz}$$
- Lock range,  $f_L = \pm \frac{7.8 f_o}{V_{CC}} \text{ Hz} = \pm \frac{7.8 f_o}{20} \quad [\because V_{CC} = 10 - (-10) \text{ V}]$ 

$$= \pm 9.75 \text{ KHz}$$
- Capture range,  $f_c = \pm \left[ \frac{f_L}{2\pi \times 3.6 \times 10^3 \times C_2} \right]^{1/2}$ 

$$= \pm \left[ \frac{9.75 \times 10^3}{2\pi \times 3.6 \times 10^3 \times 10 \times 10^{-6}} \right]^{1/2} = \pm 199.47 \text{ Hz}$$

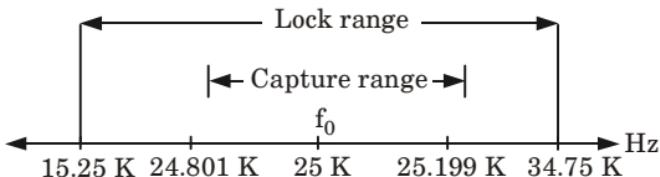


Fig. 5.17.1.

**VERY IMPORTANT QUESTIONS**

***Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.***

**Q. 1. Draw and explain the block diagram of IC 555.**

**Ans.** Refer Q. 5.1.

**Q. 2. Draw the functional block diagram of IC 555 and explain its working. Draw the circuit diagram of a monostable multivibrator using 555 and find expression for quasi state period.**

**Ans.** Refer Q. 5.4.

**Q. 3. Draw the functional block diagram of IC-555 and explain its working. Design a 555 timer as an astable multivibrator with an output signal timer frequency of 700 Hz and 60 % duty cycle.**

**Ans.** Refer Q. 5.6.

**Q. 4. For 555 astable multivibrator  $R_A = 4.7 \text{ K}\Omega$ ,  $R_B = 1 \text{ K}\Omega$  and  $C = 1 \mu\text{F}$ . Determine the positive pulse width, the negative pulse width, and the free-running frequency. What is the duty cycle of output waveform ?**

**Ans.** Refer Q. 5.8.

**Q. 5. Explain the types of phase detectors with suitable circuit diagrams and input-output waveforms.**

**Ans.** Refer Q. 5.11.

**Q. 6. Explain the working of PLL with suitable block diagram. Write down the different applications of PLL.**

**Ans.** Refer Q. 5.13.



UNIT  
1

# The 741 IC Op-Amp (2 Marks Questions)

- 1.1. What is the function of the output stage or last stage of Op-Amp ?**

**Ans.** The function of the last stage *i.e.*, the output stage of an Op-Amp is to supply the load current and provide a low impedance output. It should also provide a large output voltage saving ideally the total supply voltage *i.e.*,  $V_{CC} + V_{EE}$ .

- 1.2. Define and give significance of slew rate.**

**AKTU 2017-18, Marks 02**

**Ans.** **Slew rate :** Slew rate is defined as the maximum rate of change of output voltage with time. Its unit is  $\text{V}/\mu\text{sec}$ .

$$\text{Slew rate, } SR = \left. \frac{dV_o}{dt} \right|_{\max}$$

**Significance :** The slew rate of an ideal Op-Amp is infinite which implies that the output voltage of an ideal Op-Amp can instantaneously follow the changes to the input step voltage. Higher the value of slew rate better is the performance of Op-Amp.

- 1.3. Give the relationship between  $f_t$  and SR.**

**Ans.** The relationship is given by :

$$\begin{aligned} SR &= 2\pi f_t V_{ov} \\ SR &= \omega_t V_{ov} \end{aligned}$$

- 1.4. What do you mean by DC analysis of a circuit ?**

**AKTU 2019-20, Marks 02**

**Ans.**

- DC operating point analysis calculates the behavior of a circuit when a DC voltage or current is applied to it.
- The result of this analysis is generally referred as the bias point or quiescent point, Q-point.
- In most cases, the results of the DC Operating point analysis are intermediate values for further analysis.

**1.5. What is CMRR ? Give its mathematical term.**

**Ans.** The relative sensitivity of an Op-Amp to a difference signal as compared to a common mode signal called common mode rejection ratio (CMRR) and gives the figure of merit  $\rho$  for the differential amplifier. So, CMRR is given by :

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right| \text{ decibels (dB)}$$

where  $A_{DM}$  is differential mode gain and  $A_{CM}$  is common mode gain.

**1.6. Define voltage follower.**

**Ans.** In the non-inverting amplifier of Fig. 1.6.1, if  $R_f = 0$  and  $R_1 = \infty$ . Then the output voltage is equal to the input voltage both in magnitude and phase. Hence, the circuit is called a voltage follower.

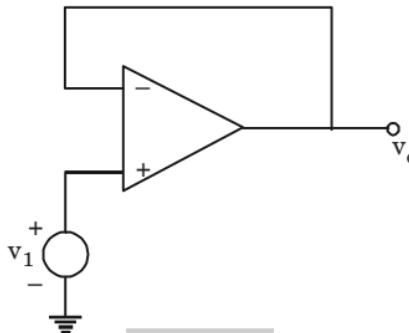


Fig. 1.6.1.

**1.7. Write advantage of a voltage follower circuit.**

AKTU 2018-19, Marks 02

**Ans.**

1. Low output impedance, almost zero.
2. The output follows the input exactly without a phase shift.

**1.8. Why the bias circuit is used ?**

**Ans.** The bias circuit is used to provide proportional current in the collector of transistor.

**1.9. Define input bias current.**

**Ans.** The input bias current of an Op-Amp is defined as,

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

For the 741 we obtain,  $I_B = \frac{I}{\beta_N}$

Using  $\beta_N = 200$ , yields  $I_B = 47.5 \text{ nA}$ .

**1.10. What is the role of coupling capacitor ( $C_c$ ) in IC-741 internal circuit ?**

AKTU 2015-16, Marks 02

**Ans.** The role of coupling capacitor ( $C_c$ ) in IC- 741 internal circuit is to compensate frequency using the Miller compensation techniques. Coupling capacitor ( $C_c$ ) is connected at the stage-II feedback path.

**1.11. What is input offset current and input offset voltage ?**

**Ans.**

**A. Input offset current :** The input offset current is defined as,  

$$I_{OS} = |I_{B1} - I_{B2}|$$

**B. Input offset voltage :** In the 741 Op-Amp, the input offset voltage is due to mismatches between  $Q_1$  and  $Q_2$ , between  $Q_3$  and  $Q_4$ , between  $Q_5$  and  $Q_6$ , and between  $R_1$  and  $R_2$ .

**1.12. Why ideal Op-Amp draw no current at both the input terminals ?**

**Ans.** An ideal Op-Amp draws no current at both the input terminals i.e.,  $i_1 = i_2 = 0$  because of infinite input impedance any signal source can drive it and there is no loading on the preceding driver stage.

**1.13. How the effect of input bias current in non-inverting amplifier is compensated ?**

AKTU 2018-19, Marks 02

**Ans.** The effect of input bias current in a non-inverting amplifier is compensated by placing a compensating resistor  $R_{comp}$  in series with the input signal  $V_1$ .

**1.14. State the reasons for the offset currents at the input of the Op-Amp.**

AKTU 2016-17, Marks 02

**Ans.**

1. The input currents of op-amp are the base currents of two transistors used in the input stage. Ideally these transistors must be perfectly matched and two currents must be equal.
2. But practically the two input base currents differ by a small amount due to mismatch of two transistors. This difference between the currents flowing into the two input terminals of the Op-Amp is called input offset current.



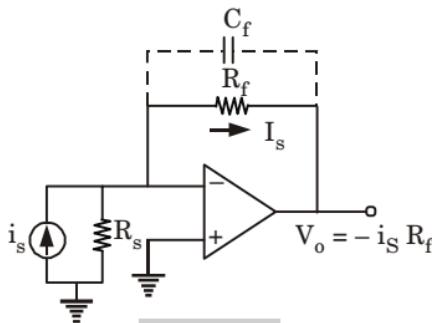
# 2

**UNIT**

## Linear Applications of IC Op-Amps (2 Marks Questions)

- 2.1. Draw the circuit diagram of current to voltage converter (transresistance amplifier).**

**Ans.**



**Fig. 2.1.1.**

- 2.2. Draw and explain the generalized impedance converter circuit.**

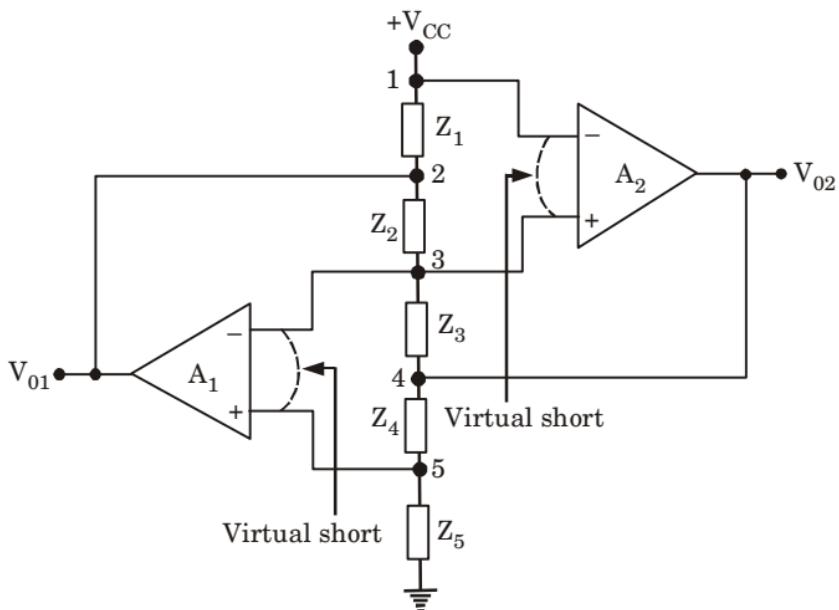
**AKTU 2016-17, Marks 02**

**Ans.**

- Generalized impedance converters (GIC) are Op-Amp circuits that employ  $RC$  networks for simulating frequency-dependent impedance elements such as inductors. Fig. 2.2.1 shows the circuit of a GIC.
- The input impedance of the circuit

$$Z_1 = \frac{V_{CC}}{I_C} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \quad \dots(2.2.1)$$

- Eq. (2.2.1) shows that the circuit shown in Fig. 2.1.1, can be used as grounded impedance whose nature and value depends on the nature and values of impedance elements  $Z_1$  to  $Z_5$ .



**Fig. 2.2.1.** Generalized impedance converter.

### 2.3. What are the requirements of power amplifier ?

**Ans.**

- i. It should have low output impedance so as to provide impedance matching for maximum power transfer.
- ii. High power conversion efficiency.
- iii. As large amount of power gets dissipated at the junction of power transistor heat sinks have to be used.

### 2.4. Write the use of an instrumentation amplifier.

**Ans.**

An instrumentation amplifier is useful for amplifying low level signals which are obtained by sensing with a transducer in the measurement of physical quantities like temperature, water flow etc.

### 2.5. What are the important features of an instrumentation amplifier ?

**Ans.**

- i. High gain accuracy.
- ii. High CMRR.
- iii. High gain stability with low temperature coefficient.

### 2.6. Write the advantages of active filters.

**Ans.**

- i. No loading problem.
- ii. Flexibility in gain and frequency adjustment.
- iii. Low cost.
- iv. Small component size.

### 2.7. What are the limitations of active filters over passive filters ?

**Ans.**

1. The design of active filter becomes costly for high frequencies.
2. Active filters require dual polarity DC power supply where as passive filters do not.
3. The active element is prone to the process parameter variations and they are sensitive to ambient conditions like temperature.

**2.8. Write the advantage of active filter over passive filter.**

AKTU 2018-19, Marks 02

**Ans.**

1. Easier to tune or adjust.
2. Active filter is small and less bulky.

**2.9. Differentiate wide band and narrow band pass filter.**

AKTU 2019-20, Marks 02

**Ans.**

S. No.	Wide band pass filter	Narrow band pass filter
1.	The wide band pass filter uses two Op-Amp.	The narrow band pass filter uses one Op-Amp.
2.	It has one feedback path.	It has two feedback path.
3.	The Op-Amp in the non-inverting configuration.	The Op-Amp in the inverting configuration.

**2.10. What do you mean by a frequency response of a filter circuit ?**

AKTU 2017-18, Marks 02

**Ans.**

1. Frequency response is the quantitative measure of the output spectrum of a filter circuit in response to a stimulus, and is used to characterize the dynamic of the system.
2. It is a measure of magnitude and phase of the output as a function of frequency, in comparison to the input.

**2.11. Design a multiple feedback narrow band pass filter with  $f_c = 1 \text{ KHz}$ ,  $Q = 3$  and  $A = 10$ .**

AKTU 2016-17, Marks 02

**Ans.**

**Given :**  $f_c = 1 \text{ KHz}$ ,  $Q = 3$  and  $A = 10$

**To Design :** Multiple feedback narrow band pass filter.

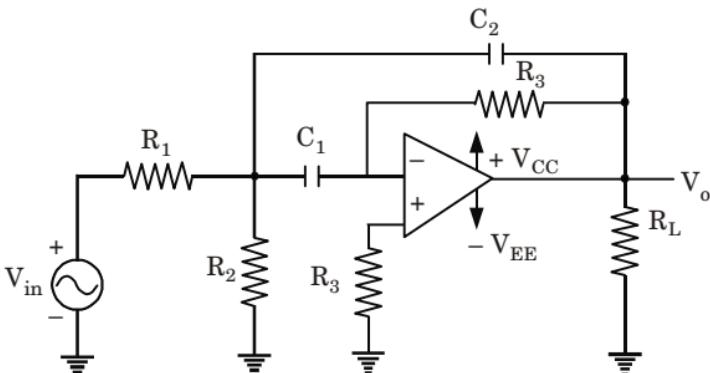
Let

$$C_1 = C_2 = C = 0.01 \mu\text{F}.$$

$$R_1 = \frac{Q}{2\pi f_c C A} = \frac{3}{(2\pi)(10^3)(10^{-8})(10)} = 4.77 \text{ K}\Omega$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A)} = \frac{3}{(2\pi)(10^3)(10^{-8})[2(3)^2 - 10]} = 5.97 \text{ K}\Omega$$

$$R_3 = \frac{Q}{\pi f_c C} = \frac{3}{(\pi)(10^3)(10^{-8})} = 95.5 \text{ K}\Omega$$



**Fig. 2.11.1.** Multiple feedback narrow band filter.

**2.12. For a first order Butterworth high pass filter, evaluate the value of  $R$  if  $C = 0.0047 \mu\text{F}$  and  $f_c = 10 \text{ KHz}$ .**

**AKTU 2016-17, Marks 02**

**Ans.**

**Given :  $C = 0.0047 \mu\text{F}$ ,  $f_c = 10 \text{ KHz}$**

**To Find :  $R$ .**

We know that,  $f_c = \frac{1}{2\pi RC}$

Therefore,  $R = \frac{1}{2\pi f_c C} = \frac{1}{2\pi(10 \times 10^3) \times 47 \times 10^{-10}} = 3.39 \text{ K}\Omega$



# 3

**UNIT**

## Frequency Compensation and Non-Linearity (2 Marks Questions)

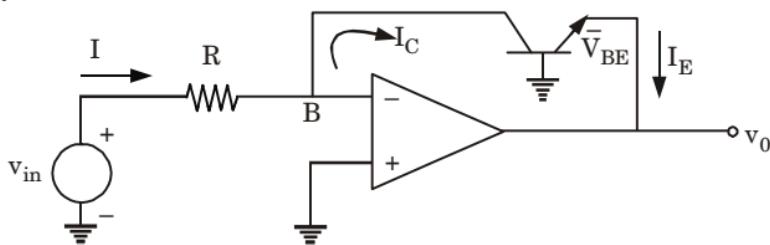
**3.1. Write the types of frequency compensation.**

**Ans.** There are two types of frequency compensation :

- Internal frequency compensation.
- External frequency compensation.

**3.2. Draw the circuit diagram of logarithmic amplifier.**

**Ans.**



**Fig. 3.2.1.**

**3.3. Give two applications of analog multiplier.**

**AKTU 2017-18, Marks 02**

**Ans.**

- Frequency doubling.
- Measurement of real power.

**3.4. What is super diode ?**

**AKTU 2017-18, Marks 02**

**Ans.** The super diode is a configuration obtained with an operational amplifier in order to have a circuit behaving like an ideal diode and rectifier. It is also known as precision rectifier.

**3.5. Define comparator and how it is used.**

**Ans.**

1. A comparator is a circuit which compares a signal voltage applied at one input of an Op-Amp with a known, reference voltage at other input.
2. The basic comparator can be used as zero crossing detector provided that  $V_{ref}$  is 0. It is used as window detector as well as phase meter.

**3.6. Differentiate between comparator and schmitt trigger.**

AKTU 2017-18, 2019-20; Marks 02

**Ans.**

S. No.	Comparator	Schmitt trigger
1.	The feedback is not used.	The feedback is used.
2.	The Op-Amp used is in open loop mode.	The Op-Amp used is in closed loop mode.
4.	A single reference voltage exists which acts as triggering voltage. i.e., $V_{ref}$ or $-V_{ref}$	The two different threshold voltages exist as $V_{UT}$ and $V_{LT}$ .
5.	The hysteresis does not exist.	Hysteresis exists with a width $H = V_{UT} - V_{LT}$ .

**3.7. What is the advantage of precision diode rectifier circuit over ordinary rectifier ?**

AKTU 2018-19, Marks 02

**Ans.**

- i. Precision rectifier more stable in comparison to ordinary rectifier.
- ii. The efficiency of precision rectifier is better than ordinary rectifier.

**3.8. How monostable multivibrator is used ?**

**Ans.** Monostable multivibrator has one stable state and the other is quasi-stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal.

**3.9. What do you understand by hysteresis voltage ?**

AKTU 2015-16, Marks 02

**Ans.** The voltage at which trigger of pulses occurs from positive level to negative level or vice-versa is known as hysteresis voltage. The hysteresis voltage is equal to the difference between  $V_{UT}$  and  $V_{LT}$ . Therefore  $V_H = V_{UT} - V_{LT}$ .

**3.10. Name the circuit that is used to detect the peak value of non-sinusoidal waveforms. Explain the operation with neat circuit diagram.**

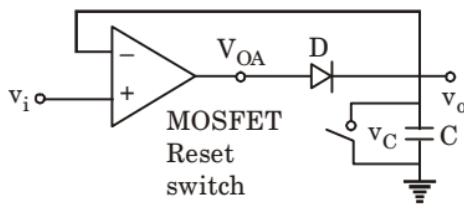
AKTU 2016-17, Marks 02

**Ans.**

1. Peak detector is used to detect the peak value of non-sinusoidal waveforms.
2. The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value (almost indefinitely) on a capacitor.
3. If a higher peak signal value comes along, this new value is stored.

The highest peak value is stored until the capacitor is discharged.

4. When input  $v_i$  exceeds  $v_c$ , the voltage across the capacitor, the diode  $D$  is forward biased and the circuit becomes a voltage follower.
5. Consequently, the output voltage  $v_o$  follows  $v_i$  as long as  $v_i$  exceeds  $v_c$ . When  $v_i$  drops below  $v_c$ , the diode becomes reverse-biased and the capacitor holds the charge till input voltage again attains a value greater than  $v_c$ .
6. Fig. 3.10.1(b) shows the voltage wave shape for the positive peak detector.



(a) Positive peak detector

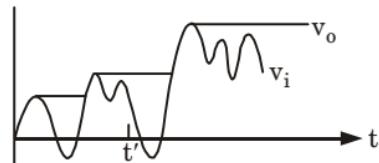
(b) Output  $v_o$  corresponding to arbitrary input  $v_i$ 

Fig. 3.10.1

### 3.11. Give the example of a square wave generator which utilizes positive feedback.

AKTU 2015-16, Marks 02

**Ans.** Schmitt trigger circuit uses positive feedback. A simple comparator circuit with positive feedback is called Schmitt trigger circuit which generates square wave from sinusoidal wave.

### 3.12. What is the application of Schmitt trigger ?

**Ans.** A Schmitt trigger is used to convert a very slowly varying input voltage into a square wave output.

### 3.13. What happens to differentiator when it is used at high frequency ?

**Ans.** At high frequencies a differentiator may become more unstable and break into oscillation. The input impedance (*i.e.*,  $1/\omega c_1$ ) decreases with increase in frequency, this making the circuit sensitive to high frequency noise.

### 3.14. Why the monostable multivibrator also called as gating circuit ?

**Ans.** The monostable multivibrator is called as gating circuit as it generate a rectangular waveform at definite time and thus could be used for gate parts of a system.

### 3.15. Write the advantages of negative feedback amplifier.

**Ans.**

- i. The negative feedback reduces noise.
- ii. It has high stabilized gain.
- iii. It can control step response of amplifier.
- iv. It has less harmonic distortion.



**4**

**UNIT**

# Digital Integrated Circuit Design

## (2 Marks Questions)

**4.1. What do you mean by a CMOS circuit logic ?**

**AKTU 2017-18, Marks 02**

**Ans.**

1. The CMOS logic gate consists of two networks.
- i. The pull-down network (PDN) constructed of NMOS transistor and
- ii. The pull-up network (PUN) constructed of PMOS transistors.
2. The two networks are operated by the input variables, in a complementary fashion.

**4.2. Why CMOS NAND is preferred over CMOS NOR ?**

**AKTU 2016-17, Marks 02**

**Ans.**

The NOR gate will require much greater area than the NAND gate because  $p$ -region is usually two to three times  $n$ -region. For this reason, NAND gates are preferred for implementing combinational logic functions in CMOS.

**4.3. What is threshold voltage ?**

**Ans.** The value of  $V_{GS}$  at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage.

**4.4. What are the advantages of implementing the depletion-load NMOS inverter circuit configuration ?**

**Ans.**

- i. Sharp VTC transition and better noise margins.
- ii. Single power supply.      iii. Smaller overall layout area.

**4.5. What is PDN and PUN ?**

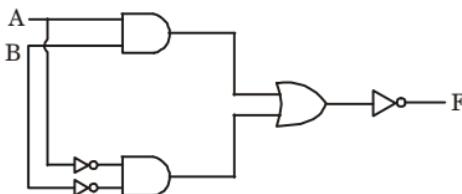
**AKTU 2018-19, Marks 02**

**Ans.**

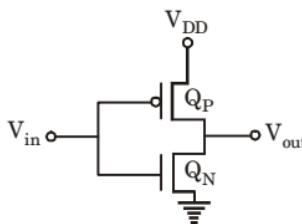
- i. **Pull up network (PUN) :** A network that provides a low resistance path to  $V_{dd}$  when output is logic 1 and provides a high resistance to  $V_{dd}$  otherwise.
- ii. **Pull down network (PDN) :** A network that provides a low resistance path to ground (GND) when output is logic 0 and provides a high resistance to ground (GND) otherwise.

**4.6. Implement  $F = \overline{AB} + \overline{A}\overline{B}$  using AND-OR-INVERT logic.**

**AKTU 2016-17, Marks 02**

**Ans.****Fig. 4.6.1.****4.7. Define the term  $V_{IH}$  and  $V_{IL}$  for the CMOS inverter.****AKTU 2015-16, Marks 02****Ans.**

- $V_{IH}$ :  $V_{IH}$  is the minimum value of input interpreted by the inverter as a logic 1.
  - $V_{IL}$ :  $V_{IL}$  is the maximum value of input interpreted by the inverter as a logic 0.
- $V_{IL}$  and  $V_{IH}$  are the points on VTC at which the slope is equal to  $-1$ .

**4.8. Draw the basic structure of CMOS inverter.****AKTU 2019-20, Marks 02****Ans.****Fig. 4.8.1. CMOS inverter circuit.****4.9. Define noise margin for the CMOS inverter.****AKTU 2015-16, Marks 02****Ans.**

- Noise margin of the inverter measures the ability of the inverter to tolerate variations in the input signal level.
- The robustness of a logic-circuit family is determined by its ability to reject noise and thus by  $NM_H$  and  $NM_L$ .

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

where,       $NM_L$  = Low noise margin

$NM_H$  = High noise margin.

**4.10. Define latch.****Ans.**

- Latch is a basic memory element. It consists of two cross-coupled logic inverters. The inverters form a positive feedback loop.

2. It has two operating points. Thus, the latch is a bistable circuit having two complementary outputs.
3. The latch together with the triggering circuitry forms a flip-flop.

#### 4.11. Define Fan-in and Fan-out.

**Ans.**

- Fan-in :** The Fan-in of a gate is the number of its inputs. A four input NOR gate has a Fan-in of 4.
- Fan-out :** Fan-out is the maximum number of similar gates that a gate can drive.

#### 4.12. How the pull up network can be synthesized ?

**Ans.** The pull up network can be directly synthesized by expressing Y as a function of the complemented variables and then applying the uncomplemented variables to the gate of the PMOS transistors.

#### 4.13. Implement $F = \overline{AB} + \overline{A}\overline{B}$ using CMOS.

**Ans.**

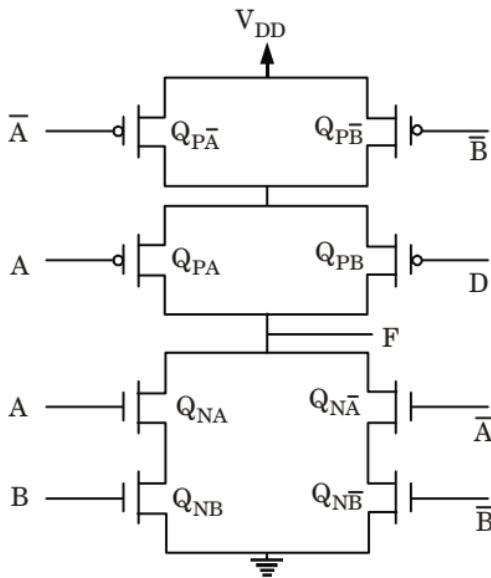


Fig. 4.13.1.

#### 4.14. How the speed of operation of the inverter is characterized ?

**Ans.**

1. The speed of operation of the inverter is characterized by its propagation delay,  $t_p$ .
2. The value of  $t_p$  is,  $t_p = (t_{PLH} + t_{PHL})/2$
3. The maximum frequency at which an inverter can be switched  $f_{max} = 1/2t_p$ .



**5****UNIT**

# Integrated Circuit Timer (2 Marks Questions)

## 5.1. Define 555 timer and write its applications.

**Ans.****A. 555 timer :**

The 555 timer is a highly stable device for generating accurate time delay or oscillation. A single 555 timer can provide time delay ranging from microseconds to hours.

**B. Applications :**

- i. Pulse generator
- ii. Ramp and square wave generator
- iii. Mono-shot multivibrator
- iv. Burglar alarm

## 5.2. Describe the need of voltage limiter circuit.

**AKTU 2017-18, 2019-20; Marks 02**

**Ans.** A voltage limiter is used to limit the voltage level. When a steady, reliable voltage is needed, then voltage limiter is the preferred device.

## 5.3. What are the basic blocks of phase-locked loop ?

**AKTU 2015-16, Marks 02****Ans.**

- 1. PLL stands for Phase Locked Loop. Block diagram of the basic phase locked loop is shown in Fig. 5.3.1.
- 2. PLL consists of :
  - i. A phase detector
  - ii. Low pass filter
  - iii. An error amplifier
  - iv. Voltage controlled oscillator.

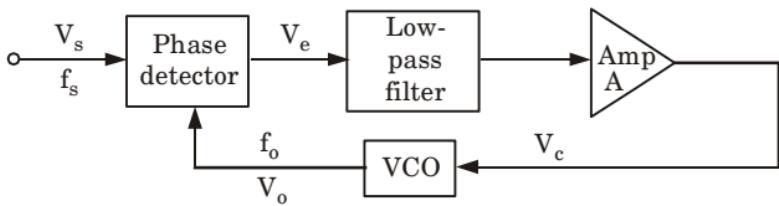


Fig. 5.3.1. Block diagram of PLL.

**5.4. What is capture range in PLL ?** AKTU 2015-16, Marks 02

**OR**

**Which block of PLL decides capture range ? Explain.**

AKTU 2016-17, Marks 02

**Ans.**

1. The capture range is the range of input frequencies within which an initially unlocked loop will get locked with an input signal.
2. In PLL, VCO block decides capture range.

**5.5. What is the chip number for phase locked loop ?**

AKTU 2015-16, Marks 02

**Ans.** Chip number of phase locked loop is NE/SE 565.

**5.6. Write the applications of PLL.**

**Ans.**

- i. Frequency multiplication/division
- ii. Frequency translation
- iii. AM detection
- iv. FM demodulation

**5.7. Write the stages of PLL.**

**Ans.**

- i. Free running
- ii. Capture
- iii. Locked or tracing

**5.8. Define pull in time.**

**Ans.**

The total time taken by PLL to establish lock is called pull in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

**5.9. How the AM detection is used using PLL ?**

**Ans.**

The AM signal which is to be demodulated is applied to  $90^\circ$  phase shifting network as well as PLL. The phase detector will produce sum and difference of the frequencies at its output.

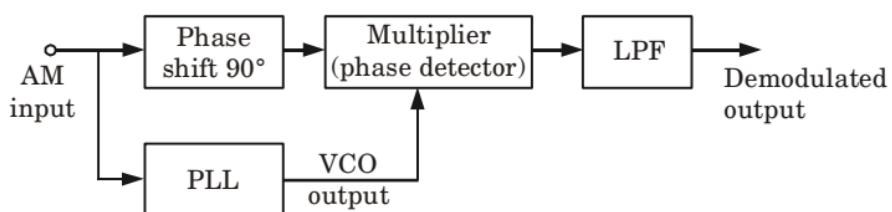


Fig. 5.9.1.

**5.10. Write the applications of monostable modes of 555 timer.****Ans.**

- Missing pulse detector.
- Linear ramp generator.
- Frequency divider.
- Pulse width modulation.

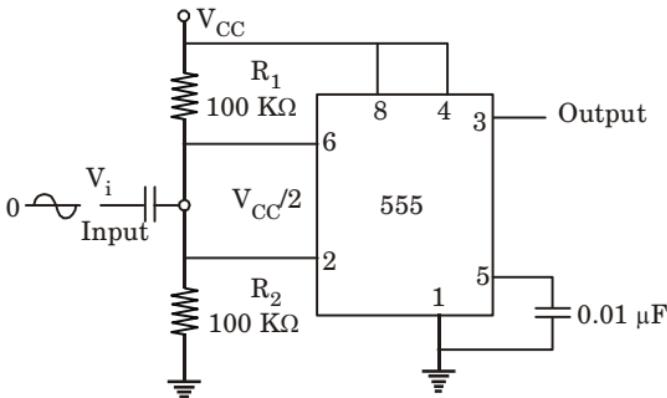
**5.11. Draw the circuit diagram of Schmitt trigger using 555 timer.****Ans.**

Fig. 5.11.1.

**5.12. Calculate the value of C for a monostable multivibrator if  $R = 100 \text{ k}\Omega$  and the time delay  $T = 100 \text{ ms}$ .**

**Ans.**

$$C = \frac{T}{1.1R} = \frac{100 \times 10^{-3}}{1.1 \times 100 \times 10^3} = 0.99 \mu\text{F}$$

**5.13. Write the application of VCO.****Ans. Applications of VCO :**

The various applications of VCO are :

- Frequency Modulation.
- Signal Generation (Triangular or Square Wave)
- Function Generation.
- Frequency Shift Keying *i.e.*, FSK demodulator.
- In frequency multipliers.
- Tone Generation.



**B.Tech.****(SEM. V) ODD SEMESTER THEORY  
EXAMINATION, 2015-16  
INTEGRATED CIRCUITS****Time : 3 Hours****Max. Marks : 100****SECTION - A**

1. Attempt all parts. All parts carry equal marks. Write answer of each part in short :  $(2 \times 10 = 20)$
- a. Why don't we normally realize the beta compensated current mirror using MOS ?
- b. What are the basic blocks of phase-locked loop ?
- c. What do you understand by hysteresis voltage ?
- d. What is the role of coupling capacitor ( $C_c$ ) in IC-741 internal circuit ?
- e. Give the example of a square wave generator which utilizes positive feedback.
- f. What is capture range in PLL ?
- g. What is the chip number for phase locked loop ?
- h. Define the term  $V_{IH}$  and  $V_{IL}$  for the CMOS inverter.
- i. The basic step of 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111.
- j. Define noise margin for the CMOS inverter.

**SECTION - B**

- Note :** Attempt any five questions from this section :  $(10 \times 5 = 50)$
2. What do you understand by the base current mirror ? How does it provide improvement over simple current mirror circuit ? Explain with the help of a neat circuit diagram.
  3. Define the slew rate. Also derive the relationship between  $f_t$  and slew rate for the IC-741.

4. Sketch the properly labeled master slave D flip-flop circuit and explain its operation with the help of proper waveform of the clock signal.
5. What is a DAC ? Describe the weighted resistor DAC. Give mathematical expressions in support of your answer.
6. Determine  $I_{C1}, I_{C2}, I_{C3}$  for the circuit shown in Fig. 1. Assume  $\beta = 125$ .

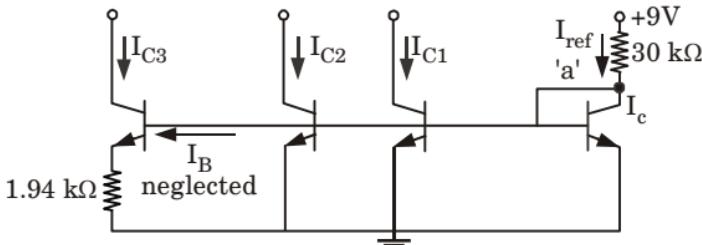


Fig. 1.

7. Draw the functional block diagram of IC-555 and explain its working. Design a 555 timer as an astable multivibrator with an output signal timer frequency of 700 Hz and 60 % duty cycle.
8. Describe the Antoniou inductance simulation circuit with properly labeled circuit diagram and give mathematical expressions in support of your answer.
9. Describe the sample and hold circuit with the help of an Op-Amp. What are the applications of sample and hold circuit ?

### SECTION - C

**Note :** Attempt any two questions from this section :  $(15 \times 2 = 30)$

10. Describe the circuit for the KHN filter using three Op-Amp. Design a second order Butterworth low-pass filter having upper cut-off frequency 1 KHz. Determine its frequency response.
11. Describe different regions of operation for CMOS inverter over its VTC characteristics.  
Consider a CMOS inverter with following parameters :

$$V_{DD} = 3.3 \text{ V}, V_{T0,n} = 0.6 \text{ V}, V_{T0,p} = 0.7 \text{ V},$$

$$k_n = 200 \mu\text{A/V}^2, k_p = 80 \mu\text{A/V}^2$$

Calculate the noise margin of the CMOS inverter circuit.

12. Describe the Schmitt trigger with the help of proper circuit diagram and transfer characteristics. A Schmitt trigger with the upper threshold level  $V_{UT} = 0 \text{ V}$  and hysteresis width is  $0.2 \text{ V}$  converts  $1 \text{ KHz}$  sine wave of amplitude  $4 \text{ V}_{PP}$  into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.



## SOLUTION OF PAPER (2015-16)

### SECTION - A

- 1.** Attempt **all** parts. All parts carry **equal** marks. Write answer of each part in short : **(2 × 10 = 20)**
- a.** Why don't we normally realize the beta compensated current mirror using MOS ?

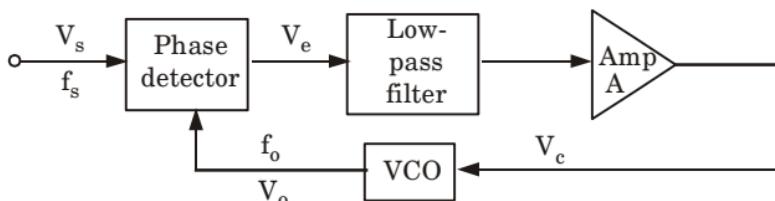
**Ans.**

1. Due to the wide variation of  $V_{th}$  discrete versions of MOS are problematic to implement. This variation can be somewhat compensated by using a source degenerate resistor.
2. However its value becomes so large that the output resistance reduces. Due to this reason we don't realize the beta compensated current mirror using MOS.

- b.** What are the basic blocks of phase-locked loop ?

**Ans.**

1. PLL stands for Phase Locked Loop. Block diagram of the basic phase locked loop is shown in Fig. 1.
2. PLL consists of :
  - i. A phase detector
  - ii. Low pass filter
  - iii. An error amplifier
  - iv. Voltage controlled oscillator.



**Fig. 1.** Block diagram of PLL.

- c.** What do you understand by hysteresis voltage ?

**Ans.** The voltage at which trigger of pulses occurs from positive level to negative level or vice-versa is known as hysteresis voltage. The hysteresis voltage is equal to the difference between  $V_{UT}$  and  $V_{LT}$ . Therefore  $V_H = V_{UT} - V_{LT}$ .

- d.** What is the role of coupling capacitor ( $C_c$ ) in IC-741 internal circuit ?

**Ans.** The role of coupling capacitor ( $C_c$ ) in IC- 741 internal circuit is to compensate frequency using the Miller compensation techniques. Coupling capacitor ( $C_c$ ) is connected at the stage-II feedback path.

- e. Give the example of a square wave generator which utilizes positive feedback.

**Ans.** Schmitt trigger circuit uses positive feedback. A simple comparator circuit with positive feedback is called Schmitt trigger circuit which generates square wave from sinusoidal wave.

- f. What is capture range in PLL ?

**Ans.**

1. The capture range is the range of input frequencies within which an initially unlocked loop will get locked with an input signal.
2. In PLL, VCO block decides capture range.

- g. What is the chip number for phase locked loop ?

**Ans.** Chip number of phase locked loop is NE/SE 565.

- h. Define the term  $V_{IH}$  and  $V_{IL}$  for the CMOS inverter.

**Ans.**

- A.  $V_{IH}$ :  $V_{IH}$  is the minimum value of input interpreted by the inverter as a logic 1.
- B.  $V_{IL}$ :  $V_{IL}$  is the maximum value of input interpreted by the inverter as a logic 0.

$V_{IL}$  and  $V_{IH}$  are the points on VTC at which the slope is equal to  $-1$ .

- i. The basic step of 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111.

**Ans.** The output voltage for input 101101111 is  

$$10.3 \times 10^{-3} \times (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0) = 10.3 \times 367 \times 10^{-3} = 3.78 \text{ V}$$

- j. Define noise margin for the CMOS inverter.

**Ans.**

1. Noise margin of the inverter measures the ability of the inverter to tolerate variations in the input signal level.
2. The robustness of a logic-circuit family is determined by its ability to reject noise and thus by  $NM_H$  and  $NM_L$ .

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

where,       $NM_L$  = Low noise margin

$NM_H$  = High noise margin.

## SECTION – B

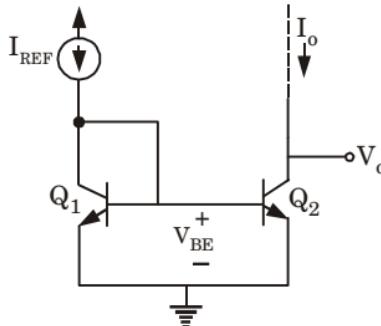
**Note :** Attempt any five questions from this section :  $(10 \times 5 = 50)$

2. What do you understand by the base current mirror? How does it provide improvement over simple current mirror circuit? Explain with the help of a neat circuit diagram.

**Ans. Base current mirror :**

- The basic BJT current mirror is shown in Fig. 2. It is very similar to MOS mirror, but differs in following respect.
- Firstly, the non-zero base current i.e., finite  $\beta$  and secondly current transfer ratio is determined by relative area of emitter-base junction of  $Q_1$  and  $Q_2$ .
- Consider  $\beta$  is high and neglect base current.  $I_{REF}$  is passed through  $Q_1$  and the corresponding voltage is  $V_{BE}$ .  $V_{BE}$  is applied between base and emitter of  $Q_2$ . Now,  $Q_2$  is matched to  $Q_1$ , i.e., same relative area of emitter-base junction and having equal collector current.

$$I_o = I_{REF}$$



**Fig. 2.** The basic BJT current mirror.

- Here  $Q_2$  is in active mode until  $V_o$  is 0.3 V or higher than emitter voltage. For obtaining the current transfer ratio, it is required to consider  $m$  times relative area of emitter-base junction (EBJ).

$$I_o = m I_{REF}$$

- The current transfer ratio,

$$\frac{I_o}{I_{REF}} = \frac{I_{s2}}{I_{s1}} = \frac{\text{Area of EBJ of } Q_2}{\text{Area of EBJ of } Q_1}$$

- From the node equation at collector of  $Q_1$ ,

$$I_{REF} = I_c + 2 I_c / \beta = I_c (1 + 2/\beta)$$

Since,

$$I_o = I_c$$

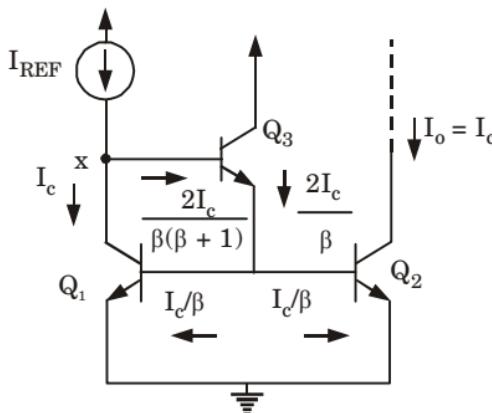
$$\frac{I_o}{I_{REF}} = \frac{I_c}{I_c (1 + 2/\beta)} = \frac{1}{1 + 2/\beta}$$

- Here for higher values of  $\beta$ , the error in the current transfer ratio can be significant, for example :  $\beta = 100$ , results 2 % error in current transfer ratio.
- However, the error due to finite  $\beta$  increases as the nominal current transfer ratio is increased.

#### **Improvement of base current mirror over simple current mirror (Base current compensation circuit) :**

- A bipolar current mirror with a current transfer ratio is less dependent on  $\beta$  than that of simple current mirror.
- This reduces dependency on  $\beta$  and is achieved by using transistor  $Q_3$ . The  $Q_3$  supplies the base current to the  $Q_1$  and  $Q_2$ .

3. The sum of base currents is divided by  $(\beta_3 + 1)$ , resulting in much smaller error current, that has to be supplied by  $I_{REF}$ .



**Fig. 3.** A current mirror with base current compensation.

4. Let us assume  $Q_1$  and  $Q_2$  are matched and having equal collector current. A node equation at node  $x$  gives

$$I_{REF} = I_c \left[ 1 + \frac{2}{\beta(\beta+1)} \right]$$

5. As,  $I_o = I_c$

The current transfer ratio of the mirror will be

$$\frac{I_o}{I_{REF}} = \frac{2}{1 + \beta(\beta+1)} \approx \frac{1}{1 + 2/\beta^2} \quad \dots(1)$$

Eq. (1) shows that the error due to finite  $\beta$  has been reduced from  $2/\beta$  to  $2/\beta^2$ .

6. However, the output resistance ( $r_o$ ) remains approximately equal to that of simple mirror.  
 7. If  $I_{REF}$  is not present, then we connect node  $x$  to the power supply  $V_{CC}$  through resistor  $R$ , then

$$I_{REF} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R}$$

3. Define the slew rate. Also derive the relationship between  $f_t$  and slew rate for the IC-741.

**Ans.**

- A. **Slew rate :** The slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per microsecond, i.e.,

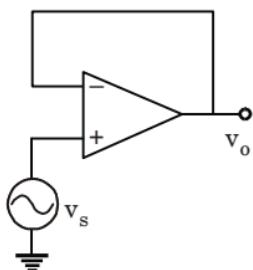
$$SR = \left. \frac{dv_o}{dt} \right|_{max} \text{ V/}\mu\text{s}$$

- B. **Relationship between  $f_t$  and SR :**

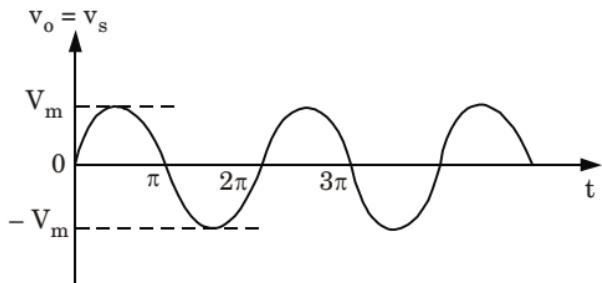
1. Consider a voltage follower shown in Fig. 4(a). The input is large amplitude, high frequency sine wave.  
 2. If  $v_s = V_m \sin \omega t$   
 Then, output  $v_o = V_m \sin \omega t$

3. Fig. 4(b) shows the input-output waveform.  
 4. The rate of change of the output is given by,

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$



(a) Voltage follower



(b) Input/output waveform

**Fig. 4.**

5. The maximum rate of change of the output occurs when  $\cos \omega t = 1$ .

That is,  $SR = \left. \frac{dv_o}{dt} \right|_{\max} = \omega V_m$

6. Therefore, slew rate =  $2\pi f V_m$  V/s

$$= \frac{2\pi f V_m}{10^6} \text{ V}/\mu\text{s}$$

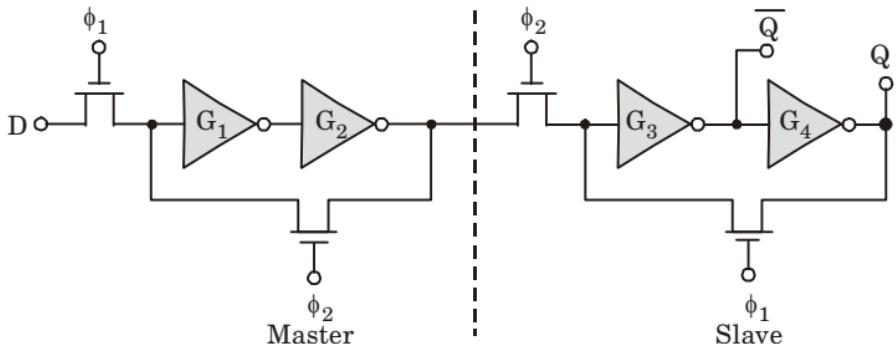
where,  $f$  = Input frequency (Hz)

$V_m$  = Peak output amplitude.

4. Sketch the properly labeled master slave D flip-flop circuit and explain its operation with the help of proper waveform of the clock signal.

**Ans.**

1. The master-slave consists of pair of D flip-flop circuits as shown in Fig. 5. To emphasize that two clock phases must be non-overlapping, we denote them by  $\phi_1$  and  $\phi_2$ .

**Fig. 5.**

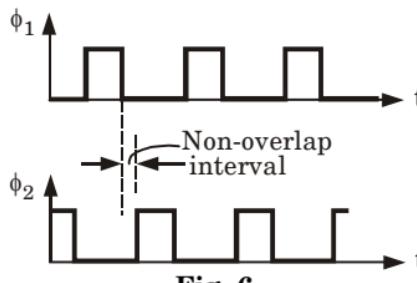


Fig. 6.

2. When  $\phi_1$  is high and  $\phi_2$  is low, the input is connected to the master latch whose feedback loop is opened, while the slave latch is isolated.
3. Thus, the output  $Q$  remains at the value stored previously in the slave latch whose loop is now closed. The node capacitances of master latch are charged to the appropriate voltages corresponding to the present value of  $D$ .
4. When  $\phi_1$  goes low, the master latch is isolated from input data line  $D$ . When  $\phi_2$  goes high, the feedback loop of the master latch is closed, locking in the value of  $D$ . Further, its output is connected to the slave latch whose loop is now open.
5. The node capacitances in the slave are appropriately charged so that, when  $\phi_1$  goes high again, the slave latch locks in the new value of  $D$  and provides the output  $Q = D$ . The  $D$  flip-flop has two inputs, data input  $D$  and a clock input  $\phi$ . The complementary outputs are labeled as  $Q$  and  $\bar{Q}$ .

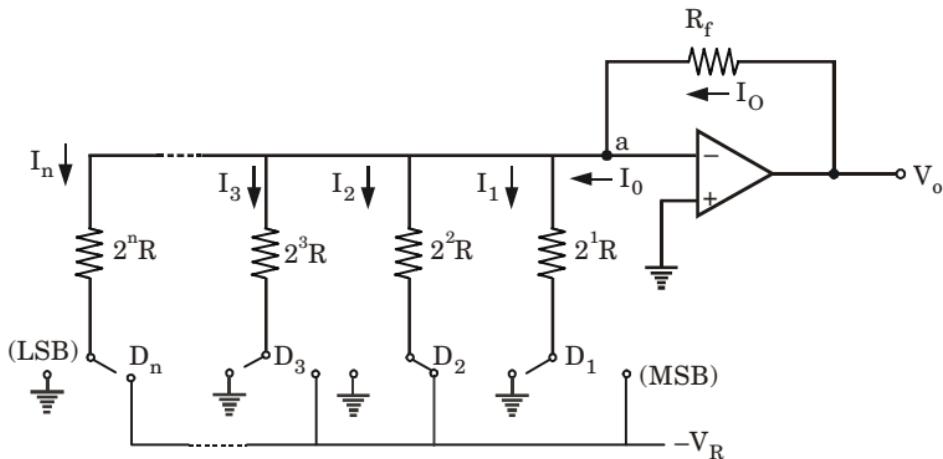
5. **What is a DAC ? Describe the weighted resistor DAC. Give mathematical expressions in support of your answer.**

**Ans.**

- A. **DAC :** In the stable state, the output  $\bar{Q}$  of the flip-flop (FF) is high. This makes the output low because of power amplifier which is basically an inverter.
- B. **Weighted resistor DAC :**
  1. In a weighted resistor  $D/A$  converter every resistor has a definite weight assigned to it.
  2. One of the simplest circuit shown in Fig. 7 is a summing amplifier with a binary weighted resistor network. It has  $n$ -electronic switches  $D_{n-1}, D_{n-2} \dots D_1, D_0$  controlled by binary input word.
  3. If the binary input to a particular switch is 1, it connects the resistor to the reference voltage ( $-V_R$ ). And if the input bit is 0, the switch connects the resistor to the ground.
  4. From Fig. 7, the output current  $I_o$  for an ideal Op-Amp can be written as

$$I_o = I_1 + I_2 + I_3 + \dots + I_n$$

$$\begin{aligned}
 &= \frac{V_R}{2R} D_1 + \frac{V_R}{2^2 R} D_2 + \frac{V_R}{2^3 R} D_3 + \dots + \frac{V_R}{2^n R} D_n \\
 &= \frac{V_R}{R} (D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} + \dots + D_n 2^{-n})
 \end{aligned}$$



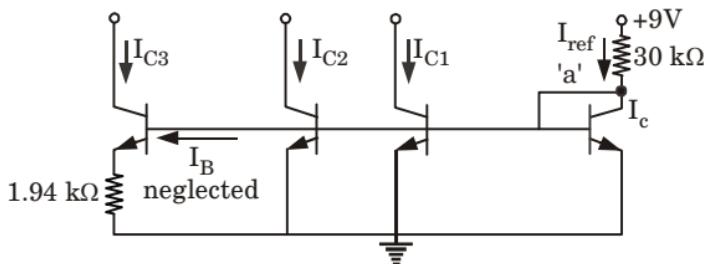
**Fig. 7.** A simple weighted resistor D/A converter.

5. The output voltage,

$$V_o = I_o R_f$$

$$= V_R \frac{R_f}{R} (D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} + \dots + D_n 2^{-n})$$

6. Determine  $I_{C1}, I_{C2}, I_{C3}$  for the circuit shown in Fig. 8. Assume  $\beta = 125$ .



**Fig. 8.**

**Ans.**

1. We know,  $I_{ref} = \frac{9V - 0.7V}{30\text{ k}\Omega} = 0.277\text{ mA}$

2. Also at node 'a'

$$\begin{aligned}
 I_{ref} &= I_C + 3I_B \quad (\text{Assume } I_{B3} \text{ of Widlar source negligible}) \\
 &= I_C \left( 1 + \frac{3}{\beta} \right) \quad \left[ \because I_B = \frac{I_C}{\beta} \right]
 \end{aligned}$$

$$I_C = I_{\text{ref}} \left( \frac{\beta}{3 + \beta} \right)$$

3. Putting the values of  $I_{\text{ref}}$  and  $\beta$  then we get,

$$I_C = 0.277 \left( \frac{125}{3 + 125} \right)$$

$$I_{C1} = I_{C2} = I_C = 0.271 \text{ mA}$$

4. Calculate  $I_{C3}$ , using equation

$$\left( \frac{1}{\beta} + 1 \right) I_{C3} R_E = V_T \ln \left( \frac{I_{C1}}{I_{C3}} \right)$$

$$1.94 = \frac{0.025}{I_{C3} \left( 1 + \frac{1}{125} \right)} \ln \frac{0.271}{I_{C3}} \quad \dots(1)$$

5. After solving the eq. (1) we obtain

$$I_{C3} = 0.0287 \text{ mA}$$

7. Draw the functional block diagram of IC-555 and explain its working. Design a 555 timer as an astable multivibrator with an output signal timer frequency of 700 Hz and 60 % duty cycle.

**Ans.**

**A. Functional block diagram and working of IC 555 :**

- In the stable state, the output  $\bar{Q}$  of the flip-flop (FF) is high. This makes the output low because of power amplifier which is basically an inverter.
- If negative going trigger pulse is applied to pin 2 and should have its DC level greater than the threshold level of the lower comparator (*i.e.*,  $V_{CC}/3$ ), now the trigger passes through ( $V_{CC}/3$ ), the output of the lower comparator goes high and sets the FF ( $Q = 1, \bar{Q} = 0$ ). Therefore the output of IC 555 becomes high.
- When the threshold voltage at pin 6 passes through ( $2/3$ )  $V_{CC}$ , the output of the upper comparator goes high and resets the FF ( $Q = 0, \bar{Q} = 1$ ).
- The reset input (pin 4) is used to reset the FF and the flip flop output  $\bar{Q}$  becomes high and the output of IC 555 becomes low because the output of FF is 1.

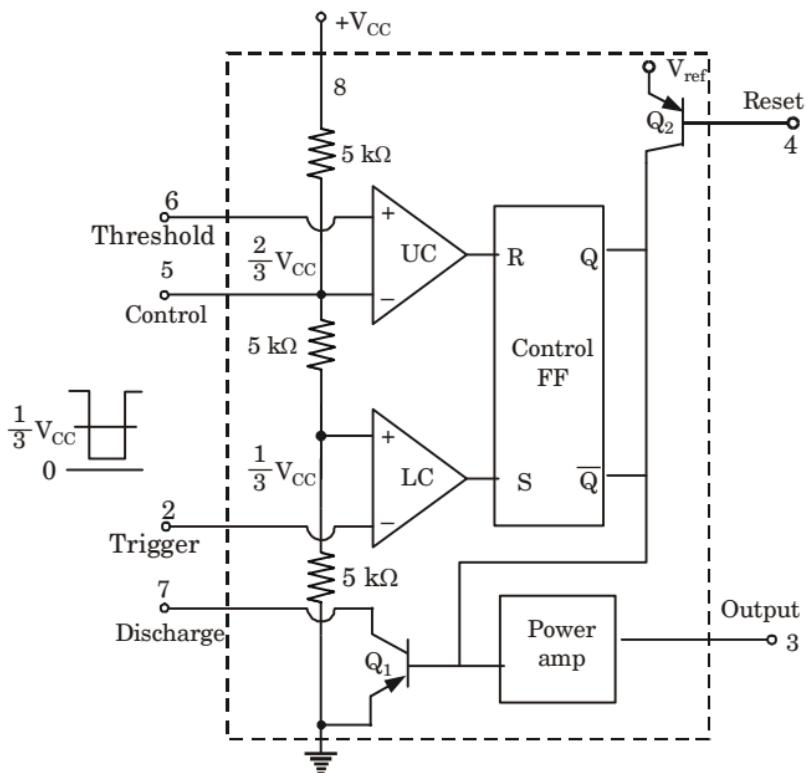


Fig. 9. Functional diagram of IC 555.

**B. Numerical :**

**Given :** Duty cycle,  $D = 60\% = 0.6$ , Frequency,  $f = 700 \text{ Hz}$

**To Design :** 555 timer as an astable multivibrator.

1. Assume,  $C = 0.01 \mu\text{F}$

2. We know,  $D = \frac{R_1 + R_2}{R_1 + 2R_2}$

$$0.6 = \frac{R_1 + R_2}{R_1 + 2R_2} \quad \dots(1)$$

3. Also,  $f = \frac{1.44}{(R_1 + 2R_2)C}$

$$0.01 \times 10^{-6} \times 700 = \frac{1.44}{R_1 + 2R_2}$$

$$R_1 + 2R_2 = \frac{1.44}{7} \times 10^6 = 2 \times 10^5 \Omega \quad \dots(2)$$

4. Substituting this value from eq. (2) in eq. (1)

$$0.6 = \frac{R_1 + R_2}{2 \times 10^5}$$

$$12 \times 10^4 = R_1 + R_2 \quad \dots(3)$$

$$R_B = 80 \text{ k}\Omega$$

$$R_A = 40 \text{ k}\Omega$$

5. The circuit is shown in Fig. 10.

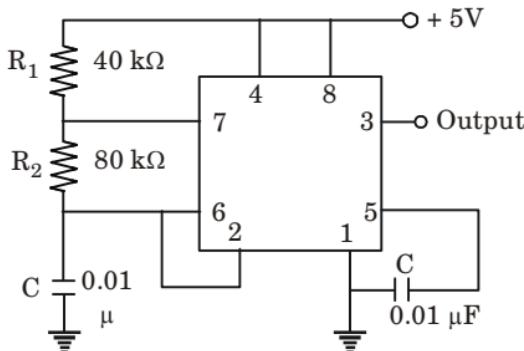


Fig. 10.

8. Describe the Antoniou inductance simulation circuit with properly labeled circuit diagram and give mathematical expressions in support of your answer.

**Ans.**

1. Fig. 11 shows the Antoniou inductance simulation circuit.

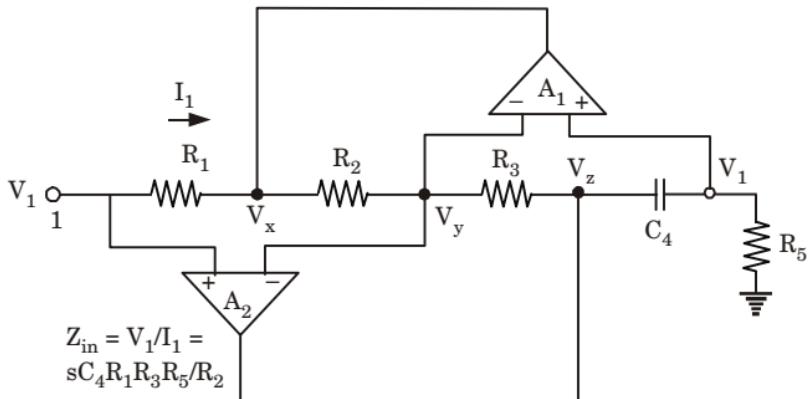


Fig. 11.

2. Applying KCL, we get

$$\frac{V_1 - V_z}{1/sC_4} + \frac{V_1}{R_5} = 0$$

$$V_z = V_1 \left[ 1 + \frac{1}{sC_4 R_5} \right]$$

3. Apply KCL, we get

$$\frac{V_y - V_x}{R_2} + \frac{V_y - V_z}{R_3} = 0 \quad \dots(1)$$

4. Substituting the value of  $V_z$  in eq. (1)

$$\frac{V_y - V_x}{R_2} + \frac{V_y - V_1 \left( 1 + \frac{1}{sC_4 R_5} \right)}{R_3} = 0$$

$$R_3(V_y - V_x) + R_2 V_y - R_2 V_1 \left( 1 + \frac{1}{sC_4 R_5} \right) = 0 \quad \dots(2)$$

5. Apply KCL, then we get

$$\frac{V_x - V_1}{R_1} + \frac{V_x - V_y}{R_2} = 0$$

$$R_2(V_x - V_1) + R_1(V_x - V_y) = 0$$

$$V_x(R_1 + R_2) = R_2 V_1 + R_1 V_y$$

$$V_y = \frac{V_x(R_1 + R_2)}{R_1} - \frac{R_2}{R_1} V_1 \quad \dots(3)$$

6. Now put the value of  $V_y$  in eq. (2),

$$\text{then, } V_x = \left( V_1 + \frac{V_1 R_2}{sC_4 R_5 R_3} \right)$$

7. Current across resistance  $R_1$ ,

$$I_1 = \left[ V_1 - \left( V_1 + \frac{V_1 R_2}{sC_4 R_5 R_3} \right) \right] \times \frac{1}{R_1}$$

$$I_1 = \frac{V_1 R_2}{sC_4 R_5 R_3 R_1}$$

8. Then input impedance

$$Z_{in} = \frac{V_1}{I_1} = \frac{sC_4 R_1 R_3 R_5}{R_2}$$

which is that of an inductance  $L$  given by,

$$L = \frac{C_4 R_1 R_3 R_5}{R_2}$$

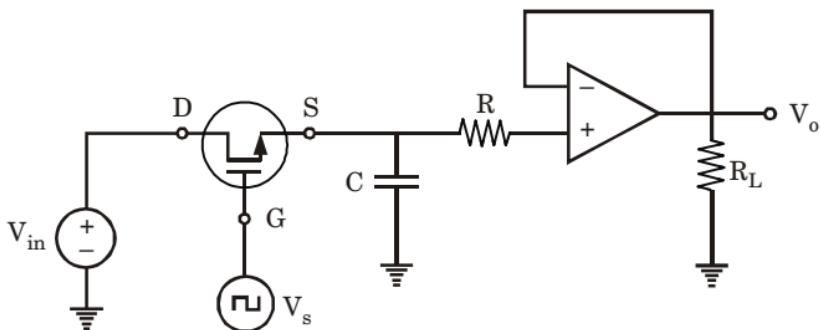
9. If  $R_1 = R_2 = R_3 = R_5 = R$  and  $C_4 = C$   
then,  $L = CR^2$ .

9. **Describe the sample and hold circuit with the help of an Op-Amp. What are the applications of sample and hold circuit ?**

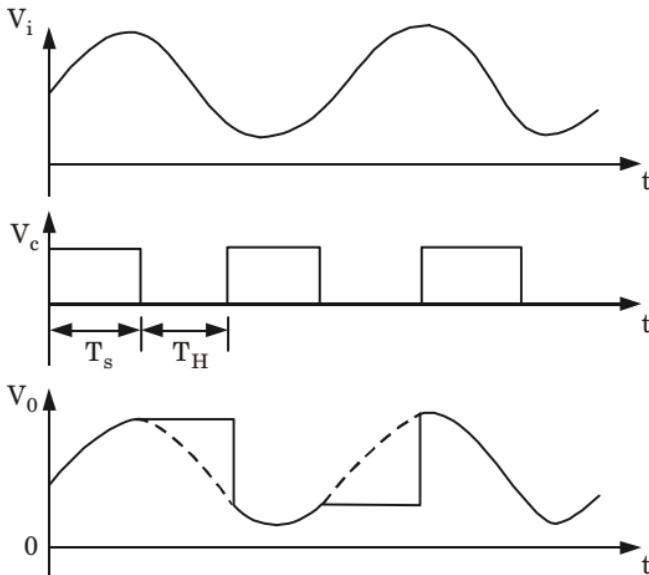
**Ans.**

A. **Sample and hold circuit :**

- Fig. 12 shows the circuit for sample and hold using Op-Amp. It samples an input signal and holds on to its last sampled value until the input is sampled again.

**Fig. 12.**

2. Op-Amp and enhancement MOSFET is used in the circuit. MOSFET acts as switch to control  $V_s$  while  $C$  serves as a storage element.  $V_{in}$  to be sampled is applied to drain and  $V_s$  across the gate of MOSFET.
3. During positive portion of  $V_s$ , the MOSFET conducts and allow input voltage to charge capacitor  $C$ .

**Fig. 13.**

4. When  $V_s$  is zero, the MOSFET is OFF and the discharge path for capacitor  $C$  is through the Op-Amp.
5. However, the input resistance of the Op-Amp voltage follower is also very high; hence the voltage across  $C$  is retained. Fig. 13 shows the input and output waveforms.
6. The time period  $T_s$  of voltage  $V_s$  during which the voltage across the  $C$  is equal to the input voltage are called sample periods.
7. The time period  $T_H$  of  $V_s$  during which the voltage across the capacitor  $C$  is constant are called hold periods as shown in Fig. 13.

**B. Applications :**

- i. PAM demodulator.
- ii. PCM.

- iii. Analog to digital converters.

### SECTION - C

**Note :** Attempt any **two** questions from this section : **(15 × 2 = 30)**

- 10. Describe the circuit for the KHN filter using three Op-Amp. Design a second order Butterworth low-pass filter having upper cut-off frequency 1 KHz. Determine its frequency response.**

**Ans.**

**A. KHN filter :**

1. The second order high-pass transfer function is

$$\frac{V_{hp}}{V_i} = \frac{Ks^2}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2} = T_{hp} \quad \dots(1)$$

where  $K$  is high frequency gain

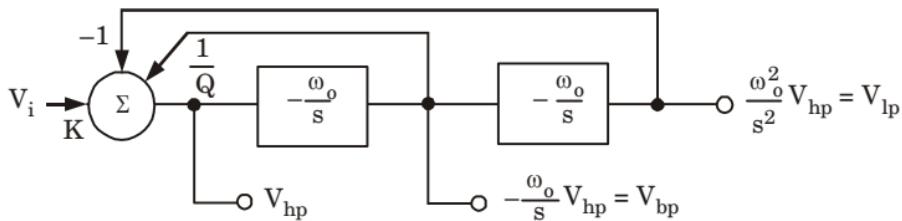
2. Simplify eq. (1) and we get,

$$V_{hp} + \frac{1}{Q} \left( \frac{\omega_o}{s} V_{hp} \right) + \left( \frac{\omega_o^2}{s^2} V_{hp} \right) = KV_i \quad \dots(2)$$

3. The signal ( $\omega_o/s$ )  $V_{hp}$  can be obtained by passing  $V_{hp}$  through an integrator with time constant equal to  $1/\omega_o$ .
4. Passing resulting signal through another identical integrator results in the third signal involving  $V_{hp}$  in eq. (2) and rearranging eq. (2), we get

$$V_{hp} = KV_i - \frac{1}{Q} \frac{\omega_o}{s} V_{hp} - \frac{\omega_o^2}{s^2} V_{hp} \quad \dots(3)$$

5. Biquad means the circuit is capable of realizing a biquadratic transfer function.
6. Eq. (3) can be transfer to block diagram as shown in Fig. 14.



**Fig. 14.**

7. The output of second integrator is labeled as  $V_{lp}$  while  $V_{bp}$  for first integrator.
8. Bandpass filter transfer function is given by

$$T_{bp} = \frac{\left(-\frac{\omega_0}{s}\right) V_{hp}}{V_i} \quad \dots(4)$$

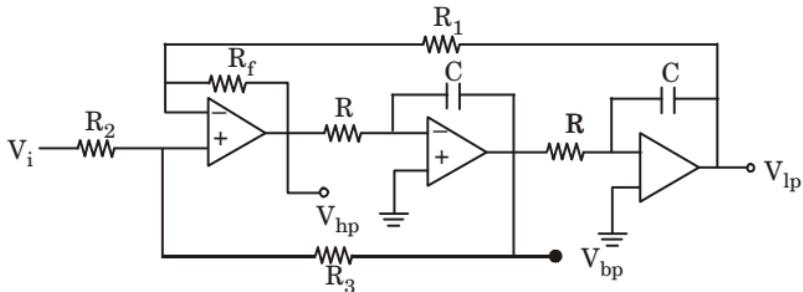
9. Using eq. (1),  $T_{bp} = \frac{-K\omega_o s}{s^2 + s(\omega_o/Q) + \omega_o^2}$  ... (5)

10. Low-pass filter transfer function is given by (using eq. (1))

$$T_{lp} = \frac{\omega_o^2}{s^2} \frac{V_{hp}}{V_i} = \frac{K\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2} \quad \dots (6)$$

11. To obtain Op-Amp circuit in Fig. 15, we replace each integrator with Miller integrator circuit having  $CR = 1/\omega$ , also replace summer block with Op-Amp summing circuit.

12. The resulting circuit is known as Kerwin-Huelsman-Newcomb or KHN biquad as shown in Fig. 15.



**Fig. 15.** KHN biquad filter.

13. Select suitable values of  $C$  and  $R$  of integrator so  $CR = 1/\omega_L$ . For resistors, we use superposition to express the output of summer  $V_{hp}$  in terms of its inputs,

$$V_{bp} = -\left(\frac{\omega_o}{s}\right)V_{hp} \text{ and } V_{lp} = \left(\frac{\omega_o^2}{s^2}\right)V_{hp}$$

as,

$$V_{hp} = \frac{R_3}{R_2 + R_3} \left(1 + \frac{R_f}{R_1}\right) V_i + \frac{R_2}{R_2 + R_3} \left(1 + \frac{R_f}{R_1}\right) \left(-\frac{\omega_o}{s} V_{hp}\right) - \frac{R_f}{R_1} \left(\frac{\omega_o^2}{s^2} V_{hp}\right) \quad \dots (7)$$

14. Equating the last RHS term of eq. (3) and (7) gives

$$\frac{R_f}{R_1} = 1$$

15. Now equating second to last terms on RHS of eq. (3) and (4) and let  $R_1 = R_f$

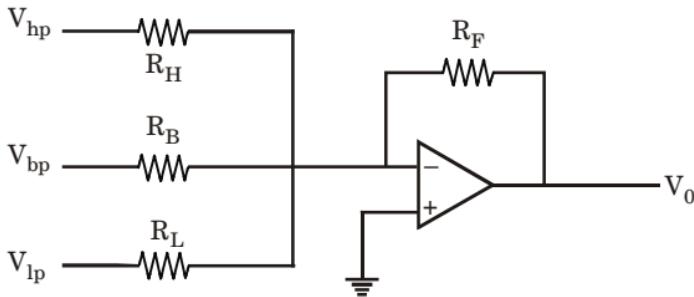
$$\frac{R_3}{R_2} = 2Q - 1$$

16. Finally equating coefficients of  $V_i$  in eq. (3) and (7) and substituting  $R_f = R_1$  and  $R_2/R_3$

Then,  $K = 2 - \left(\frac{1}{Q}\right)$

17. The KHN biquad can be used to realize notch and all-pass functions by summing weighted versions of the three outputs LP, BP, and HP. Such an Op-Amp summer is shown in Fig. 16.
18. From Fig. 16, we can write

$$\begin{aligned} V_0 &= - \left( \frac{R_F}{R_H} V_{hp} + \frac{R_F}{R_B} V_{bp} + \frac{R_F}{R_L} V_{lp} \right) \\ &= - V_i \left( \frac{R_F}{R_H} T_{hp} + \frac{R_F}{R_B} T_{bp} + \frac{R_F}{R_L} T_{lp} \right) \end{aligned} \quad \dots(8)$$



**Fig. 16.** Notch and all pass filter using KHN filter.

19. Substituting for  $T_{hp}$ ,  $T_{bp}$ , and  $T_{lp}$  from eq. (1), (5) and (6) give the overall transfer function

$$\frac{V_0}{V_i} = -K \frac{(R_F / R_H)s^2 - s(R_F / R_B)\omega_0 + (R_F / R_L)\omega_0^2}{s^2 + s(\omega_0 / Q) + \omega_0^2}$$

20. To obtain notch function by selecting  $R_B = \infty$

$$\frac{R_H}{R_L} = \left( \frac{\omega}{\omega_0} \right)^2$$

### B. Numerical :

**Given :**  $f_H = 1 \text{ KHz} = 1/2\pi RC$

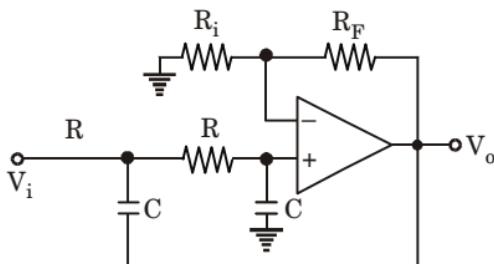
**To Design :** Second order low-pass Butterworth filter.

- Let  $C = 0.1 \mu\text{F}$ , gives the choice of  $R = 1.6 \text{ K}\Omega$ .
- For  $n = 2$ , the damping factor  $\alpha = 1.414$ . Then the passband gain,  $A_o = 3 - \alpha = 3 - 1.414 = 1.586$ .
- The transfer function of the normalized second order low-pass Butterworth filter is

$$= \frac{1.586}{s_n^2 + 1.414 s_n + 1}$$

Now,  $A_o = 1 + \frac{R_F}{R_i} = 1.586 = 1 + 0.586$

- Let,  $R_F = 5.86 \text{ K}\Omega$  and  $R_i = 10 \text{ K}\Omega$ . Then, we get  $A_o = 1.586$ .
- The circuit realized in the Fig. 17 with component values as  $R = 1.6 \text{ K}\Omega$ ,  $C = 0.1 \mu\text{F}$ ,  $R_F = 5.86 \text{ K}\Omega$  and  $R_i = 10 \text{ K}\Omega$ .



**Fig. 17.** Second order low-pass butterworth filter.

6. For minimum DC offset,  $R_i \parallel R_F = 2R$ , which has not been taken into consideration here, otherwise, we would have to modify the values of  $R$  and  $C$  accordingly which comes out to be  $R = 1.85 \text{ K}\Omega$ ,  $C = 0.086 \mu\text{F}$ ,  $R_F = 5.86 \text{ K}\Omega$ ,  $R_i = 10 \text{ K}\Omega$ .

#### C. Frequency response :

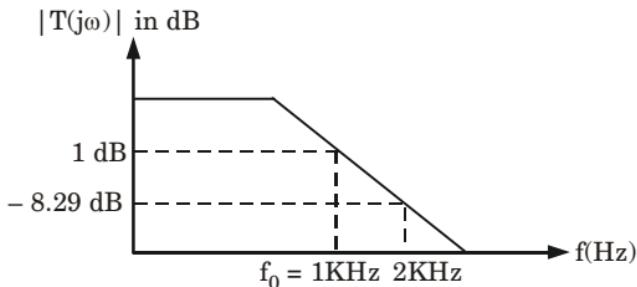
1. The gain of second order low-pass Butterworth filter is given by

$$|T(j\omega)| = \frac{1.586}{\sqrt{1 + \left(\frac{f}{1 \times 10^3}\right)^4}}$$

$$|T(j\omega)|_{\text{dB}} = 20 \log \frac{1.586}{\sqrt{1 + \left(\frac{f}{1 \times 10^3}\right)^4}}$$

Input frequency (Hz)	$ T(j\omega) $ dB
10	4.34
100	4.005
1000	0.99 $\approx$ 1
2000	-8.298

2. Frequency response is shown in Fig. 18.



**Fig. 18.**

- 11. Describe different regions of operation for CMOS inverter over its VTC characteristics.**

Consider a CMOS inverter with following parameters :

$$V_{DD} = 3.3 \text{ V}, V_{T0,N} = 0.6 \text{ V}, V_{T0,P} = 0.7 \text{ V}, \\ k_n = 200 \mu\text{A/V}^2, k_p = 80 \mu\text{A/V}^2$$

Calculate the noise margin of the CMOS inverter circuit.

**Ans.**

**A. Regions of operation for CMOS :**

1. The NMOS transistor operates in saturation if  $V_{in} > V_{T0,N}$  and if the following condition is satisfied.

$$V_{DS,N} \geq V_{GS,N} - V_{T0,N} \Leftrightarrow V_{out} \geq V_{in} - V_{T0,N} \quad \dots(1)$$

2. The PMOS transistor operates in saturation if  $V_{in} < (V_{DD} + V_{T0,P})$ , and if :

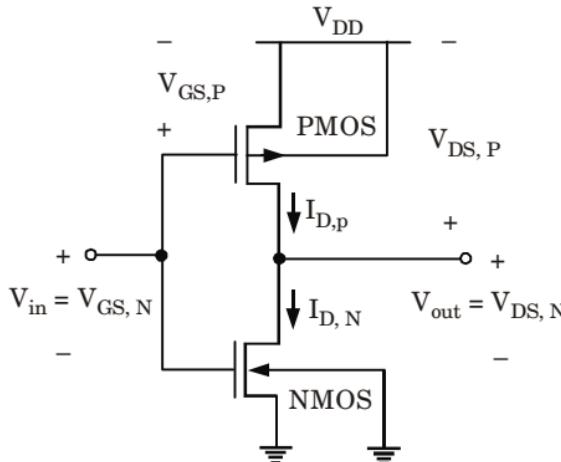
$$V_{DS,P} \leq V_{GS,P} - V_{T0,P} \Leftrightarrow V_{out} \leq V_{in} - V_{T0,P} \quad \dots(2)$$

3. The table 1 lists these regions and the corresponding critical input and output voltage levels.

**Table 1.**

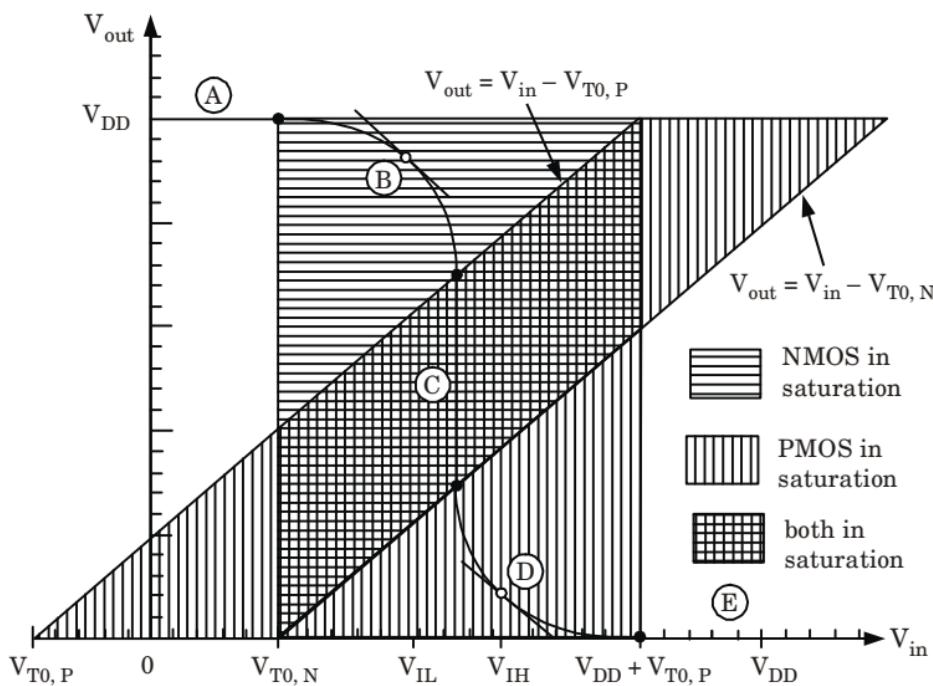
Region	$V_{in}$	$V_{out}$	NMOS	PMOS
A	$< V_{T0,N}$	$V_{OH}$	cut-off	linear
B	$V_{IL}$	high $\approx V_{OH}$	saturation	linear
C	$V_{th}$	$V_{th}$	saturation	saturation
D	$V_{IH}$	low $\approx V_{OL}$	linear	saturation
E	$> (V_{DD} + V_{T0,P})$	$V_{OL}$	linear	cut-off

4. In region A, where  $V_{in} < V_{T0,N}$ , the NMOS transistor is cut-off and the output voltage is equal to  $V_{OH} = V_{DD}$ .



**Fig. 19.** CMOS inverter circuit.

5. As the input voltage is increased beyond  $V_{T0,N}$  (into region B), the NMOS transistor starts conducting in saturation mode and the output voltage begins to decrease. The critical voltage  $V_{IL}$  which corresponds to  $(dV_{out}/dV_{in}) = -1$  is located within region B.
6. As the output voltage further decreases, the PMOS transistor enters saturation at the boundary of region C. It is seen from, Fig. 19 that the inverter threshold voltage, where  $V_{in} = V_{out}$ , is located in region.
7. When the output voltage  $V_{out}$  falls below  $(V_{in} - V_{T0,N})$ , the NMOS transistor starts to operate in linear mode. This corresponds to region D in Fig. 20, where the critical voltage point  $V_{IH}$  with  $(dV_{out}/dV_{in}) = -1$  is also located.
8. Finally, in region E, with the input voltage  $V_{in} > (V_{DD} + V_{T0,P})$ , the PMOS transistor is cut-off, and the output voltage is  $V_{OL} = 0$ .



**Fig. 20.** Operating regions of the NMOS and the PMOS transistors.

### B. Numerical :

**Given :**  $V_{DD} = 3.3 \text{ V}$ ,  $V_{T0,N} = 0.6 \text{ V}$ ,  $V_{T0,P} = 0.7 \text{ V}$ ,  $k_n = 200 \mu\text{A/V}^2$ ,  $k_p = 80 \mu\text{A/V}^2$

**To Find :** Noise margin.

1. We know,  $k_R = \frac{k_n}{k_p} = \frac{200}{80} = 2.5$
2. As  $V_{OL} = 0$  and  $V_{OH} = 3.3 \text{ V}$ , to calculate  $V_{IL}$  in terms of the output voltage, we use

$$\begin{aligned}
 V_{IL} &= \frac{2V_{out} + V_{T0,P} - V_{DD} + k_R V_{T0,N}}{1 + k_R} \\
 &= \frac{2V_{out} - 0.7 - 3.3 + 1.5}{1 + 2.5} \\
 &= 0.57 V_{out} - 0.71
 \end{aligned} \quad \dots(1)$$

$$3. \text{ Also, } k_n(V_{IL} - V_{T0,N}) = k_p(2V_{out} - V_{IL} + V_{T0,P} - V_{DD}) \quad \dots(2)$$

4. Putting value of  $V_{IL}$  in eq. (2), we get

$$\begin{aligned}
 2.5(0.57 V_{out} - 0.71 - 0.6)^2 &= 2(0.57 V_{out} - 0.71 - 3.3 + 0.7) \\
 (V_{out} - 3.3) - (V_{out} - 3.3)^2 &
 \end{aligned} \quad \dots(3)$$

5. This expression yields a second-order polynomial in  $V_{out}$ , as follows :

$$0.66 V_{out}^2 + 0.05 V_{out} - 6.65 = 0 \quad \dots(4)$$

$$V_{out} = 3.14 \text{ V} \quad \dots(5)$$

6. From eq. (1), we can calculate the critical voltage  $V_{IL}$  as :

$$V_{IL} = 0.57 \times 3.14 - 0.71 = 1.08 \text{ V}$$

7. To calculate  $V_{IH}$  in terms of the output voltage, use :

$$\begin{aligned}
 V_{IH} &= \frac{V_{DD} + V_{T0,P} + k_R (2V_{out} + V_{T0,N})}{1 + k_R} \quad \dots(6) \\
 &= \frac{3.3 - 0.7 + 2.5(2V_{out} + 0.6)}{1 + 2.5} = 1.43 V_{out} + 1.17
 \end{aligned} \quad \dots(7)$$

$$8. \text{ Again, } k_n(-V_{IH} + V_{T0,N} + 2V_{out}) = k_p(V_{IH} - V_{DD} - V_{T0,P}) \quad \dots(8)$$

9. Now, substitute the value of  $V_{IH}$  in eq. (8),

$$2.5[2(1.43 V_{out} + 1.17 - 0.6)V_{out} - V_{out}^2] = (1.43 V_{out} - 1.43)^2 \quad \dots(9)$$

$$2.61 V_{out}^2 + 6.94 V_{out} - 2.04 = 0$$

10. On solving, we get,

$$V_{out} = 0.27 \text{ V} \quad \dots(10)$$

11. From eq. (9) and (10) we can calculate the critical voltage  $V_{IH}$  as :

$$V_{IH} = 1.43 \times 0.27 + 1.17 = 1.55 \text{ V}$$

12. Finally, we find the noise margins for low voltage levels and for high voltage levels

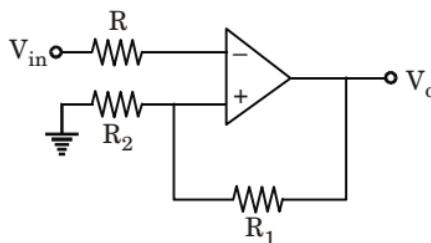
$$NM_L = V_{IL} - V_{OL} = 1.08 \text{ V}$$

$$NM_H = V_{OH} - V_{IH} = 1.75 \text{ V}$$

12. **Describe the Schmitt trigger with the help of proper circuit diagram and transfer characteristics. A Schmitt trigger with the upper threshold level  $V_{UT} = 0 \text{ V}$  and hysteresis width is  $0.2 \text{ V}$  converts  $1 \text{ KHz}$  sine wave of amplitude  $4 V_{PP}$  into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.**

**Ans.****A. Schmitt trigger and its transfer characteristics :**

- If positive feedback is added to the comparator circuit, gain can be increased greatly. This circuit is called Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback.
- Schmitt trigger also exhibits the phenomenon of hysteresis. The input voltage is applied to the (-ve) input terminal and feedback voltage to the (+ve) input terminal.
- Input voltage  $V_{in}$  triggers output  $V_o$ , every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage ( $V_{UT}$ ) and lower threshold voltage ( $V_{LT}$ ).

**Fig. 21.** Schmitt trigger.

- Now, suppose the output  $V_o = +V_{sat}$ . The voltage at (+) input terminal will be

$$V_{UT} = \frac{R_2}{R_1 + R_2} (+V_{sat}) \quad \dots(1)$$

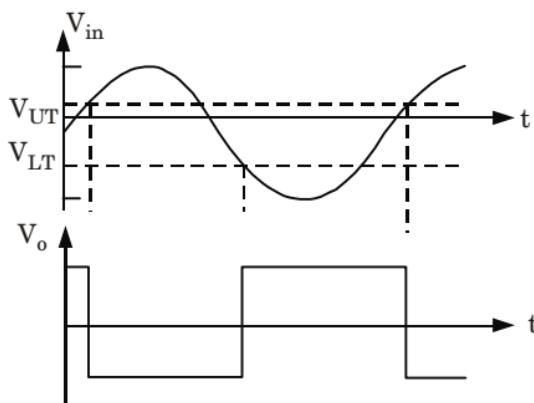
This voltage is upper threshold voltage. As long as  $V_{in}$  is less than  $V_{UT}$ , the output  $V_o$  remains constant at  $+V_{sat}$ .

- When  $V_{in}$  is just greater than  $V_{UT}$ , the output then switches to  $-V_{sat}$  and remains at this level as long as  $V_{in} > V_{UT}$ .
- For  $V_o = -V_{sat}$ , the voltage at (+ve) input terminal will be

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{sat}) \quad \dots(2)$$

This voltage is called lower threshold voltage.

- The output voltage is  $-V_{sat}$  as long as  $V_{in}$  is above or positive with respect to  $V_{LT}$ . The output voltage  $V_o$  changes to  $+V_{sat}$  if  $V_{in}$  goes more negative than or below  $V_{LT}$ . Resistor  $R$  is shown as  $R_1 \parallel R_2$  compensate for input bias current.
- Input and output voltage waveforms are shown in Fig. 22.

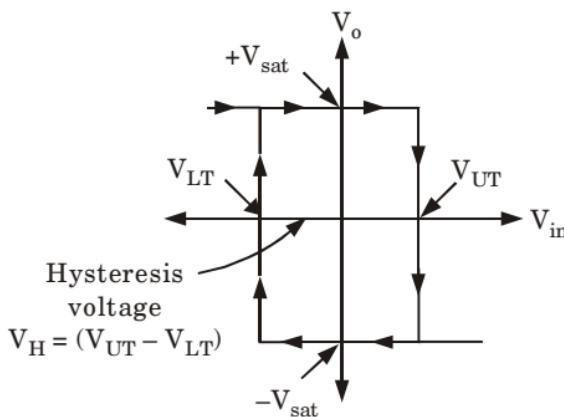
**Fig. 22.****9. Hysteresis curve (Transfer characteristics) :**

- From eq. (1) and (2),

$$V_{UT} > V_{LT}$$

$$\therefore V_{UT} - V_{LT} = \frac{2R_2}{R_1 + R_2} V_{sat}$$

This difference is called hysteresis width.

**Fig. 23.**

- $V_H$  is also called dead band because change in  $V_{in}$  do not change the output voltage. That is when the input exceeds  $V_{UT}$ , out switches from  $+ V_{sat}$  to  $- V_{sat}$  and reverts back to its original state,  $+ V_{sat}$ , when the input goes below  $V_{LT}$ .

- Uses :** Schmitt trigger is used to convert any wave into a square wave.

**B. Numerical :**

**Given :**  $V_{UT} = 0$ ,  $V_H = 0.2$  V,  $f = 1$  KHz

**To Find :** Time duration.

1.  $V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$

So,  $V_{LT} = -0.2 \text{ V}$

2. In Fig. 24 the angle  $\theta$  can be calculated as

$$-0.2 = V_m \sin(\pi + \theta) = -V_m \sin \theta = -2 \sin \theta$$

$$\theta = \arcsin 0.1 = 0.1 \text{ radian}$$

3. The period,  $T = 1/f = 1/1000 = 1 \text{ ms}$

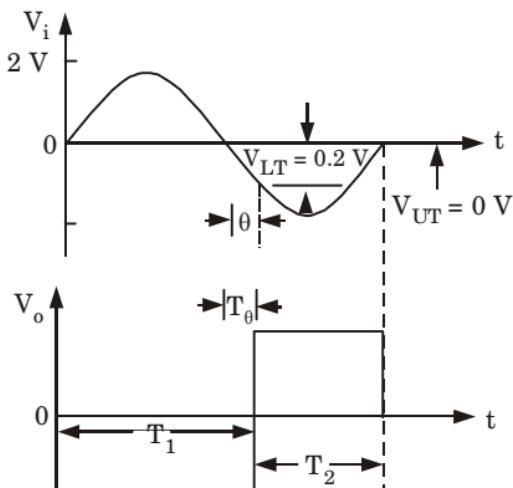
$$\omega T_0 = 2\pi (1000) T_0 = 0.1$$

$$T_0 = (0.1/2\pi) \text{ ms} = 0.016 \text{ ms}$$

4. So,  $T_1 = T/2 + T_0 = 0.516 \text{ ms}$

and

$$T_2 = T/2 - T_0 = 0.484 \text{ ms}$$



**Fig. 24.**



**B. Tech.****(SEM. V) ODD SEMESTER THEORY  
EXAMINATION, 2016-17  
INTEGRATED CIRCUITS****Time : 3 Hours****Max. Marks : 100****SECTION-A**

1. Attempt **all** parts. All parts carry equal marks. Write answer of each part in short. **(2 × 10 = 20)**
- a. Design a multiple feedback narrow band pass filter with  $f_c = 1 \text{ kHz}$ ,  $Q = 3$  and  $A = 10$ .
- b. For a first order Butterworth high pass filter, evaluate the value of  $R$  if  $C = 0.0047 \mu\text{F}$  and  $f_c = 10 \text{ kHz}$ .
- c. Implement  $F = \overline{AB} + \overline{\overline{A}\overline{B}}$  using AND-OR-INVERT logic.
- d. Why CMOS NAND is preferred over CMOS NOR ?
- e. Name the circuit that is used to detect the peak value of non-sinusoidal waveforms. Explain the operation with neat circuit diagram.
- f. Draw and explain the generalized impedance converter circuit.
- g. What is the advantage of Widlar current source over constant current source ?
- h. For a dual slope ADC,  $t_1$  is 83.33 ms and the reference voltage is 100 mV. Calculate  $t_2$  if  $V_i$  is
  - i. 100 mV and ii. 200 mV.
- i. Which block of PLL decides capture range ? Explain.
- j. State the reasons for the offset currents at the input of the Op-Amp.

**SECTION-B**Attempt any **five** questions from this section :**(10 × 5 = 50)**

2. For 555 astable multivibrator  $R_A = 4.7 \text{ k}\Omega$ ,  $R_B = 1 \text{ k}\Omega$  and  $C = 1 \mu\text{F}$ . Determine the positive pulse width, the negative pulse width, and the free-running frequency. What is the duty cycle of output waveform ?
3. Why we need BJT base current compensation mirror circuit ? Draw the circuit and express relation between  $I_{\text{ref}}$  and  $I_0$  for same.
4. Explain the working of PLL with suitable block diagram. Write down the different applications of PLL.
5. Realize a simpler CMOS implementation of clocked SR flip-flop. Also explain the working of circuit.
6. Design a wide band pass filter with lower cut-off frequency  $f_L = 200 \text{ Hz}$ , higher cut-off frequency  $f_H = 1 \text{ kHz}$  and a passband gain = 4.
7. Explain working of precision full wave rectifier with necessary waveform.
8. Draw the circuit of KHN filter and derive the expression for its voltage gain.
9. Explain the types of phase detector with suitable circuit diagram and input-output waveforms.

### SECTION-C

Attempt any **two** questions from this section :  $(15 \times 2 = 30)$

10. Explain the generation of square and triangular waveforms from astable multivibrator operation using Op-Amp. Also find expression of the time period for both cases.
11. a. Design a CMOS half adder circuit with inputs  $A$  and  $B$ .  
b. Derive the formula for  $V_{IL}$  and  $V_{IH}$  of CMOS inverter.
12. Explain the circuit of Wilson MOS current mirror. Also discuss how it can be improved ? Draw the circuits and find expression of  $I_0$  for both, Wilson and modified Wilson current mirrors.



**SOLUTION OF PAPER (2016-17)****SECTION-A**

- 1.** Attempt **all** parts. All parts carry equal marks. Write answer of each part in short.  $(2 \times 10 = 20)$
- a.** Design a multiple feedback narrow band pass filter with  $f_c = 1 \text{ kHz}$ ,  $Q = 3$  and  $A = 10$ .

**Ans.****Given :**  $f_c = 1 \text{ kHz}$ ,  $Q = 3$  and  $A = 10$ **To Design :** Multiple feedback narrow band pass filter.

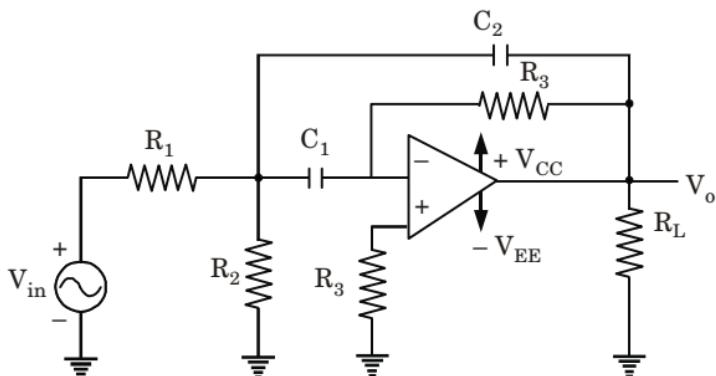
Let

$$C_1 = C_2 = C = 0.01 \mu\text{F}$$

$$R_1 = \frac{Q}{2\pi f_c C A} = \frac{3}{(2\pi)(10^3)(10^{-8})(10)} = 4.77 \text{ k}\Omega$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A)} = \frac{3}{(2\pi)(10^3)(10^{-8})[2(3)^2 - 10]} = 5.97 \text{ k}\Omega$$

$$R_3 = \frac{Q}{\pi f_c C} = \frac{3}{(\pi)(10^3)(10^{-8})} = 95.5 \text{ k}\Omega$$

**Fig. 1.**

- b.** For a first order Butterworth high pass filter, evaluate the value of  $R$  if  $C = 0.0047 \mu\text{F}$  and  $f_c = 10 \text{ kHz}$ .

**Ans.****Given :**  $C = 0.0047 \mu\text{F}$ ,  $f_c = 10 \text{ kHz}$ **To Find :**  $R$ .

$$\text{We know that, } f_c = \frac{1}{2\pi RC}$$

$$\text{Therefore, } R = \frac{1}{2\pi f_c C} = \frac{1}{2\pi(10 \times 10^3) \times 47 \times 10^{-10}} = 3.39 \text{ k}\Omega$$

- c. Implement  $F = \overline{AB} + \overline{A}\overline{B}$  using AND-OR-INVERT logic.

**Ans.**

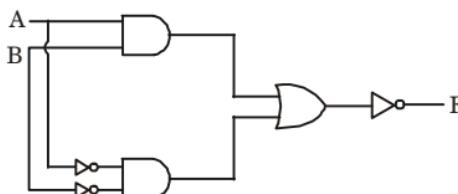


Fig. 2.

- d. Why CMOS NAND is preferred over CMOS NOR ?

**Ans.** The NOR gate will require much greater area than the NAND gate because  $p$ -region is usually two to three times  $n$ -region. For this reason, NAND gates are preferred for implementing combinational logic functions in CMOS.

- e. Name the circuit that is used to detect the peak value of non-sinusoidal waveforms. Explain the operation with neat circuit diagram.

**Ans.**

1. Peak detector is used to detect the peak value of non-sinusoidal waveforms.
2. The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value (almost indefinitely) on a capacitor.
3. If a higher peak signal value comes along, this new value is stored. The highest peak value is stored until the capacitor is discharged.
4. When input  $v_i$  exceeds  $v_c$ , the voltage across the capacitor, the diode  $D$  is forward biased and the circuit becomes a voltage follower.
5. Consequently, the output voltage  $v_o$  follows  $v_i$  as long as  $v_i$  exceeds  $v_c$ . When  $v_i$  drops below  $v_c$ , the diode becomes reverse-biased and the capacitor holds the charge till input voltage again attains a value greater than  $v_c$ .
6. Fig. 3(b) shows the voltage wave shape for the positive peak detector.

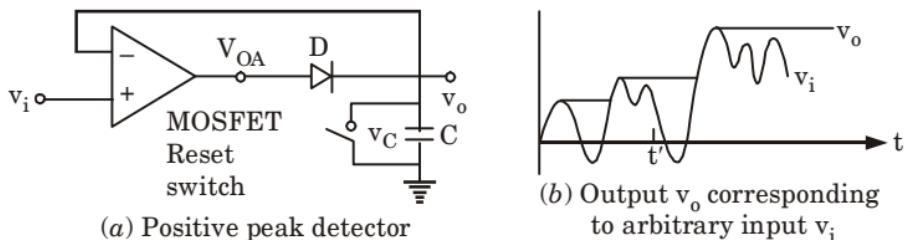


Fig. 3.

- f. Draw and explain the generalized impedance converter circuit.**

**Ans.**

- Generalized impedance converters (GIC) are Op-Amp circuits that employ  $RC$  networks for simulating frequency-dependent impedance elements such as inductors. Fig. 4 shows the circuit of a GIC.
- The input impedance of the circuit

$$Z_1 = \frac{V_{CC}}{I_C} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \quad \dots(1)$$

- Eq. (1) shows that the circuit shown in Fig. 4, can be used as grounded impedance whose nature and value depends on the nature and values of impedance elements  $Z_1$  to  $Z_5$ .

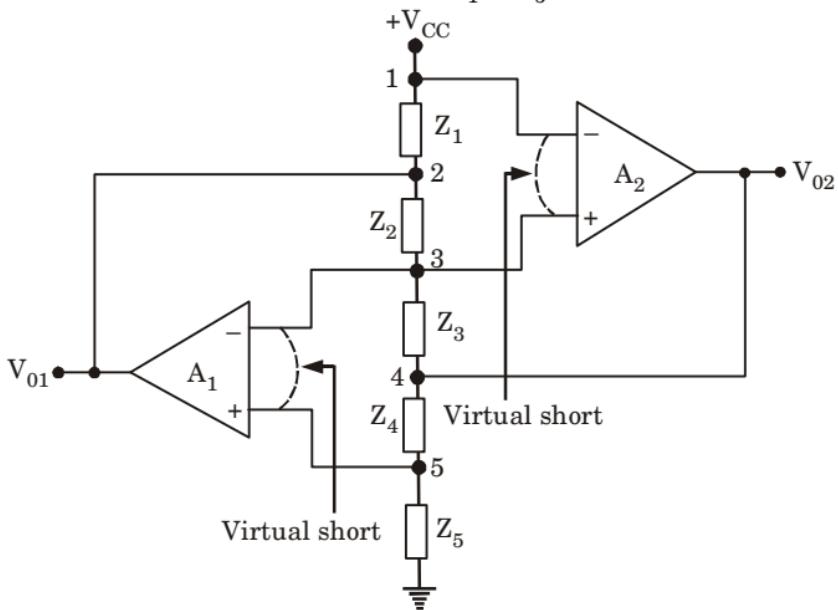


Fig. 4.

- g. What is the advantage of Widlar current source over constant current source ?**

**Ans.**

1. It requires less chip area.
2. The output resistance  $R_o$  is higher than basic current source; this is due to the emitter resistance  $R_E$ .
  
- h. For a dual slope ADC,  $t_1$  is 83.33 ms and the reference voltage is 100 mV. Calculate  $t_2$  if  $V_i$  is**
  - i. 100 mV and
  - ii. 200 mV.

**Ans.**

**Given :**  $t_1 = 83.33 \text{ ms}$ ,  $V_R = 100 \text{ mV}$

**To Find :**  $T_2$

We know that,

$$V_i = V_R \times \frac{t_2}{t_1} \quad \dots(1)$$

$$\therefore t_2 = \frac{V_i}{V_R} t_1$$

i. Given,  $V_i = 100 \text{ mV}$

$$t_2 = \frac{100}{100} \times 83.33 = 83.33 \text{ ms}$$

ii. Given,  $V_i = 200 \text{ mV}$

$$t_2 = \frac{200}{100} \times 83.33 = 166.66 \text{ ms}$$

**i. Which block of PLL decides capture range ? Explain.**

**Ans.**

1. In PLL, VCO block decides capture range.
2. The capture range is the range of input frequencies within which an initially unlocked loop will get locked with an input signal.

**j. State the reasons for the offset currents at the input of the Op-Amp.**

**Ans.**

1. The input currents of Op-Amp are the base currents of two transistors used in the input stage. Ideally these transistors must be perfectly matched and two currents must be equal.
2. But practically the two input base currents differ by a small amount due to mismatch of two transistors. This difference between the currents flowing into the two input terminals of the Op-Amp is called input offset current.

## SECTION-B

Attempt any **five** questions from this section :

**(10 × 5 = 50)**

- 2. For 555 astable multivibrator  $R_A = 4.7 \text{ k}\Omega$ ,  $R_B = 1 \text{ k}\Omega$  and  $C = 1 \mu\text{F}$ . Determine the positive pulse width, the negative pulse width, and the free-running frequency. What is the duty cycle of output waveform ?**

**Ans.**

**Given :**  $R_A = 4.7 \text{ K}\Omega$ ,  $R_B = 1 \text{ k}\Omega$ ,  $C = 1 \mu\text{F}$

**To Find :** Duty cycle,  $D$ .

- Positive pulse width,

$$t_c = 0.69 (R_A + R_B)C \\ = 0.69 (4.7 \text{ K}\Omega + 1 \text{ k}\Omega) (10^{-6}) = 3.933 \text{ ms}$$

- Negative pulse width,

$$t_d = 0.69 (R_B)C \\ = 0.69 (1 \text{ k}\Omega) (10^{-6}) = 0.69 \text{ ms}$$

- Free-running frequency,

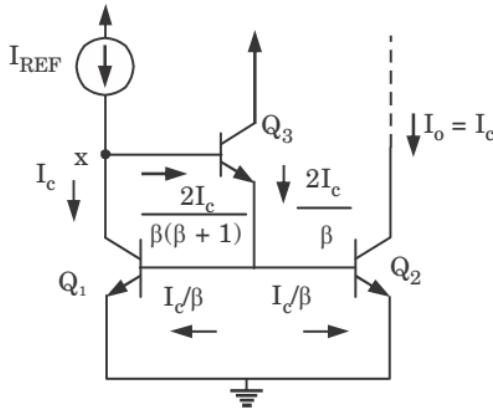
$$f_o = \frac{1}{t_c + t_d} = \frac{1}{(3.933 + 0.69)(10^{-3})} = 0.216 \text{ kHz}$$

$$4. \quad \% \text{ Duty cycle} = \frac{t_c}{t_c + t_d} \times 100 = \frac{3.933}{(3.933 + 0.69)} \times 100 = 85.07 \%$$

- Why we need BJT base current compensation mirror circuit ? Draw the circuit and express relation between  $I_{\text{ref}}$  and  $I_0$  for same.

**Ans.**

- A bipolar current mirror with a current transfer ratio is less dependent on  $\beta$  than that of simple current mirror.
- This reduces dependency on  $\beta$  and is achieved by using transistor  $Q_3$ . The  $Q_3$  supplies the base current to the  $Q_1$  and  $Q_2$ .
- The sum of base currents is divided by  $(\beta_3 + 1)$ , resulting in much smaller error current, that has to be supplied by  $I_{\text{REF}}$ .



**Fig. 5.** A current mirror with base current compensation.

- Let us assume  $Q_1$  and  $Q_2$  are matched and having equal collector current. A node equation at node  $x$  gives

$$I_{REF} = I_c \left[ 1 + \frac{2}{\beta(\beta+1)} \right]$$

5. As,

$$I_o = I_c$$

The current transfer ratio of the mirror will be

$$\frac{I_o}{I_{REF}} = \frac{2}{1 + \beta(\beta+1)} \approx \frac{1}{1 + 2/\beta^2} \quad \dots(1)$$

Eq. (1) shows that the error due to finite  $\beta$  has been reduced from  $2/\beta$  to  $2/\beta^2$ .

6. However, the output resistance ( $r_o$ ) remains approximately equal to that of simple mirror.
7. If  $I_{REF}$  is not present, then we connect node  $x$  to the power supply  $V_{CC}$  through resistor  $R$ , then

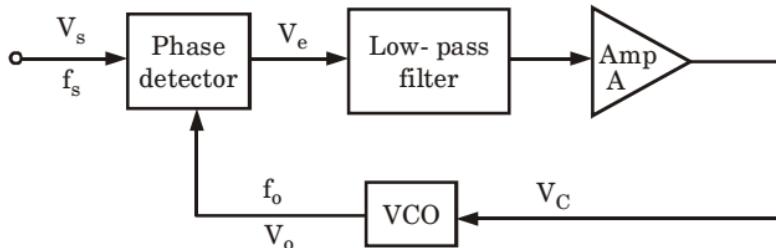
$$I_{REF} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R}$$

4. Explain the working of PLL with suitable block diagram. Write down the different applications of PLL.

**Ans.**

#### A. Principle of operation of PLL :

1. The two inputs of the phase detector or comparator are the input voltage  $V_s$  at frequency  $f_s$  and the feedback voltage from a voltage controlled oscillator (VCO) at frequency  $f_o$ .
2. The phase detector compares these two signals and produces a DC voltage  $V_e$  which is proportional to the phase difference between  $f_s$  and  $f_o$ .
3. The output voltage  $V_e$  of the phase detector is called as error voltage. This error voltage is then applied to low-pass filter.
4. Low-pass filter removes the high frequency noise present in the phase detector output and produces a ripple free DC level.
5. This DC level is amplified to an adequate level by the amplifier and applied to a VCO.
6. The DC amplifier output voltage is called as the control voltage  $V_C$ .



**Fig. 6.**

7. The control voltage  $V_C$  is applied at the input of a VCO. The output frequency of VCO is directly proportional to the DC control voltage  $V_C$ .

8. The VCO frequency  $f_o$  is compared with the input frequency  $f_s$  by the phase detector and it is adjusted continuously until it is equal to the input frequency  $f_s$  i.e.,  $f_o = f_s$ .
9. Once, the action of shifting VCO frequency in a direction to reduce the frequency difference between  $f_s$  and  $f_o$  starts, we say the signal is in the capture range.
10. When the output frequency is exactly the same as the input frequency, PLL is then said to be locked.
11. Once locked the output frequency  $f_o$  is identical to  $f_s$  except for a finite phase difference.
12. This phase difference generates a control voltage  $V_C$  to shift VCO frequency from  $f_o$  to  $f_s$  thereby maintaining the lock. Once locked, PLL tracks the frequency changes of the input signal.

### B. Applications :

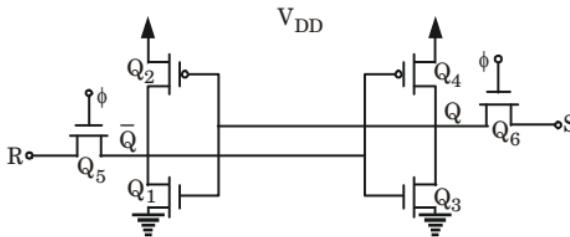
1. Frequency divider
2. Frequency multiplier
3. Frequency synthesizer
4. AM detector
5. FM detector
6. FSK demodulator.

5. Realize a simpler CMOS implementation of clocked SR flip-flop. Also explain the working of circuit.

**Ans.**

### A. CMOS Implementation :

1. A simpler implementation of a clocked SR flip-flop is shown in Fig. 7. Here, pass transistor logic is employed to implement the clocked set-reset function.



**Fig. 7.**

2. The SR flip-flop comprising two cross-coupled inverters and two pass transistors  $Q_5$  and  $Q_6$ . The pass transistors are turned ON when the clock ( $\phi$ ) is high, and they connect the flip-flop input  $S$  and  $R$ . The pass transistors act as transmission gates allowing the inputs  $S$  and  $R$ .

### B. Operation :

1. Consider the flip-flop output has the initial state  $Q = 1$  and  $\bar{Q} = 0$ , and the input  $R = 1$  and  $S = 0$  is applied to the input of flip-flop.
2. When the clock  $\phi$  is high, the transistors  $Q_5$  and  $Q_6$  are turned ON.

3. For this input  $R = 1$  and  $S = 0$ , the transistor  $Q_3$  is turned ON and pull down the output  $Q = 0$ .
4. These output  $Q$  is applied to the input of  $Q_2$  and  $Q_1$  transistors, this will make the transistor  $Q_2$  is turned ON and the output  $\bar{Q}$  becomes high.
5. Now consider the output has initial state  $Q = 0$  and  $\bar{Q} = 1$ , and the input  $R = 0$  and  $S = 1$ . When the clock  $\phi$  is high, the pass transistors  $Q_5$  and  $Q_6$  are turned ON. For this input  $R = 0$  and  $S = 1$ , the transistor  $Q_1$  turned ON and  $Q_2$  is turned OFF.
6. This causes the output  $\bar{Q} = 0$  and  $\bar{Q}$  is applied to the input of transistors  $Q_3$  and  $Q_4$ . Now the transistor  $Q_4$  turned ON and this make the output  $Q$  is high.
6. **Design a wide band pass filter with lower cut-off frequency  $f_L = 200$  Hz, higher cut-off frequency  $f_H = 1$  kHz and a passband gain = 4.**

**Ans.****Given :**  $f_L = 200$  kHz,  $f_H = 1$  kHz,  $A = 4$ **To Design :** Wide bandpass filter.**A. Components of the low-pass filter :**

1. Let  $C_L' = 0.01 \mu\text{F}$

2.  $R_L' = \frac{1}{2\pi f_H C_L'} = \frac{1}{2\pi \times 1000 \times 0.01 \times 10^{-6}} = 15.91 \text{ k}\Omega$

3. The gain of the low-pass filter can be considered half,

$A_{LF} = 2$

$$2 = 1 + \frac{R_{FL}}{R_L}$$

$R_{FL} = R_L = 10 \text{ k}\Omega \text{ (assume)}$

**B. Components of the high-pass filter :**

1. Let  $C_H' = 0.05 \mu\text{F}$

2.  $R_H' = \frac{1}{2\pi f_L C_H'} = \frac{1}{2\pi \times 200 \times 0.05 \times 10^{-6}}$   
 $R_H' = 15.91 \text{ K}\Omega$

3. The gain = 2

$$1 + \frac{R_{FH}}{R_H} = 2$$

$R_{FH} = R_H = 10 \text{ k}\Omega \text{ (assume)}$

4. Quality factor,  $Q = \frac{f_c}{f_H - f_L} = \frac{\sqrt{f_H f_L}}{f_H - f_L}$

$$= \frac{\sqrt{200 \times 1000}}{800} = 0.56$$

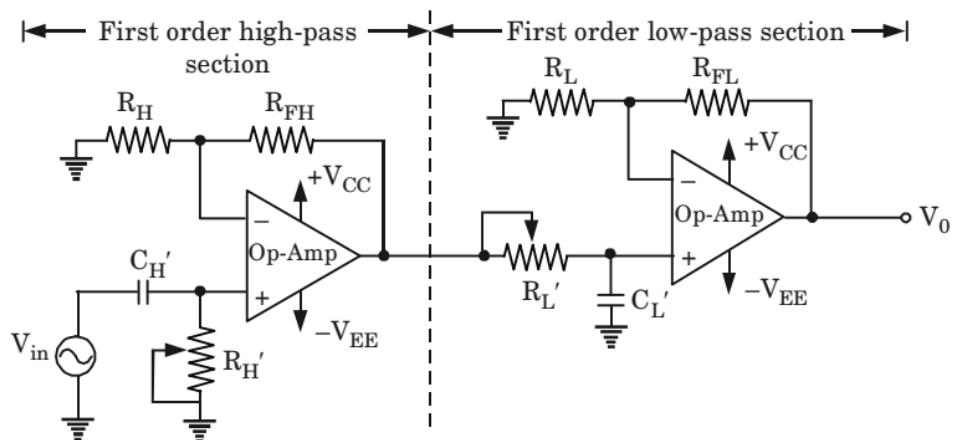


Fig. 8.

- 7. Explain working of precision full wave rectifier with necessary waveform.**

**Ans. Full wave precision rectifier :**

- For positive half cycle of  $V_{in}$ , diode  $D_1$  will be ON and  $D_2$  will be OFF. Both the Op-Amps will act like inverter and thus,  $V_o$  will follow the input  $V_{in}$ . From Fig. 10,

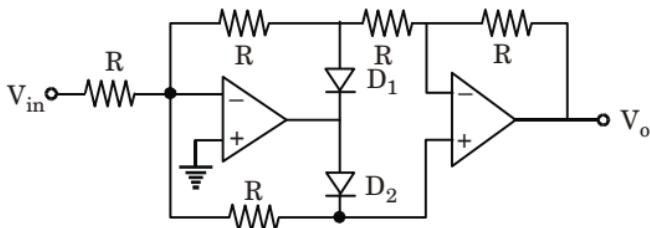


Fig. 9.

$$\text{Hence, } V_{01} = \frac{-R}{R} V_{in} = -V_{in}$$

$$\text{and } V_0 = \frac{-R}{R} (-V_{in}) = V_{in}$$

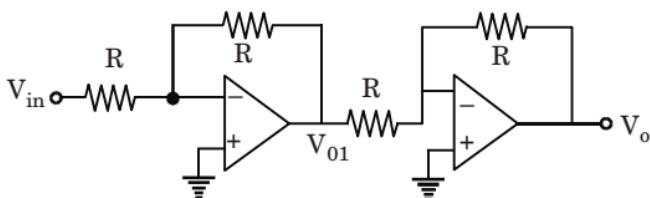
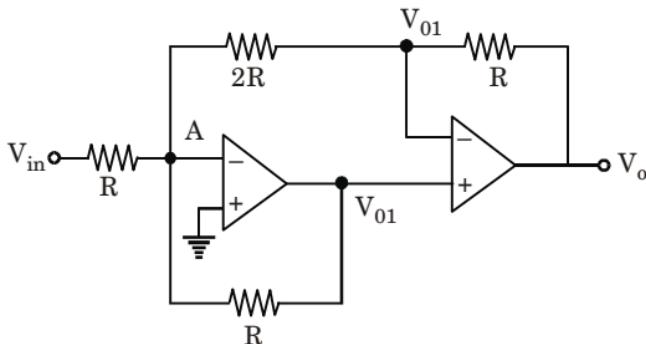


Fig. 10.

- In negative half cycle of  $V_{in}$ , diode  $D_1$  will be OFF and  $D_2$  will be ON.

**Fig. 11.**

- i. Applying KCL at node  $A$ ,

$$\frac{V_A - V_{in}}{R} + \frac{V_A - V_{01}}{R} + \frac{V_A - V_{01}}{2R} = 0$$

- ii. Now,

[Virtual ground concept]

$$-\frac{V_{in}}{R} - \frac{V_{01}}{R} - \frac{V_{01}}{2R} = 0$$

$$V_{in} = -\frac{3}{2}V_{01}$$

$$V_{01} = -\frac{2}{3}V_{in}$$

- iii. Also,

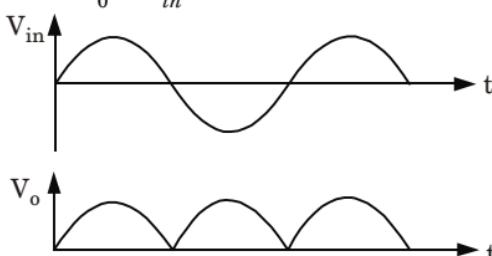
$$V_o = \left(1 + \frac{R}{2R}\right)V_{01} = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3}V_{in}\right)$$

$$V_o = -V_{in}$$

Hence, for

$$V_{in} < 0,$$

$$V_o = V_{in}$$

**Fig. 12.**

8. Draw the circuit of KHN filter and derive the expression for its voltage gain.

**Ans.**

1. The second order high-pass transfer function is

$$\frac{V_{hp}}{V_i} = \frac{Ks^2}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2} = T_{hp} \quad \dots(1)$$

where  $K$  is high frequency gain

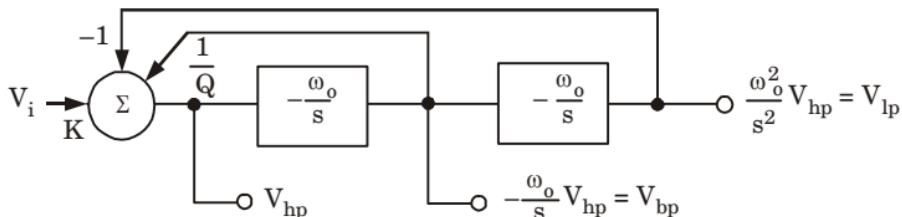
2. Simplify eq. (1) and we get,

$$V_{hp} + \frac{1}{Q} \left( \frac{\omega_o}{s} V_{hp} \right) + \left( \frac{\omega_o^2}{s^2} V_{hp} \right) = KV_i \quad \dots(2)$$

3. The signal  $(\omega_o/s) V_{hp}$  can be obtained by passing  $V_{hp}$  through an integrator with time constant equal to  $1/\omega_o$ .
4. Passing resulting signal through another identical integrator results in the third signal involving  $V_{hp}$  in eq. (2) and rearranging eq. (2), we get

$$V_{hp} = KV_i - \frac{1}{Q} \frac{\omega_o}{s} V_{hp} - \frac{\omega_o^2}{s^2} V_{hp} \quad \dots(3)$$

5. Biquad means the circuit is capable of realizing a biquadratic transfer function.
6. Eq. (3) can be transferred to block diagram as shown in Fig. 13.



**Fig. 13.**

7. The output of second integrator is labeled as  $V_{lp}$  while  $V_{bp}$  for first integrator.
8. Bandpass filter transfer function is given by

$$T_{bp} = \frac{\left( -\frac{\omega_0}{s} \right) V_{hp}}{V_i} \quad \dots(4)$$

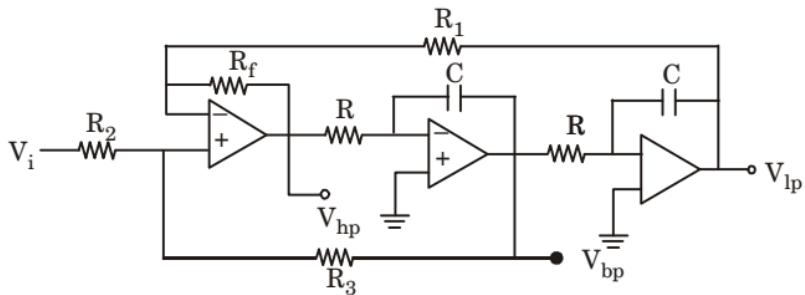
9. Using eq. (1),

$$T_{bp} = \frac{-K\omega_o s}{s^2 + s(\omega_o / Q) + \omega_o^2} \quad \dots(5)$$

10. Low-pass filter transfer function is given by (using eq. (1))

$$T_{lp} = \frac{\omega_o^2}{s^2} \frac{V_{hp}}{V_i} = \frac{K\omega_o^2}{s^2 + s(\omega_o / Q) + \omega_o^2} \quad \dots(6)$$

11. To obtain Op-Amp circuit in Fig. 14, we replace each integrator with Miller integrator circuit having  $CR = 1/\omega$ , also replace summer block with Op-Amp summing circuit.
12. The resulting circuit is known as Kerwin-Huelsman-Newcomb or KHN biquad as shown in Fig. 14.

**Fig. 14.**

13. Select suitable values of  $C$  and  $R$  of integrator so  $CR = 1/\omega_L$ . For resistors, we use superposition to express the output of summer  $V_{hp}$  in terms of its inputs,

$$V_{bp} = -\left(\frac{\omega_o}{s}\right)V_{hp} \text{ and } V_{lp} = \left(\frac{\omega_o^2}{s^2}\right)V_{hp}$$

as,

$$V_{hp} = \frac{R_3}{R_2 + R_3} \left(1 + \frac{R_f}{R_1}\right) V_i + \frac{R_2}{R_2 + R_3} \left(1 + \frac{R_f}{R_1}\right) \left(-\frac{\omega_o}{s} V_{hp}\right) - \frac{R_f}{R_1} \left(\frac{\omega_o^2}{s^2} V_{hp}\right) \quad \dots(7)$$

14. Equating the last RHS term of eq. (3) and (7) gives

$$\frac{R_f}{R_1} = 1$$

15. Now equating second to last terms on RHS of eq. (3) and (4) and let  $R_1 = R_f$

$$\frac{R_3}{R_2} = 2Q - 1$$

16. Finally equating coefficients of  $V_i$  in eq. (3) and (7) and substituting  $R_f = R_1$  and  $R_2/R_3$

Then,  $K = 2 - \left(\frac{1}{Q}\right)$

17. The KHN biquad can be used to realize notch and all-pass functions by summing weighted versions of the three outputs LP, BP, and HP. Such an Op-Amp summer is shown in Fig. 15.

18. From Fig. 15, we can write

$$\begin{aligned} V_0 &= -\left(\frac{R_F}{R_H} V_{hp} + \frac{R_F}{R_B} V_{bp} + \frac{R_F}{R_L} V_{lp}\right) \\ &= -V_i \left(\frac{R_F}{R_H} T_{hp} + \frac{R_F}{R_B} T_{bp} + \frac{R_F}{R_L} T_{lp}\right) \end{aligned} \quad \dots(8)$$

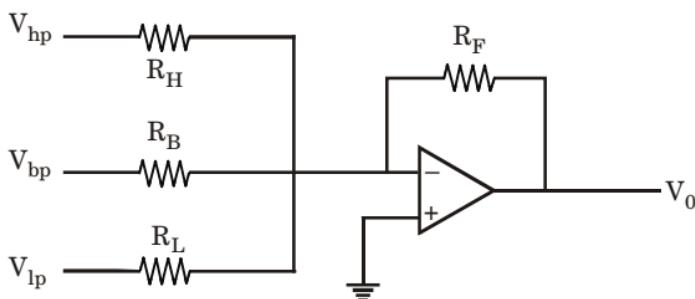


Fig. 15.

19. Substituting for \$T\_{hp}\$, \$T\_{bp}\$, and \$T\_{lp}\$ from eq. (1), (5) and (6) give the overall transfer function

$$\frac{V_0}{V_i} = -K \frac{(R_F / R_H)s^2 - s(R_F / R_B)\omega_0 + (R_F / R_L)\omega_0^2}{s^2 + s(\omega_0 / Q) + \omega_0^2}$$

20. To obtain notch function by selecting \$R\_B = \infty\$

$$\frac{R_H}{R_L} = \left( \frac{\omega_n}{\omega_0} \right)^2$$

## 9. Explain the types of phase detector with suitable circuit diagram and input-output waveforms.

**Ans.** Phase detectors or comparators used in a PLL can be of two types :

### A. Analog phase detector :

- Fig. 16 shows a switch type phase detector. Here, switch is an electronic switch which is being opened and closed by the VCO output signal.
- Switch is closed only when VCO output is positive and switch is open for negative VCO output.

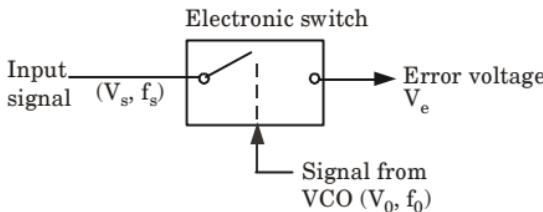


Fig. 16.

- Fig. 17 shows the input signal \$V\_s\$ at the same frequency \$f\_o\$ but at different phase shifts \$\phi = 0^\circ, 90^\circ\$ and \$180^\circ\$.
- For \$V\_s\$ having \$\phi = 0^\circ\$, a positive error voltage will be produced.
- When \$\phi = 90^\circ\$, the average value of error voltage produced at the switch is zero and when \$\phi = 180^\circ\$, only the negative half cycles of input appear across the output, thus error voltage is negative.
- Error voltage is zero for \$\phi = 90^\circ\$, hence perfect lock thus, VCO output and input signal \$V\_s\$ should be \$90^\circ\$ out of phase.

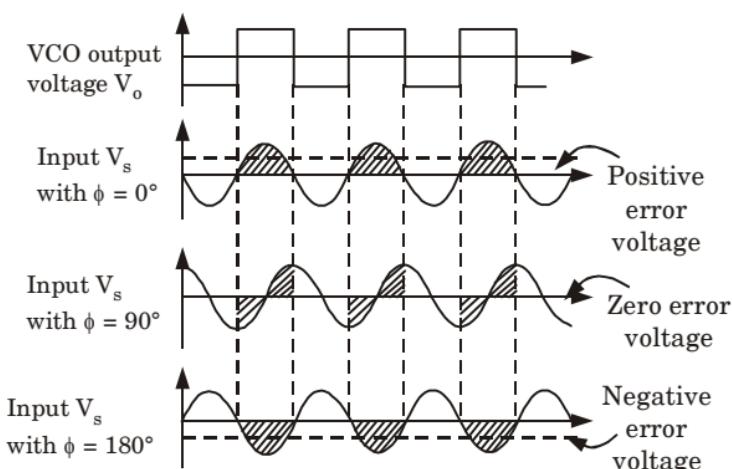


Fig. 17.

**B. Digital phase detector :**

1. A digital phase detector is a simple XOR gate. XOR gate output is high only if one of its inputs is high.
2. The two inputs of the gate are connected to the input signal ( $V_s, f_s$ ) and output signal ( $V_o, f_o$ ) respectively.

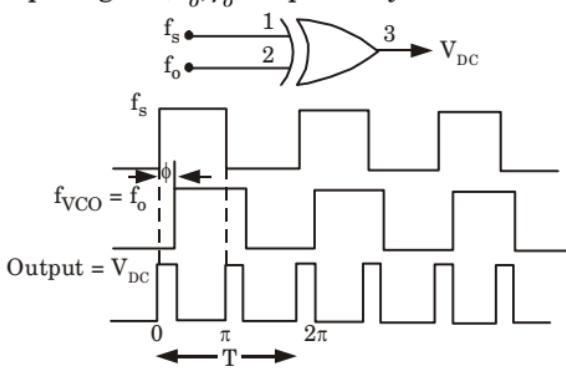


Fig. 18.

3. Output will increase with increase in the phase difference  $\phi$ .
4. For  $\phi = 0^\circ$  the waveforms at inputs  $f_s$  and  $f_o$  overlap and output is always zero. Therefore, the average error voltage will be zero. It will be maximum for  $\phi = 180^\circ$ .
5. Thus, in this phase detector, phase  $\phi$  must be zero for zero error voltage i.e., for perfect lock condition.

**SECTION-C**

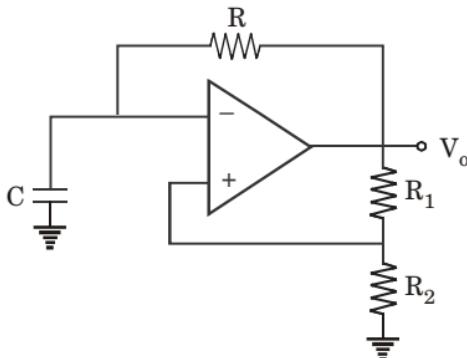
Attempt any **two** questions from this section : **(15 × 2 = 30)**

10. Explain the generation of square and triangular waveforms from astable multivibrator operation using Op-Amp. Also find expression of the time period for both cases.

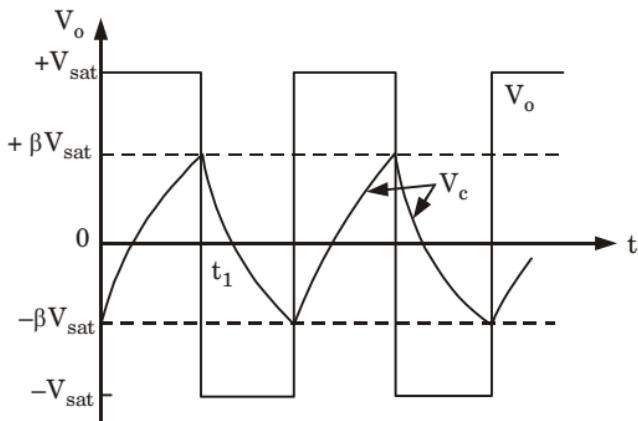
**Ans.****A. Generation of square waveforms :**

1. Square wave generator is also called as astable multivibrator or free running oscillator.
2. Circuit of square wave generator is as shown in Fig. 19. The principle of generation of square wave output is to force an Op-Amp to operate in the saturation region.
3. A fraction of output is fed back to the (+ ve) input terminal. This fraction is given by,

$$\beta = \frac{R_2}{R_1 + R_2}$$

**Fig. 19.**

4. Thus, the reference voltage is  $\beta V_o$  and may take values as  $+\beta V_{sat}$  or  $-\beta V_{sat}$ . The output is also fed back to the (- ve) input terminal after integrating by  $RC$  combination. When (- ve) input terminal voltage exceeds  $V_{REF}$ , switching takes place resulting in square wave output.

**Fig. 20.**

5. Now, consider the waveform shown in Fig. 20. When the output is at  $+V_{\text{sat}}$ , capacitor  $C$  starts charging through  $R$ . Voltage at (+ ve) input terminal is  $+ \beta V_{\text{sat}}$ . Now as the charge  $C$  rises above this reference voltage  $+ \beta V_{\text{sat}}$ , output switches to  $-V_{\text{sat}}$ .
6. At this instant, voltage on the capacitor is  $+ \beta V_{\text{sat}}$ , hence it starts discharging through  $R$  i.e., towards  $- \beta V_{\text{sat}}$ . When output voltage switches to  $-V_{\text{sat}}$ , the capacitor charges more negatively until its voltage just exceeds  $- \beta V_{\text{sat}}$ .
7. The output switches back to  $+V_{\text{sat}}$  and hence the cycle repeats itself.
8. Now, voltage across the capacitor, as a function of time is given by

$$V_c(t) = V_{\text{final}} + (V_{\text{initial}} - V_{\text{final}}) e^{-t/RC}$$

As,

$$V_{\text{final}} = +V_{\text{sat}}$$

and

$$V_{\text{initial}} = - \beta V_{\text{sat}}$$

$$V_c(t) = V_{\text{sat}} + (- \beta V_{\text{sat}} - V_{\text{sat}}) e^{-t/RC}$$

$$V_c(t) = V_{\text{sat}} - V_{\text{sat}} (1 + \beta) e^{-t/RC}$$

9. At  $t = t_1$ , voltage across capacitor reaches to  $+ \beta V_{\text{sat}}$ , therefore,

$$V_c(t_1) = \beta V_{\text{sat}} = V_{\text{sat}} - V_{\text{sat}} (1 + \beta) e^{-t_1/RC}$$

After solving,

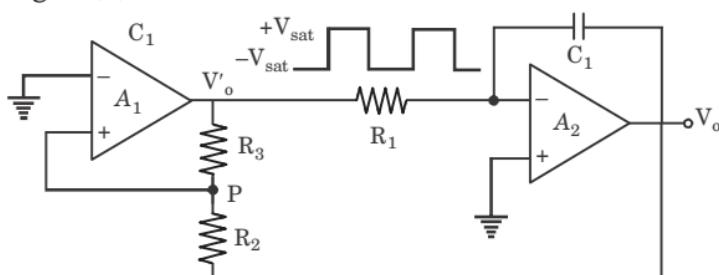
$$t_1 = RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

This is only half of the total period.

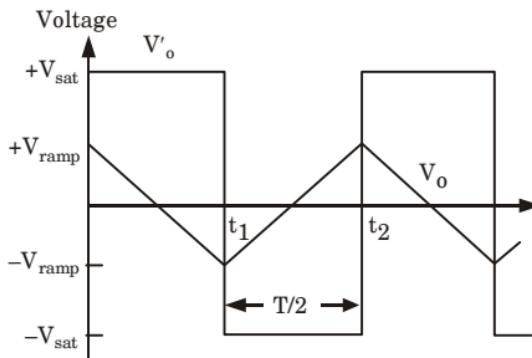
$$\therefore \text{Total time period} = 2t_1 = 2RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

## B. Generation of triangular waveforms :

1. A triangular wave can be simply obtained by integrating a square wave.
2. Triangular wave generator along with waveforms is shown in Fig. 21(a).



(a) Triangular waveform generator



(b) Waveforms.

**Fig. 21.****Working :**

1. Assume output of comparator  $A_1$  is at  $\pm V_{\text{sat}}$  so output of integrator will be a negative going ramp as shown in Fig. 21(b).
2. When the negative going ramp reaches to  $-V_{\text{ramp}}$ , the output of  $A_1$  switches from  $+V_{\text{sat}}$  to  $-V_{\text{sat}}$ . The sequence then repeats to give triangular wave at the output of  $A_2$ .
3. The frequency of triangular waveform can be calculated as follows :
  - i. The effective voltage at point  $P$  during the time when output of  $A_1$  is at  $+V_{\text{sat}}$  level is given by,

$$-V_{\text{ramp}} + \frac{R_2}{R_2 + R_3} [+V_{\text{sat}} - (V_{\text{ramp}})] \quad \dots(1)$$

- ii. At  $t = t_1$ , the voltage at point  $P$  becomes equal to zero. Therefore from eq. (1)

$$-V_{\text{ramp}} = - \frac{R_2}{R_3} (+V_{\text{sat}}) \quad \dots(2)$$

- iii. Similarly, at  $t = t_2$ , when the output of  $A_1$  switches from  $-V_{\text{sat}}$  to  $+V_{\text{sat}}$ ,

$$V_{\text{ramp}} = \frac{-R_2}{R_3} (-V_{\text{sat}}) = \frac{R_2}{R_3} (V_{\text{sat}})$$

- iv. Therefore, peak to peak amplitude of the triangular wave is

$$V_o(pp) = +V_{\text{ramp}} - (-V_{\text{ramp}}) = 2 \frac{R_2}{R_3} V_{\text{sat}} \quad \dots(3)$$

- v. The output switches from  $-V_{\text{ramp}}$  to  $+V_{\text{ramp}}$  in half the time period  $T/2$ .

Putting the values in the basic integrator equation,

$$V_o = -\frac{1}{RC} \int v_i dt$$

$$V_o(pp) = -\frac{1}{R_1 C_1} \int_0^{T/2} (-V_{\text{sat}}) dt = \frac{V_{\text{sat}}}{R_1 C_1} \left( \frac{T}{2} \right)$$

$$\text{or, } T = 2R_1C_1 \frac{V_o(pp)}{V_{sat}} \quad \dots(4)$$

vi. Putting the value of  $V_o(pp)$  from eq. (4), we get

$$T = \frac{4R_1C_1R_2}{R_3}$$

Hence the frequency of oscillation  $f_o$  is,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}$$

### 11. a. Design a CMOS half adder circuit with inputs A and B.

**Ans.**

- For CMOS half adder :

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = AB$$

- CMOS half-adder circuit is shown in Fig. 22.

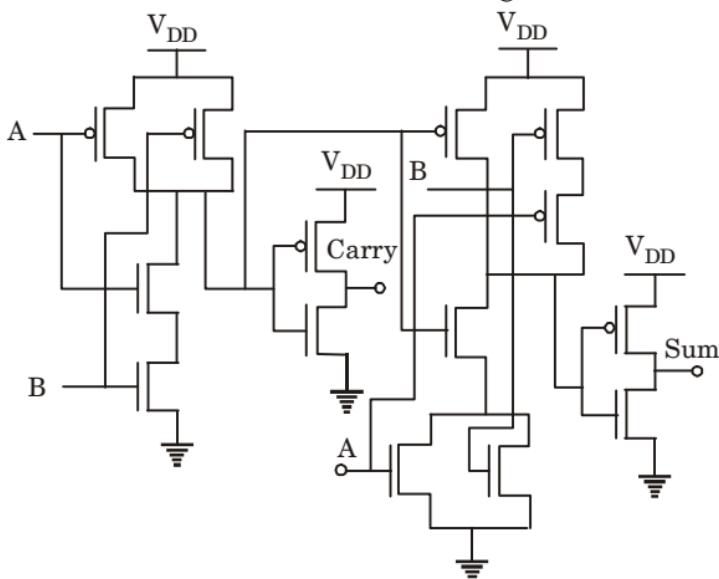


Fig. 22.

### b. Derive the formula for $V_{IL}$ and $V_{IH}$ of CMOS inverter.

**Ans.**

#### A. Derivation of $V_{IL}$ :

- By definition, the slope of the VTC is equal to (-1), i.e.,  $dV_{out}/dV_{in} = -1$  when the input voltage is  $V_{in} = V_{IL}$ .
- Note that in this case, the NMOS transistor operates in saturation while the PMOS transistor operates in the linear region.
- From  $I_{D,N} = I_{D,P}$ , we obtain the following current equation :

$$\frac{k_n}{2} (V_{GS,N} - V_{T0,N})^2 = \frac{k_p}{2} [2(V_{GS,P} - V_{T0,P})V_{DS,P} - V_{DS,P}^2] \quad \dots(1)$$

$$\frac{k_n}{2} (V_{in} - V_{T0,N})^2 = \frac{k_p}{2} [2(V_{in} - V_{DD} - V_{T0,P})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2] \quad \dots(2)$$

4. To satisfy the derivative condition at  $V_{IL}$ , we differentiate both sides of eq. (2) with respect to  $V_{in}$ .

$$k_n (V_{in} - V_{T0,N}) = k_p \left[ (V_{in} - V_{DD} - V_{T0,P}) \left( \frac{dV_{out}}{dV_{in}} \right) + (V_{out} - V_{DD}) \left( \frac{dV_{out}}{dV_{in}} \right) \right] \quad \dots(3)$$

5. Substituting  $V_{in} = V_{IL}$  and  $(dV_{out}/dV_{in}) = -1$  in eq. (3), we obtain

$$k_n (V_{IL} - V_{T0,N}) = k_p (2V_{out} - V_{IL} + V_{T0,P} - V_{DD}) \quad \dots(4)$$

6. The critical voltage  $V_{IL}$  can now be found as a function of the output voltage  $V_{out}$ , as follows :

$$V_{IL} = \frac{2V_{out} + V_{T0,P} - V_{DD} + k_R V_{T0,N}}{1 + k_R} \quad \dots(5)$$

where  $k_R$  is defined as,

$$k_R = \frac{k_n}{k_p}$$

### B. Derivation of $V_{IH}$ :

1. When the input is equal to  $V_{IH}$ , the NMOS transistor operates in the linear region and the PMOS transistor operates in saturation.
2. From  $I_{D,N} = I_{D,P}$

$$\frac{k_n}{2} [2(V_{GS,N} - V_{T0,N})V_{DS,N} - V_{DS,N}^2] = \frac{k_p}{2} (V_{GS,P} - V_{T0,P})^2 \quad \dots(6)$$

$$\frac{k_n}{2} [2(V_{in} - V_{T0,N})V_{out} - V_{out}^2] = \frac{k_p}{2} (V_{in} - V_{DD} - V_{T0,P})^2 \quad \dots(7)$$

3. Now, differentiate both sides of eq. (7) with respect to  $V_{in}$ .

$$k_n \left[ (V_{in} - V_{T0,N}) \left( \frac{dV_{out}}{dV_{in}} \right) + V_{out} - V_{out} \left( \frac{dV_{out}}{dV_{in}} \right) \right] = k_p (V_{in} - V_{DD} - V_{T0,P}) \quad \dots(8)$$

4. Substituting  $V_{in} = V_{IH}$  and  $(dV_{out}/dV_{in}) = -1$  in eq. (8), we obtain

$$k_n (-V_{IH} + V_{T0,N} + 2V_{out}) = k_p (V_{IH} - V_{DD} - V_{T0,P}) \quad \dots(9)$$

5. The critical voltage  $V_{IH}$  can now be found as a function of  $V_{out}$  as follows :

$$V_{IH} = \frac{V_{DD} + V_{T0,P} + k_R (2V_{out} + V_{T0,N})}{1 + k_R} \quad \dots(10)$$

12. Explain the circuit of Wilson MOS current mirror. Also discuss how it can be improved ? Draw the circuits and

**find expression of  $I_0$  for both, Wilson and modified Wilson current mirrors.**

**Ans. Wilson MOS circuit :**

- Fig. 23 shows the MOS based Wilson current mirror. Note that the  $V_{DS}$  value of  $Q_1$  and  $Q_2$  are not equal.

$$\text{i.e., } V_{DS1} = V_{DS1} + V_{GS3}$$

- From Fig. 23,

$$V_{GS1} = V_{GS2}$$

So,

$$I_1 \approx I_2$$

$$3. \text{ Now } \frac{I_0}{I_{REF}} = \frac{(W/L)_1}{(W/L)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

$$= \frac{(W/L)_1}{(W/L)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda (V_{DS2} + V_{GS3})}$$

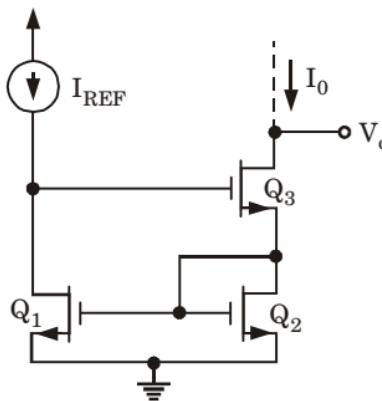


Fig. 23.

- Since  $\lambda$  is not zero, the ratio of  $(I_0/I_{REF})$  is slightly different from the aspect ratios. This problem is solved by modified Wilson current source as shown in Fig. 24.

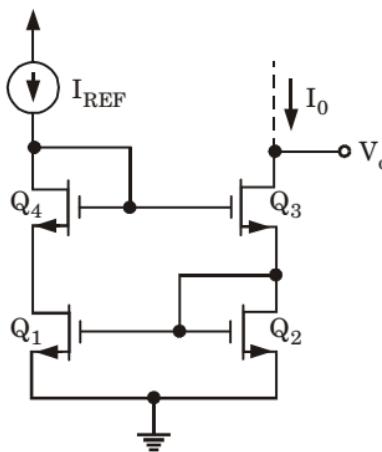


Fig. 24. Improved Wilson current mirror.

4. Here,  $V_{DS1} = V_{DS2} + V_{GS3} - V_{GS4}$

If  $V_{GS3} = V_{GS4}$

Then,  $V_{DS1} = V_{DS2}$

So,  $(I_0 / I_{REF})$  can be given as

$$\frac{I_0}{I_{REF}} = \frac{(W/L)_1}{(W/L)_2} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} = \frac{(W/L)_1}{(W/L)_2}$$

Hence, there is no error in the current gain.



**B. Tech.****(SEM. V) ODD SEMESTER THEORY  
EXAMINATION, 2017-18  
INTEGRATED CIRCUITS****Time : 3 Hours****Max. Marks : 100**

**Note :** All sections are compulsory. If require any missing data; then choose suitably.

**SECTION-A**

1. This question consists of short answer questions. Attempt all parts of this question. All parts carry equal marks.  $(2 \times 10 = 20)$
- a. If the open loop gain of an operational amplifier is very large. Does closed loop gain depend upon the external components of the operational amplifier justify.
- b. What is meant by the term matched transistors ?
- c. Define and give significance of slew rate.
- d. What is super diode ?
- e. Give two application of analog multiplier.
- f. What do you mean by a frequency response of a filter circuit ?
- g. Differentiate between comparator and Schmitt trigger.
- h. Describe the need of voltage limiter circuits.
- i. The basic step of a 8-bit DAC is 20 mV. If 00000000 represents 0 V, what is represented by the input 10110111 ?
- j. What do you mean by a CMOS circuit logic ?

**SECTION-B**

2. Attempt any three parts of this question. All parts carry equal marks.  $(10 \times 3 = 30)$

- a. What are the desirable characteristics of current mirror circuits ? Explain the circuit of Wilson MOS current mirror. Also discuss how it can be improved.
- b. Derived the expression of voltage gain in KHN Biquad filter. Draw the KHN Biquad filter and derive transfer function of the BPF and LPF from that.
- c. Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR-AND-INVERT (OAI) function using CMOS logic circuit.
- d. What do you mean by the quadrant operation of multiplier ? Draw and explain a GILBERT analog multiplier.
- e. Draw the block diagram of a PLL and explain its operation. Explain lock-in-range, capture range and pull-in time of a PLL. List the application of PLL.

### SECTION-C

Attempt any **two** parts of each questions of this section. All question carry equal mark. **(10 × 5 = 50)**

3. a. Describe the operation and characteristics of a BJT complementary push-pull output stage.
- b. Determine the small-signal model of the second stage of the 741 Op-Amp.
- c. The parameter of the three transistor CM are  $V_{CC} = 9$  V,  $V_{EE} = 0$ ,  $R_1 = 12$  k $\Omega$ ,  $V_{BE(on)} = 0.7$  V,  $\beta = 75$ ,  $V_A = \infty$ . Calculate the value of current,  $I_{ref}$ ,  $I_o$ ,  $I_{C1}$ ,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$ ,  $I_{E3}$ .
4. a. Draw the generalized impedance converter and derive its impedance equation. Also simulate an inductor.
- b. Derive the output expression for  $RC$  phase shift oscillator.
- c. Compare and contrast active filters and passive filters. Design a second order low pass Butterworth filter to have cut-off frequency of 1 kHz.
5. a. Give CMOS implementation of a  $SR$  flip-flop and explain its working.

- b. Give two different CMOS realization of the Exclusive-OR gate function in which the PDN and PUN are dual network.
- c. Discuss D-F/F circuit using NAND CMOS gates.
6. a. Draw and explain the circuit of triangular wave generator. How square wave can be obtained using this triangular wave.
- b. Describe temperature compensated log amplifier using two Op-Amp and explain its operation.
- c. Explain how a Schmitt trigger circuit works with a neat diagram. Design a Schmitt trigger with  $V_{UT} = 2$  V,  $V_{LT} = -2$  V. Assume  $\pm V_{sat} = \pm 13$  V.
7. a. Draw and explain the block diagram of IC 555.
- b. Explain the operation of dual slope ADC.
- c. Design a 555 timer as astable multivibrator giving its block diagram which provide an output signal frequency of 2 kHz and 75 % duty cycle.



## SOLUTION OF PAPER (2017-18)

**Note :** All sections are compulsory. If require any missing data; then choose suitably.

### SECTION-A

1. This question consists of short answer questions. Attempt **all** parts of this question. All parts carry equal marks. **(2 × 10 = 20)**
- a. **If the open loop gain of an operational amplifier is very large. Does closed loop gain depend upon the external components of the operational amplifier justify.**

**Ans.** The closed loop gain is obtained by

$$A_{\text{closed}} = \frac{A_{\text{open}}}{1 + A_{\text{open}} \text{ feedback}} = \frac{A}{1 + A\beta}$$

Since,  $A_{\text{open}} \gg 1$ , so neglecting 1, we get,

$$A_{\text{closed}} = \frac{A}{A\beta} = \frac{1}{\beta}$$

Therefore, for the large open loop gain, closed loop gain will depend on negative feedback  $\beta$ , if  $\beta$  increases, closed loop gain decreases as they are inversely proportional.

- b. **What is meant by the term matched transistors ?**

**Ans.** If the two transistors are designed to be equal *i.e.*, same size, same orientation, same surrounding and have identical values of saturation current, current gain and early voltage, then this pair of transistors is referred as matched transistors.

- c. **Define and give significance of slew rate.**

**Ans.** **Slew rate :** Slew rate is defined as the maximum rate of change of output voltage with time. Its unit is V/ $\mu$ sec.

$$\text{Slew rate, } SR = \left. \frac{dV_o}{dt} \right|_{\text{max}}$$

**Significance :** The slew rate of an ideal Op-Amp is infinite which implies that the output voltage of an ideal Op-Amp can instantaneously follow the changes to the input step voltage. Higher the value of slew rate better is the performance of Op-Amp.

- d. **What is super diode ?**

**Ans.** The super diode is a configuration obtained with an operational amplifier in order to have a circuit behaving like an ideal diode and rectifier. It is also known as precision rectifier.

**e. Give two application of analog multiplier.****Ans.**

- Frequency doubling.
- Measurement of real power.

**f. What do you mean by a frequency response of a filter circuit ?****Ans.**

- Frequency response is the quantitative measure of the output spectrum of a filter circuit in response to a stimulus, and is used to characterize the dynamic of the system.
- It is a measure of magnitude and phase of the output as a function of frequency, in comparison to the input.

**g. Differentiate between comparator and Schmitt trigger.****Ans.**

S. No.	<b>Comparator</b>	<b>Schmitt trigger</b>
1.	The feedback is not used.	The feedback is used.
2.	The Op-Amp used is in open loop mode.	The Op-Amp used is in closed loop mode.
4.	A single reference voltage exists which acts as triggering voltage. i.e., $V_{ref}$ or $-V_{ref}$	The two different threshold voltages exist as $V_{UT}$ and $V_{LT}$ .
5.	The hysteresis does not exist.	Hysteresis exists with a width $H = V_{UT} - V_{LT}$ .

**h. Describe the need of voltage limiter circuits.**

**Ans.** A voltage limiter is used to limit the voltage level. When a steady, reliable voltage is needed, then voltage limiter is the preferred device.

**i. The basic step of a 8-bit DAC is 20 mV. If 00000000 represents 0 V, what is represented by the input 10110111 ?**

**Ans.** The output voltage for input 10110111 is given by

$$\begin{aligned}
 & 20 \text{ mV} (1 \times 2^7 + 0 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 \\
 & \quad + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0) \\
 & = 20 \text{ mV} (128 + 32 + 16 + 4 + 2) \\
 & = 20 \times 182 = 3640 \text{ mV} = 3.64 \text{ V}
 \end{aligned}$$

**j. What do you mean by a CMOS circuit logic ?****Ans.**

- The CMOS logic gate consists of two networks.

- i. The pull-down network (PDN) constructed of NMOS transistor and
- ii. The pull-up network (PUN) constructed of PMOS transistors.
2. The two networks are operated by the input variables, in a complementary fashion.

## SECTION-B

2. Attempt **any** three parts of this question. All parts carry equal marks.  $(10 \times 3 = 30)$
- a. **What are the desirable characteristics of current mirror circuits ? Explain the circuit of Wilson MOS current mirror. Also discuss how it can be improved.**

**Ans.**

**A. Characteristics of current mirror circuits :**

- i. More accurate current transfer ratio.
- ii. Higher output resistance.

**B. Wilson MOS current mirror :**

1. Fig. 1 shows the MOS based Wilson current mirror. Note that the  $V_{DS}$  value of  $Q_1$  and  $Q_2$  are not equal.

$$\text{i.e., } V_{DS1} = V_{DS1} + V_{GS3}$$

2. From Fig. 1,

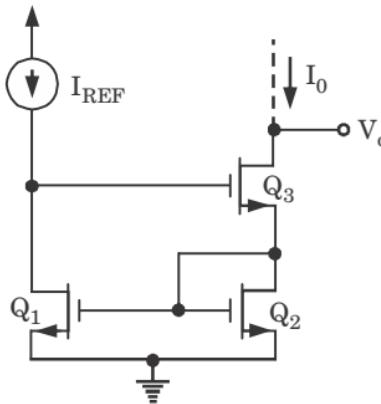
$$V_{GS1} = V_{GS2}$$

So,

$$I_1 \approx I_2$$

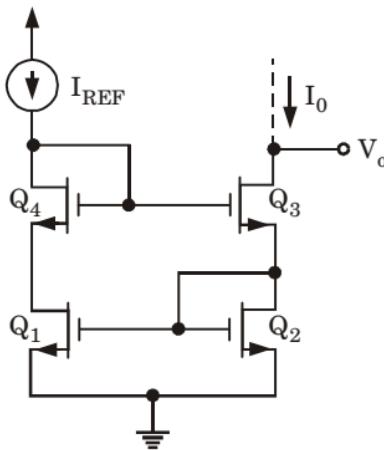
$$3. \text{ Now } \frac{I_0}{I_{REF}} = \frac{(W/L)_1}{(W/L)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

$$= \frac{(W/L)_1}{(W/L)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda (V_{DS2} + V_{GS3})}$$



**Fig. 1.**

3. Since  $\lambda$  is not zero, the ratio of  $(I_0 / I_{REF})$  is slightly different from the aspect ratios. This problem is solved by modified Wilson current source as shown in Fig. 2.



**Fig. 2.** Improved Wilson current mirror.

4. Here,  $V_{DS1} = V_{DS2} + V_{GS3} - V_{GS4}$

If  $V_{GS3} = V_{GS4}$

Then,  $V_{DS1} = V_{DS2}$

So,  $(I_0 / I_{\text{BEE}})$  can be given as

*L* (W/L)

$$\frac{I_0}{I_{REF}} = \frac{(W/L)_1}{(W/L)_2} \frac{1 + \kappa V_{DS2}}{1 + \lambda V_{DS1}} = \frac{(W/L)_1}{(W/L)_2}$$

Hence, there is no error in the current gain.

- b. Derived the expression of voltage gain in KHN Biquad filter. Draw the KHN Biquad filter and derive transfer function of the BPF and LPF from that.

**Ans.**

1. The second order high-pass transfer function is

$$\frac{V_{hp}}{V_i} = \frac{Ks^2}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2} = T_{hp} \quad ... (1)$$

where  $K$  is high frequency gain

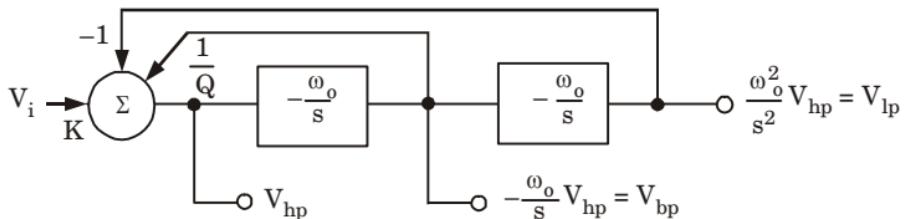
2. Simplify eq. (1) and we get,

$$V_{hp} + \frac{1}{Q} \left( \frac{\omega_o}{s} V_{hp} \right) + \left( \frac{\omega_o^2}{s^2} V_{hp} \right) = KV_i \quad ... (2)$$

- The signal  $(\omega_o/s) V_{hp}$  can be obtained by passing  $V_{hp}$  through an integrator with time constant equal to  $1/\omega_o$ .
  - Passing resulting signal through another identical integrator results in the third signal involving  $V_{hp}$  in eq. (2) and rearranging eq. (2), we get

$$V_{hp} = KV_i - \frac{1}{Q} \frac{\omega_o}{s} V_{hp} - \frac{\omega_o^2}{s^2} V_{hp} \quad \dots(3)$$

5. Biquad means the circuit is capable of realizing a biquadratic transfer function.  
 6. Eq. (3) can be transferred to block diagram as shown in Fig. 3.

**Fig. 3.**

7. The output of second integrator is labeled as  $V_{lp}$  while  $V_{bp}$  for first integrator.  
 8. Bandpass filter transfer function is given by

$$T_{bp} = \frac{\left(-\frac{\omega_0}{s}\right) V_{hp}}{V_i} \quad \dots(4)$$

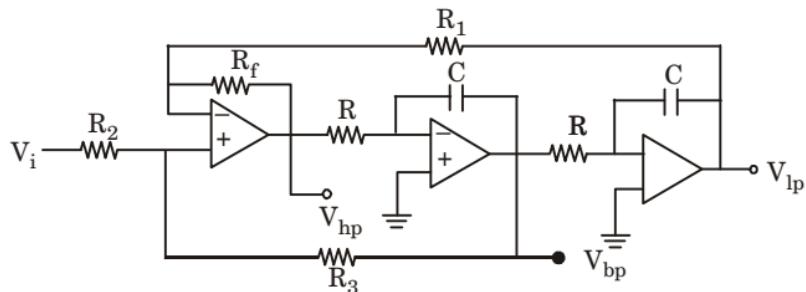
9. Using eq. (1),

$$T_{bp} = \frac{-K\omega_0 s}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad \dots(5)$$

10. Low-pass filter transfer function is given by (using eq. (1))

$$T_{lp} = \frac{\omega_0^2}{s^2} \frac{V_{hp}}{V_i} = \frac{K\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad \dots(6)$$

11. To obtain Op-Amp circuit in Fig. 4, we replace each integrator with Miller integrator circuit having  $CR = 1/\omega$ , also replace summer block with Op-Amp summing circuit.  
 12. The resulting circuit is known as Kerwin-Huelsman-Newcomb or KHN biquad as shown in Fig. 4.

**Fig. 4.**

13. Select suitable values of  $C$  and  $R$  of integrator so  $CR = 1/\omega_L$ . For resistors, we use superposition to express the output of summer  $V_{hp}$  in terms of its inputs,

$$V_{bp} = -\left(\frac{\omega_0}{s}\right) V_{hp} \text{ and } V_{lp} = \left(\frac{\omega_0^2}{s^2}\right) V_{hp}$$

as,

$$V_{hp} = \frac{R_3}{R_2 + R_3} \left( 1 + \frac{R_f}{R_1} \right) V_i + \frac{R_2}{R_2 + R_3} \left( 1 + \frac{R_f}{R_1} \right) \left( -\frac{\omega_o}{s} V_{hp} \right) - \frac{R_f}{R_1} \left( \frac{\omega_o^2}{s^2} V_{hp} \right) \quad \dots(7)$$

14. Equating the last RHS term of eq. (3) and (7) gives

$$\frac{R_f}{R_1} = 1$$

15. Now equating second to last terms on RHS of eq. (3) and (4) and let  $R_1 = R_f$

$$\frac{R_3}{R_2} = 2Q - 1$$

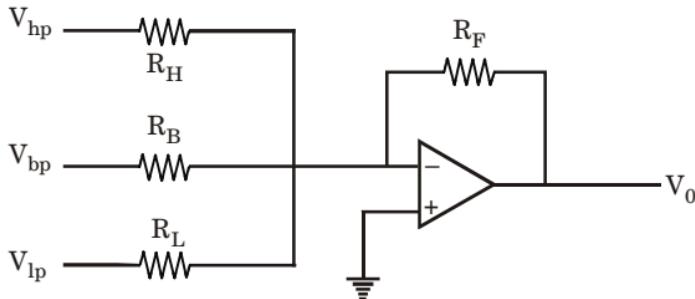
16. Finally equating coefficients of  $V_i$  in eq. (3) and (7) and substituting  $R_f = R_1$  and  $R_2/R_3$

Then,  $K = 2 - \left( \frac{1}{Q} \right)$

17. The KHN biquad can be used to realize notch and all-pass functions by summing weighted versions of the three outputs LP, BP, and HP. Such an Op-Amp summer is shown in Fig. 5.

18. From Fig. 5, we can write

$$\begin{aligned} V_0 &= - \left( \frac{R_F}{R_H} V_{hp} + \frac{R_F}{R_B} V_{bp} + \frac{R_F}{R_L} V_{lp} \right) \quad \dots(8) \\ &= - V_i \left( \frac{R_F}{R_H} T_{hp} + \frac{R_F}{R_B} T_{bp} + \frac{R_F}{R_L} T_{lp} \right) \end{aligned}$$



**Fig. 5.**

19. Substituting for  $T_{hp}$ ,  $T_{bp}$ , and  $T_{lp}$  from eq. (1), (5) and (6) give the overall transfer function

$$\frac{V_0}{V_i} = -K \frac{(R_F / R_H)s^2 - s(R_F / R_B)\omega_0 + (R_F / R_L)\omega_0^2}{s^2 + s(\omega_0 / Q) + \omega_0^2}$$

20. To obtain notch function by selecting  $R_B = \infty$

$$\frac{R_H}{R_L} = \left( \frac{\omega_n}{\omega_0} \right)^2$$

- c. Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR-AND-INVERT (OAI) function using CMOS logic circuit.

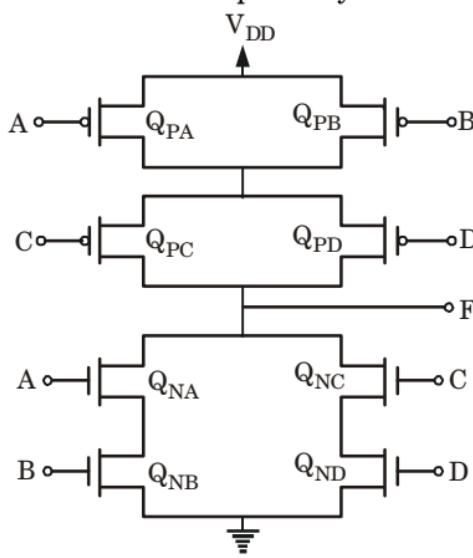
**Ans.**

**A. Feature of CMOS circuit :**

1. The output is always connected to  $V_{DD}$  or GND and in steady state; it gives full logic swing (between 0 V and  $V_{DD}$ ) voltage transfer characteristics and large noise margins.
2. Logic levels are not dependent upon the relative sizes of the devices.
3. There is no direct path between  $V_{DD}$  and GND in steady state. Thus, static power dissipation of CMOS circuit is negligible.
4. It has high input impedance and fast switching speed.

**B. AOI and OAI functions :**

1. AOI and OAI functions can be implemented with just one gate level transistor. Both the complex gates have a propagation delay equivalent to that of a single NAND or NOR gate.
2. AOI and OAI gates are essentially representations of SOP and POS expressions of functions respectively.



**Fig. 6.**

3. Let us implement the function,  $F = \overline{AB + CD}$

Here,  $AB$  and  $CD$  are two AND functions and their sum is the OR function, which is finally inverted. Thus  $F$  can be implemented as an AOI gate.

4. Fig. 6 shows the CMOS realization of an AOI gate.
5. The CMOS realization of the OR-AND-INVERT (OAI) gate is the dual of that for the AND-OR-INVERT gate and is easily obtained by flipping the latter end-for-end while interchanging all NMOS circuits with PMOS circuits and vice versa, as shown in Fig. 7.
6. The output expression for OAI gate is,

$$F = \overline{(A + B)(C + D)}$$

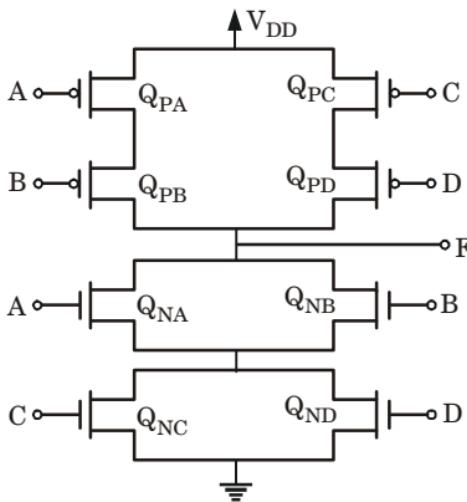


Fig. 7.

- d. What do you mean by the quadrant operation of multiplier ?  
Draw and explain a GILBERT analog multiplier.

**Ans.**

**A. Quadrant operation of multiplier :**

1. The quadrant defines the applicability of the circuit for bipolar signals at its inputs.
2. First-quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four-quadrant device accepts two bipolar signals.

**B. GILBERT analog multiplier :**

1. The GILBERT multiplier cell is a modification of the emitter coupled cell and this allows four-quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced multipliers.

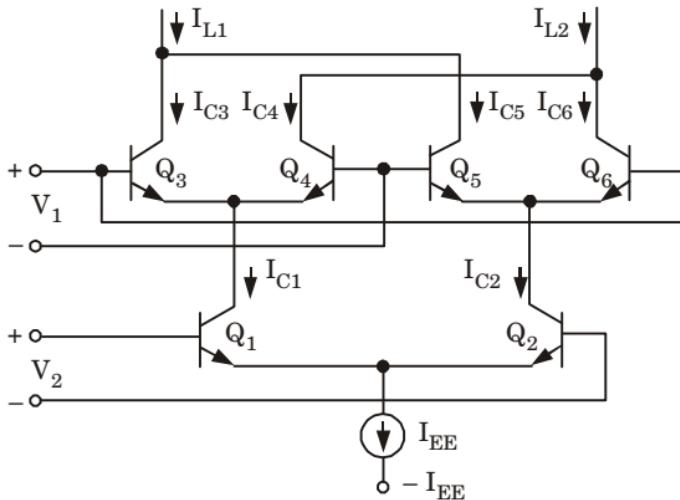


Fig. 8.

2. Two cross-coupled emitter-coupled pairs in series connection with an emitter coupled pair form the structure of the GILBERT multiplier cell.
3. The collector currents of  $Q_3$  and  $Q_4$  are given by

$$I_{C3} = \frac{I_{C1}}{1 + e^{-V_1/V_T}} \quad \dots(1)$$

and  $I_{C4} = \frac{I_{C1}}{1 + e^{V_1/V_T}}$  ... (2)

4. Similarly the collector currents of  $Q_5$  and  $Q_6$  are given by

$$I_{C5} = \frac{I_{C2}}{1 + e^{V_1/V_T}} \quad \dots(3)$$

and  $I_{C6} = \frac{I_{C2}}{1 + e^{-V_1/V_T}}$  ... (4)

5. The collector currents  $I_{C1}$  and  $I_{C2}$ , of transistors  $Q_1$  and  $Q_2$  can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_2/V_T}} \quad \dots(5)$$

and  $I_{C2} = \frac{I_{EE}}{1 + e^{V_2/V_T}}$  ... (6)

6. Substituting eq. (5) in eq. (1) and (2), we get

$$I_{C3} = \frac{I_{EE}}{[1 + e^{-V_1/V_T}][1 + e^{-V_2/V_T}]} \quad \dots(7)$$

and  $I_{C4} = \frac{I_{EE}}{[1 + e^{V_1/V_T}][1 + e^{-V_2/V_T}]}$  ... (8)

7. Similarly, substituting eq. (6) in eq. (3) and (4), we get

$$I_{C5} = \frac{I_{EE}}{[1 + e^{V_1/V_T}][1 + e^{V_2/V_T}]} \quad \dots(9)$$

and  $I_{C6} = \frac{I_{EE}}{[1 + e^{-V_1/V_T}][1 + e^{V_2/V_T}]}$  ... (10)

8. The differential output current  $\Delta I$  is given by

$$\Delta I = I_{L1} - I_{L2}$$

That is,  $\Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6})$

or  $\Delta I = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5})$  ... (11)

9. Substituting eq. (7) to (10) in eq. (11) and employing exponential formulae for hyperbolic functions, we get

$$\Delta I = I_{EE} \left[ \tanh\left(\frac{V_1}{2V_T}\right) \tanh\left(\frac{V_2}{2V_T}\right) \right] \quad \dots(12)$$

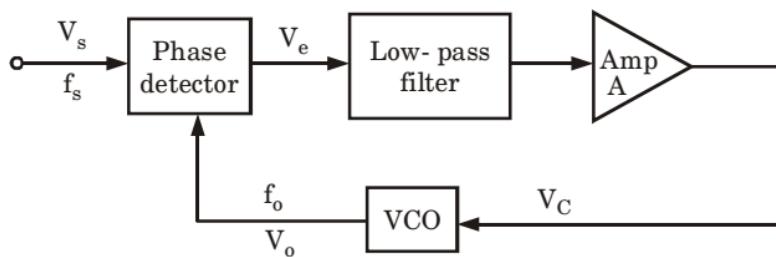
eq. (12) shows that when  $V_1$  and  $V_2$  are small, the GILBERT cell shown in Fig. 8 can be used as a four-quadrant analog multiplier with the use of current-to-voltage converters.

- e. Draw the block diagram of a PLL and explain its operation. Explain lock-in-range, capture range and pull-in time of a PLL. List the application of PLL.

**Ans.**

**A. Principle of operation of PLL :**

1. The two inputs of the phase detector or comparator are the input voltage  $V_s$  at frequency  $f_s$  and the feedback voltage from a voltage controlled oscillator (VCO) at frequency  $f_o$ .
2. The phase detector compares these two signals and produces a DC voltage  $V_e$  which is proportional to the phase difference between  $f_s$  and  $f_o$ .
3. The output voltage  $V_e$  of the phase detector is called as error voltage. This error voltage is then applied to low-pass filter.
4. Low-pass filter removes the high frequency noise present in the phase detector output and produces a ripple free DC level.
5. This DC level is amplified to an adequate level by the amplifier and applied to a VCO.
6. The DC amplifier output voltage is called as the control voltage  $V_C$ .



**Fig. 9.**

7. The control voltage  $V_C$  is applied at the input of a VCO. The output frequency of VCO is directly proportional to the DC control voltage  $V_C$ .
  8. The VCO frequency  $f_o$  is compared with the input frequency  $f_s$  by the phase detector and it is adjusted continuously until it is equal to the input frequency  $f_s$  i.e.,  $f_o = f_s$ .
  9. Once, the action of shifting VCO frequency in a direction to reduce the frequency difference between  $f_s$  and  $f_o$  starts, we say the signal is in the capture range.
  10. When the output frequency is exactly the same as the input frequency, PLL is then said to be locked.
  11. Once locked the output frequency  $f_o$  is identical to  $f_s$  except for a finite phase difference.
  12. This phase difference generates a control voltage  $V_C$  to shift VCO frequency from  $f_o$  to  $f_s$  thereby maintaining the lock. Once locked, PLL tracks the frequency changes of the input signal.
- B. Lock-in range :** Once the PLL is locked, it can track the frequency changes in the incoming signals. The range of frequencies over

which the PLL can maintain lock with the incoming signal is called lock-in range or tracking range.

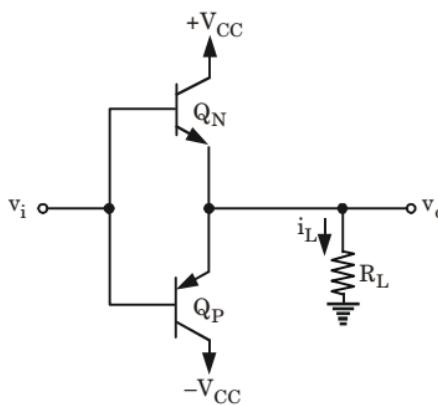
- C. **Capture range :** The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range.
- D. **Pull-in time :** The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the loop gain and loop filter characteristics.
- E. **Applications :**
  1. Frequency divider
  2. Frequency multiplier
  3. Frequency synthesizer
  4. AM detector
  5. FM detector
  6. FSK demodulator.

### SECTION-C

Attempt any **two** parts of each questions of this section. All question carry equal mark. **(10 × 5 = 50)**

- 3. a. Describe the operation and characteristics of a BJT complementary push-pull output stage.**

**Ans.** Fig. 10 shows a class B output stage. It consists of a complementary pair of transistors (*npn* and *pnp*) connected in such a way that both cannot conduct simultaneously.



**Fig. 10.** A class B output stage.

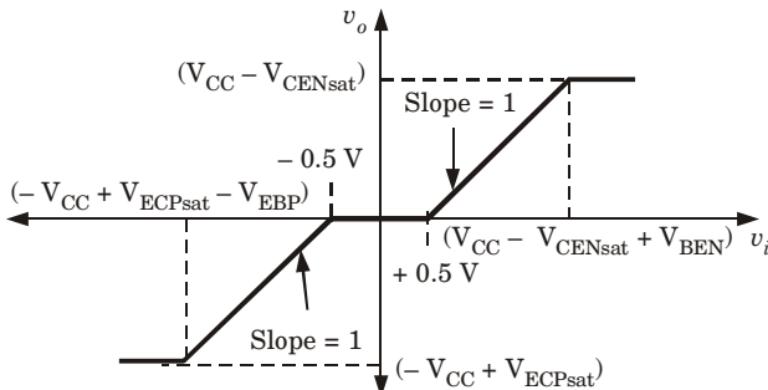
#### **Operation :**

1. When the input voltage  $v_i$  is zero, both transistors are cut-off and the output voltage  $v_o$  is zero.
2. As  $v_i$  goes positive and exceeds about 0.5 V,  $Q_N$  conducts and operates as an emitter follower. In this case  $v_o$  follows  $v_i$  (*i.e.*,  $v_o = v_i - v_{BE(N)}$ ) and  $Q_N$  supplies the load current.

3. Meanwhile, the emitter-base junction of  $Q_P$  will be reverse-biased by the  $V_{BE}$  of  $Q_N$ , which is approximately 0.7 V. Thus  $Q_P$  will be cut-off.
4. If the input goes negative by more than about 0.5 V,  $Q_P$  turns ON and acts as an emitter follower.
5. Again  $v_o$  follows  $v_i$  (*i.e.*,  $v_o = v_i + v_{EBP}$ ), but in this case  $Q_P$  supplies the load current and  $Q_N$  will be cut-off.
6. We conclude that the transistors in the class *B* stage of Fig. 11 are biased at zero current and conduct only when the input signal is present.
7. The circuit operates in a push-pull fashion :
  - i.  $Q_N$  pushes (sources) current into the load when  $v_i$  is positive, and
  - ii.  $Q_P$  pulls (sinks) current from the load when  $v_i$  is negative.

#### **Transfer characteristic :**

1. In Fig. 11 there exists a range of  $v_i$  centered around zero where both transistors are cut-off and  $v_o$  is zero. This dead band results in the cross-over distortion.
2. The effect of cross-over distortion will be most pronounced when the amplitude of the input signal is small. Cross-over distortion in audio power amplifiers gives rise to unpleasant sounds.



**Fig. 11.** Transfer characteristic for the class *B* output stage.

- b. Determine the small-signal model of the second stage of the 741 Op-Amp.

**Ans.**

1. Fig. 12 shows the 741 second stage Op-Amp prepared for small-signal analysis. Now we analyze the second stage to determine the values of the parameters of the equivalent circuit shown in Fig. 13.

- a. **Input resistance :** The input resistance  $R_{i2}$  can be found by

$$R_{i2} = (\beta_{16} + 1) \{ r_{e16} + [R_9 \parallel (\beta_{17} + 1)(r_{e17} + R_S)] \} \quad \dots(1)$$

Substituting the appropriate parameter values yields  $R_{i2} \approx 4 \text{ M}\Omega$ .

**b. Transconductance :**

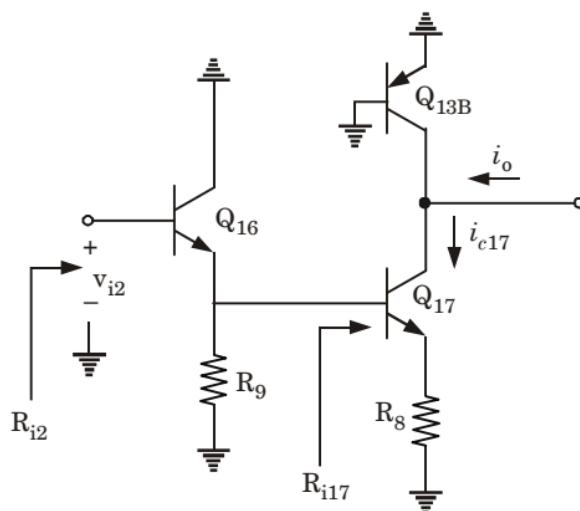
- From the equivalent circuit of Fig. 13, we see that the transconductance  $G_{m2}$  is the ratio of the short-circuit output current to the input voltage.
- Short-circuiting the output terminal of the second stage to ground makes the signal current through the output resistance of  $Q_{13B}$  zero, and the output short-circuit current becomes equal to the collector signal current of  $Q_{17}(i_{17})$ . This can be easily related to  $v_{i2}$  as follows :

$$i_{c17} = \frac{\alpha v_{b17}}{r_{e17} + R_8} \quad \dots(2)$$

$$v_{b17} = v_{i2} \frac{(R_9 \parallel R_{i17})}{(R_9 \parallel R_{i17}) + r_{e16}} \quad \dots(3)$$

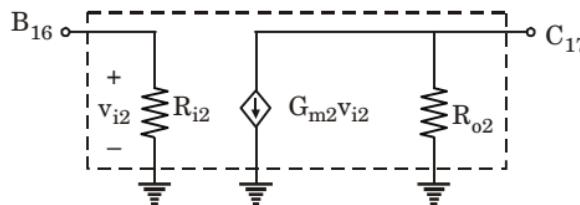
$$R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8) \quad \dots(4)$$

where we have neglected  $r_{o16}$  because  $r_{o16} \gg R_9$ .

**Fig. 12.**

- These equations can be combined to obtain

$$G_{m2} \equiv \frac{i_{c17}}{v_{i2}} \quad \dots(5)$$

**Fig. 13.**

**c. Output resistance :**

- To determine the output resistance  $R_{o2}$  of the second stage in Fig. 13 we ground the input terminal and find the resistance looking back into the output terminal.
- So,  $R_{o2}$  is given by

$$R_{o2} = (R_{o13B} \parallel R_{o17})$$

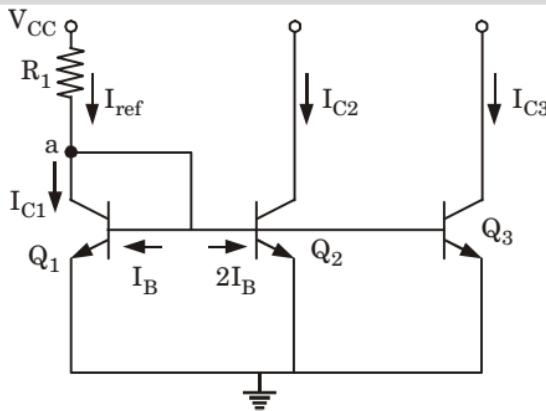
where  $R_{o13B}$  is the resistance looking into the collector  $Q_{13B}$  while its base and emitter are connected to ground and  $R_{o17}$  is the resistance looking into the collector of  $Q_{17}$ .

- The parameter of the three transistor CM are  $V_{CC} = 9$  V,  $V_{EE} = 0$ ,  $R_1 = 12$  k $\Omega$ ,  $V_{BE(on)} = 0.7$  V,  $\beta = 75$ ,  $V_A = \infty$ . Calculate the value of current,  $I_{ref}$ ,  $I_o$ ,  $I_{C1}$ ,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$ ,  $I_{E3}$ .

**Ans.**

**Given :**  $V_{CC} = 9$  V,  $V_{EE} = 0$ ,  $R_1 = 12$  k $\Omega$ ,  $V_{BE(on)} = 0.7$  V,  $\beta = 75$ ,  $V_A = \infty$

**To Calculate :**  $I_{ref}$ ,  $I_o$ ,  $I_{C1}$ ,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$ ,  $I_{E3}$ .



**Fig. 14.**

- From Fig. 14, we can write

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$$

$$I_{ref} = \frac{9\text{ V} - 0.7\text{ V}}{12\text{ k}\Omega} = 0.691\text{ mA} \quad \dots(1)$$

Here,

$$I_0 = I_{C1} = I_{C2} = I_{C3} = I_C \text{ and } I_{B1} = I_{B2} = I_{B3} = I_B$$

- At node 'a',

$$\begin{aligned} I_{ref} &= I_C + I_B + 2I_B \\ I_{ref} &= I_C + 3I_B \end{aligned}$$

$$= I_C \left( 1 + \frac{3}{\beta} \right)$$

$$0.691 \times 10^{-3} = I_C \left( 1 + \frac{3}{75} \right)$$

$$I_C = \frac{0.691 \times 10^{-3}}{1.04} = 0.664 \text{ mA}$$

$$I_C = I_{C1} = I_{C2} = I_{C3} = 0.664 \text{ mA}$$

3. In eq. (2), substitute the value of  $I_C$ , we get,

$$I_B = \frac{0.691 \text{ mA} - 0.664 \text{ mA}}{3} = 0.0135 \text{ mA}$$

$$I_E = I_B + I_C = 0.0135 + 0.664 = 0.675 \text{ mA}$$

Here,  $I_{E1} = I_{E2} = I_{E3} = I_E$

4. a. Draw the generalized impedance converter and derive its impedance equation. Also simulate an inductor.

**Ans.**

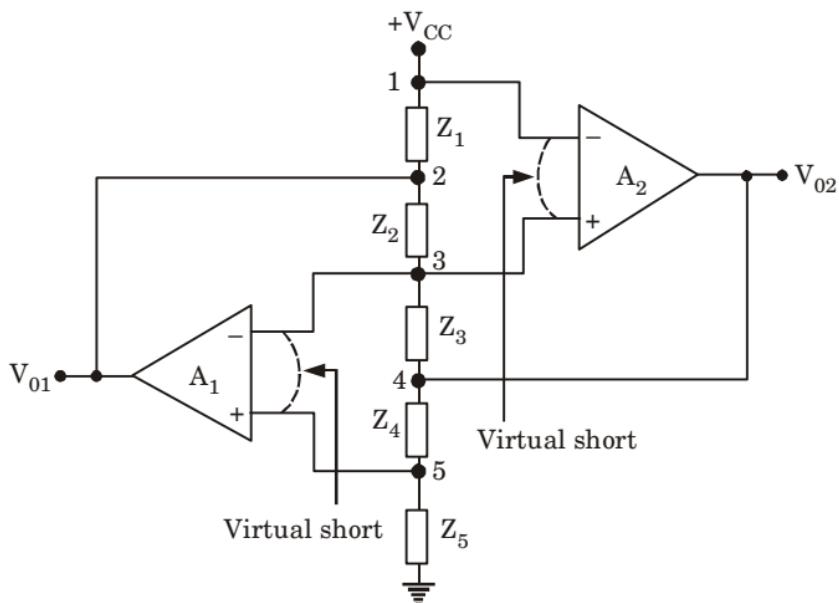
**A. General Impedance Converter (GIC) :**

- Generalized impedance converters (GICs) are Op-Amp circuits that employ  $RC$  networks for simulating frequency-dependent impedance elements such as inductors. Fig. 15 shows the circuit of a GIC.
- From Fig. 15, at node 1,

$$I_C = \frac{V_1 - V_2}{Z_1} = \frac{V_{CC} - V_{01}}{Z_1} \quad \dots(1)$$

where  $V_1 = V_{CC}$  and  $V_2 = V_{01}$ . Now, between nodes 2 and 4, we obtain (using KCL)

$$\frac{V_2 - V_3}{Z_2} = \frac{V_3 - V_4}{Z_3} \quad \dots(2)$$



**Fig. 15.**

3. From the Fig. 15, we observe that nodes 1 and 3 are virtually shorted, and hence using KCL

$$\frac{V_{01} - V_{CC}}{Z_2} = \frac{V_{CC} - V_{02}}{Z_3} \quad \dots(3)$$

where  $V_{02} = V_4$ .

4. Rearranging eq. (3) yields

$$(Z_2 + Z_3) V_{CC} = V_{02} Z_2 + V_{01} Z_3 \quad \dots(4)$$

5. Now by using KCL between nodes 4 and 5, we have

$$\frac{V_{02} - V_5}{Z_4} = \frac{V_5}{Z_5} \quad \dots(5)$$

6. Substitution for  $V_5 = V_{CC}$  and rearrangements give

$$V_{02} = \frac{V_{CC}(Z_4 + Z_5)}{Z_5} \quad \dots(6)$$

7. Substituting for  $V_{02}$  from eq. (6) into eq. (4), we get

$$(Z_2 + Z_3) V_{CC} = \frac{V_{CC}(Z_4 + Z_5)}{Z_5} Z_2 + V_{01} Z_3 \quad \dots(7)$$

8. Rearranging eq. (7), we have

$$V_{CC} \left[ (Z_2 + Z_3) - \frac{(Z_4 + Z_5)}{Z_5} Z_2 \right] = V_{01} Z_3$$

$$V_{CC} \frac{[(Z_2 Z_5 + Z_3 Z_5) - (Z_4 Z_2 + Z_5 Z_2)]}{Z_3 Z_5} = V_{01}$$

$$\text{or, } V_{CC} \frac{Z_3 Z_5 - Z_4 Z_2}{Z_3 Z_5} = V_{01} \quad \dots(8)$$

9. Substituting for  $V_{01}$  from eq. (8) into (1) and simplifying, we obtain

$$I_C Z_1 = V_{CC} \left[ \frac{Z_3 Z_5 - (Z_3 Z_5 - Z_4 Z_2)}{Z_3 Z_5} \right] \quad \dots(9)$$

10. Rearrangement of eq. (9) yields the input impedance of the circuit

$$Z = \frac{V_{CC}}{I_C} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \quad \dots(10)$$

11. Eq. (10) shows that the circuit shown in Fig. 15 can be used as grounded impedance whose nature and value depends on the nature and values of impedance elements  $Z_1$  to  $Z_5$ .

### B. Simulation of Inductor :

- Fig. 16 shows the Antoniou inductance simulation circuit.
- Applying KCL, we get

$$\frac{V_1 - V_z}{1/sC_4} + \frac{V_1}{R_5} = 0$$

$$V_z = V_1 \left[ 1 + \frac{1}{sC_4 R_5} \right]$$

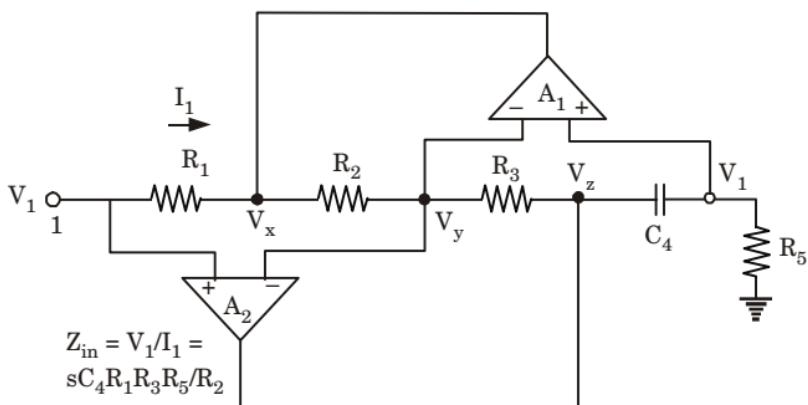


Fig. 16.

3. Apply KCL, we get

$$\frac{V_y - V_x}{R_2} + \frac{V_y - V_z}{R_3} = 0 \quad \dots(11)$$

4. Substituting the value of  $V_z$  in eq. (11)

$$\frac{V_y - V_x}{R_2} + \frac{V_y - V_1 \left( 1 + \frac{1}{sC_4R_5} \right)}{R_3} = 0$$

$$R_3(V_y - V_x) + R_2V_y - R_2V_1 \left( 1 + \frac{1}{sC_4R_5} \right) = 0 \quad \dots(12)$$

5. Apply KCL, then we get

$$\begin{aligned} \frac{V_x - V_1}{R_1} + \frac{V_x - V_y}{R_2} &= 0 \\ R_2(V_x - V_1) + R_1(V_x - V_y) &= 0 \\ V_x(R_1 + R_2) &= R_2V_1 + R_1V_y \\ V_y &= \frac{V_x(R_1 + R_2)}{R_1} - \frac{R_2}{R_1}V_1 \end{aligned} \quad \dots(13)$$

6. Now put the value of  $V_y$  in eq. (12),

then,  $V_x = \left( V_1 + \frac{V_1R_2}{sC_4R_5R_3} \right)$

7. Current across resistance  $R_1$ ,

$$I_1 = \left[ V_1 - \left( V_1 + \frac{V_1R_2}{sC_4R_5R_3} \right) \right] \times \frac{1}{R_1}$$

$$I_1 = \frac{V_1R_2}{sC_4R_5R_3R_1}$$

8. Then input impedance

$$Z_{in} = \frac{V_1}{I_1} = \frac{sC_4 R_1 R_3 R_5}{R_2}$$

which is that of an inductance  $L$  given by,

$$L = \frac{C_4 R_1 R_3 R_5}{R_2}$$

9. If  $R_1 = R_2 = R_3 = R_5 = R$  and  $C_4 = C$   
then,  $L = CR^2$ .

### b. Derive the output expression for $RC$ phase shift oscillator.

**Ans.**

- The circuit of an  $RC$  phase shift oscillator is shown in Fig. 17. The Op-Amp is used in the inverting mode and therefore provides  $180^\circ$  phase shift. The additional phase of  $180^\circ$  is provided by the  $RC$  feedback network to obtain a total phase shift of  $360^\circ$ .
- The feedback network consists of three identical  $RC$  stages. Each of the  $RC$  stage provides a  $60^\circ$  phase shift so that the total phase shift due to feedback network is  $180^\circ$ .
- The feedback factor  $\beta$  of the  $RC$  network can be calculated by writing the KVL equations from Fig. 18.

$$I_1 \left( R + \frac{1}{sC} \right) - I_2 R = V_0 \quad \dots(1)$$

$$-I_1 R + I_2 \left( 2R + \frac{1}{sC} \right) - I_3 R = 0 \quad \dots(2)$$

$$0 - I_2 R + I_3 \left( 2R + \frac{1}{sC} \right) = 6 \quad \dots(3)$$

and  $V_f = I_3 R$

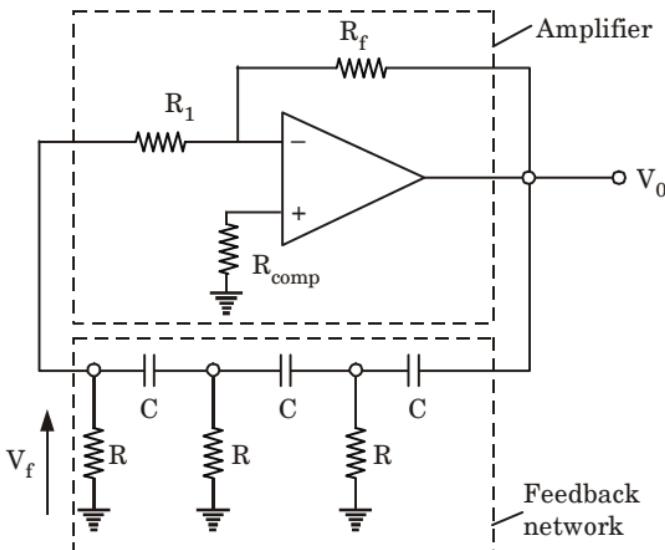
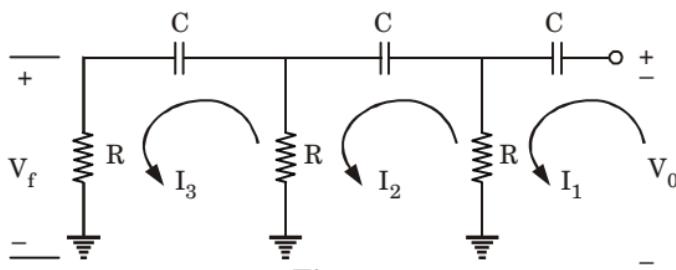


Fig. 17.

**Fig. 18.**

4. Solving eq. (1), (2) and (3) for  $I_3$ , we get

$$I_3 = \frac{V_0 R^2 s^3 C^3}{1 + 5sRC + 6s^2 C^2 R^2 + s^3 C^3 R^3}$$

and

$$V_f = I_3 R = \frac{V_0 R^3 s^3 C^3}{1 + 5sRC + 6s^2 C^2 R^2 + s^3 C^3 R^3}$$

$$= \frac{1}{1 + \frac{6}{sRC} + \frac{5}{s^2 C^2 R^2} + \frac{1}{s^3 C^3 R^3}}$$

5. Replacing  $s = j\omega$ ,  $s^2 = -\omega^2$  and  $s^3 = -j\omega^3$ , we get

$$\beta = \frac{1}{1 + \frac{6}{j\omega RC} - \frac{5}{\omega^2 R^2 C^2} - \frac{1}{j\omega^3 R^3 C^3}}$$

$$= \frac{1}{(1 - 5\alpha^2) + j\alpha(6 - \alpha^2)} \quad \dots(4)$$

where,  $\alpha = \frac{1}{\omega RC}$

6. For  $A\beta = 1$ ,  $\beta$  should be real, that is the imaginary term in eq. (4) must be zero, thus

$$\alpha(6 - \alpha^2) = 0$$

or,  $\alpha^2 = 6$

$$\alpha = \sqrt{6}$$

That is,  $\frac{1}{\omega RC} = \sqrt{6}$

7. The expression for frequency of oscillation,  $f_o$ , is therefore given by

$$f_o = \frac{1}{2\pi RC \sqrt{6}}$$

8. Putting  $\alpha^2 = 6$  in eq. (4), we get

$$\beta = -\frac{1}{29}$$

The negative sign indicates that the feedback network produces a phase shift of  $180^\circ$ .

9. So,  $|\beta| = \frac{1}{29}$

Since  $|A\beta| \geq 1$

Therefore, for sustained oscillations,

$$|A| \geq 29$$

10. The gain  $A_v$  is kept greater than 29 to ensure that variations in circuit parameters will not make  $|A_v\beta| < 1$ , otherwise oscillations will die out.

- c. Compare and contrast active filters and passive filters.  
Design a second order low pass Butterworth filter to have cut-off frequency of 1 kHz.

**Ans.**

**A. Comparison :**

S. No.	Active filter	Passive filter
1.	Active filters have a power gain i.e., can add energy into the circuit.	Passive filters cannot cause power gain, i.e., they cannot bring energy into the circuit.
2.	Active filters require an external power supply.	Passive filters do not require any external power.
3.	Active filters have frequency limitation due to active elements.	Passive filters have no frequency limitations.
4.	It provides complex control system and therefore expensive than passive filters.	Passive filters are relatively cheaper than active filters.

**B. Numerical :**

**Given :**  $f_H = 1 \text{ KHz} = 1/2\pi RC$

**To Design :** Second order low-pass Butterworth filter.

- Let  $C = 0.1 \mu\text{F}$ , gives the choice of  $R = 1.6 \text{ k}\Omega$ .
- For  $n = 2$ , the damping factor  $\alpha = 1.414$ . Then the passband gain,  

$$A_o = 3 - \alpha = 3 - 1.414 = 1.586.$$
- The transfer function of the normalized second order low-pass Butterworth filter is

$$= \frac{1.586}{s_n^2 + 1.414 s_n + 1}$$

Now, 
$$A_o = 1 + \frac{R_F}{R_i} = 1.586 = 1 + 0.586$$

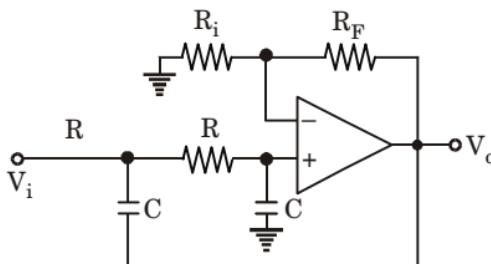


Fig. 19.

4. Let,  $R_F = 5.86 \text{ k}\Omega$  and  $R_i = 10 \text{ k}\Omega$ . Then, we get  $A_o = 1.586$ .
5. The circuit realized in the Fig. 19 with component values as  $R = 1.6 \text{ k}\Omega$ ,  $C = 0.1 \mu\text{F}$ ,  $R_F = 5.86 \text{ k}\Omega$  and  $R_i = 10 \text{ k}\Omega$ .
6. For minimum DC offset,  $R_i \parallel R_F = 2R$ , which has not been taken into consideration here, otherwise, we would have to modify the values of  $R$  and  $C$  accordingly which comes out to be  $R = 1.85 \text{ k}\Omega$ ,  $C = 0.086 \mu\text{F}$ ,  $R_F = 5.86 \text{ k}\Omega$ ,  $R_i = 10 \text{ k}\Omega$ .

- 5. a. Give CMOS implementation of a SR flip-flop and explain its working.**

**Ans.**

**A. CMOS Implementation :**

1. A simpler implementation of a clocked SR flip-flop is shown in Fig. 20. Here, pass transistor logic is employed to implement the clocked set-reset function.

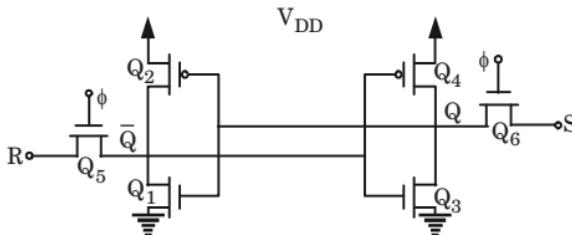


Fig. 20.

2. The SR flip-flop comprising two cross-coupled inverters and two pass transistors  $Q_5$  and  $Q_6$ . The pass transistors are turned ON when the clock ( $\phi$ ) is high, and they connect the flip-flop input S and R. The pass transistors act as transmission gates allowing the inputs S and R.

**B. Operation :**

1. Consider the flip-flop output has the initial state  $Q = 1$  and  $\bar{Q} = 0$ , and the input  $R = 1$  and  $S = 0$  is applied to the input of flip-flop.
2. When the clock  $\phi$  is high, the transistors  $Q_5$  and  $Q_6$  are turned ON.
3. For this input  $R = 1$  and  $S = 0$ , the transistor  $Q_3$  is turned ON and pull down the output  $Q = 0$ .

4. These output  $Q$  is applied to the input of  $Q_2$  and  $Q_1$  transistors, this will make the transistor  $Q_2$  turned ON and the output  $\bar{Q}$  becomes high.
  5. Now consider the output has initial state  $Q = 0$  and  $\bar{Q} = 1$ , and the input  $R = 0$  and  $S = 1$ . When the clock  $\phi$  is high, the pass transistors  $Q_5$  and  $Q_6$  are turned ON. For this input  $R = 0$  and  $S = 1$ , the transistor  $Q_1$  turned ON and  $Q_2$  is turned OFF.
  6. This causes the output  $\bar{Q} = 0$  and  $\bar{Q}$  is applied to the input of transistors  $Q_3$  and  $Q_4$ . Now the transistor  $Q_4$  turned ON and this make the output  $Q$  is high.
- b. Give two different CMOS realization of the Exclusive-OR gate function in which the PDN and PUN are dual network.**

**Ans.**

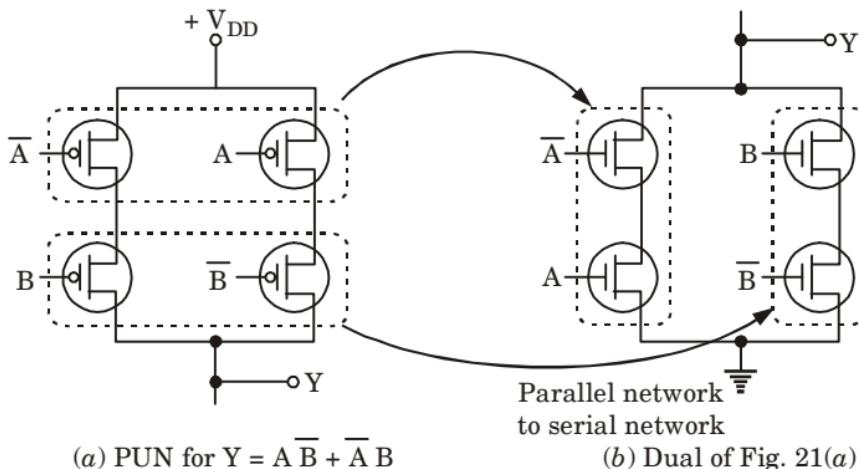
1. For Exclusive - OR function we have,

$$Y = A\bar{B} + \bar{A}B$$

$$\text{and } \bar{Y} = \overline{A\bar{B} + \bar{A}B} = \overline{A\bar{B}} \cdot \overline{\bar{A}B} = (\bar{A} + B) \cdot (A + \bar{B}) \\ = AB + \bar{A}\bar{B}$$

#### i. Realization I :

1. Note that Fig. 21(b) is drawn by converting parallel networks of Fig. 21(a) to serial networks.
2. Now by connecting PUN of Fig. 21(a) with PDN of Fig. 21(b) we can realize Exclusive-OR function.

**Fig. 21.**

#### ii. Realization II :

1. PDN for  $\bar{Y} = AB + \bar{A}\bar{B}$  is shown in Fig. 22(a).
2. Note that Fig. 22(b) is drawn by converting series networks into parallel networks.

3. Now by connecting PUN of Fig. 22(b) with PDN of Fig. 22(a) we can realize Exclusive-OR function.

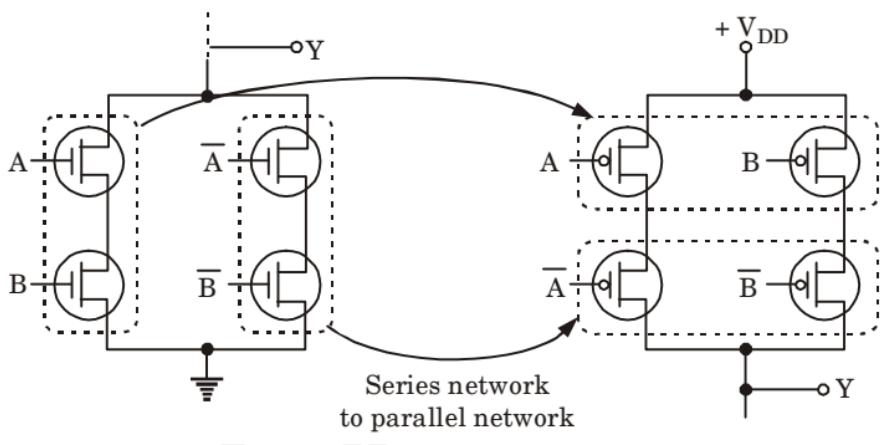


Fig. 22.

### c. Discuss D-F/F circuit using NAND CMOS gates.

**Ans.**

- Fig. 23 shows the circuit realization of  $D$  flip-flop with CMOS NAND gate. This circuit consists of two stages implemented by  $SR$  NAND latches.

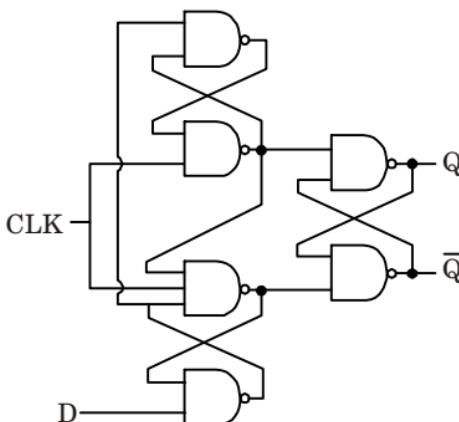
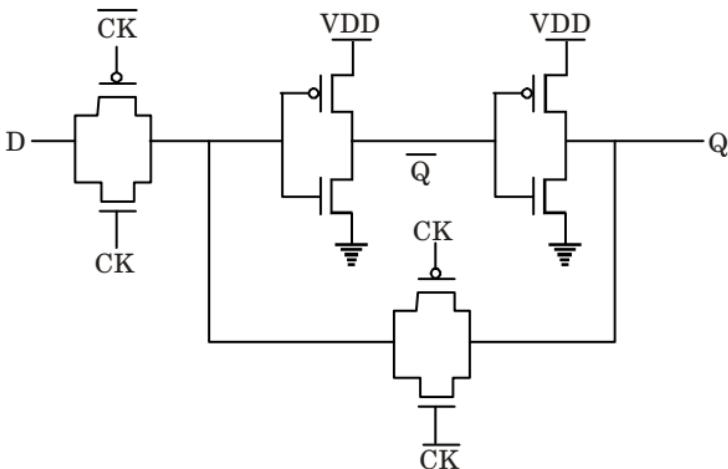


Fig. 23.

- The input stage (the two latches on the left) processes the clock and data signals to ensure correct input signals for the output stage (the single latch on the right).
- If the clock is low, both the output signals of the input stage are high regardless of the data signal; the output latch is unaffected and it stores the previous state.
- When the clock signal changes from low to high, only one of the output voltages (depending on the data signal) goes low and set/resets the output latch. If  $D = 0$ , the lower output becomes low; if  $D = 1$ , the upper output becomes low.

5. If the clock signal continues staying high, the outputs keep their states regardless of the data input and force the output latch to stay in the corresponding state as the input logical zero remains active while the clock is high.
6. Hence the role of the output latch is to store the data only while the clock is low.
7. The  $D$  latch is normally, implemented with transmission gate (TG) switches as shown in the Fig. 24.

**Fig. 24.**

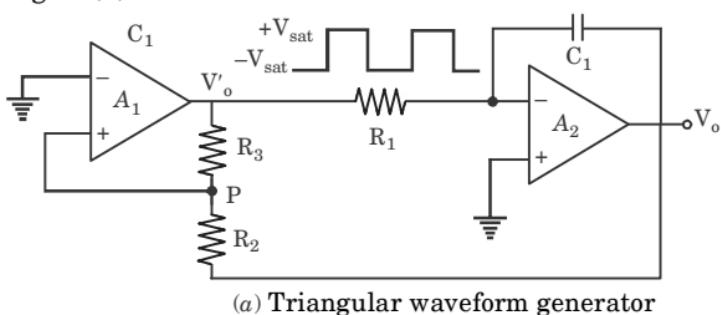
8. Input  $D$  is accepted when  $CK$  goes high. When  $CK$  goes low, the input is open-circuited and the latch is set with the prior data  $D$ .

**6. a. Draw and explain the circuit of triangular wave generator. How square wave can be obtained using this triangular wave.**

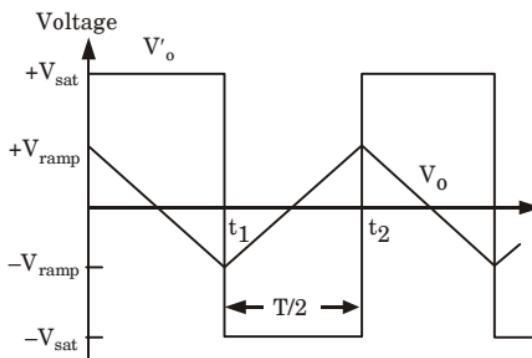
**Ans.**

**A. Generation of triangular waveforms :**

1. A triangular wave can be simply obtained by integrating a square wave.
2. Triangular wave generator along with waveforms is shown in Fig. 25(a).



(a) Triangular waveform generator



(b) Waveforms.

**Fig. 25.****Working :**

1. Assume output of comparator  $A_1$  is at  $\pm V_{\text{sat}}$  so output of integrator will be a negative going ramp as shown in Fig. 25(b).
2. When the negative going ramp reaches to  $-V_{\text{ramp}}$ , the output of  $A_1$  switches from  $+V_{\text{sat}}$  to  $-V_{\text{sat}}$ . The sequence then repeats to give triangular wave at the output of  $A_2$ .
3. The frequency of triangular waveform can be calculated as follows :
  - i. The effective voltage at point  $P$  during the time when output of  $A_1$  is at  $+V_{\text{sat}}$  level is given by,

$$-V_{\text{ramp}} + \frac{R_2}{R_2 + R_3} [+V_{\text{sat}} - (V_{\text{ramp}})] \quad \dots(1)$$

- ii. At  $t = t_1$ , the voltage at point  $P$  becomes equal to zero. Therefore from eq. (1)

$$-V_{\text{ramp}} = - \frac{R_2}{R_3} (+V_{\text{sat}}) \quad \dots(2)$$

- iii. Similarly, at  $t = t_2$ , when the output of  $A_1$  switches from  $-V_{\text{sat}}$  to  $+V_{\text{sat}}$ ,

$$V_{\text{ramp}} = \frac{-R_2}{R_3} (-V_{\text{sat}}) = \frac{R_2}{R_3} (V_{\text{sat}})$$

- iv. Therefore, peak to peak amplitude of the triangular wave is

$$V_o(pp) = +V_{\text{ramp}} - (-V_{\text{ramp}}) = 2 \frac{R_2}{R_3} V_{\text{sat}} \quad \dots(3)$$

- v. The output switches from  $-V_{\text{ramp}}$  to  $+V_{\text{ramp}}$  in half the time period  $T/2$ .

Putting the values in the basic integrator equation,

$$V_o = -\frac{1}{RC} \int v_i dt$$

$$V_o(pp) = -\frac{1}{R_1 C_1} \int_0^{T/2} (-V_{\text{sat}}) dt = \frac{V_{\text{sat}}}{R_1 C_1} \left( \frac{T}{2} \right)$$

$$\text{or, } T = 2R_1C_1 \frac{V_o(pp)}{V_{sat}} \quad \dots(4)$$

vi. Putting the value of  $V_o(pp)$  from eq. (4), we get

$$T = \frac{4R_1C_1R_2}{R_3}$$

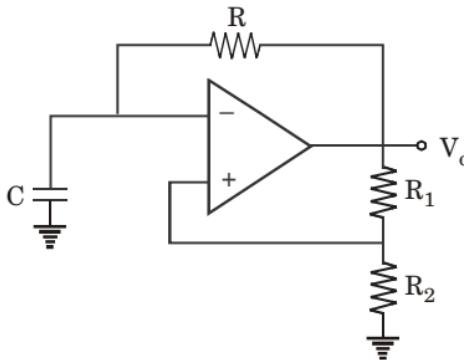
Hence the frequency of oscillation  $f_o$  is,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}$$

### B. Generating of square waveforms :

1. Square wave generator is also called as astable multivibrator or free running oscillator.
2. Circuit of square wave generator is as shown in Fig. 26. The principle of generation of square wave output is to force an Op-Amp to operate in the saturation region.
3. A fraction of output is fed back to the (+ ve) input terminal. This fraction is given by,

$$\beta = \frac{R_2}{R_1 + R_2}$$



**Fig. 26.**

4. Thus, the reference voltage is  $\beta V_o$  and may take values as  $+ \beta V_{sat}$  or  $- \beta V_{sat}$ . The output is also fed back to the (- ve) input terminal after integrating by  $RC$  combination. When (- ve) input terminal voltage exceeds  $V_{REF}$ , switching takes place resulting in square wave output.
5. Now, consider the waveform shown in Fig. 27. When the output is at  $+ V_{sat}$ , capacitor C starts charging through R. Voltage at (+ ve) input terminal is  $+ \beta V_{sat}$ . Now as the charge C rises above this reference voltage  $+ \beta V_{sat}$ , output switches to  $- V_{sat}$ .
6. At this instant, voltage on the capacitor is  $+ \beta V_{sat}$ , hence it starts discharging through R i.e., towards  $- \beta V_{sat}$ . When output voltage switches to  $- V_{sat}$ , the capacitor charges more negatively until its voltage just exceeds  $- \beta V_{sat}$ .

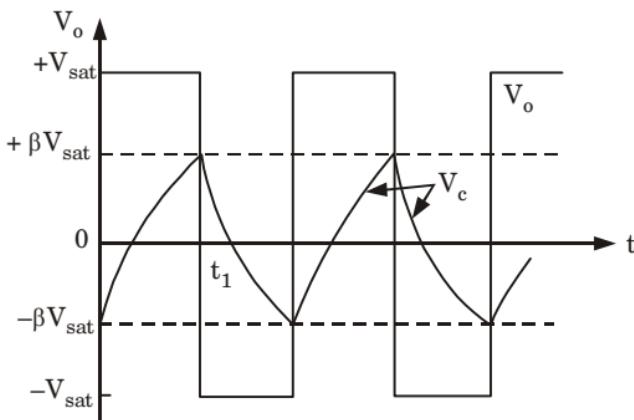


Fig. 27.

7. The output switches back to  $+V_{sat}$  and hence the cycle repeats itself.
8. Now, voltage across the capacitor, as a function of time is given by

$$V_c(t) = V_{final} + (V_{initial} - V_{final}) e^{-t/RC}$$

As,

$$V_{final} = +V_{sat}$$

and

$$V_{initial} = -\beta V_{sat}$$

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/RC}$$

$$V_c(t) = V_{sat} - V_{sat} (1 + \beta) e^{-t/RC}$$

9. At  $t = t_1$ , voltage across capacitor reaches to  $+\beta V_{sat}$ , therefore,

$$V_c(t_1) = \beta V_{sat} = V_{sat} - V_{sat} (1 + \beta) e^{-t_1/RC}$$

After solving,

$$t_1 = RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

This is only half of the total period.

$$\therefore \text{Total time period} = 2t_1 = 2RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

- b. Describe temperature compensated log amplifier using two Op-Amp and explain its operation.**

**Ans.**

1. The logarithmic amplifier is very sensitive to temperature. To minimize the temperature effects, the circuit called temperature-compensated logarithmic amplifier is used, in which two matched diodes are used to cancel the temperature-dependent offset term  $\log I_S$ .
2. Similarly, a thermistor, which is a temperature-sensitive resistor can be used to cancel the temperature-dependent scaling factor ' $\eta V_T$ '.

3. The output voltage of Op-Amp  $A_1$  is negative of the voltage across diode  $D_1$  and is given by

$$v_{01} = -V_{f1} = -\eta V_T \left[ \log \frac{v_I}{R_1} - \log I_S \right] \quad \dots(1)$$

4. Similarly, the voltage across diode  $D_2$  is given by

$$V_{f2} = \eta V_T (\log I - \log I_S) \quad \dots(2)$$

where  $I$  is the forward current and  $I_S$  is the reverse saturation current of diode  $D_2$ .

5. As both diodes are matched, their reverse saturation currents are same. The voltage at the non-inverting terminal of Op-Amp  $A_2$  is given by

$$V_2 = v_{01} + V_{f2} = -\eta V_T \log \left( \frac{v_I}{IR_1} \right) \quad \dots(3)$$

6. Thus, the temperature-dependent offset term is eliminated from the output of  $A_1$ . The Op-Amp  $A_2$  is a non-inverting amplifier and its output is given by

$$v_0 = \left( 1 + \frac{R_f}{R_1 + R_T} \right) V_2 \quad \dots(4)$$

$$v_0 = - \left( \frac{R_1 + R_T + R_f}{R_1 + R_T} \right) \eta V_T \log \frac{v_I}{IR_1} \quad \dots(5)$$

7. Thus the circuit shown in Fig. 28 cancels the temperature-dependent terms present at the output of the log amplifier and provides a temperature-independent logarithmic output.

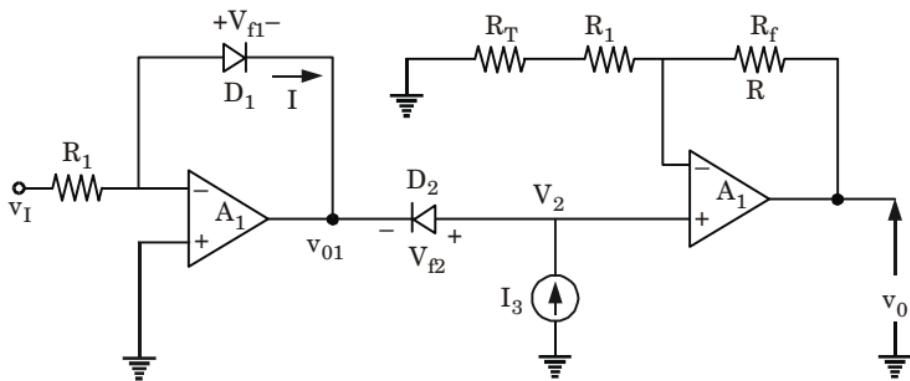
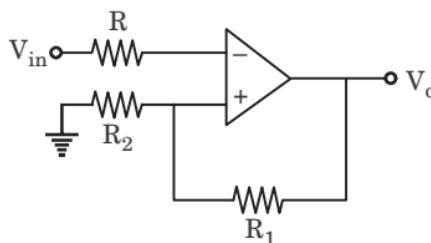


Fig. 28.

- c. Explain how a Schmitt trigger circuit works with a neat diagram. Design a Schmitt trigger with  $V_{UT} = 2$  V,  $V_{LT} = -2$  V. Assume  $\pm V_{sat} = \pm 13$  V.

**Ans.****A. Schmitt trigger :**

- If positive feedback is added to the comparator circuit, gain can be increased greatly. This circuit is called Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback.
- Schmitt trigger also exhibits the phenomenon of hysteresis. The input voltage is applied to the (-ve) input terminal and feedback voltage to the (+ve) input terminal.
- Input voltage  $V_{in}$  triggers output  $V_o$ , every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage ( $V_{UT}$ ) and lower threshold voltage ( $V_{LT}$ ).

**Fig. 29.** Schmitt trigger.

- Now, suppose the output  $V_o = +V_{sat}$ . The voltage at (+) input terminal will be

$$V_{UT} = \frac{R_2}{R_1 + R_2} (+V_{sat}) \quad \dots(1)$$

This voltage is upper threshold voltage. As long as  $V_{in}$  is less than  $V_{UT}$ , the output  $V_o$  remains constant at  $+V_{sat}$ .

- When  $V_{in}$  is just greater than  $V_{UT}$ , the output then switches to  $-V_{sat}$  and remains at this level as long as  $V_{in} > V_{UT}$ .
- For  $V_o = -V_{sat}$ , the voltage at (+ve) input terminal will be

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{sat}) \quad \dots(2)$$

This voltage is called lower threshold voltage.

- The output voltage is  $-V_{sat}$  as long as  $V_{in}$  is above or positive with respect to  $V_{LT}$ . The output voltage  $V_o$  changes to  $+V_{sat}$  if  $V_{in}$  goes more negative than or below  $V_{LT}$ . Resistor  $R$  is shown as  $R_1 \parallel R_2$  compensate for input bias current.
- Input and output voltage waveforms are shown in Fig. 30.

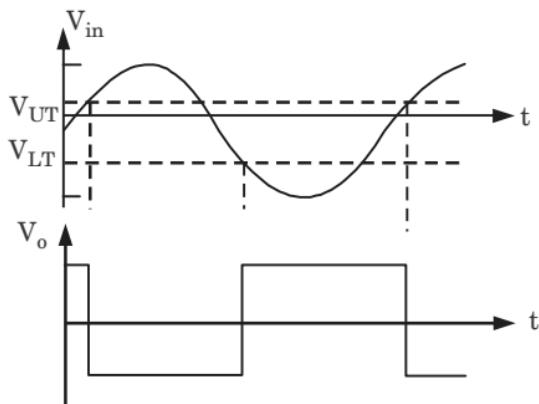


Fig. 30.

**B. Numerical :**

**Given :**  $V_{UT} = 2 \text{ V}$ ,  $V_{LT} = -2 \text{ V}$ ,  $\pm V_{\text{sat}} = \pm 13 \text{ V}$

**To Design :** Schmitt trigger.

$$1. \text{ We know, } V_{UT} = \frac{R_2}{R_1 + R_2} (+ V_{\text{sat}})$$

$$2 \text{ V} = \frac{R_2}{R_1 + R_2} (+ 13)$$

$$\frac{R_2}{R_1 + R_2} = \frac{2}{13} = 0.154 \quad \dots(1)$$

$$\text{and} \quad V_{LT} = \frac{R_2}{R_1 + R_2} (- V_{\text{sat}})$$

$$-2 \text{ V} = \frac{R_2}{R_1 + R_2} (-13)$$

$$\frac{R_2}{R_1 + R_2} = \frac{-2}{-13} = 0.154 \quad \dots(2)$$

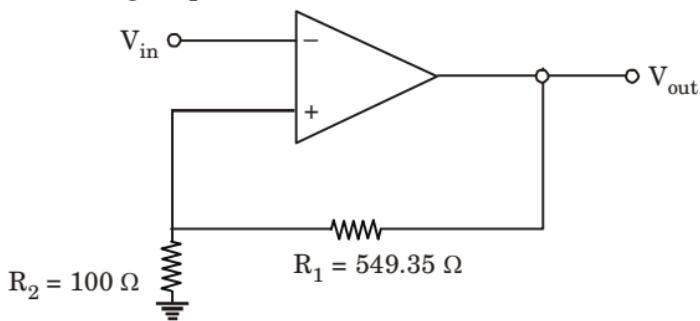


Fig. 31.

2. From eq. (1) and (2)

$$\frac{R_2}{R_1 + R_2} = 0.154$$

Let  $R_2 = 100 \Omega$

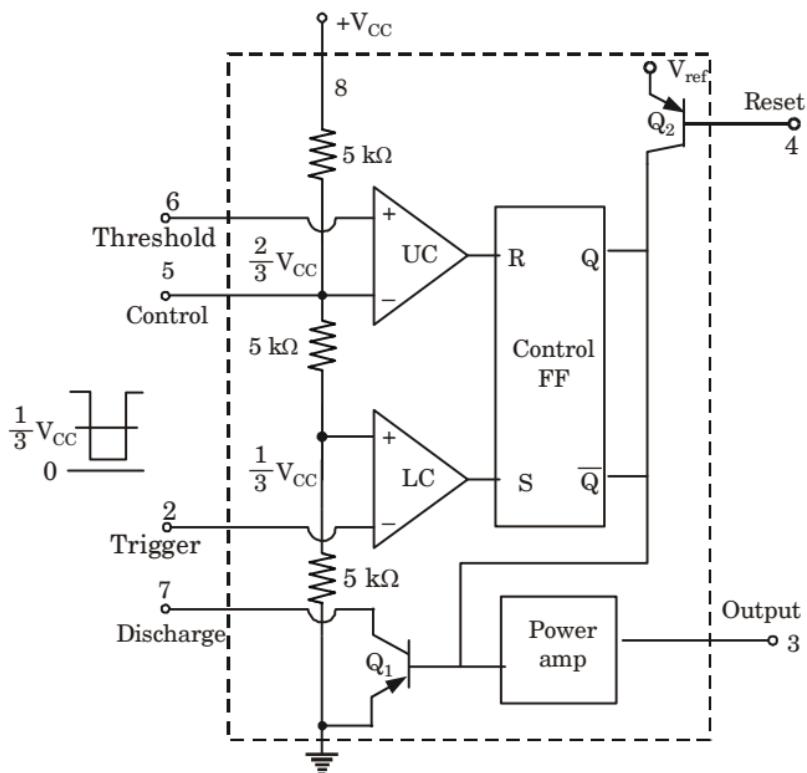
$$\therefore \frac{100}{R_1 + 100} = 0.154$$

$$\Rightarrow R_1 = 549.35 \Omega$$

### 7. a. Draw and explain the block diagram of IC 555.

**Ans.**

1. In the stable state, the output  $\bar{Q}$  of the flip-flop (FF) is high. This makes the output low because of power amplifier which is basically an inverter.
2. If negative going trigger pulse is applied to pin 2 and should have its DC level greater than the threshold level of the lower comparator (*i.e.*,  $V_{CC}/3$ ), now the trigger passes through ( $V_{CC}/3$ ), the output of the lower comparator goes high and sets the FF ( $Q = 1, \bar{Q} = 0$ ). Therefore the output of IC 555 becomes high.
3. When the threshold voltage at pin 6 passes through  $(2/3)V_{CC}$ , the output of the upper comparator goes high and resets the FF ( $Q = 0, \bar{Q} = 1$ ).



**Fig. 32.**

4. The reset input (pin 4) is used to reset the FF and the flip flop output  $\bar{Q}$  becomes high and the output of IC 555 becomes low because the output of FF is 1.

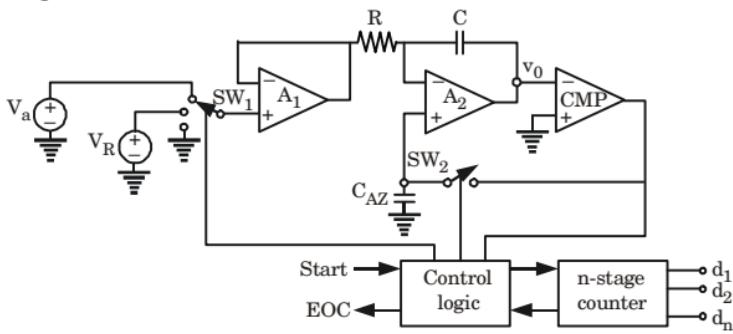
### b. Explain the operation of dual slope ADC.

**Ans.**

- Fig. 33(a) shows the dual slope ADC functional diagram. The circuit consists of a high input impedance buffer  $A_1$ , precision integrator  $A_2$  and a voltage comparator.
- The converter first integrates the analog input signal  $V_a$  for a fixed duration of  $2^n$  clock periods as shown in Fig. 33(b).
- Then it integrates an internal reference voltage  $V_R$  of opposite polarity until the integrator output is zero.
- The number  $N$  of clock cycles required to return the integrator to zero is proportional to the value of  $V_a$  averaged over the integration period. Hence  $N$  represents the desired output code.

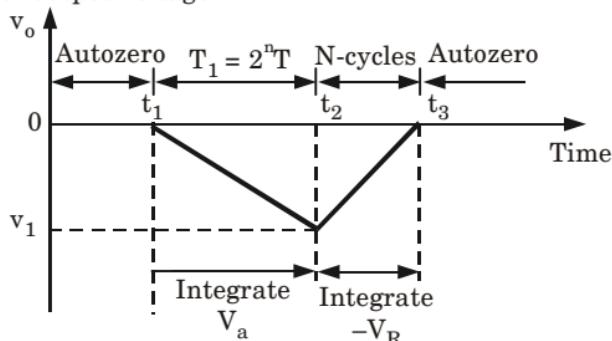
#### Operation :

- Before the START command arrives, the switch  $SW_1$  is connected to ground and  $SW_2$  is closed.
- Any offset voltage present in the  $A_1$ ,  $A_2$ , comparator loop after integration, appears across the capacitor  $C_{AZ}$  till the threshold of the comparator is achieved.
- The capacitor  $C_{AZ}$  thus provides automatic compensation for the input-offset voltages of all the three amplifiers.
- Later, when  $SW_2$  opens,  $C_{AZ}$  acts as a memory to hold the voltage required to keep the offset nulled.
- At the arrival of the START command at  $t = t_1$ , the control logic opens  $SW_2$  and connects  $SW_1$  to  $V_a$  and enables the counter starting from zero.
- The analog voltage  $V_a$  is integrated for a fixed number  $2^n$  counts of clock pulses after which the counter resets to zero.
- If the clock period is  $T$ , the integration takes place for a time  $T_1 = 2^n \times T$  and the output is a ramp going downwards as shown in Fig. 33(b).



(a) Functional diagram of the dual slope ADC.

Integrator output voltage



(b) Integrated output waveform for the dual slope ADC.

**Fig. 33.**

8. The counter resets itself to zero at the end of the interval  $T_1$  and the switch  $SW_1$  is connected to the reference voltage ( $-V_R$ ).
9. The output voltage  $v_o$  will now have a positive slope. However, when  $v_o$  becomes just zero at time  $t = t_3$ , the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter.

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{Clock rate}} \quad \text{and} \quad t_3 - t_2 = \frac{\text{Digital count } N}{\text{Clock rate}}$$

10. For an integrator,  $\Delta v_o = (-1/RC) V(\Delta t)$
11. The voltage  $v_o$  will be equal to  $v_1$  at the instant  $t_2$  and can be written as

$$v_1 = (-1/RC) V_a(t_2 - t_1)$$

12. The voltage  $v_1$  is also given by  $v_1 = (-1/RC) (-V_R)(t_2 - t_3)$   
So,  $V_a(t_2 - t_1) = V_R(t_3 - t_2)$   
Putting the value of  $(t_2 - t_1) = 2^n$  and  $(t_3 - t_2) = N$ , we get  
 $V_a(2^n) = (V_R)N$  or,  $V_a = (V_R)(N/2^n)$

- c. Design a 555 timer as astable multivibrator giving its block diagram which provide an output signal frequency of 2 kHz and 75 % duty cycle.

**Ans.**

**Given :** Frequency,  $f_c = 2$  kHz, Duty cycle,  $D = 75\%$

**To Design :** 555 timer as an astable multivibrator.

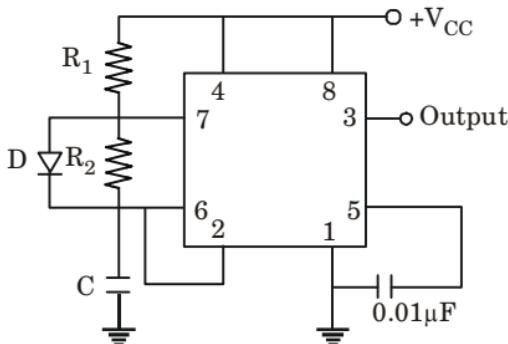
1. We know,  $T = \frac{1}{f} = \frac{1}{2 \times 10^3} = 0.5 \text{ ms}$

$$D = \frac{T_{\text{ON}}}{T}$$

$$\text{i.e.,} \quad T_{\text{ON}} = 0.5 \times 0.75 = 3.75 \times 10^{-4} \text{ sec}$$

$$T_{\text{OFF}} = T - T_{\text{ON}} = 1.25 \times 10^{-4} \text{ sec}$$

2. Duty cycle is more than 50 % hence modified circuit must be used.
3. The modified circuit is shown in Fig. 34.



**Fig. 34.**

4. Let  $C = 0.01 \mu\text{F}$

The charging of  $C$  takes place through  $R_1$  and diode  $D$  while discharging takes place through  $R_2$  only

$$\therefore T_{\text{ON}} = 0.693 R_1 C$$

$$\text{and } T_{\text{OFF}} = 0.693 R_2 C$$

5. Using values of  $T_{\text{ON}}$ ,  $T_{\text{OFF}}$  and  $C$ ,

$$R_1 = 8.658 \text{ k}\Omega$$

$$\text{and } R_2 = 20.202 \text{ k}\Omega$$



**B. Tech.****(SEM. V) ODD SEMESTER THEORY  
EXAMINATION, 2018-19  
INTEGRATED CIRCUITS****Time : 3 Hours****Max. Marks : 70**

**Note :** Be precise in your answer. In case of numerical problem assume data wherever not provided.

**SECTION-A**

1. Attempt all the questions : **(2 × 7 = 14)**
- a. What is full power bandwidth ?
- b. How the effect of input bias current in non-inverting amplifier is compensated ?
- c. Write the advantage of active filter over passive filter.
- d. What is PDN and PUN ?
- e. Write advantage of a voltage follower circuit.
- f. What is the advantage of precision diode rectifier circuit over ordinary rectifier ?
- g. An 8 bit DAC has an input of 10011011 and 10 V reference, find the corresponding output voltage.

**SECTION-B**

2. Attempt any three questions of the following questions : **(7 × 3 = 21)**
- a. Discuss Wilson current mirror and Widlar current source. What are the advantages of Widlar current source over Wilson current mirror ?
- b. Classify active filter. Design second order low pass filter with  $f_H = 2$  kHz and passband gain of 3.
- c. i. Sketch the CMOS logic circuit realization of the expression

$$Y = \overline{A(B + C)} + DE$$

- ii. Draw the  $D$  flip flop using CMOS.
- d. Write short notes on the following :
  - i. Analog multiplier.
  - ii. Logarithmic amplifier.
- e. i. Draw the functional block diagram of IC 555 and explain its working.
- ii. Write a short note on Ex-OR as a phase detector.

### SECTION-C

3. Attempt any one question :  $(7 \times 1 = 7)$
- a. i. How the short circuit protection is achieved in the output stage of 741 Op-Amp ?
  - ii. Draw and explain the frequency response of IC 741.
  - b. What do you understand by the base current mirror ? How does it provide improvement over simple current mirror circuit ? Explain with the help of a neat circuit diagram.
4. Attempt any one question :  $(7 \times 1 = 7)$
- a. Design a wide bandpass filter with  $f_L = 500$  Hz and  $f_H = 1500$  Hz and passband gain of 5, draw the frequency response of the filter and find value of  $Q$ .
  - b. Draw and explain  $I$ - $V$  and  $V$ - $I$  converters and derive its output.
5. Attempt any one question :  $(7 \times 1 = 7)$
- a. Give CMOS implementation of a clocked SR flip-flop and explain its working.
  - b. Derive the formula for  $V_{IL}$  and  $V_{IH}$  of CMOS inverter.
6. Attempt any one question :  $(7 \times 1 = 7)$
- a. i. Describe the Schmitt trigger with help of proper circuit diagram and transfer characteristics.
  - ii. Explain the working of peak detectors.
  - b. Draw the circuit diagram of full wave precision rectifier and find expression for output voltage for both positive and negative half cycle of input sinusoidal waveform.
7. Attempt any one question :  $(7 \times 1 = 7)$

- a. Draw the functional block diagram of IC 555 and explain its working. Draw the circuit diagram of a monostable multivibrator using 555 and find expression for quasi state period.
  
- b. i. Write a short note on analog to digital converter.  
ii. Explain the working of PLL with suitable block diagram.



## SOLUTION OF PAPER (2018-19)

**Note :** Be precise in your answer. In case of numerical problem assume data wherever not provided.

### SECTION-A

1. Attempt **all** the questions : **(2 × 7 = 14)**

**a. What is full power bandwidth ?**

**Ans.** The full power bandwidth,  $f_m$  is the maximum frequency at which an output sinusoidal with an amplitude equal to the Op-Amp rated output voltage ( $V_{o \max}$ ) can be produced without distortion,  

$$f_m = S_R / 2\pi V_{o \max}$$

**b. How the effect of input bias current in non-inverting amplifier is compensated ?**

**Ans.** The effect of input bias current in a non-inverting amplifier is compensated by placing a compensating resistor  $R_{comp}$  in series with the input signal  $V_1$ .

**c. Write the advantage of active filter over passive filter.**

**Ans.**

1. Easier to tune or adjust.
2. Active filter is small and less bulky.

**d. What is PDN and PUN ?**

**Ans.**

- i. **Pull up network (PUN) :** A network that provides a low resistance path to  $V_{dd}$  when output is logic 1 and provides a high resistance to  $V_{dd}$  otherwise.
- ii. **Pull down network (PDN) :** A network that provides a low resistance path to ground (GND) when output is logic 0 and provides a high resistance to ground (GND) otherwise.

**e. Write advantage of a voltage follower circuit.**

**Ans.**

1. Low output impedance, almost zero.
2. The output follows the input exactly without a phase shift.

**f. What is the advantage of precision diode rectifier circuit over ordinary rectifier ?**

**Ans.**

- i. Precision rectifier more stable in comparison to ordinary rectifier.
- ii. The efficiency of precision rectifier is better than ordinary rectifier.

- g. An 8 bit DAC has an input of 10011011 and 10 V reference, find the corresponding output voltage.**

**Ans.** The output voltage for input 10011011

$$= 10 \times (1 \times 2^7 + 0 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$$

$$= 10 \times (154) = 1540 \text{ V} = 1.5 \text{ kV}$$

## SECTION-B

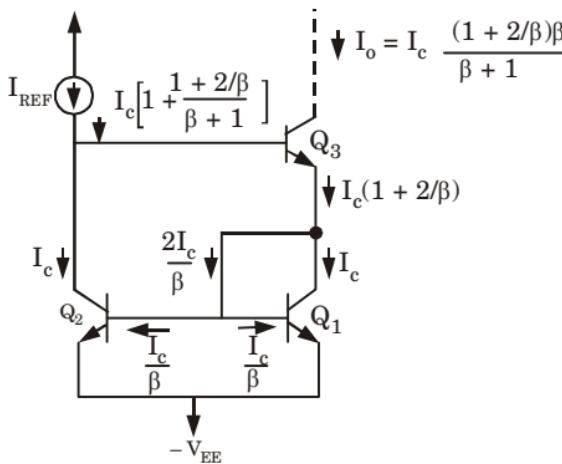
- 2. Attempt any three questions of the following questions : (7 × 3 = 21)**

- a. Discuss Wilson current mirror and Widlar current source. What are the advantages of Widlar current source over Wilson current mirror ?**

**Ans.**

**A. Wilson current mirror :**

1. Wilson current mirror is the modification of basic bipolar mirror with reduced  $\beta$  dependency and increased output resistance.
2. The analysis to determine the effect of finite  $\beta$  on current transfer ratio is shown in Fig. 1.



**Fig. 1.** Analysis to determine the current transfer ratio.

$$\begin{aligned}\frac{I_o}{I_{REF}} &= \frac{I_c \left(1 + \frac{2}{\beta}\right) \frac{\beta}{(\beta + 1)}}{I_c \left[1 + \frac{\left(1 + \frac{2}{\beta}\right)}{(\beta + 1)}\right]} \\ &= \frac{\beta + 1}{\beta + 1 + \frac{\beta + 2}{\beta}} = \frac{\beta + 2}{\beta + 2 + \frac{2}{\beta}}\end{aligned}$$

$$= \frac{1}{1 + \frac{2}{\beta(\beta+2)}} \approx \frac{1}{1 + \frac{2}{\beta^2}}$$

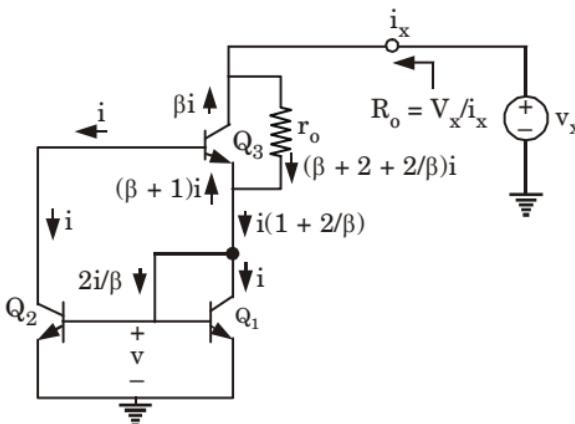
3. The collector emitter voltage of  $Q_1$  and  $Q_2$  are not equal and introduces a current offset error. Analysis to determine the output resistance of the Wilson mirror is shown in Fig. 2.

$$i_x = 2i \left(1 + \frac{1}{\beta}\right)$$

$$v = i \left(1 + \frac{1}{\beta}\right) r_e$$

$$v_x = \left(\beta + 2 + \frac{2}{\beta}\right) ir_o + ir_e \left(1 + \frac{1}{\beta}\right)$$

$$R_o = \frac{v_x}{i_x} \approx \frac{\beta r_o}{2}$$



**Fig. 2.** Analysis for output resistance.

4. Wilson mirror is preferred over the cascade because latter has same dependency on  $\beta$  as the simple mirror. Wilson mirror requires an additional  $V_{BE}$  drop for its operation and so 1 V is allowed across the Wilson-mirror output.

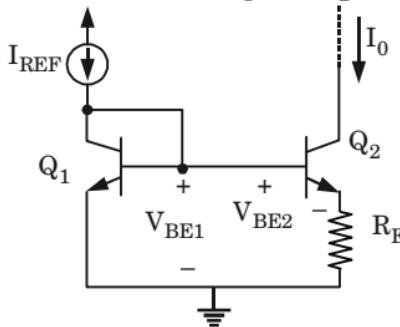
#### B. Widlar current source :

- Fig. 3 shows a Widlar current source which is particularly suitable for low value of currents.
- The circuit differs from the basic current mirror only in the resistance  $R_E$ , that is included in the emitter lead of  $Q_2$ .
- A voltage difference is produced across resistor  $R_E$ , so that  $B-E$  voltage of  $Q_2$  is less than the  $B-E$  voltage of  $Q_1$ .
- A smaller  $B-E$  voltage produces a small collector current, which in turn means that the load current  $I_0$  is less than the reference current  $I_{REF}$ .
- Neglecting base currents,

$$V_{BE1} = V_T \ln \left( \frac{I_{REF}}{I_s} \right) \quad \dots(1)$$

and  $V_{BE2} = V_T \ln \left( \frac{I_0}{I_s} \right) \quad \dots(2)$

here, we have assumed that  $Q_1$  and  $Q_2$  are matched devices



**Fig. 3.** Widlar current source.

6. Combining eq. (1) and (2) gives

$$V_{BE1} - V_{BE2} = V_T \ln \left( \frac{I_{REF}}{I_0} \right) \quad \dots(3)$$

7. But from the circuit shown in Fig. 3.

$$V_{BE1} = V_{BE2} + I_0 R_E$$

Thus,  $I_0 R_E = V_T \ln \left( \frac{I_{REF}}{I_0} \right) \quad \dots(4)$

8. This eq. (4) gives the relationship between the reference and bias currents.

#### C. Advantage of Widlar current source over Wilson current source :

- Using Widlar current circuit, a small current can be generated using relatively small resistors, so chip area is reduced.
- Output resistance is higher than Wilson current source; this is due to emitter degeneration resistance  $R_E$ .

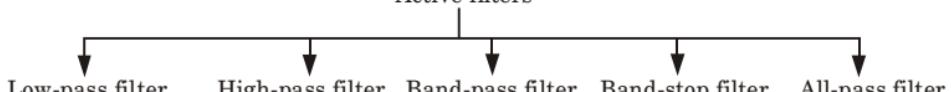
- b. Classify active filter. Design second order low pass filter with  $f_H = 2 \text{ kHz}$  and passband gain of 3.

**Ans.**

#### A. Classification of active filters :

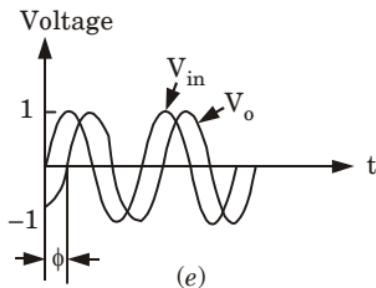
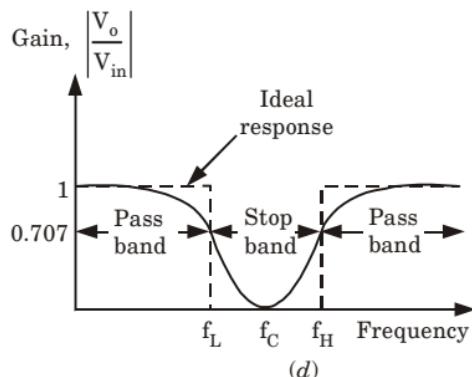
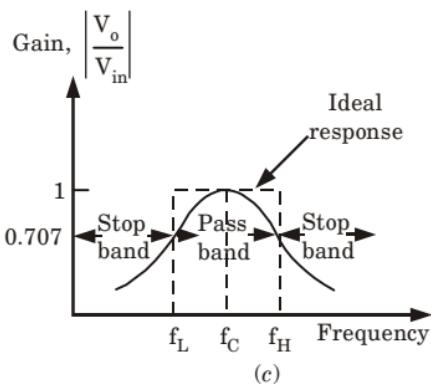
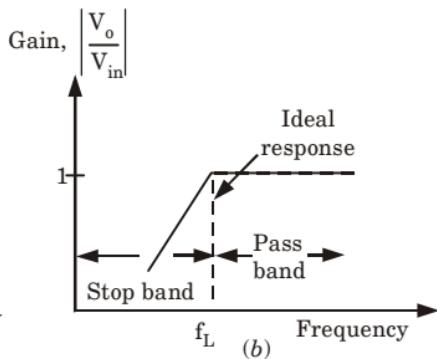
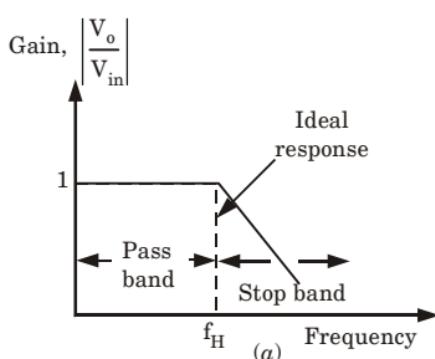
- Active filters employ transistors or Op-Amps in addition to resistors and capacitors.
- The type of element used dictates the operating frequency range of the filter. The classification of active filter is shown in Fig. 4.

Active filters



**Fig. 4.**

3. Each of these filters uses an Op-Amp as the active element and resistors and capacitors as the passive elements.



**Fig. 5.** Frequency response of the major active filters :

- (a) Low-pass ; (b) High-pass ; (c) Band-pass ; (d) Band-reject ;  
(e) Phase shift between input and output voltage of an all-pass filter.

4. Fig. 5 shows frequency response characteristics of the five types of filters. The ideal response is shown by dashed curves, while the solid lines indicate the practical filter response.

#### B. Numerical :

**Given :** Gain = 3,  $f_H = 2 \text{ kHz}$

**To Design :** Second order low-pass filter.

1. Let,  $C_2 = C_3 = 0.0047 \mu\text{F}$

Then,  $R_2 = R_3 = \frac{1}{2\pi f_H C} = \frac{1}{2\pi(2 \times 10^3)(47 \times 10^{-10})}$   
 $= 16.93 \text{ k}\Omega \approx 17 \text{ k}\Omega$

2. Voltage gain,  $A_{vf} = 1 + \frac{R_f}{R_1}$

$$3 = 1 + \frac{R_f}{R_1}$$

$$R_f = 2R_1$$

Assuming,  $R_1 = 27 \text{ k}\Omega$

$$\therefore R_f = 2 \times 27 = 54 \text{ k}\Omega$$

3. The required circuit shown in Fig. 6.

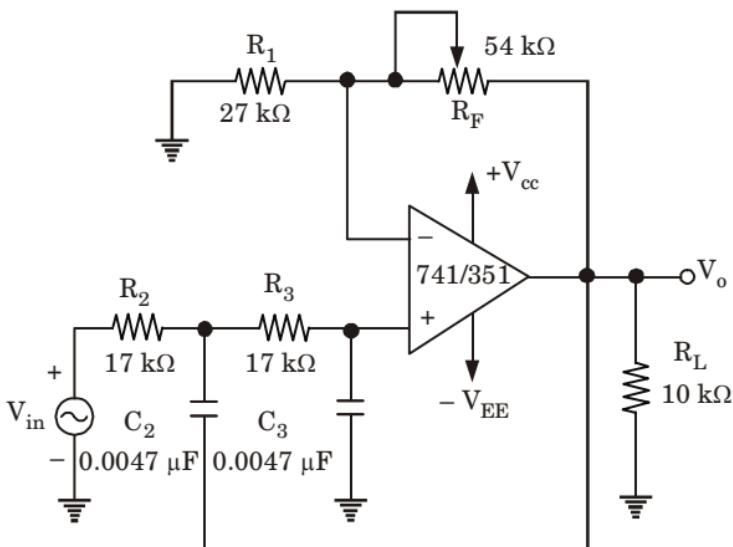


Fig. 6.

c. i. Sketch the CMOS logic circuit realization of the expression

$$Y = \overline{A(B + C) + DE}$$

ii. Draw the D flip flop using CMOS.

**Ans.**

i.  $Y = \overline{A(B + C) + DE}$

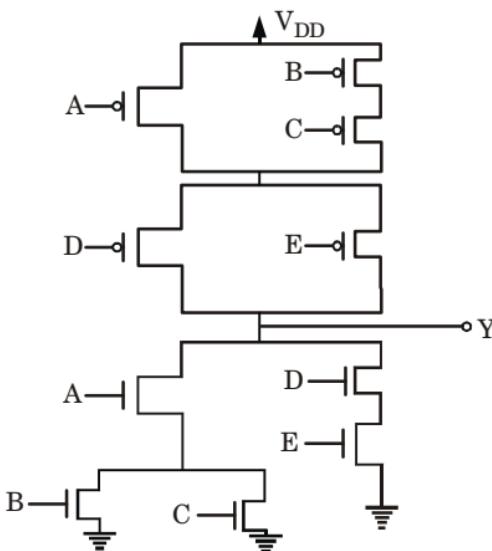


Fig. 7.

**ii. D flip-flop using CMOS :**

1. The  $D$  flip-flop has two inputs, data input  $D$  and a clock input  $\phi$ . The complementary outputs are labeled as  $Q$  and  $\bar{Q}$ .
2. When clock is low, the flip-flop is in the memory or reset state, and any changes on  $D$  input line have no effect on the state of flip-flop.
3. As clock goes high, flip-flop output is equal to  $D$  line just before the rising edge of the clock, such flip-flop is said to be edge triggered.
4. A CMOS based circuit implementation of  $D$  flip-flop is shown in Fig. 8.
5. The circuit consists of two inverters connected in positive feedback loop, and the loop is closed at particular time when the clock is low ( $\phi = 0$  and  $\bar{\phi} = 1$ ).
6. The input  $D$  is connected to the flip-flop through the switch that closes when the clock is high.

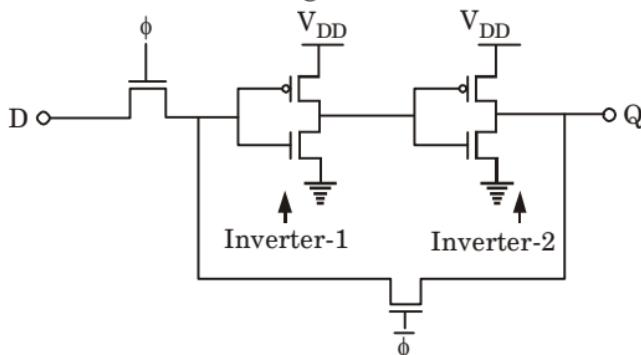


Fig. 8.

7. When  $\phi$  is high, the loop is opened, the  $D$  input connected to input of inverter 1.

8. The capacitance at input node of inverter 1 is charged to value of  $D$ , while capacitance at input node of inverter 2 is charged to value of  $\bar{D}$ .
9. When clock is low, the input line is isolated from flip-flop, the feedback loop is closed and the latch requires the state corresponding to the value of  $D$  just before  $\phi$  went down and providing an output  $Q = D$ .

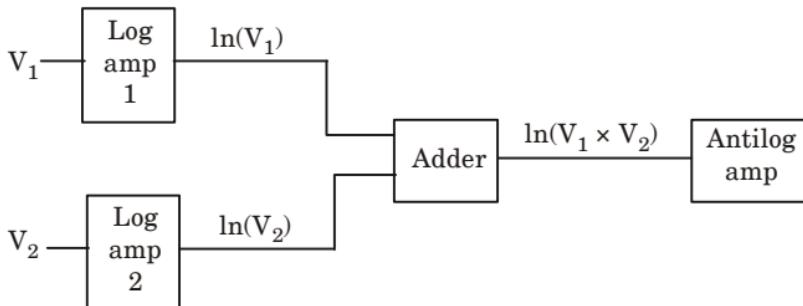
**d. Write short notes on the following :**

- i. **Analog multiplier.**
- ii. **Logarithmic amplifier.**

**Ans.**

**i. Analog multiplier :**

1. A multiplier is an active network whose output is proportional to the product of two input signals.
2. Fig. 9 shows the basic block diagram of an analog multiplier, which uses two logarithmic amplifiers, an adder, and an antilog amplifier.



**Fig. 9.**

3. The input signals, which are to be multiplied, are applied to the input logarithmic amplifiers.
4. The logarithmic amplifiers produce the logarithm of the input signal and these outputs are applied to the adder circuit.
5. The output of the adder circuit, which is the logarithm of product of the two input signals, is fed to the anti-log amplifier.
6. The anti-log amplifier finally removes the logarithm of the terms and produces the multiplication of the input signals.

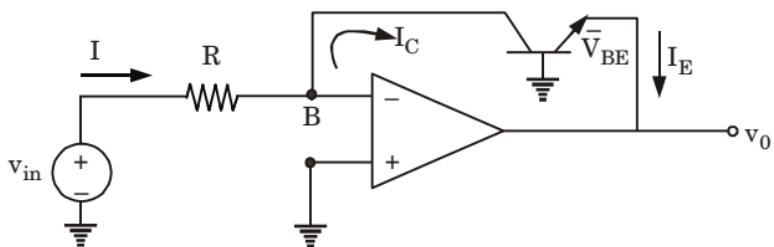
$$\text{i.e., } V_1 \times V_2 = \text{Anti-log}(V_1 \times V_2)$$

**ii. Logarithmic amplifier :**

1. A fundamental log amplifier is formed by placing a transistor in negative feedback path of Op-Amp as shown in Fig. 10.
2. The node  $B$  is at virtual ground hence  $V_B = 0$ . The current through resistor  $R$  can be written as

$$I = \frac{v_{in} - V_B}{R} = \frac{v_{in}}{R} \quad \dots(1)$$

$$I = I_C = I_E = \frac{v_{in}}{R} \quad \dots(2)$$

**Fig. 10.**

3. At the Op-Amp input current is zero

$$I = I_C = \text{Collector current} \quad \dots(3)$$

4. The voltage  $V_{CB} = 0$  as the collector is at virtual ground and base is grounded. Hence, we can write the equation of  $I_C$  as,

$$I_C = I_E = I_S (e^{V_{BE}/V_T}) \quad \dots(4)$$

5. Take natural log on both sides of eq. (4)

$$V_{BE} = V_T \ln \left( \frac{I_E}{I_S} \right) \quad \dots(5)$$

6. Substitute the eq. (2) in eq. (5), we get

$$V_{BE} = V_T \ln \left( \frac{v_{in}}{I_S R} \right) = V_T \ln \left( \frac{v_{in}}{v_{REF}} \right) \quad \dots(6)$$

where  $v_{ref} = I_s R$  and the output is same as  $V_{BE}$

$$\therefore v_0 = -V_{BE}$$

$$v_0 = -V_T \ln \left( \frac{v_{in}}{v_{REF}} \right) \quad \dots(7)$$

- e. i. Draw the functional block diagram of IC 555 and explain its working.

- ii. Write a short note on Ex-OR as a phase detector.

**Ans.**

- i. Functional block diagram of IC-555 :

- In the stable state, the output  $\bar{Q}$  of the flip-flop (FF) is high. This makes the output low because of power amplifier which is basically an inverter.
- If negative going trigger pulse is applied to pin 2 and should have its DC level greater than the threshold level of the lower comparator (i.e.,  $V_{CC}/3$ ), now the trigger passes through ( $V_{CC}/3$ ), the output of the lower comparator goes high and sets the FF ( $Q = 1, \bar{Q} = 0$ ). Therefore the output of IC 555 becomes high.
- When the threshold voltage at pin 6 passes through  $(2/3) V_{CC}$ , the output of the upper comparator goes high and resets the FF ( $Q = 0, \bar{Q} = 1$ ).

4. The reset input (pin 4) is used to reset the FF and the flip flop output  $\bar{Q}$  becomes high and the output of IC 555 becomes low because the output of FF is 1.

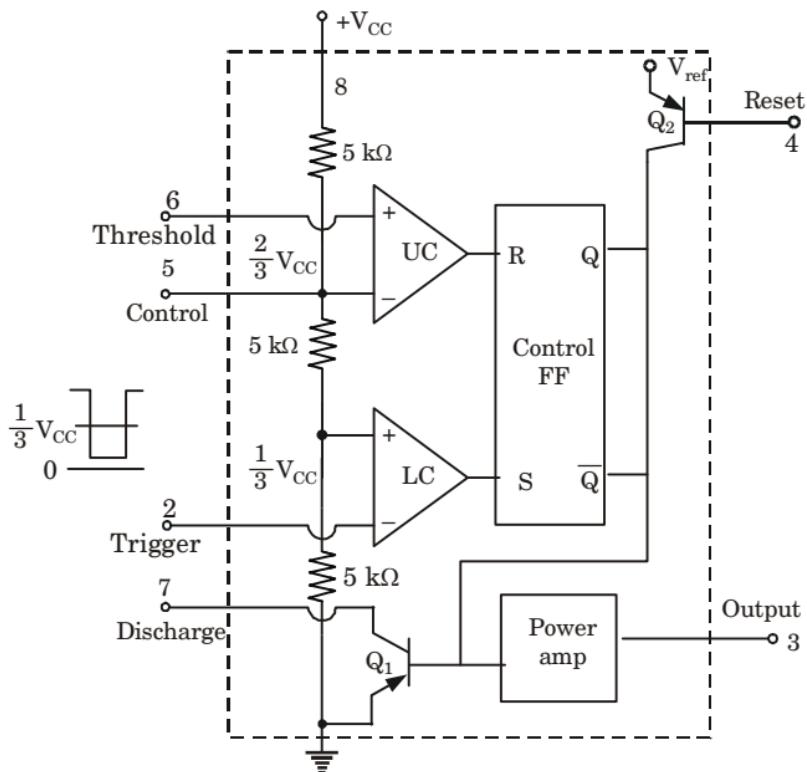


Fig. 11.

### ii. Ex-OR as a phase detector :

1. The Exclusive-OR phase detector is shown in Fig. 12. The output of Ex-OR gate circuit is high only when any one of the two input signals, namely  $f_o$  or  $f_i$  is high.



Fig. 12.

2. The input and output waveform for  $f_i = f_o$  are shown in Fig. 13. In a digital phase detector, the phase error  $\phi$  is defined as

$$\phi = \frac{\tau}{T} 2\pi$$

where  $T$  is the period of input signals of same frequency and  $\tau$  is the time difference between the leading edges of the two signals.

3. Fig. 13 shows that  $f_o$  leads  $f_i$  by  $\phi$  degrees and the DC output voltage of the Ex-OR gate is a function of the phase error  $\phi$  between the two inputs.

4. Ex-OR phase detector can be realized using ICs such as CD4070. The output DC voltage depends on the duty cycle of the input waveforms. Therefore, this type of phase detector is employed when the waveforms of  $f_i$  and  $f_o$  are of square waveform with 50 % duty cycle.

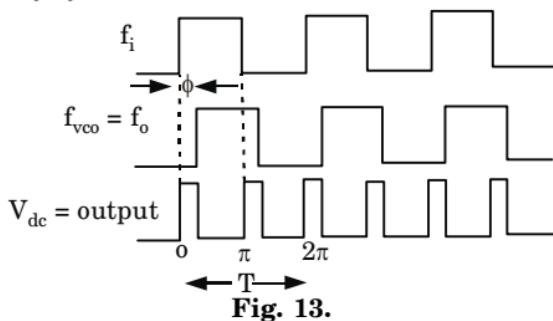


Fig. 13.

## **SECTION-C**

3. Attempt any one question : (7 x 1 = 7)

a. i. How the short circuit protection is achieved in the output stage of 741 Op-Amp ?

ii. Draw and explain the frequency response of IC 741.

**Ans.**

- #### i. Short circuit protection :

1. The short-circuit protection circuitry is shown in the Fig. 14.

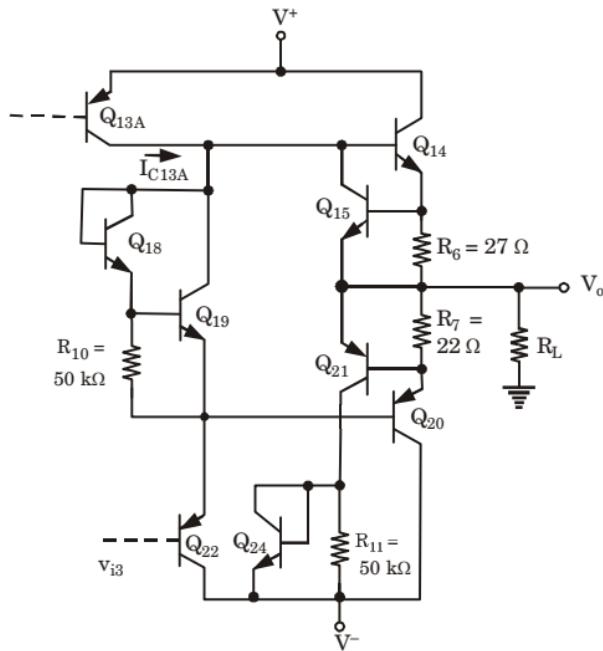


Fig. 14.

2. The Op-Amp 741 contains a number of transistors that are normally in the OFF state.
3. When the output terminal gets shorted to the ground, while keeping a positive output voltage due to certain input signal, this will induce a large current in the output transistor  $Q_{14}$ .
4. This will result in producing heat and cause burn-out of the transistor. Therefore, when current flow in  $Q_{14}$  reaches 20 mA, voltage drop across  $R_6$  becomes  $27 \times 20 = 540$  mV, which bias the transistor  $Q_{15}$ .
5. Similarly, the maximum current in  $Q_{20}$  is limited by  $R_7$ ,  $Q_{21}$  and  $Q_{24}$ .
6. When the current increases, the voltage drop across  $R_7$  becomes sufficient and the transistor  $Q_{21}$  becomes ON and  $Q_{21}$  and  $Q_{24}$  shunt the excess current away from the transistor  $Q_{20}$ , hence protects the output transistor.

#### ii. Frequency response of IC 741 :

1. The system employs the Miller compensation technique.
2. A capacitor ( $C_c$ ) of about 30 pF is connected in the negative feedback path of the second stage.
3. An estimation of frequency of poles can be obtained as,

$$C_{in} = C_c (1 + |A_2|)$$

$A_2$  = Gain of second stage

4. Let  $A_2 = -515$

$$\text{then } C_{in} = 15480 \text{ pF}$$

Since, this value of capacitor is large so we neglect all other capacitances between the base and ground of transistor.

5. The total resistance,

$$\begin{aligned} R_t &= (R_{o1} \parallel R_{i2}) \\ &= (6.7 \text{ M}\Omega \parallel 4 \text{ M}\Omega) \\ &= 2.5 \text{ M}\Omega \end{aligned}$$

6. The dominant pole has a frequency  $f_p$ ,

$$f_p = \frac{1}{2\pi C_{in} R_t} = 4.1 \text{ Hz}$$

7. Calculate all the values of poles and a bode plot is shown in Fig. 15.

$$f_t = A_o f_{3 \text{ dB}} = 243147 \times 4.1 \approx 1 \text{ MHz}$$

where,  $f_t$  is unity-gain bandwidth.

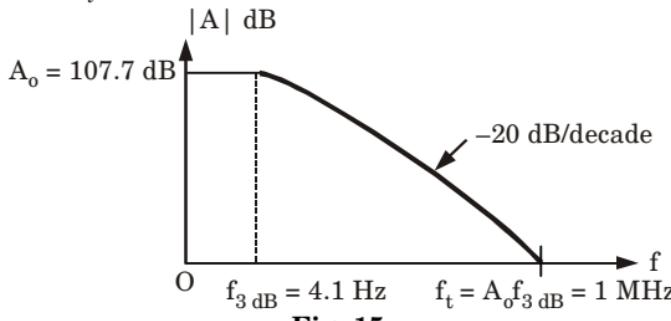


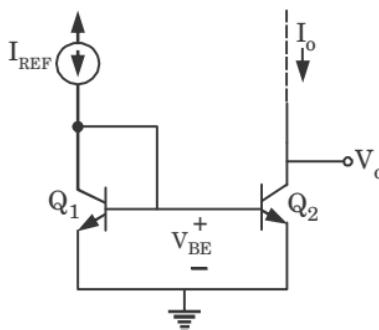
Fig. 15.

9. Bode plot signifies that the phase shift at  $f_t$  is  $-90^\circ$  and thus phase margin is  $90^\circ$ . This phase margin is sufficient to provide stable operation of closed-loop amplifiers with any value of feedback factor  $\beta$ .
- b. **What do you understand by the base current mirror? How does it provide improvement over simple current mirror circuit? Explain with the help of a neat circuit diagram.**

**Ans. Base current mirror :**

1. The basic BJT current mirror is shown in Fig. 16. It is very similar to MOS mirror, but differs in following respect.
2. Firstly, the non-zero base current i.e., finite  $\beta$  and secondly current transfer ratio is determined by relative area of emitter base junction of  $Q_1$  and  $Q_2$ .
3. Consider  $\beta$  is high and neglect base current.  $I_{REF}$  is passed through  $Q_1$  and the corresponding voltage is  $V_{BE}$ .  $V_{BE}$  is applied between base and emitter of  $Q_2$ . Now,  $Q_2$  is matched to  $Q_1$ , i.e., same relative area of emitter-base junction and having equal collector current.

$$I_o = I_{REF}$$



**Fig. 16.** The basic BJT current mirror.

4. Here  $Q_2$  is in active mode until  $V_o$  is 0.3 V or higher than emitter voltage. For obtaining the current transfer ratio, it is required to consider  $m$  times relative area of emitter-base junction (EBJ).

$$I_o = m I_{REF}$$

5. The current transfer ratio,

$$\frac{I_o}{I_{REF}} = \frac{I_{s2}}{I_{s1}} = \frac{\text{Area of EBJ of } Q_2}{\text{Area of EBJ of } Q_1}$$

6. From the node equation at collector of  $Q_1$ ,

$$I_{REF} = I_c + 2 I_c / \beta = I_c (1 + 2 / \beta)$$

Since,  $I_o = I_c$

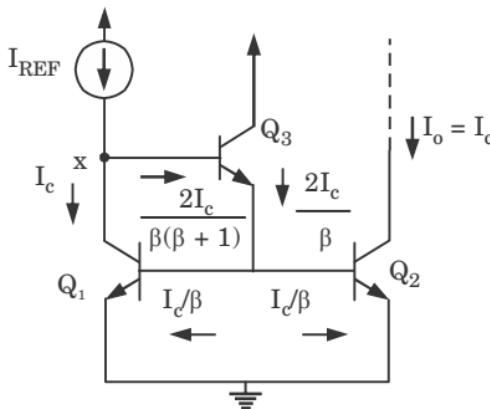
$$\frac{I_o}{I_{REF}} = \frac{I_c}{I_c (1 + 2 / \beta)} = \frac{1}{1 + 2 / \beta}$$

7. Here for higher values of  $\beta$ , the error in the current transfer ratio can be significant, for example :  $\beta = 100$ , results 2 % error in current transfer ratio.

8. However, the error due to finite  $\beta$  increases as the nominal current transfer ratio is increased.

#### **Improvement of base current mirror over simple current mirror (Base current compensation circuit) :**

1. A bipolar current mirror with a current transfer ratio is less dependent on  $\beta$  than that of simple current mirror.
2. This reduces dependency on  $\beta$  and is achieved by using transistor  $Q_3$ . The  $Q_3$  supplies the base current to the  $Q_1$  and  $Q_2$ .
3. The sum of base currents is divided by  $(\beta + 1)$ , resulting in much smaller error current, that has to be supplied by  $I_{REF}$ .



**Fig. 17.** A current mirror with base current compensation.

4. Let us assume  $Q_1$  and  $Q_2$  are matched and having equal collector current. A node equation at node  $x$  gives

$$I_{REF} = I_c \left[ 1 + \frac{2}{\beta(\beta + 1)} \right]$$

5. As,

$$I_o = I_c$$

The current transfer ratio of the mirror will be

$$\frac{I_o}{I_{REF}} = \frac{2}{1 + \beta(\beta + 1)} \approx \frac{1}{1 + 2/\beta^2} \quad \dots(1)$$

Eq. (1) shows that the error due to finite  $\beta$  has been reduced from  $2/\beta$  to  $2/\beta^2$ .

6. However, the output resistance ( $r_o$ ) remains approximately equal to that of simple mirror.
7. If  $I_{REF}$  is not present, then we connect node  $x$  to the power supply  $V_{CC}$  through resistor  $R$ , then

$$I_{REF} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R}$$

4. Attempt any **one** question :  $(7 \times 1 = 7)$
- a. Design a wide bandpass filter with  $f_L = 500$  Hz and  $f_H = 1500$  Hz and passband gain of 5, draw the frequency response of the filter and find value of  $Q$ .

**Ans.****Given :**  $f_L = 500 \text{ Hz}$ ;  $f_H = 1500 \text{ Hz}$ ;  $A = 5$ **To Find :**  $Q$ .**A. Components of the low-pass filter :**

1. Let  $C_{L'} = 0.01 \mu\text{F}$

2.  $R_{L'} = \frac{1}{2\pi f_H C_{L'}} = \frac{1}{2\pi \times 1500 \times 0.01 \times 10^{-6}} = 10.6 \text{ k}\Omega$

3. The gain of the low-pass filter can be considered half,

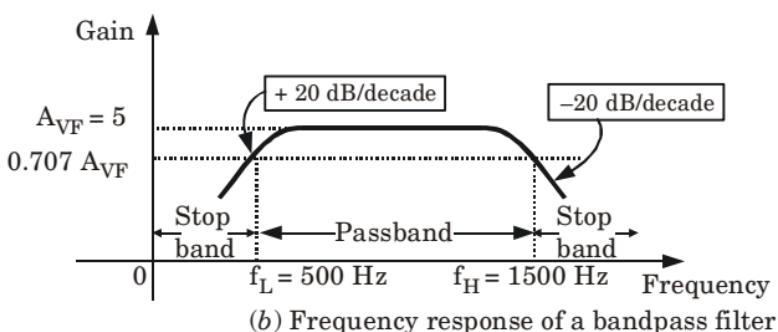
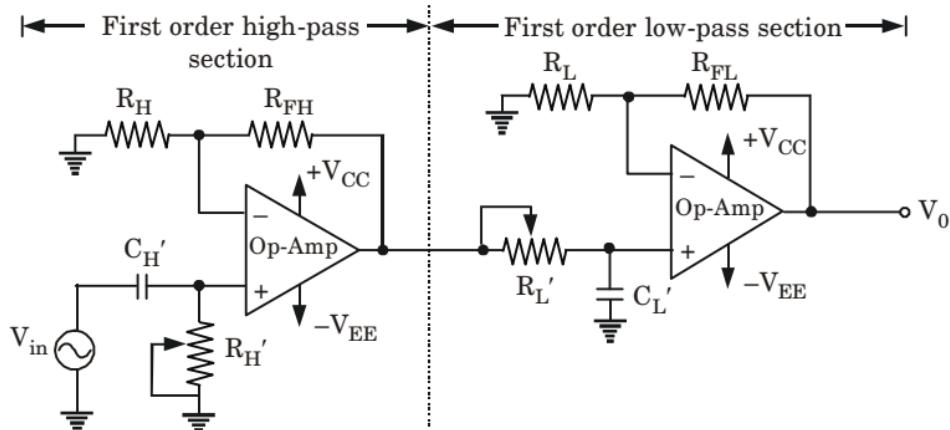
$A_{LF} = 2.5$

$2.5 = 1 + \frac{R_{FL}}{R_L}$

$R_{FL} = 1.5 R_L$

Let we choose  $R_L = 10 \text{ k}\Omega$ 

\therefore  $R_{FL} = 15 \text{ k}\Omega$

**B. Components of the high-pass filter :****Fig. 18.**

1. Let  $C_{H'} = 0.05 \mu\text{F}$

2.  $R_{H'} = \frac{1}{2\pi f_L C_{H'}} = \frac{1}{2\pi \times 500 \times 0.05 \times 10^{-6}}$

$$R_H' = 6.37 \text{ k}\Omega$$

3. The gain = 2.5

$$1 + \frac{R_{FH}}{R_H} = 2.5$$

$$R_{FH} = 1.5 R_H$$

Let we choose

$$R_H = 10 \text{ k}\Omega$$

$$\therefore R_{FH} = 15 \text{ k}\Omega$$

$$4. \text{ Quality factor, } Q = \frac{f_c}{f_H - f_L} = \frac{\sqrt{f_H f_L}}{f_H - f_L} = \frac{\sqrt{500 \times 1500}}{1000} = 0.866$$

- b. Draw and explain I-V and V-I converters and derive its output.**

**Ans.**

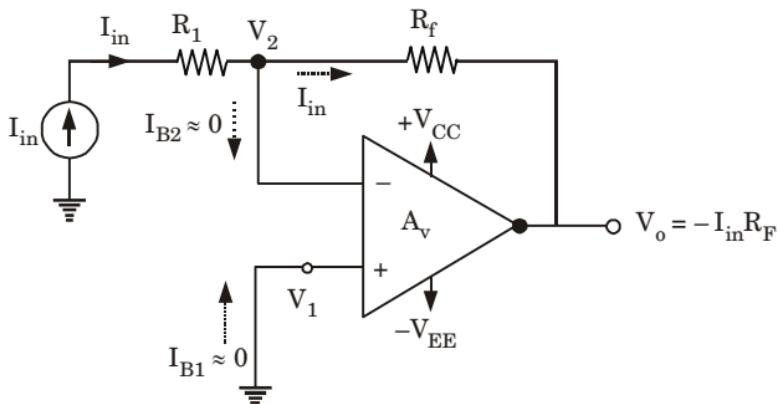
**A. I-V converter :**

1. The current to voltage converter is shown in Fig. 19.
2. The open-loop gain  $A_v$  of the Op-Amp is very large, so due to virtual short concept,

$$V_1 \approx V_2$$

3. As the input impedance of Op-Amp is very high,

$$\therefore I_{B1} = I_{B2} \approx 0$$



**Fig. 19.**

4. Gain of inverting amplifier is given by

$$A_v = \frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

$$\text{or } V_o = \frac{-R_f}{R_1} V_{in} \quad \dots(1)$$

5. But  $V_1 \approx V_2$  and

$$V_1 = 0$$

$$\therefore V_2 = 0$$

6. Thus the inverting terminal is also at ground potential and entire input voltage appears across  $R_1$

$$\therefore I_{in} = \frac{V_{in}}{R_1}$$

$$\text{or } V_{in} = I_{in} R_1 \quad \dots(2)$$

7. Substituting eq. (2) in eq. (1), we get

$$V_o = \frac{-R_f}{R_1} \times I_{in} R_1$$

$$V_o = -R_f I_{in} \quad \dots(3)$$

8. The eq. (3) shows how this circuit converts input current into a proportional voltage.

### B. V-I converter :

- The Fig. 20 shows an arrangement of voltage to current converter with load resistor  $R_L$ . Here  $R_L$  is in floating condition i.e., not connected to ground.
- The input is applied to non-inverting end and the feedback voltage across  $R_1$  drives the inverting input end.
- The feedback voltage across  $R_1$  depends on the output current  $i_o$  and it is in series with the input difference voltage  $V_{id}$ .
- Due to the concept of virtual ground, the voltage at node A will be  $V_{in}$ .

Thus,  $i_o = V_{in}/R_1$   
i.e., an input voltage  $V_{in}$  is converted into an output current of  $V_{in}/R_1$ .

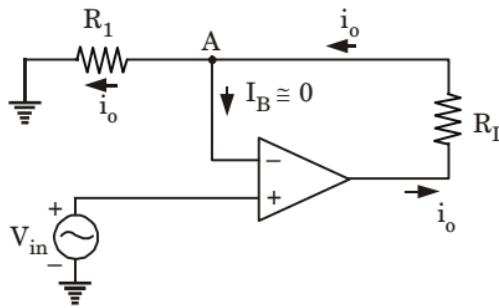


Fig. 20.

5. Attempt any **one** question :  $(7 \times 1 = 7)$

- a. Give CMOS implementation of a clocked SR flip-flop and explain its working.

**Ans.**

### A. CMOS Implementation :

- A simpler implementation of a clocked SR flip-flop is shown in Fig. 21. Here, pass transistor logic is employed to implement the clocked set-reset function.

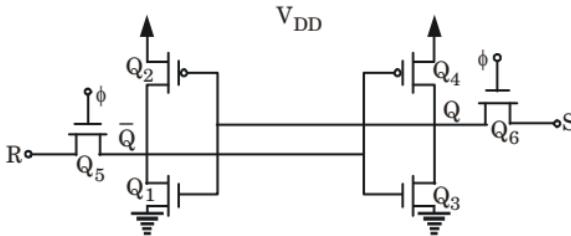


Fig. 21.

- The SR flip-flop comprising two cross-coupled inverters and two pass transistors  $Q_5$  and  $Q_6$ . The pass transistors are turned ON when the clock ( $\phi$ ) is high, and they connect the flip-flop input  $S$  and  $R$ . The pass transistors act as transmission gates allowing the inputs  $S$  and  $R$ .

### B. Operation :

- Consider the flip-flop output has the initial state  $Q = 1$  and  $\bar{Q} = 0$ , and the input  $R = 1$  and  $S = 0$  is applied to the input of flip-flop.
- When the clock  $\phi$  is high, the transistors  $Q_5$  and  $Q_6$  are turned ON.
- For this input  $R = 1$  and  $S = 0$ , the transistor  $Q_3$  is turned ON and pull down the output  $Q = 0$ .
- These output  $Q$  is applied to the input of  $Q_2$  and  $Q_1$  transistors, this will make the transistor  $Q_2$  is turned ON and the output  $\bar{Q}$  becomes high.
- Now consider the output has initial state  $Q = 0$  and  $\bar{Q} = 1$ , and the input  $R = 0$  and  $S = 1$ . When the clock  $\phi$  is high, the pass transistors  $Q_5$  and  $Q_6$  are turned ON. For this input  $R = 0$  and  $S = 1$ , the transistor  $Q_1$  turned ON and  $Q_2$  is turned OFF.
- This causes the output  $\bar{Q} = 0$  and  $\bar{Q}$  is applied to the input of transistors  $Q_3$  and  $Q_4$ . Now the transistor  $Q_4$  turned ON and this make the output  $Q$  is high.

### b. Derive the formula for $V_{IL}$ and $V_{IH}$ of CMOS inverter.

**Ans.**

#### A. Derivation of $V_{IL}$ :

- By definition, the slope of the VTC is equal to  $(-1)$ , i.e.,  $dV_{out}/dV_{in} = -1$  when the input voltage is  $V_{in} = V_{IL}$ .
- Note that in this case, the NMOS transistor operates in saturation while the PMOS transistor operates in the linear region.
- From  $I_{D,N} = I_{D,P}$ , we obtain the following current equation :

$$\frac{k_n}{2} (V_{GS,N} - V_{T0,N})^2 = \frac{k_p}{2} [2(V_{GS,P} - V_{T0,P})V_{DS,P} - V_{DS,P}^2] \quad \dots(1)$$

$$\frac{k_n}{2} (V_{in} - V_{T0,N})^2 = \frac{k_p}{2} [2(V_{in} - V_{DD} - V_{T0,P})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2] \quad \dots(2)$$

4. To satisfy the derivative condition at  $V_{IL}$ , we differentiate both sides of eq. (2) with respect to  $V_{in}$ .

$$k_n (V_{in} - V_{T0,N}) = k_p \left[ (V_{in} - V_{DD} - V_{T0,P}) \left( \frac{dV_{out}}{dV_{in}} \right) + (V_{out} - V_{DD}) \left( \frac{dV_{out}}{dV_{in}} \right) \right] \quad \dots(3)$$

5. Substituting  $V_{in} = V_{IL}$  and  $(dV_{out}/dV_{in}) = -1$  in eq. (3), we obtain

$$k_n (V_{IL} - V_{T0,N}) = k_p (2V_{out} - V_{IL} + V_{T0,P} - V_{DD}) \quad \dots(4)$$

6. The critical voltage  $V_{IL}$  can now be found as a function of the output voltage  $V_{out}$ , as follows :

$$V_{IL} = \frac{2V_{out} + V_{T0,P} - V_{DD} + k_R V_{T0,N}}{1 + k_R} \quad \dots(5)$$

where  $k_R$  is defined as,

$$k_R = \frac{k_n}{k_p}$$

### B. Derivation of $V_{IH}$ :

1. When the input is equal to  $V_{IH}$ , the NMOS transistor operates in the linear region and the PMOS transistor operates in saturation.
2. From  $I_{D,N} = I_{D,P}$

$$\frac{k_n}{2} [2(V_{GS,N} - V_{T0,N})V_{DS,N} - V_{DS,N}^2] = \frac{k_p}{2} (V_{GS,P} - V_{T0,P})^2 \quad \dots(6)$$

$$\frac{k_n}{2} [2(V_{in} - V_{T0,N})V_{out} - V_{out}^2] = \frac{k_p}{2} (V_{in} - V_{DD} - V_{T0,P})^2 \quad \dots(7)$$

3. Now, differentiate both sides of eq. (7) with respect to  $V_{in}$ .

$$k_n \left[ (V_{in} - V_{T0,N}) \left( \frac{dV_{out}}{dV_{in}} \right) + V_{out} - V_{out} \left( \frac{dV_{out}}{dV_{in}} \right) \right] = k_p (V_{in} - V_{DD} - V_{T0,P}) \quad \dots(8)$$

4. Substituting  $V_{in} = V_{IH}$  and  $(dV_{out}/dV_{in}) = -1$  in eq. (8), we obtain

$$k_n (-V_{IH} + V_{T0,N} + 2V_{out}) = k_p (V_{IH} - V_{DD} - V_{T0,P}) \quad \dots(9)$$

5. The critical voltage  $V_{IH}$  can now be found as a function of  $V_{out}$  as follows :

$$V_{IH} = \frac{V_{DD} + V_{T0,P} + k_R (2V_{out} + V_{T0,N})}{1 + k_R} \quad \dots(10)$$

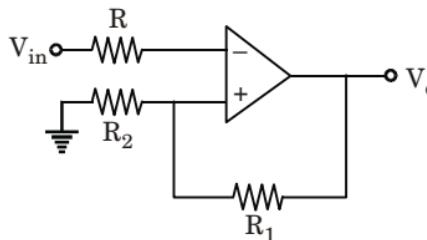
6. Attempt any one question : (7 × 1 = 7)

- i. **Describe the Schmitt trigger with help of proper circuit diagram and transfer characteristics.**
- ii. **Explain the working of peak detectors.**

**Ans.**

i. **Schmitt trigger and its transfer characteristics :**

- If positive feedback is added to the comparator circuit, gain can be increased greatly. This circuit is called Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback.



**Fig. 22.**

- Schmitt trigger also exhibits the phenomenon of hysteresis. The input voltage is applied to the (-ve) input terminal and feedback voltage to the (+ve) input terminal.
- Input voltage  $V_{in}$  triggers output  $V_o$ , every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage ( $V_{UT}$ ) and lower threshold voltage ( $V_{LT}$ ).
- Now, suppose the output  $V_o = +V_{sat}$ . The voltage at (+) input terminal will be

$$V_{UT} = \frac{R_2}{R_1 + R_2} (+V_{sat}) \quad \dots(1)$$

This voltage is upper threshold voltage. As long as  $V_{in}$  is less than  $V_{UT}$ , the output  $V_o$  remains constant at  $+V_{sat}$ .

- When  $V_{in}$  is just greater than  $V_{UT}$ , the output then switches to  $-V_{sat}$  and remains at this level as long as  $V_{in} > V_{UT}$ .
- For  $V_o = -V_{sat}$ , the voltage at (+ve) input terminal will be

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{sat}) \quad \dots(2)$$

This voltage is called lower threshold voltage.

- The output voltage is  $-V_{sat}$  as long as  $V_{in}$  is above or positive with respect to  $V_{LT}$ . The output voltage  $V_o$  changes to  $+V_{sat}$  if  $V_{in}$  goes more negative than or below  $V_{LT}$ . Resistor  $R$  is shown as  $R_1 \parallel R_2$  to compensate for input bias current,
- Input and output voltage waveforms are shown in Fig. 23.

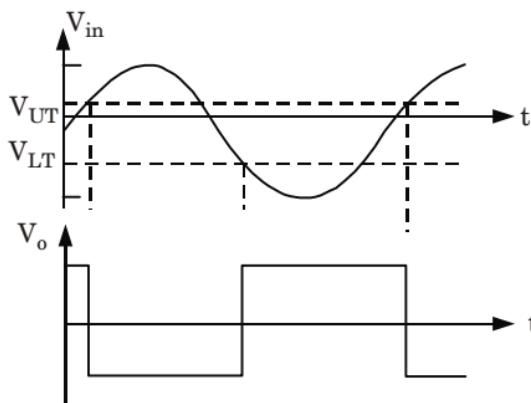


Fig. 23.

**9. Hysteresis curve (Transfer characteristics) :**

- From eq. (1) and (2),

$$V_{UT} > V_{LT}$$

$$\therefore V_{UT} - V_{LT} = \frac{2R_2}{R_1 + R_2} V_{sat}$$

This difference is called hysteresis width.

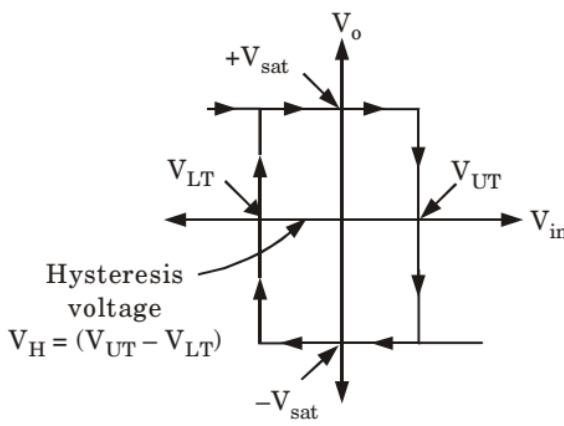


Fig. 24.

- $V_H$  is also called dead band because change in  $V_{in}$  do not change the output voltage. That is when the input exceeds  $V_{UT}$ , out switches from  $+V_{sat}$  to  $-V_{sat}$  and reverts back to its original state,  $+V_{sat}$ , when the input goes below  $V_{LT}$ .

- Uses :** Schmitt trigger is used to convert any wave into a square wave.

**ii. Working of peak detector :**

- Fig. 25 shows a peak detector that measures the positive peak values of square wave input.
- For positive half-cycle of  $V_{in}$ , the diode  $D_1$  conducts and charge capacitor  $C$  to positive peak value  $V_p$  of the input  $V_{in}$ , i.e. the Op-Amp acts as a voltage follower.

3. During negative half cycle of  $V_{in}$ , diode  $D_1$  is reversed biased and open-circuit. Here voltage across  $C$  is retained.
4. For proper operation of the circuit, the charging time constant ( $CR_d$ ) and discharging time constant ( $CR_L$ ) must satisfy,

$$CR_d \leq T / 10$$

Here,

$R_d$  = Resistance of forward bias diode

$T$  = Time period of input waveform

and,

$$CR_L \geq 10T$$

Here,  $R_L$  is load resistor.

5. If  $R_L$  is very small, then use of buffer is needed between  $C$  and  $R_L$ .

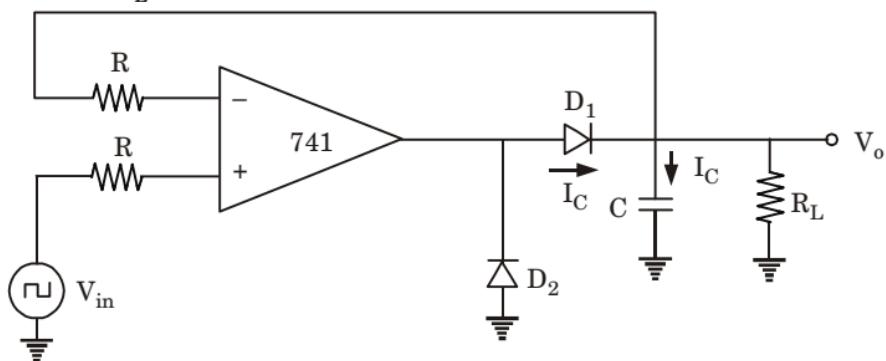


Fig. 25.

6. Resistance  $R$  is used to protect the Op-Amp against the excessive discharge currents, when power supply is switched OFF.  $D_2$  conducts during negative half cycle to prevent Op-Amp from going into negative saturation and helps to reduce recovery time of Op-Amp.
7. The input and output waveforms is shown in Fig. 26.

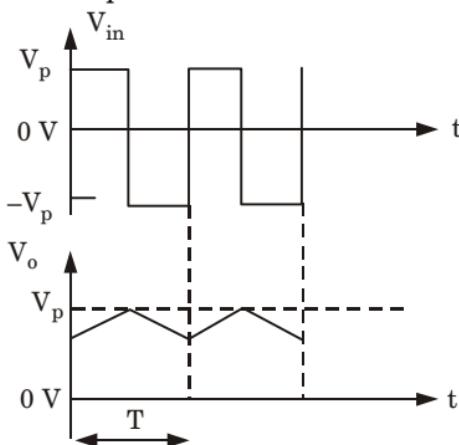
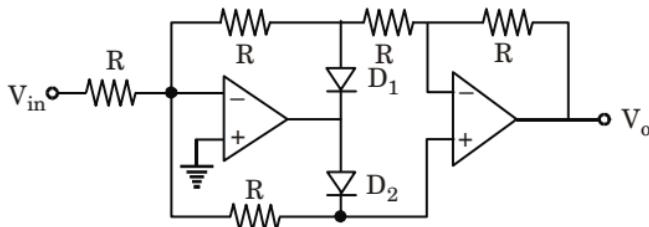


Fig. 26.

- b. Draw the circuit diagram of full wave precision rectifier and find expression for output voltage for both positive and negative half cycle of input sinusoidal waveform.

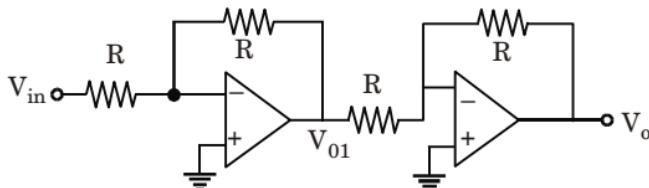
**Ans.**

1. For positive half cycle of  $V_{in}$ , diode  $D_1$  will be ON and  $D_2$  will be OFF. Both the Op-Amps will act like inverter and thus,  $V_o$  will follow the input  $V_{in}$ . From Fig. 27.

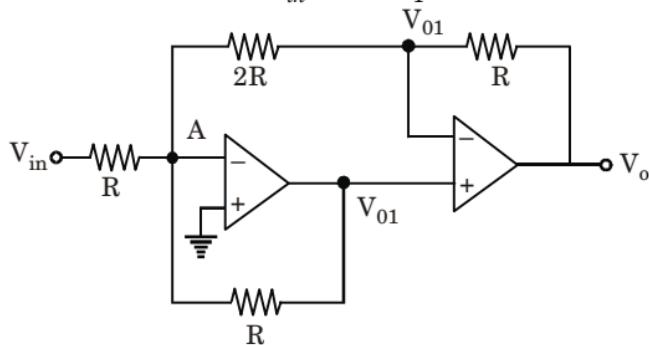
**Fig. 27.**

$$\text{Hence, } V_{01} = \frac{-R}{R} V_{in} = -V_{in}$$

$$\text{and } V_o = \frac{-R}{R} (-V_{in}) = V_{in}$$

**Fig. 28.**

2. In negative half cycle of  $V_{in}$ , diode  $D_1$  will be OFF and  $D_2$  will be ON.

**Fig. 29.**

- i. Applying KCL at node A,

$$\frac{V_A - V_{in}}{R} + \frac{V_A - V_{01}}{R} + \frac{V_A - V_{01}}{2R} = 0$$

- ii. Now,  $V_A = 0$

[Virtual ground concept]

$$-\frac{V_{in}}{R} - \frac{V_{01}}{R} - \frac{V_{01}}{2R} = 0$$

$$V_{in} = -\frac{3}{2} V_{01}$$

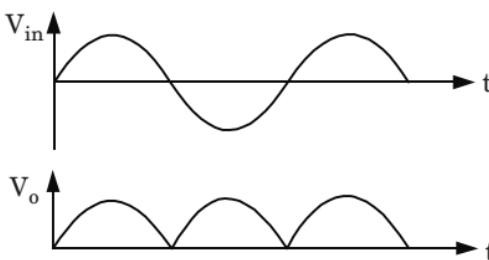
$$V_{01} = -\frac{2}{3}V_{in}$$

iii. Also,  $V_o = \left(1 + \frac{R}{2R}\right)V_{01} = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3}V_{in}\right)$

$$V_o = -V_{in}$$

Hence, for  $V_{in} < 0$ ,

$$V_o = V_{in}$$



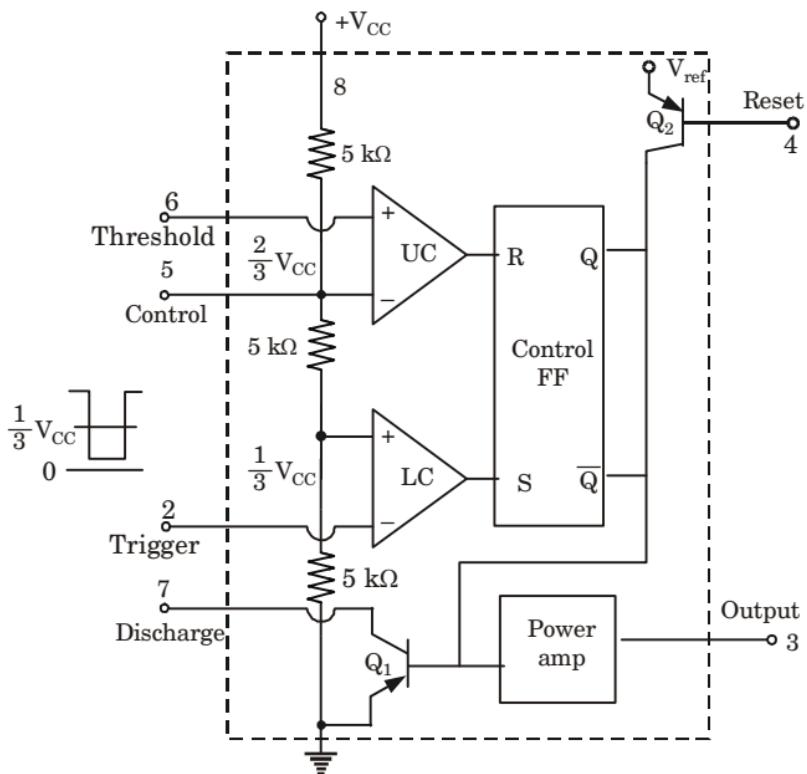
**Fig. 30.**

7. Attempt any **one** question :  $(7 \times 1 = 7)$
- Draw the functional block diagram of IC 555 and explain its working. Draw the circuit diagram of a monostable multivibrator using 555 and find expression for quasi state period.**

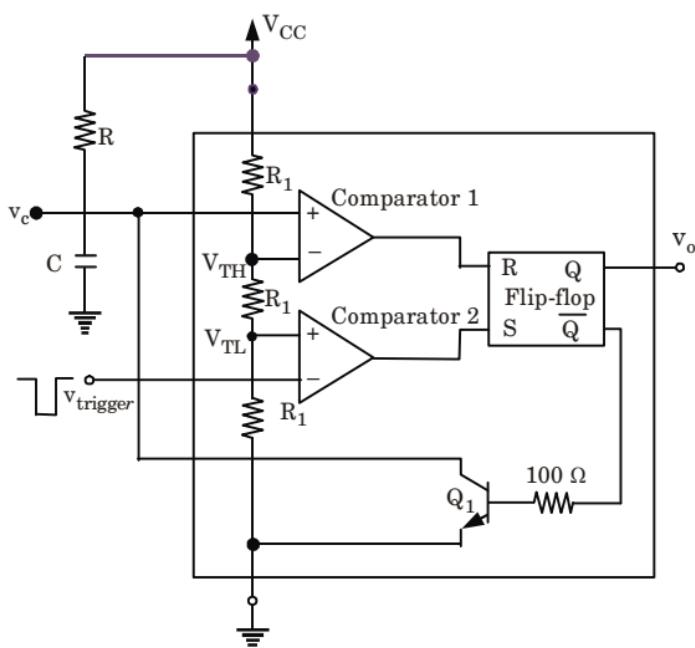
**Ans.**

**A. Functional block diagram of IC 555 and its working :**

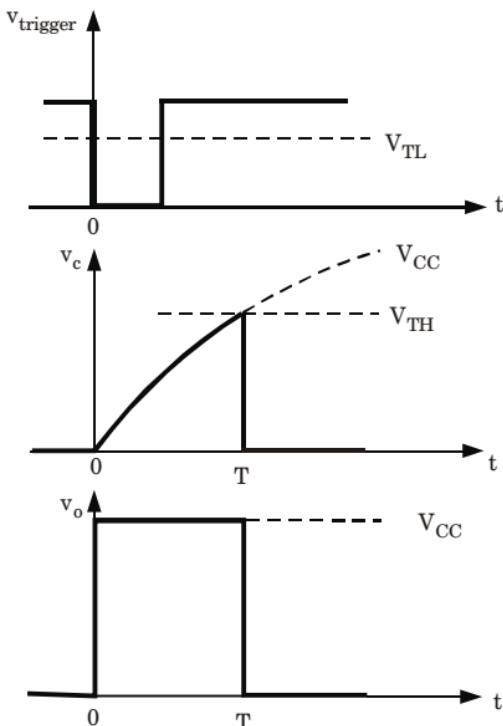
- In the stable state, the output  $\bar{Q}$  of the flip-flop (FF) is high. This makes the output low because of power amplifier which is basically an inverter.
- If negative going trigger pulse is applied to pin 2 and should have its DC level greater than the threshold level of the lower comparator (*i.e.*,  $V_{CC}/3$ ), now the trigger passes through ( $V_{CC}/3$ ), the output of the lower comparator goes high and sets the FF ( $Q = 1, \bar{Q} = 0$ ). Therefore the output of IC 555 becomes high.
- When the threshold voltage at pin 6 passes through  $(2/3)V_{CC}$ , the output of the upper comparator goes high and resets the FF ( $Q = 0, \bar{Q} = 1$ ).
- The reset input (pin 4) is used to reset the FF and the flip flop output  $\bar{Q}$  becomes high and the output of IC 555 becomes low because the output of FF is 1.

**Fig. 31.****B. Monostable multivibrator using IC 555 :**

1. Fig. 32 shows a monostable multivibrator implemented using the 555 IC together with an external resistor  $R$  and an external capacitor  $C$ .
2. In the stable state the flip-flop will be in the reset state, and thus its  $\bar{Q}$  output will be high, turning ON transistor  $Q_1$ , transistor  $Q_1$  will be saturated, and thus  $v_c$  will be close to 0 V, resulting in a low level at the output of comparator 1.
3. The voltage at the trigger input terminal, labeled  $v_{\text{trigger}}$  is kept high (greater than  $V_{TL}$ ), and thus the output comparator 2 also will be low.
4. Since the flip-flop in the reset state,  $Q$  will be low and thus  $v_o$  will be closed to 0 V.
5. To trigger the monostable multivibrator, a negative input pulse is applied to the trigger input terminal. As  $v_{\text{trigger}}$  goes below  $V_{TL}$ , the output of comparator 2 goes high to level, thus setting the flip-flop. Output  $Q$  of the flip-flop goes high, and thus  $v_o$  goes high, and output  $\bar{Q}$  goes low, turning OFF transistor  $Q_1$ .

**Fig. 32.**

6. Capacitor  $C$  now begins to charge up through resistor  $R$ , and its voltage  $v_c$  rises exponentially toward  $V_{CC}$ , as shown in Fig. 33 the monostable multivibrator is now in its quasi-stable state.

**Fig. 33.**

7. This state prevails until  $v_c$  reaches the threshold of comparator 1,  $V_{TH}$ , at that time the output of comparator 1 goes high, resetting the flip-flop.
8. Output  $Q$  of the flip-flop now goes high and turns ON transistor  $Q_1$ .
9. In turn, transistor  $Q_1$  rapidly discharges capacitor  $C$ , causing  $v_c$  to go to 0 V. Also, when the flip-flop resets its  $Q$ , output goes low and thus  $v_o$  goes back to 0 V. The monostable multivibrator is now back in its stable state and is ready to receive a new triggering pulse.
10. The width of the pulse,  $T$ , is the time interval that the monostable multivibrator spends in the quasi-stable state; it can be determined by reference to the waveforms in Fig. 33 at which the trigger pulse is applied as  $t = 0$ , the exponential waveform of  $v_c$  can be expressed as

$$v_c = V_{CC}(1 - e^{-t/CR})$$

Substituting  $v_c = V_{TH} = \frac{2}{3}V_{CC}$  at  $t = T$

$$T = RC \ln 3 \approx 1.1 RC$$

where,  $T$  = Time delay

**b. i. Write a short note on analog to digital converter.**

**ii. Explain the working of PLL with suitable block diagram.**

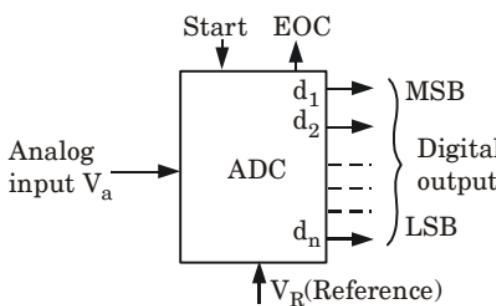
**Ans.**

**i. Analog to digital converter :**

1. The block schematic of ADC in Fig. 34, provides the function just opposite to that of a DAC.
2. It accepts an analog input  $V_a$  and produces an output binary word  $d_1, d_2, \dots, d_n$  of functional value  $D$ , so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n} \quad \dots(1)$$

where  $d_1$  is the most significant bit and  $d_n$  is the least significant bit.



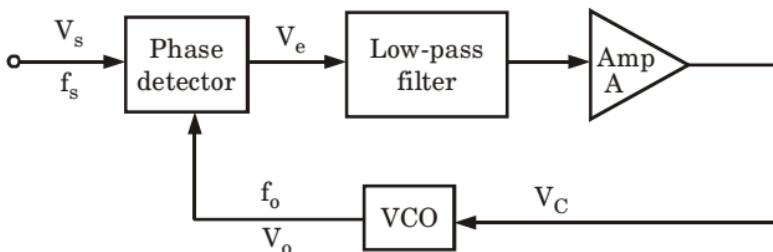
**Fig. 34.** Functional diagram of ADC.

3. An ADC usually has two additional control lines, the Start input to ADC when to start the conversion and the EOC (end of conversion) output to announce when the conversion is completed.

4. Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

### ii. PLL :

1. The two inputs of the phase detector or comparator are the input voltage  $V_s$  at frequency  $f_s$  and the feedback voltage from a voltage controlled oscillator (VCO) at frequency  $f_o$ .
2. The phase detector compares these two signals and produces a DC voltage  $V_e$  which is proportional to the phase difference between  $f_s$  and  $f_o$ .
3. The output voltage  $V_e$  of the phase detector is called as error voltage. This error voltage is then applied to low-pass filter.
4. Low-pass filter removes the high frequency noise present in the phase detector output and produces a ripple free DC level.
5. This DC level is amplified to an adequate level by the amplifier and applied to a VCO.
6. The DC amplifier output voltage is called as the control voltage  $V_C$ .



**Fig. 35.** Block diagram of PLL.

7. The control voltage  $V_C$  is applied at the input of a VCO. The output frequency of VCO is directly proportional to the DC control voltage  $V_C$ .
8. The VCO frequency  $f_o$  is compared with the input frequency  $f_s$  by the phase detector and it is adjusted continuously until it is equal to the input frequency  $f_s$  i.e.,  $f_o = f_s$ .
9. Once, the action of shifting VCO frequency in a direction to reduce the frequency difference between  $f_s$  and  $f_o$  starts, we say the signal is in the capture range.
10. When the output frequency is exactly the same as the input frequency, PLL is then said to be locked.
11. Once locked the output frequency  $f_o$  is identical to  $f_s$  except for a finite phase difference.
12. This phase difference generates a control voltage  $V_C$  to shift VCO frequency from  $f_o$  to  $f_s$  thereby maintaining the lock. Once locked, PLL tracks the frequency changes of the input signal.



**B. Tech.****(SEM. V) ODD SEMESTER THEORY  
EXAMINATION, 2019-20  
INTEGRATED CIRCUITS****Time : 3 Hours****Max. Marks : 70****Note :** Attempt all sections. If require any missing data; then choose suitably.**SECTION-A**

1. Attempt **all** the questions : **(2 × 7 = 14)**
- a. **What is a current mirror circuit ? Give its need.**
  - b. **What do you mean by DC analysis of a circuit ?**
  - c. **Describe the need of voltage limiter circuits.**
  - d. **Differentiate wide band and narrow band pass filter.**
  - e. **Draw the basic structure of CMOS inverter.**
  - f. **Differentiate between comparator and schmitt trigger.**
  - g. **The basic step of a 8-bit DAC is 20 mV. If 00000000 represents 0 V, what is represented by the input 10110111 ?**

**SECTION-B**

2. Attempt any **three** questions of the following : **(7 × 3 = 21)**
- a. **Find out the overall gain of an Op-Amp IC741 giving its cascaded equivalent circuit derived for its three stages. Also derive the relationship between  $f_T$  and slew rate for IC741.**
  - b. **Draw the generalized impedance converter and derive its impedance equation. Also simulate an inductor.**
  - c. **Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR-AND-INVERT (OAI) function using CMOS logic circuit.**
  - d. **What are precision rectifiers ? Describe the working of single Op-Amp based full wave precision rectifier.**

- e. Draw the block diagram of a PLL and explain its operation. Explain lock-in-range; capture range and pull-in time of a PLL. List the application of PLL.

### SECTION-C

3. Attempt any **one** part of the following :  $(7 \times 1 = 7)$
- Describe what is mean by output short circuit protection and explain how it is achieved in the output stage of IC741.
  - Discuss how the reference portion of the CM circuit can be designed with MOSFETs only.
4. Attempt any **one** part of the following :  $(7 \times 1 = 7)$
- Draw and explain narrow band-reject filter. Also, find its transfer function.
  - Derive the expression of voltage gain in KHN biquad filter. Draw the KHN biquad filter and drive transfer function of the BPF and LPF from that.
5. Attempt any **one** question :  $(7 \times 1 = 7)$
- Realize the circuit of 2 input NOR gate and 2 input NAND gate using CMOS and explain the operation.
  - Give CMOS implementation of a SR flip-flop and explain its working.
6. Attempt any **one** question :  $(7 \times 1 = 1)$
- What do you mean by the quadrant operation of multiplier ? Draw and explain a GILBERT analog multiplier.
  - Draw and explain the working of monostable multivibrator using Op-Amp.
7. Attempt any **one** question :  $(7 \times 1 = 7)$
- Explain the block diagram of IC 555. Derive the expression for time delay of a monostable multi-vibrator using 555.
  - Explain the operation R-2R Ladder D/A converter.  
**OR**  
Explain the operation of dual slope ADC.



## SOLUTION OF PAPER (2019-20)

**Note :** Attempt all sections. If require any missing data; then choose suitably.

### SECTION-A

1. Attempt **all** the questions : **(2 × 7 = 14)**

- a. **What is a current mirror circuit ? Give its need.**

**Ans.** **Current mirror circuit :** The circuit in which the output current is forced to equal the input current is called as current mirror circuit. In a current mirror circuit, the output current is the mirror image of input current.

**Need :**

Current mirror circuits are often used within integrated circuits as well as a number of other areas where they enable current to be balanced between two legs.

- b. **What do you mean by DC analysis of a circuit ?**

**Ans.**

1. DC operating point analysis calculates the behavior of a circuit when a DC voltage or current is applied to it.
2. The result of this analysis is generally referred as the bias point or quiescent point, Q-point.
3. In most cases, the results of the DC Operating point analysis are intermediate values for further analysis.

- c. **Describe the need of voltage limiter circuits.**

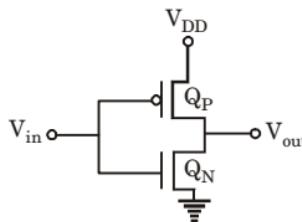
**Ans.** A voltage limiter is used to limit the voltage level. When a steady, reliable voltage is needed, then voltage limiter is the preferred device.

- d. **Differentiate wide band and narrow band pass filter.**

**Ans.**

S. No.	Wide band pass filter	Narrow band pass filter
1.	The wide band pass filter uses two Op-Amp.	The narrow band pass filter uses one Op-Amp.
2.	It has one feedback path.	It has two feedback path.
3.	The Op-Amp in the non-inverting configuration.	The Op-Amp in the inverting configuration.

- e. **Draw the basic structure of CMOS inverter.**

**Ans.****Fig. 1.** CMOS inverter circuit.**f. Differentiate between comparator and schmitt trigger.****Ans.**

S. No.	<b>Comparator</b>	<b>Schmitt trigger</b>
1.	The feedback is not used.	The feedback is used.
2.	The Op-Amp used is in open loop mode.	The Op-Amp used is in closed loop mode.
4.	A single reference voltage exists which acts as triggering voltage. i.e., $V_{ref}$ or $-V_{ref}$	The two different threshold voltages exist as $V_{UT}$ and $V_{LT}$ .
5.	The hysteresis does not exist.	Hysteresis exists with a width $H = V_{UT} - V_{LT}$ .

- g. The basic step of a 8-bit DAC is 20 mV. If 00000000 represents 0 V, what is represented by the input 10110111 ?**

**Ans.** The output voltage for input 10110111 is given by  
 $20 \text{ mV} (1 \times 2^7 + 0 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3$

$$\begin{aligned}
 &+ 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0) \\
 &= 20 \text{ mV} (128 + 32 + 16 + 4 + 2) \\
 &= 20 \times 182 = 3640 \text{ mV} = 3.64 \text{ V}
 \end{aligned}$$

**SECTION-B**

- 2. Attempt any three questions of the following : (7 × 3 = 21)**
- a. Find out the overall gain of an Op-Amp IC741 giving its cascaded equivalent circuit derived for its three stages. Also derive the relationship between  $f_T$  and slew rate for IC741.**

**Ans.**

- A. Overall gain of an Op-Amp IC-741 :**

The overall voltage gain  $A_v$  of the Op-Amp is the product of voltage gains of each stage as given by,

$$A_v = |A_d \parallel A_2 \parallel A_3|$$

where,  $A_d$  = Gain of differential amplifier stage

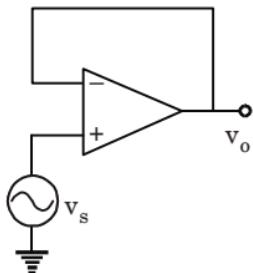
$A_2$  = Gain of the second stage

$A_3$  = Gain of the output stage

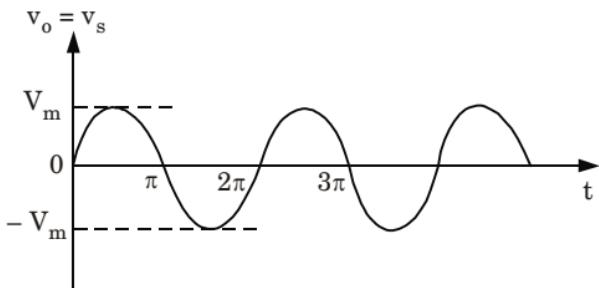
**B. Relationship between  $f_t$  and SR :**

- Consider a voltage follower shown in Fig. 2(a). The input is large amplitude, high frequency sine wave.
- If  $v_s = V_m \sin \omega t$   
Then, output  $v_o = V_m \sin \omega t$
- Fig. 2(b) shows the input-output waveform.
- The rate of change of the output is given by,

$$\frac{dv_o}{dt} = V_m \omega \cos \omega t$$



(a) Voltage follower



(b) Input/output waveform

**Fig. 2.**

- The maximum rate of change of the output occurs when  $\cos \omega t = 1$ .

That is,  $SR = \left. \frac{dv_o}{dt} \right|_{\max} = \omega V_m$

- Therefore, slew rate  $= 2\pi f V_m$  V/s

$$= \frac{2\pi f V_m}{10^6} \text{ V}/\mu\text{s}$$

where,  $f$  = Input frequency (Hz)

$V_m$  = Peak output amplitude.

- Draw the generalized impedance converter and derive its impedance equation. Also simulate an inductor.

**Ans.**

**A. General Impedance Converter (GIC) :**

- Generalized impedance converters (GICs) are Op-Amp circuits that employ  $RC$  networks for simulating frequency-dependent impedance elements such as inductors. Fig. 3 shows the circuit of a GIC.
- From Fig. 3, at node 1,

$$I_C = \frac{V_1 - V_2}{Z_1} = \frac{V_{CC} - V_{01}}{Z_1} \quad \dots(1)$$

where  $V_1 = V_{CC}$  and  $V_2 = V_{01}$ . Now, between nodes 2 and 4, we obtain (using KCL)

$$\frac{V_2 - V_3}{Z_2} = \frac{V_3 - V_4}{Z_3} \quad \dots(2)$$

3. From the Fig. 3, we observe that nodes 1 and 3 are virtually shorted, and hence using KCL

$$\frac{V_{01} - V_{CC}}{Z_2} = \frac{V_{CC} - V_{02}}{Z_3} \quad \dots(3)$$

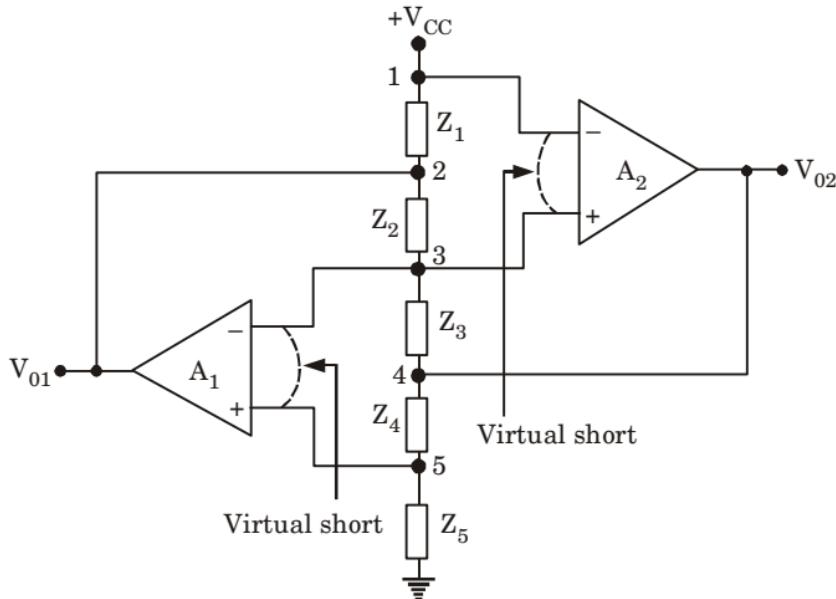
where  $V_{02} = V_4$ .

4. Rearranging eq. (3) yields

$$(Z_2 + Z_3) V_{CC} = V_{02} Z_2 + V_{01} Z_3 \quad \dots(4)$$

5. Now by using KCL between nodes 4 and 5, we have

$$\frac{V_{02} - V_5}{Z_4} = \frac{V_5}{Z_5} \quad \dots(5)$$



**Fig. 3.** Generalized impedance converter.

6. Substitution for  $V_5 = V_{CC}$  and rearrangements give

$$V_{02} = \frac{V_{CC}(Z_4 + Z_5)}{Z_5} \quad \dots(6)$$

7. Substituting for  $V_{02}$  from eq. (6) into eq. (4), we get

$$(Z_2 + Z_3) V_{CC} = \frac{V_{CC}(Z_4 + Z_5)}{Z_5} Z_2 + V_{01} Z_3 \quad \dots(7)$$

8. Rearranging eq. (7), we have

$$V_{CC} \left[ (Z_2 + Z_3) - \frac{(Z_4 + Z_5)}{Z_5} Z_2 \right] = V_{01} Z_3$$

$$V_{CC} \frac{[(Z_2 Z_5 + Z_3 Z_5) - (Z_4 Z_2 + Z_5 Z_2)]}{Z_3 Z_5} = V_{01}$$

$$\text{or, } V_{CC} \frac{Z_3 Z_5 - Z_4 Z_2}{Z_3 Z_5} = V_{01} \quad \dots(8)$$

9. Substituting for  $V_{01}$  from eq. (8) into eq. (1) and simplifying, we obtain

$$I_C Z_1 = V_{CC} \left[ \frac{Z_3 Z_5 - (Z_3 Z_5 - Z_4 Z_2)}{Z_3 Z_5} \right] \quad \dots(9)$$

10. Rearrangement of eq. (9) yields the input impedance of the circuit

$$Z = \frac{V_{CC}}{I_C} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \quad \dots(10)$$

11. Eq. (10) shows that the circuit shown in Fig. 3 can be used as grounded impedance whose nature and value depends on the nature and values of impedance elements  $Z_1$  to  $Z_5$ .

### B. Simulation of Inductor :

1. Fig. 4 shows the Antoniou inductance simulation circuit.

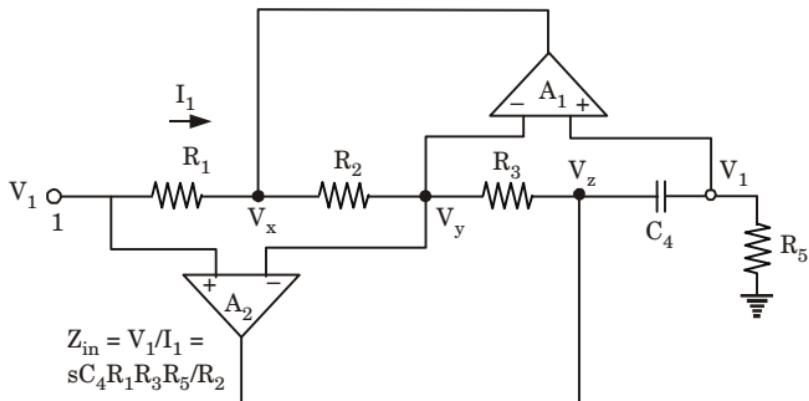


Fig. 4.

2. Applying KCL, we get

$$\frac{V_1 - V_z}{1/sC_4} + \frac{V_1}{R_5} = 0$$

$$V_z = V_1 \left[ 1 + \frac{1}{sC_4 R_5} \right]$$

3. Apply KCL, we get

$$\frac{V_y - V_x}{R_2} + \frac{V_y - V_z}{R_3} = 0 \quad \dots(1)$$

4. Substituting the value of  $V_z$  in eq. (1)

$$\frac{V_y - V_x}{R_2} + \frac{V_y - V_1 \left( 1 + \frac{1}{sC_4 R_5} \right)}{R_3} = 0$$

$$R_3(V_y - V_x) + R_2V_y - R_2V_1 \left(1 + \frac{1}{sC_4R_5}\right) = 0 \quad \dots(2)$$

5. Apply KCL, then we get

$$\begin{aligned} \frac{V_x - V_1}{R_1} + \frac{V_x - V_y}{R_2} &= 0 \\ R_2(V_x - V_1) + R_1(V_x - V_y) &= 0 \\ V_x(R_1 + R_2) &= R_2V_1 + R_1V_y \\ V_y &= \frac{V_x(R_1 + R_2)}{R_1} - \frac{R_2}{R_1}V_1 \end{aligned} \quad \dots(3)$$

6. Now put the value of  $V_y$  in eq. (2),

$$\text{then, } V_x = \left(V_1 + \frac{V_1R_2}{sC_4R_5R_3}\right)$$

7. Current across resistance  $R_1$ ,

$$I_1 = \left[V_1 - \left(V_1 + \frac{V_1R_2}{sC_4R_5R_3}\right)\right] \times \frac{1}{R_1}$$

$$I_1 = \frac{V_1R_2}{sC_4R_5R_3R_1}$$

8. Then input impedance

$$Z_{in} = \frac{V_1}{I_1} = \frac{sC_4R_1R_3R_5}{R_2}$$

which is that of an inductance  $L$  given by,

$$L = \frac{C_4R_1R_3R_5}{R_2}$$

9. If  $R_1 = R_2 = R_3 = R_5 = R$  and  $C_4 = C$   
then,  $L = CR^2$ .

c. Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR-AND-INVERT (OAI) function using CMOS logic circuit.

**Ans.**

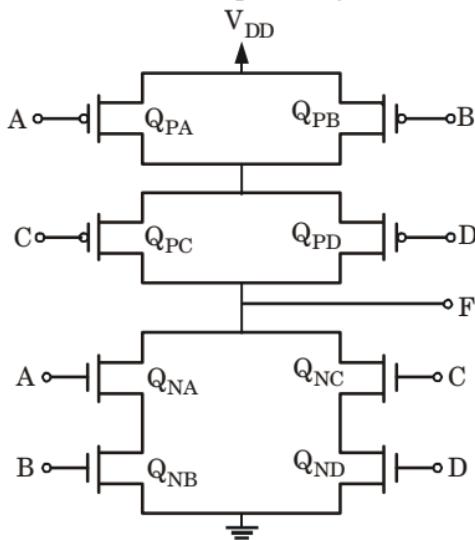
**A. Features of CMOS circuit :**

1. The output is always connected to  $V_{DD}$  or GND and in steady state; it gives full logic swing (between 0 V and  $V_{DD}$ ) voltage transfer characteristics and large noise margins.
2. Logic levels are not dependent upon the relative sizes of the devices.
3. There is no direct path between  $V_{DD}$  and GND in steady state. Thus, static power dissipation of CMOS circuit is negligible.
4. It has high input impedance and fast switching speed.

**B. AOI and OAI functions :**

1. AOI and OAI functions can be implemented with just one gate level transistor. Both the complex gates have a propagation delay equivalent to that of a single NAND or NOR gate.

2. AOI and OAI gates are essentially representations of SOP and POS expressions of functions respectively.



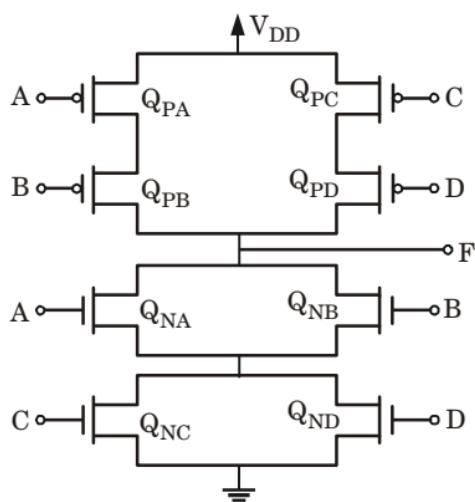
**Fig. 5.** AOI realisation using CMOS logic circuit.

3. Let us implement the function,  $F = \overline{AB + CD}$

Here,  $AB$  and  $CD$  are two AND functions and their sum is the OR function, which is finally inverted. Thus  $F$  can be implemented as an AOI gate.

4. Fig. 5 shows the CMOS realization of an AOI gate.  
 5. The CMOS realization of the OR-AND-INVERT (OAI) gate is the dual of that for the AND-OR-INVERT gate and is easily obtained by flipping the latter end-for-end while interchanging all NMOS circuits with PMOS circuits and vice versa, as shown in Fig. 6.

6. The output expression for OAI gate is,  $F = \overline{(A + B)(C + D)}$



**Fig. 6.** CMOS realisation of an OAI gate.

- d. What are precision rectifiers? Describe the working of single Op-Amp based full wave precision rectifier.

**Ans.**

- A. **Precision rectifier :** A circuit which can act as an ideal diode for rectifying voltages which are below the level of cut-in voltage of the diode are called precision rectifier circuit.
- B. **Full wave precision rectifier :**
- For positive half cycle of  $V_{in}$ , diode  $D_1$  will be ON and  $D_2$  will be OFF. Both the Op-Amps will act like inverter and thus,  $V_o$  will follow the input  $V_{in}$ . From Fig. 7,

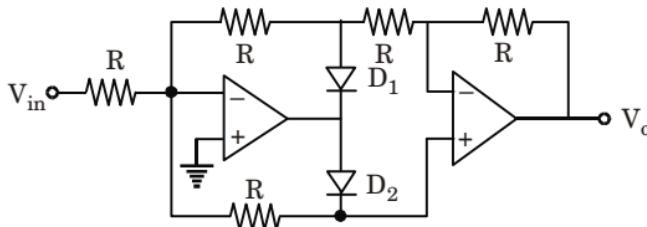


Fig. 7.

$$\text{Hence, } V_{01} = \frac{-R}{R} V_{in} = -V_{in}$$

$$\text{and } V_o = \frac{-R}{R} (-V_{in}) = V_{in}$$

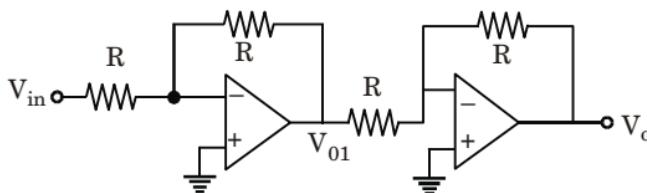


Fig. 8.

- In negative half cycle of  $V_{in}$ , diode  $D_1$  will be OFF and  $D_2$  will be ON.

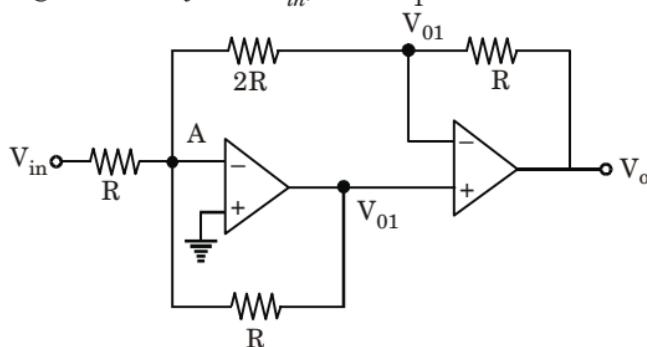


Fig. 9.

- Applying KCL at node  $A$ ,

$$\frac{V_A - V_{in}}{R} + \frac{V_A - V_{01}}{R} + \frac{V_A - V_{01}}{2R} = 0$$

- Now,  $V_A = 0$

[Virtual ground concept]

$$-\frac{V_{in}}{R} - \frac{V_{01}}{R} - \frac{V_{01}}{2R} = 0$$

$$V_{in} = -\frac{3}{2} V_{01}$$

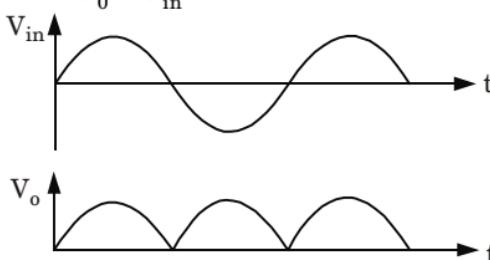
$$V_{01} = -\frac{2}{3} V_{in}$$

iii. Also,  $V_o = \left(1 + \frac{R}{2R}\right) V_{01} = \left(1 + \frac{R}{2R}\right) \left(-\frac{2}{3} V_{in}\right)$

$$V_o = -V_{in}$$

Hence, for  $V_{in} < 0$ ,

$$V_o = V_{in}$$



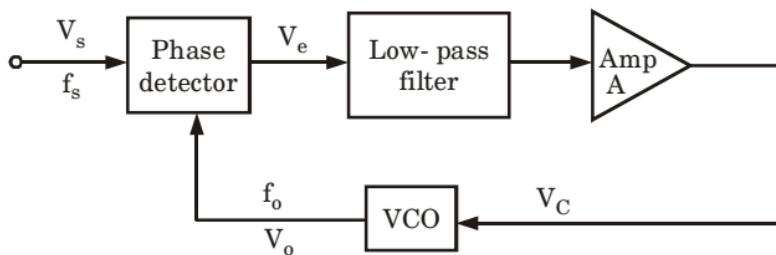
**Fig. 10.** Input and output waveforms of full wave rectifier.

- e. Draw the block diagram of a PLL and explain its operation. Explain lock-in-range; capture range and pull-in time of a PLL. List the application of PLL.

**Ans.**

**A. Principle of operation of PLL :**

1. The two inputs of the phase detector or comparator are the input voltage  $V_s$  at frequency  $f_s$  and the feedback voltage from a voltage controlled oscillator (VCO) at frequency  $f_o$ .
2. The phase detector compares these two signals and produces a DC voltage  $V_e$  which is proportional to the phase difference between  $f_s$  and  $f_o$ .
3. The output voltage  $V_e$  of the phase detector is called as error voltage. This error voltage is then applied to low-pass filter.
4. Low-pass filter removes the high frequency noise present in the phase detector output and produces a ripple free DC level.
5. This DC level is amplified to an adequate level by the amplifier and applied to a VCO.
6. The DC amplifier output voltage is called as the control voltage  $V_C$ .
7. The control voltage  $V_C$  is applied at the input of a VCO. The output frequency of VCO is directly proportional to the DC control voltage  $V_C$ .
8. The VCO frequency  $f_o$  is compared with the input frequency  $f_s$  by the phase detector and it is adjusted continuously until it is equal to the input frequency  $f_s$  i.e.,  $f_o = f_s$ .

**Fig. 11.** Block diagram of PLL.

9. Once, the action of shifting VCO frequency in a direction to reduce the frequency difference between  $f_s$  and  $f_o$  starts, we say the signal is in the capture range.
10. When the output frequency is exactly the same as the input frequency, PLL is then said to be locked.
11. Once locked the output frequency  $f_o$  is identical to  $f_s$  except for a finite phase difference.
12. This phase difference generates a control voltage  $V_C$  to shift VCO frequency from  $f_o$  to  $f_s$  thereby maintaining the lock. Once locked, PLL tracks the frequency changes of the input signal.

- B. Lock-in range :** Once the PLL is locked, it can track the frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called lock-in range or tracking range.
- C. Capture range :** The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range.
- D. Pull-in time :** The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the loop gain and loop filter characteristics.

**E. Applications :**

- |                          |                         |
|--------------------------|-------------------------|
| 1. Frequency divider     | 2. Frequency multiplier |
| 3. Frequency synthesizer | 4. AM detector          |
| 5. FM detector           | 6. FSK demodulator.     |

### SECTION-C

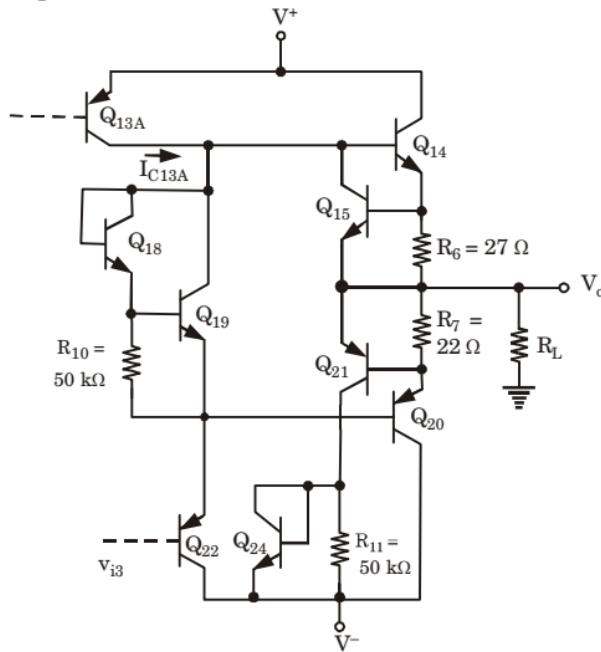
3. Attempt any **one** part of the following :  $(7 \times 1 = 7)$
- a. Describe what is mean by output short circuit protection and explain how it is achieved in the output stage of IC741.**

**Ans.**

1. The short-circuit protection circuitry is shown in the Fig. 12.
2. The Op-Amp 741 contains a number of transistors that are normally in the OFF state.
3. When the output terminal gets shorted to the ground, while keeping a positive output voltage due to certain input signal, this will induce a large current in the output transistor  $Q_{14}$ .
4. This will result in producing heat and cause burn-out of the transistor. Therefore, when current flow in  $Q_{14}$  reaches 20 mA,

voltage drop across  $R_6$  becomes  $27 \times 20 = 540$  mV, which bias the transistor  $Q_{15}$ .

5. Similarly, the maximum current in  $Q_{20}$  is limited by  $R_7$ ,  $Q_{21}$  and  $Q_{24}$ .
6. When the current increases, the voltage drop across  $R_7$  becomes sufficient and the transistor  $Q_{21}$  becomes ON and  $Q_{21}$  and  $Q_{24}$  shunt the excess current away from the transistor  $Q_{20}$ , hence protects the output transistor.

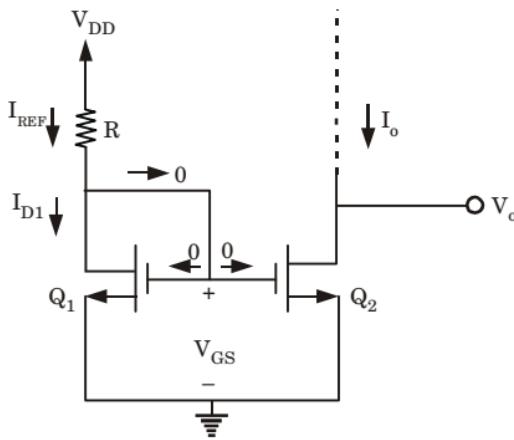


**Fig. 12.**

- b. Discuss how the reference portion of the CM circuit can be designed with MOSFETs only.

**Ans. Working of basic MOSFET current source :**

1. Fig. 13 shows the basic circuit diagram of MOSFET constant current source.



**Fig. 13.** MOSFET constant current source.

2. The circuit is driven by the transistor  $Q_1$ .  $Q_1$  is operating in saturation mode as the drain is shorted to its gate. The current equation is given as,

$$I_{D1} = \frac{1}{2} K'_n \left( \frac{W}{L} \right)_1 (V_{GS} - V_t)^2 \quad \dots(1)$$

3. Since the gate currents are zero,  $I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$

4. Similarly for  $Q_2$

$$I_0 = I_{D2} = \frac{1}{2} K'_n \left( \frac{W}{L} \right)_2 (V_{GS} - V_t)^2 \quad \dots(2)$$

5. From eq. (1) and (2)

$$\frac{I_0}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

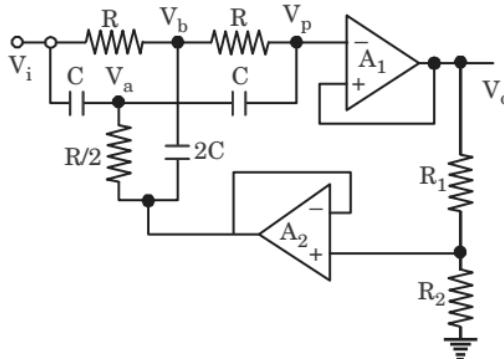
6. The connections of  $Q_1$  and  $Q_2$  provides the output current  $I_0$  in relation with  $I_{REF}$  by the aspect ratios of the transistors.

4. Attempt any one part of the following :  $(7 \times 1 = 7)$

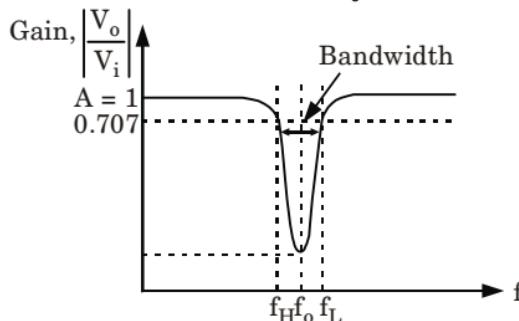
- a. Draw and explain narrow band-reject filter. Also, find its transfer function.

**Ans.**

1. The narrow band-reject filter, often called the notch filter, is the twin T network cascaded with the voltage follower as shown in Fig. 14(a).



(a) Circuit of a narrow band-reject (notch) filter



(b) Its frequency response.

Fig. 14.

2. Applying Kirchhoff's current law at node  $V_a$ , we get

$$(V_i - V_a)sC + (V_o - V_a)sC + (KV_o - V_a)2G = 0 \\ sCV_i + (sC + 2KG)V_0 = 2(sC + G)V_a \quad \dots(1)$$

where  $K = \frac{R_2}{(R_1 + R_2)}$  and  $G = \frac{1}{R}$

3. Applying Kirchhoff current law at node  $V_b$ , we get

$$(V_i - V_b)G + (V_o - V_b)G + 2(KV_o - V_b)sC = 0 \\ GV_i + (G + 2KsC)V_o = 2(G + sC)V_b \quad \dots(2)$$

At node  $V_p$ ,

$$(V_a - V_o)sC + (V_b - V_o)G = 0 \\ sCV_a + GV_b = (G + sC)V_o \quad \dots(3)$$

4. From the above three node voltage eq. (1), (2) and (3), the transfer function can be written as

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{G^2 + s^2 C^2}{G^2 + S^2 C^2 + 4(1-K)sCG} \\ = \frac{s^2 + \left(\frac{G}{C}\right)^2}{s^2 + \left(\frac{G}{C}\right)^2 + 4(1-K)s\left(\frac{G}{C}\right)}$$

5. In the steady-state, that is  $s = j\omega$ ,

$$H(j\omega) = \frac{\omega^2 - \omega_o^2}{\omega^2 - \omega_o^2 - j4(1-K)\omega\omega_o}$$

where  $\omega_o = \frac{G}{C} = \frac{1}{RC}$  or  $f_o = \frac{1}{2\pi RC}$

6. At 3 dB cut-off frequency,

$$|H| = \frac{1}{\sqrt{2}}$$

7. Therefore,  $\omega^2 - \omega_o^2 = \pm 4(1-K)\omega\omega_o$

$$\left(\frac{\omega}{\omega_o}\right)^2 \pm 4(1-K)\left(\frac{\omega}{\omega_o}\right) - 1 = 0$$

8. Upon solving the above quadratic equation, we obtain the upper and lower half power frequencies as,

$$f_H = f_o [\sqrt{1 + 4(1-K)^2} + 2(1-K)]$$

and  $f_L = f_o [\sqrt{1 + 4(1-K)^2} - 2(1-K)]$

9. The 3 dB bandwidth is

$$B = f_H - f_L = 4(1-K)f_o$$

$$Q = \frac{f_o}{B} = \frac{1}{4(1-K)}$$

- b. Derive the expression of voltage gain in KHN biquad filter. Draw the KHN biquad filter and drive transfer function of the BPF and LPF from that.**

**Ans.**

- The second order high-pass transfer function is

$$\frac{V_{hp}}{V_i} = \frac{Ks^2}{s^2 + s\left(\frac{\omega_o}{Q}\right) + \omega_o^2} = T_{hp} \quad \dots(1)$$

where  $K$  is high frequency gain

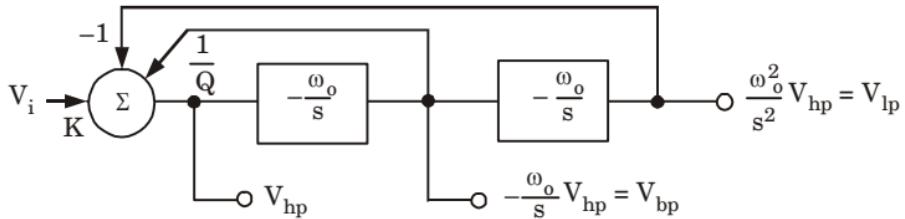
- Simplify eq. (1) and we get,

$$V_{hp} + \frac{1}{Q} \left( \frac{\omega_o}{s} V_{hp} \right) + \left( \frac{\omega_o^2}{s^2} V_{hp} \right) = KV_i \quad \dots(2)$$

- The signal  $(\omega_o/s) V_{hp}$  can be obtained by passing  $V_{hp}$  through an integrator with time constant equal to  $1/\omega_o$ .
- Passing resulting signal through another identical integrator results in the third signal involving  $V_{hp}$  in eq. (2) and rearranging eq. (2), we get

$$V_{hp} = KV_i - \frac{1}{Q} \frac{\omega_o}{s} V_{hp} - \frac{\omega_o^2}{s^2} V_{hp} \quad \dots(3)$$

- Biquad means the circuit is capable of realizing a biquadratic transfer function.
- Eq. (3) can be transfer to block diagram as shown in Fig. 15.



**Fig. 15.**

- The output of second integrator is labeled as  $V_{lp}$  while  $V_{bp}$  for first integrator.
- Bandpass filter transfer function is given by

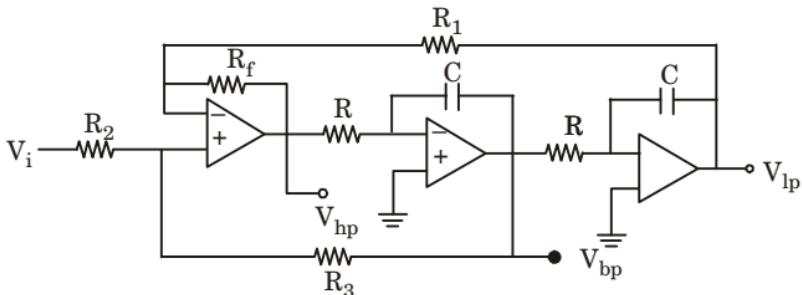
$$T_{bp} = \frac{\left(-\frac{\omega_0}{s}\right) V_{hp}}{V_i} \quad \dots(4)$$

- Using eq. (1),  $T_{bp} = \frac{-K\omega_0 s}{s^2 + s(\omega_0/Q) + \omega_0^2}$   $\dots(5)$

- Low-pass filter transfer function is given by (using eq. (1))

$$T_{lp} = \frac{\omega_o^2}{s^2} \frac{V_{hp}}{V_i} = \frac{K\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2} \quad \dots(6)$$

11. To obtain Op-Amp circuit in Fig. 16, we replace each integrator with Miller integrator circuit having  $CR = 1/\omega$ , also replace summer block with Op-Amp summing circuit.
12. The resulting circuit is known as Kerwin-Huelsman-Newcomb or KHN biquad as shown in Fig. 16.



**Fig. 16.** KHN biquad filter.

13. Select suitable values of  $C$  and  $R$  of integrator so  $CR = 1/\omega_L$ . For resistors, we use superposition to express the output of summer  $V_{hp}$  in terms of its inputs,

$$V_{bp} = -\left(\frac{\omega_o}{s}\right)V_{hp} \text{ and } V_{lp} = \left(\frac{\omega_o^2}{s^2}\right)V_{hp}$$

as,

$$V_{hp} = \frac{R_3}{R_2 + R_3} \left(1 + \frac{R_f}{R_1}\right) V_i + \frac{R_2}{R_2 + R_3} \left(1 + \frac{R_f}{R_1}\right) \left(-\frac{\omega_o}{s} V_{hp}\right) - \frac{R_f}{R_1} \left(\frac{\omega_o^2}{s^2} V_{hp}\right) \quad \dots(7)$$

14. Equating the last RHS term of eq. (3) and (7) gives

$$\frac{R_f}{R_1} = 1$$

15. Now equating second to last terms on RHS of eq. (3) and (4) and let  $R_1 = R_f$

$$\frac{R_3}{R_2} = 2Q - 1$$

16. Finally equating coefficients of  $V_i$  in eq. (3) and (7) and substituting  $R_f = R_1$  and  $R_2/R_3$

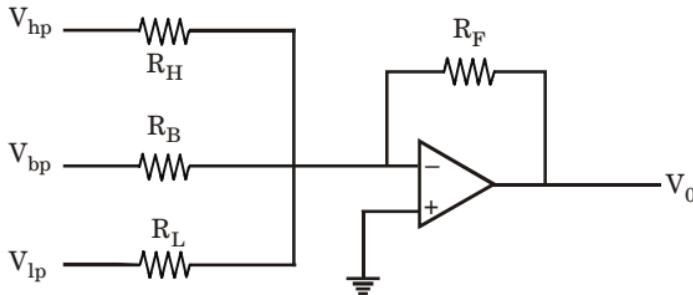
$$\text{Then, } K = 2 - \left(\frac{1}{Q}\right)$$

17. The KHN biquad can be used to realize notch and all-pass functions by summing weighted versions of the three outputs LP, BP, and HP. Such an Op-Amp summer is shown in Fig. 17.

18. From Fig. 17, we can write

$$V_0 = - \left( \frac{R_F}{R_H} V_{hp} + \frac{R_F}{R_B} V_{bp} + \frac{R_F}{R_L} V_{lp} \right) \quad \dots(8)$$

$$= - V_i \left( \frac{R_F}{R_H} T_{hp} + \frac{R_F}{R_B} T_{bp} + \frac{R_F}{R_L} T_{lp} \right)$$



**Fig. 17.** Notch and all pass filter using KHN filter.

19. Substituting for  $T_{hp}$ ,  $T_{bp}$ , and  $T_{lp}$  from eq. (1), (5) and (6) give the overall transfer function

$$\frac{V_0}{V_i} = -K \frac{(R_F / R_H)s^2 - s(R_F / R_B)\omega_0 + (R_F / R_L)\omega_0^2}{s^2 + s(\omega_0 / Q) + \omega_0^2}$$

20. To obtain notch function by selecting  $R_B = \infty$

$$\frac{R_H}{R_L} = \left( \frac{\omega_n}{\omega_0} \right)^2$$

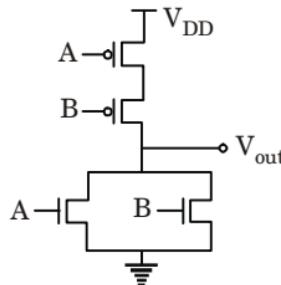
5. Attempt any **one** question : **(7 × 1 = 7)**

- a. **Realize the circuit of 2 input NOR gate and 2 input NAND gate using CMOS and explain the operation.**

**Ans.**

**A. 2 input NOR gate :**

Realization of 2 input NOR gate circuit is shown in Fig. 18.



**Fig. 18.**

**Operation :** The logic operation of NOR gate is such that the output is HIGH only when all inputs are LOW for remaining all other conditions, the output is LOW.

**B. 2 input NAND gate :**

Realization of 2 input NAND gate circuit is shown in Fig. 19.

**Operation :** A NAND gate produces a LOW output only when all the inputs are HIGH. When any of the inputs is LOW, the output will be HIGH.

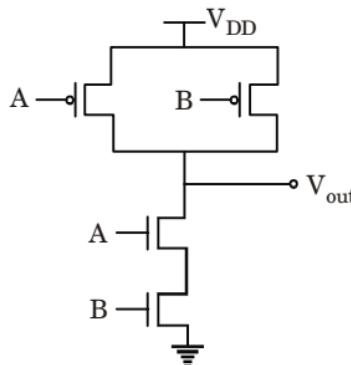


Fig. 19.

- Give CMOS implementation of a SR flip-flop and explain its working.

**Ans.**

#### A. CMOS Implementation :

- A simpler implementation of a clocked SR flip-flop is shown in Fig. 20. Here, pass transistor logic is employed to implement the clocked set-reset function.

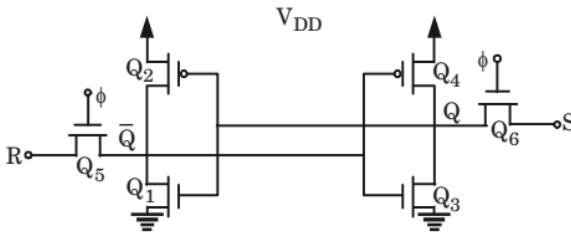


Fig. 20. A simpler CMOS implementation of the clocked SR flip-flop.

- The SR flip-flop comprising two cross-coupled inverters and two pass transistors  $Q_5$  and  $Q_6$ . The pass transistors are turned ON when the clock ( $f$ ) is high, and they connect the flip-flop input  $S$  and  $R$ . The pass transistors act as transmission gates allowing the inputs  $S$  and  $R$ .

#### B. Operation :

- Consider the flip-flop output has the initial state  $Q = 1$  and  $\bar{Q} = 0$ , and the input  $R = 1$  and  $S = 0$  is applied to the input of flip-flop.
- When the clock  $f$  is high, the transistors  $Q_5$  and  $Q_6$  are turned ON.
- For this input  $R = 1$  and  $S = 0$ , the transistor  $Q_3$  is turned ON and pull down the output  $Q = 0$ .
- These output  $Q$  is applied to the input of  $Q_2$  and  $Q_1$  transistors, this will make the transistor  $Q_2$  is turned ON and the output  $\bar{Q}$  becomes high.

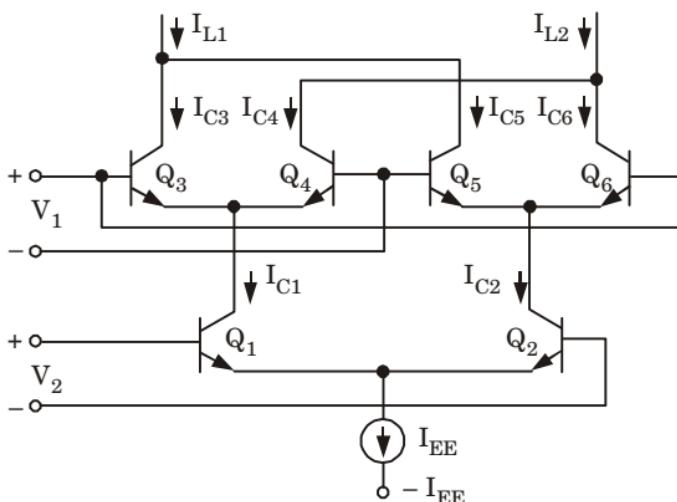
5. Now consider the output has initial state  $Q = 0$  and  $\bar{Q} = 1$ , and the input  $R = 0$  and  $S = 1$ . When the clock  $\phi$  is high, the pass transistors  $Q_5$  and  $Q_6$  are turned ON. For this input  $R = 0$  and  $S = 1$ , the transistor  $Q_1$  turned ON and  $Q_2$  is turned OFF.
  6. This causes the output  $\bar{Q} = 0$  and  $\bar{Q}$  is applied to the input of transistors  $Q_3$  and  $Q_4$ . Now the transistor  $Q_4$  turned ON and this make the output  $Q$  is high.
  6. Attempt any **one** question :  $(7 \times 1 = 1)$
- a. **What do you mean by the quadrant operation of multiplier ? Draw and explain a GILBERT analog multiplier.**

**Ans.****A. Quadrant operation of multiplier :**

1. The quadrant defines the applicability of the circuit for bipolar signals at its inputs.
2. First-quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four-quadrant device accepts two bipolar signals.

**B. GILBERT analog multiplier :**

1. The GILBERT multiplier cell is a modification of the emitter coupled cell and this allows four-quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced multipliers.
2. Two cross-coupled emitter-coupled pairs in series connection with an emitter coupled pair form the structure of the GILBERT multiplier cell.

**Fig. 21.** GILBERT multiplier cell.

3. The collector currents of  $Q_3$  and  $Q_4$  are given by

$$I_{C3} = \frac{I_{C1}}{1 + e^{-V_1/V_T}} \quad \dots(1)$$

$$\text{and } I_{C4} = \frac{I_{C1}}{1 + e^{V_1/V_T}} \quad \dots(2)$$

4. Similarly the collector currents of  $Q_5$  and  $Q_6$  are given by

$$I_{C5} = \frac{I_{C2}}{1 + e^{V_1/V_T}} \quad \dots(3)$$

$$\text{and } I_{C6} = \frac{I_{C2}}{1 + e^{-V_1/V_T}} \quad \dots(4)$$

5. The collector currents  $I_{C1}$  and  $I_{C2}$ , of transistors  $Q_1$  and  $Q_2$  can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_2/V_T}} \quad \dots(5)$$

$$\text{and } I_{C2} = \frac{I_{EE}}{1 + e^{V_2/V_T}} \quad \dots(6)$$

6. Substituting eq. (5) in eq. (1) and (2), we get

$$I_{C3} = \frac{I_{EE}}{[1 + e^{-V_1/V_T}][1 + e^{-V_2/V_T}]} \quad \dots(7)$$

$$\text{and } I_{C4} = \frac{I_{EE}}{[1 + e^{V_1/V_T}][1 + e^{-V_2/V_T}]} \quad \dots(8)$$

7. Similarly, substituting eq. (6) in eq. (3) and (4), we get

$$I_{C5} = \frac{I_{EE}}{[1 + e^{V_1/V_T}][1 + e^{V_2/V_T}]} \quad \dots(9)$$

$$\text{and } I_{C6} = \frac{I_{EE}}{[1 + e^{-V_1/V_T}][1 + e^{V_2/V_T}]} \quad \dots(10)$$

8. The differential output current  $\Delta I$  is given by

$$\Delta I = I_{L1} - I_{L2}$$

$$\text{That is, } \Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6})$$

$$\text{or } \Delta I = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5}) \quad \dots(11)$$

9. Substituting eq. (7) to (10) in eq. (11) and employing exponential formulae for hyperbolic functions, we get

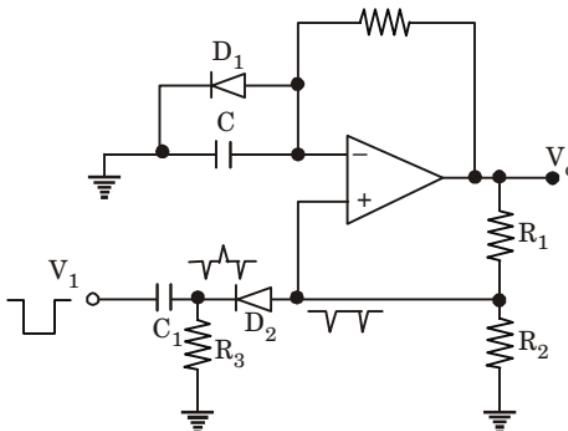
$$\Delta I = I_{EE} \left[ \tanh\left(\frac{V_1}{2V_T}\right) \tanh\left(\frac{V_2}{2V_T}\right) \right] \quad \dots(12)$$

eq. (12) shows that when  $V_1$  and  $V_2$  are small, the GILBERT cell shown in Fig. 21 can be used as a four-quadrant analog multiplier with the use of current-to-voltage converters.

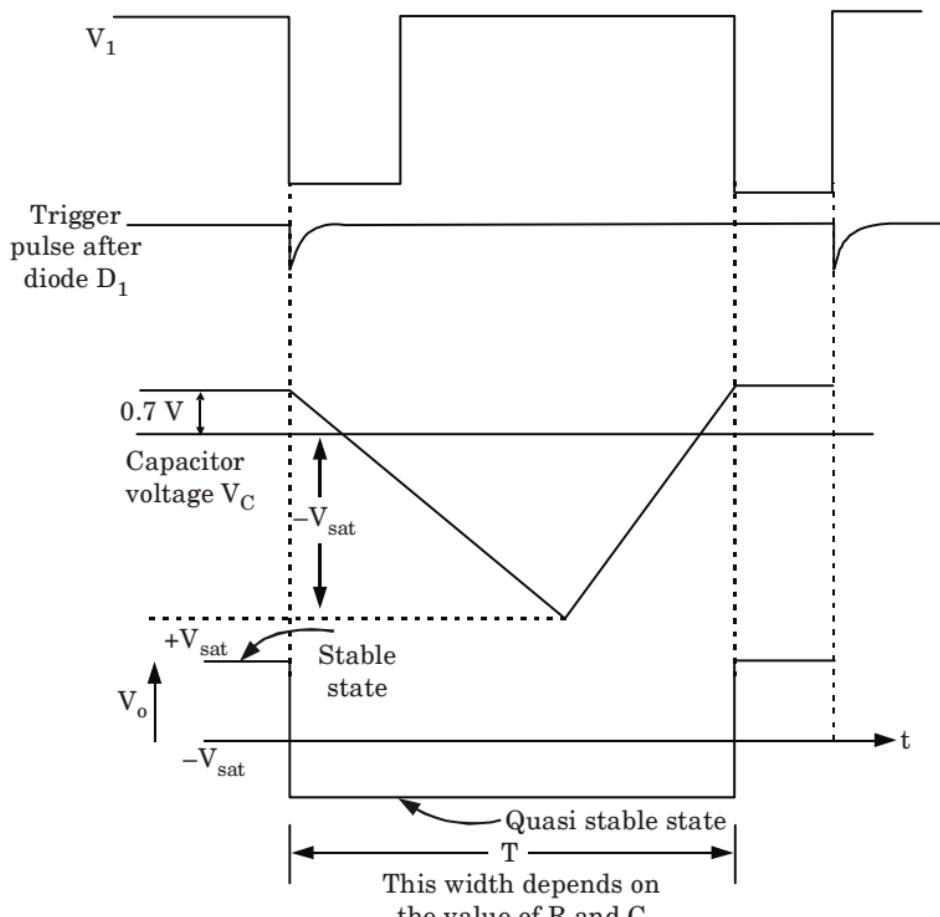
- b. Draw and explain the working of monostable multivibrator using Op-Amp.**

**Ans.**

- Fig. 22 shows the circuit diagram of monostable multivibrator. A diode  $D_1$  clamps the capacitor voltage to 0.7 V when the output is at  $+V_{sat}$ .
- The negative going pulse signal of magnitude  $V_1$  (triggering signal) passing through the differentiator  $R_3C_1$  and diode  $D_2$  produces a negative going triggering pulse and is applied to the (+) input terminal.

**Fig. 22.****Operation :**

- For monostable operation, the trigger pulse width  $T_p$  should be much less than  $T$ , the pulse width of the monostable multivibrator.
- The diode  $D_2$  is used to avoid malfunctioning by blocking the positive spikes that may be present at the differentiated trigger input.
- Fig. 23 shows the trigger and output waveform.
- When  $V_o$  is  $+V_{sat}$ , voltage divider  $R_1$  and  $R_2$  feedback  $V_{UT}$  to the (+ve) input. The diode  $D_1$  clamps the (-ve) input at approximately 0.7 V (because the diode is forward biased).
- The feedback voltage at (+ve) terminal is higher than (-ve) terminal therefore Op-Amp holds  $V_o$  at  $+V_{sat}$ . This output state is called as stable state.
- If the negative spike (trigger signal) is applied to (+ve) of Op-Amp which is higher than the voltage at (-ve) terminal. The combination of feedback voltage and negative trigger voltage will be pulled below the voltage at (-ve) input.
- Once the (+ve) input becomes negative with respect to the (-ve) input,  $V_o$  switches to  $-V_{sat}$ . With this change, the one-shot is now in its timing state. This state is an unstable state.
- Due to  $V_o = -V_{sat}$ , the diode  $D_1$  is reverse biased and the capacitor  $C$  charges, the (-ve) input becomes more and more negative with respect to ground. When the capacitor voltage is more than (+ve) terminal,  $V_o$  switches to  $+V_{sat}$ .



**Fig. 23.** Input and output waveform.

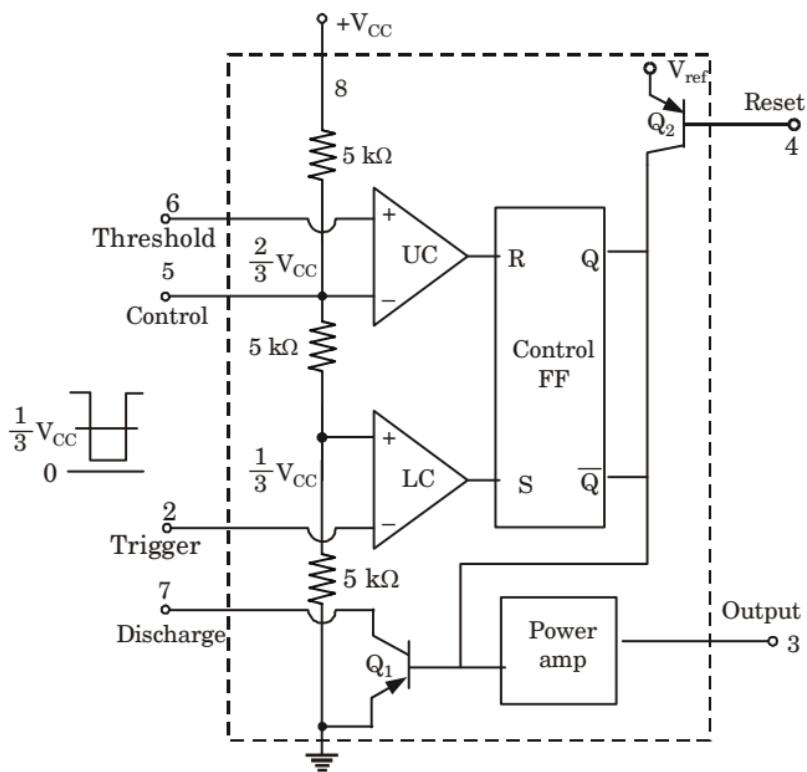
7. Attempt any **one** question :  $(7 \times 1 = 7)$
- Explain the block diagram of IC 555. Derive the expression for time delay of a monostable multi-vibrator using 555.**

**Ans.**

**A. Functional block diagram IC 555 :**

- In the stable state, the output  $\bar{Q}$  of the flip-flop (FF) is high. This makes the output low because of power amplifier which is basically an inverter.
- If negative going trigger pulse is applied to pin 2 and should have its DC level greater than the threshold level of the lower comparator (*i.e.*,  $V_{CC}/3$ ), now the trigger passes through ( $V_{CC}/3$ ), the output of the lower comparator goes high and sets the FF ( $Q = 1, \bar{Q} = 0$ ). Therefore the output of IC 555 becomes high.
- When the threshold voltage at pin 6 passes through  $(2/3) V_{CC}$ , the output of the upper comparator goes high and resets the FF ( $Q = 0, \bar{Q} = 1$ ).

4. The reset input (pin 4) is used to reset the FF and the flip flop output  $\bar{Q}$  becomes high and the output of IC 555 becomes low because the output of FF is 1.

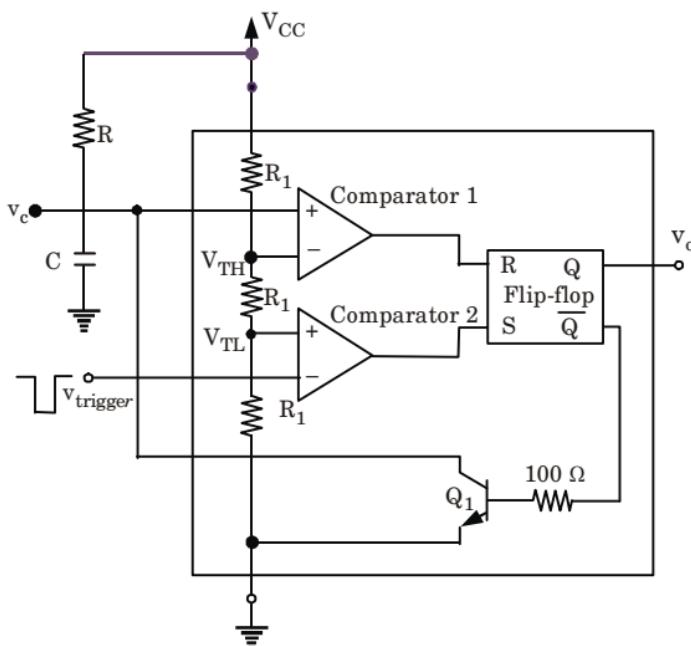


**Fig. 24.** Functional diagram of IC 555.

#### B. Derivation for time delay of monostable multivibrator :

- Fig. 25 shows a monostable multivibrator implemented using the 555 IC together with an external resistor  $R$  and an external capacitor  $C$ .
- In the stable state the flip-flop will be in the reset state, and thus its  $\bar{Q}$  output will be high, turning ON transistor  $Q_1$ , transistor  $Q_1$  will be saturated, and thus  $v_c$  will be close to 0 V, resulting in a low level at the output of comparator 1.
- The voltage at the trigger input terminal, labeled  $v_{trigger}$  is kept high (greater than  $V_{TL}$ ), and thus the output comparator 2 also will be low.
- Since the flip-flop in the reset state,  $Q$  will be low and thus  $v_o$  will be closed to 0 V.
- To trigger the monostable multivibrator, a negative input pulse is applied to the trigger input terminal. As  $v_{trigger}$  goes below  $V_{TL}$ , the output of comparator 2 goes high to level, thus setting the

flip-flop. Output  $Q$  of the flip-flop goes high, and thus  $v_o$  goes high, and output  $\bar{Q}$  goes low, turning OFF transistor  $Q_1$ .



**Fig. 25.** The 555 timer connected to implement a monostable multivibrator.

6. Capacitor  $C$  now begins to charge up through resistor  $R$ , and its voltage  $v_c$  rises exponentially toward  $V_{CC}$ , as shown in Fig. 26 the monostable multivibrator is now in its quasi-stable state.
7. This state prevails until  $v_c$  reaches the threshold of comparator 1,  $V_{TH}$ , at that time the output of comparator 1 goes high, resetting the flip-flop.
8. Output  $Q$  of the flip-flop now goes high and turns ON transistor  $Q_1$ .
9. In turn, transistor  $Q_1$  rapidly discharges capacitor  $C$ , causing  $v_c$  to go to 0 V. Also, when the flip-flop resets its  $Q$ , output goes low and thus  $v_o$  goes back to 0 V. The monostable multivibrator is now back in its stable state and is ready to receive a new triggering pulse.
10. The width of the pulse,  $T$ , is the time interval that the monostable multivibrator spends in the quasi-stable state; it can be determined by reference to the waveforms in Fig. 26 at which the trigger pulse is applied as  $t = 0$ , the exponential waveform of  $v_c$  can be expressed as

$$v_c = V_{CC}(1 - e^{-t/CR})$$

Substituting  $v_c = V_{TH} = \frac{2}{3}V_{CC}$  at  $t = T$

$$T = RC \ln 3 \approx 1.1 RC$$

where,  $T = \text{Time delay}$

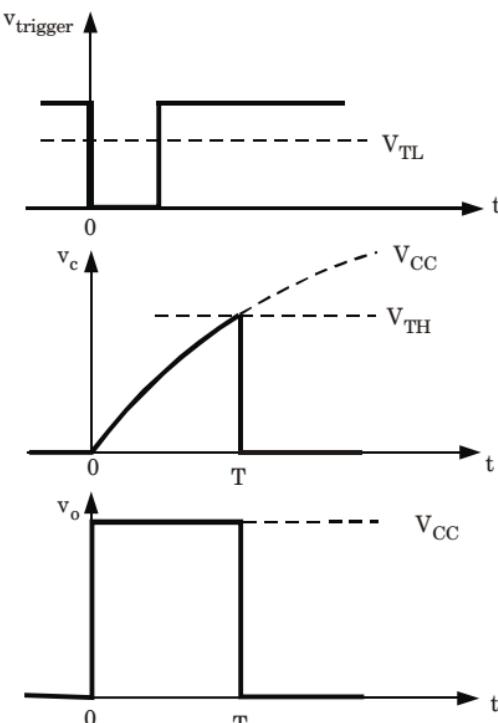


Fig. 26. Waveform of the circuit.

- b. Explain the operation **R-2R Ladder D/A converter**.  
OR

Explain the operation of dual slope ADC.

**Ans.**

**A. R-2R Ladder D/A converter :**

1. This network uses resistors of only two values  $R$  and  $2R$ . The inputs to the resistor network are applied through digitally controlled switches.

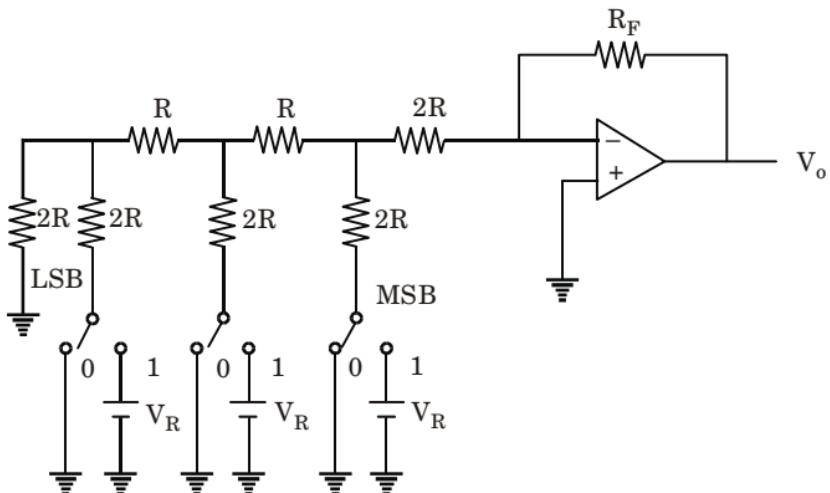
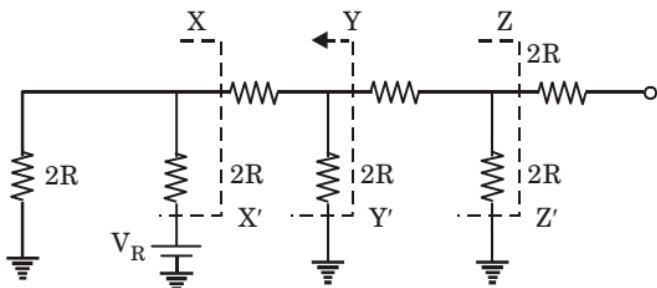
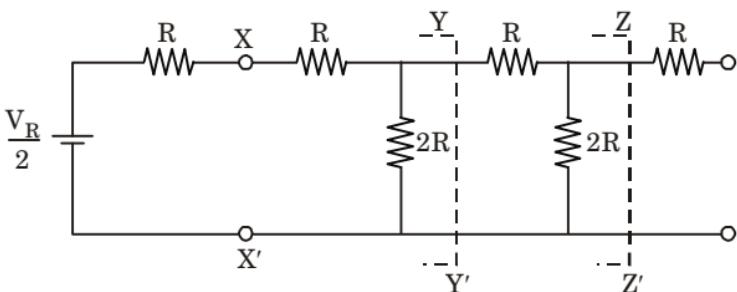


Fig. 27.

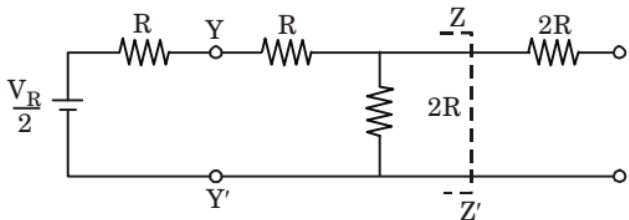
2. Consider a 3 bit  $R-2R$  Ladder D/A network. Let us assume a digital input of 001. The equivalent circuit becomes as shown in Fig. 28.

**Fig. 28.**

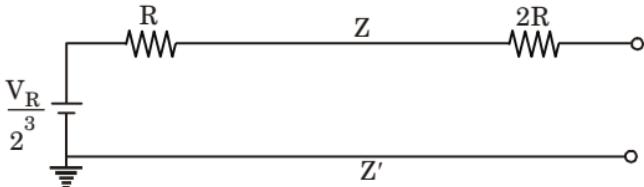
3. Applying Thevenin's theorem at point  $XX'$ , we get

**Fig. 29.**

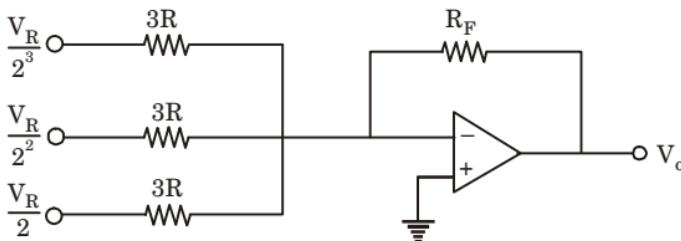
4. Applying Thevenin's theorem at  $YY'$ , we get

**Fig. 30.**

5. Applying Thevenin's theorem at  $ZZ'$ , we get

**Fig. 31.**

6. The equivalent resistance is  $3R$  in each case. The circuit reduces to



**Fig. 32.**

7. The output voltage is given as

$$V_o = -\left(\frac{R_f}{3R} \frac{V_R}{2^3} b_0 + \frac{R_f}{3R} \frac{V_R}{2^2} b_1 + \frac{R_f}{3R} \frac{V_R}{2^1} b_2\right) = -\frac{R_f}{3R} \frac{V_R}{2^3} [4b_2 + 2b_1 + b_0]$$

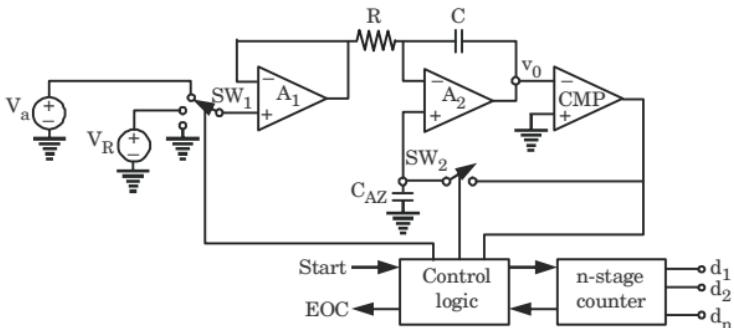
8. The number of resistors required for  $N$ -bit D/A converter is  $2N$  in the case of  $R$ - $2R$  ladder D/A converter.

#### B. Dual slope ADC :

1. Fig. 33(a) shows the dual slope ADC functional diagram. The circuit consists of a high input impedance buffer  $A_1$ , precision integrator  $A_2$  and a voltage comparator.
2. The converter first integrates the analog input signal  $V_a$  for a fixed duration of  $2^n$  clock periods as shown in Fig. 33(b).
3. Then it integrates an internal reference voltage  $V_R$  of opposite polarity until the integrator output is zero.
4. The number  $N$  of clock cycles required to return the integrator to zero is proportional to the value of  $V_a$  averaged over the integration period. Hence  $N$  represents the desired output code.

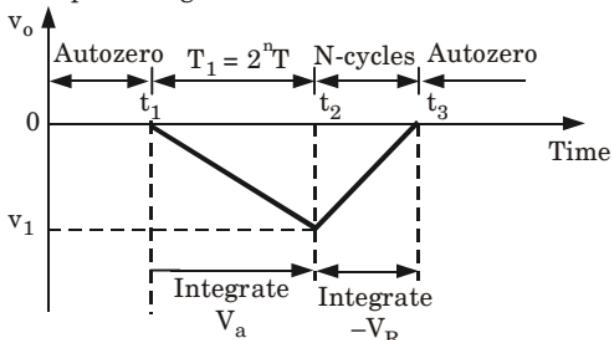
#### Operation :

1. Before the START command arrives, the switch  $SW_1$  is connected to ground and  $SW_2$  is closed.
2. Any offset voltage present in the  $A_1$ ,  $A_2$ , comparator loop after integration, appears across the capacitor  $C_{AZ}$  till the threshold of the comparator is achieved.
3. The capacitor  $C_{AZ}$  thus provides automatic compensation for the input-offset voltages of all the three amplifiers.
4. Later, when  $SW_2$  opens,  $C_{AZ}$  acts as a memory to hold the voltage required to keep the offset nulled.
5. At the arrival of the START command at  $t = t_1$ , the control logic opens  $SW_2$  and connects  $SW_1$  to  $V_a$  and enables the counter starting from zero.
6. The analog voltage  $V_a$  is integrated for a fixed number  $2^n$  counts of clock pulses after which the counter resets to zero.
7. If the clock period is  $T$ , the integration takes place for a time  $T_1 = 2^n \times T$  and the output is a ramp going downwards as shown in Fig. 33(b).



(a) Functional diagram of the dual slope ADC.

Integrator output voltage



(b) Integrated output waveform for the dual slope ADC.

Fig. 33.

8. The counter resets itself to zero at the end of the interval  $T_1$  and the switch  $SW_1$  is connected to the reference voltage ( $-V_R$ ).
9. The output voltage  $v_o$  will now have a positive slope. However, when  $v_o$  becomes just zero at time  $t = t_3$ , the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter.

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{Clock rate}} \text{ and } t_3 - t_2 = \frac{\text{Digital count } N}{\text{Clock rate}}$$

10. For an integrator,  $\Delta v_o = (-1/RC) V(\Delta t)$
11. The voltage  $v_o$  will be equal to  $v_1$  at the instant  $t_2$  and can be written as

$$v_1 = (-1/RC) V_a(t_2 - t_1)$$

12. The voltage  $v_1$  is also given by  $v_1 = (-1/RC) (-V_R)(t_2 - t_3)$

$$\text{So, } V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

Putting the value of  $(t_2 - t_1) = 2^n$  and  $(t_3 - t_2) = N$ , we get

$$V_a(2^n) = (V_R)N \quad \text{or,} \quad V_a = (V_R)(N/2^n)$$

