

**PART- 1***Diode Circuits.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 1.1.** Explain half wave rectifier with its input-output waveform.

**Answer**

- ✓ 1. It is shown in Fig. 1.1.1. In this half portion of input is rectified (either positive half or negative half).
- ✓ 2. Only single diode and a step down transformer are required for this circuit.

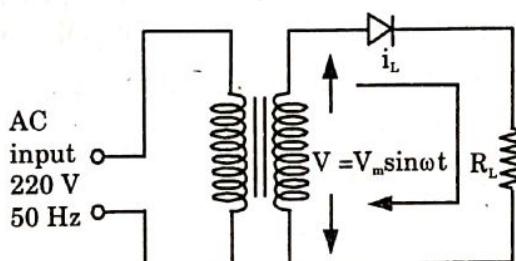


Fig. 1.1.1. Half wave rectifier circuit.

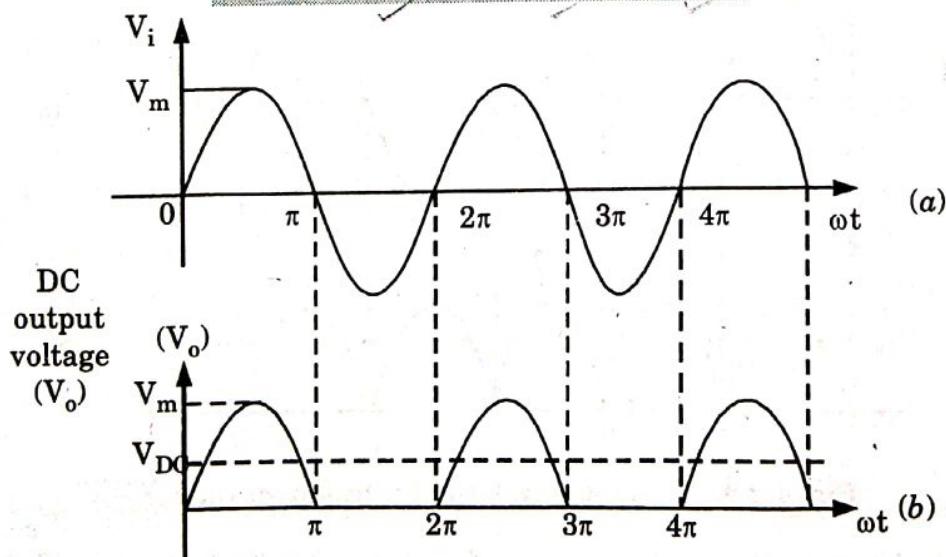


Fig. 1.1.2. (a) Input voltage (b) Output voltage.

**Que 1.2.** Explain the working of full wave bridge rectifier. What are the advantages of full wave rectifier ?

**Answer**

**Full wave rectifier :** This circuit gives the output for full cycle (i.e., for both positive and negative half cycles). There are two types of circuits used for it :

i. **Center tap rectifier :**

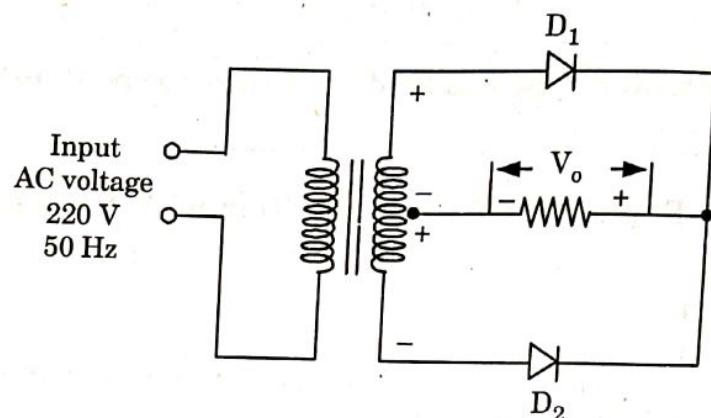


Fig. 1.2.1. Full wave rectifier.

1. In center-tap full wave rectifier circuit, diode  $D_1$  will be ON for positive half cycle (i.e., 0 to  $\pi$ ) and the diode  $D_2$  will be OFF during this cycle.
2. The diode  $D_2$  will be ON for negative half cycle (i.e.,  $\pi$  to  $2\pi$ ) while the diode  $D_1$  will be OFF during this cycle.
3. The input and output waveforms are shown in Fig. 1.2.2.

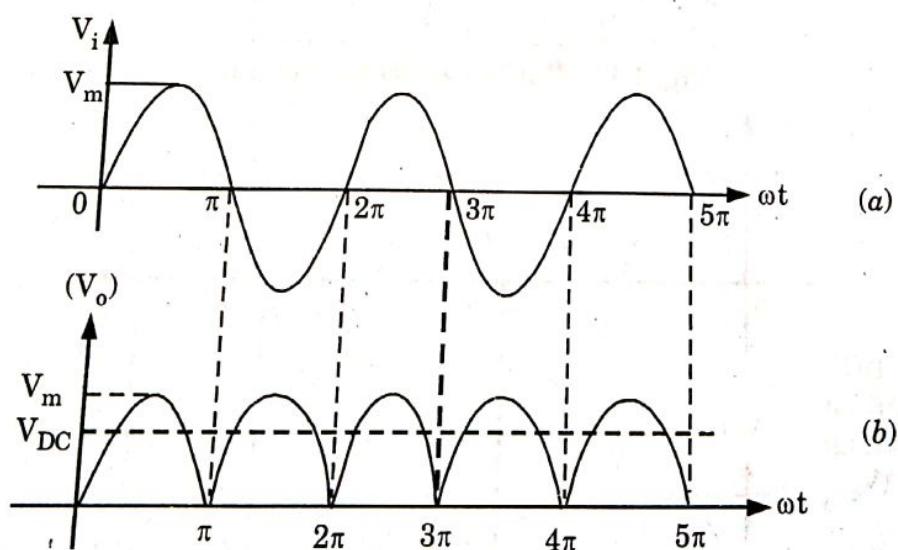
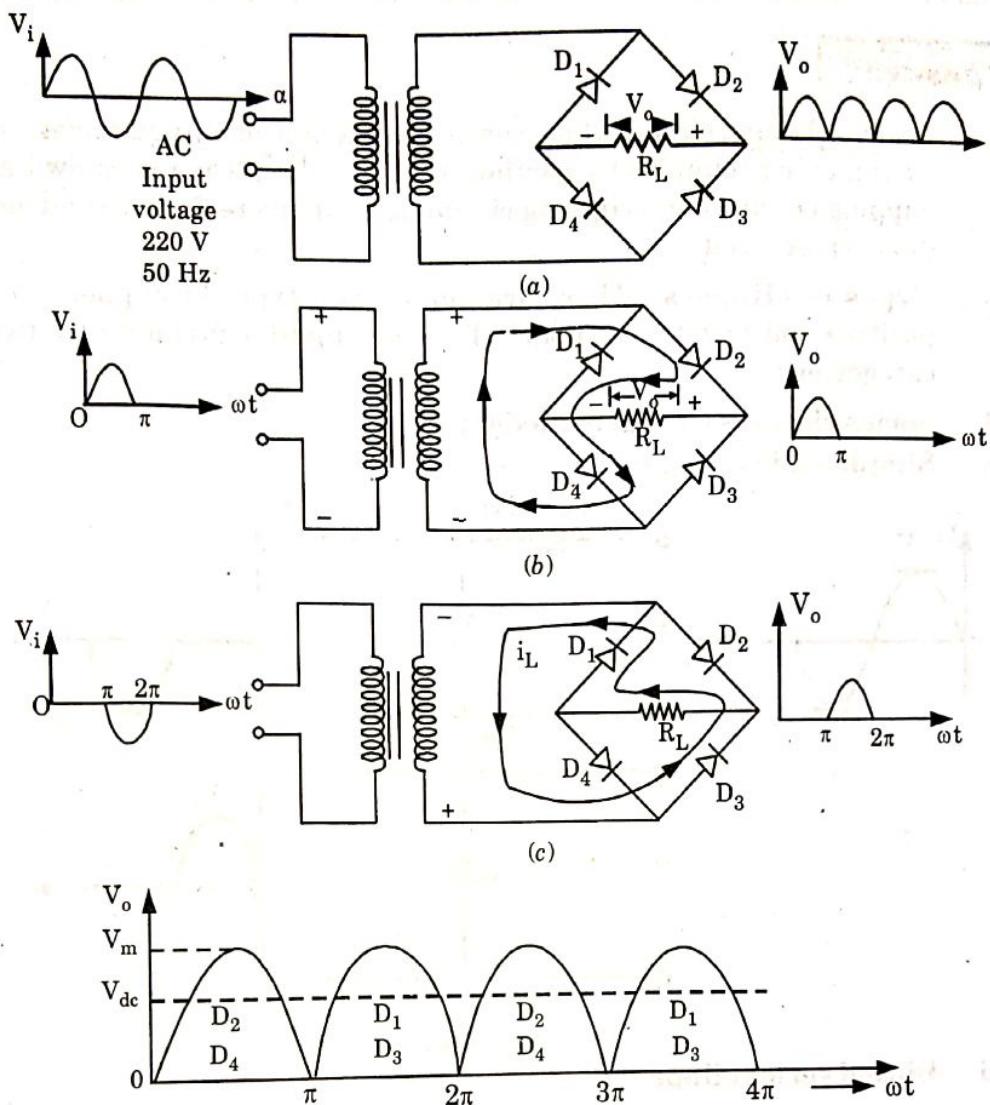


Fig. 1.2.2. (a) Input waveform (b) Output waveform.

- ii. **Bridge rectifier :** As shown in Fig. 1.2.3(b) only diodes  $D_2$  and  $D_4$  are active during positive half cycle while diodes  $D_1$  and  $D_3$  are active for negative half cycle as shown in Fig. 1.2.3(c) and Fig. 1.2.3(d) shows the total output with the active diodes for a particular cycle.



**Fig. 1.2.3.** (a) Basic bridge rectifier circuit  
 (b) Output of bridge rectifier for positive half cycle.  
 (c) Output of bridge rectifier for negative half cycle.  
 (d) Output for full cycle.

#### Advantages of full wave rectifier :

- i. Full wave rectifiers are more efficient than half wave rectifier. The maximum efficiency of full wave rectifier is 81.2% while the maximum efficiency of half wave rectifier is 40.6%.
- ii. The output waveform of full wave rectifier has fewer ripples.

**Que 1.3.** What do you mean by clipping circuits ? What are the different types of clipper circuits ?

OR

Draw a simple clipping circuit with suitable waveform and explain types of clippers.

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**Answer**

A wave shaping circuit which controls the shape of output waveform by removing (clipping) a portion of the applied wave is known as clipping circuit. For a clipping circuit at least one resistance and one diode is required.

**Types of clippers :** There are mainly two types of clippers i.e., positive and negative clippers. They are further divided into two categories :

**1. Series clippers (for ideal diode) :**

**i. Simple series clippers :**

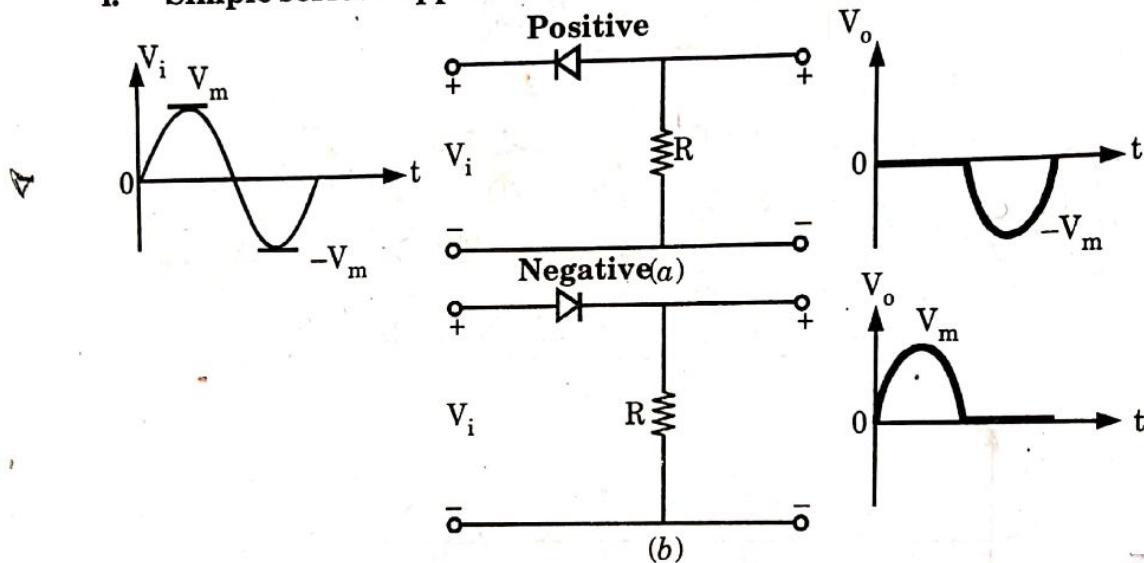
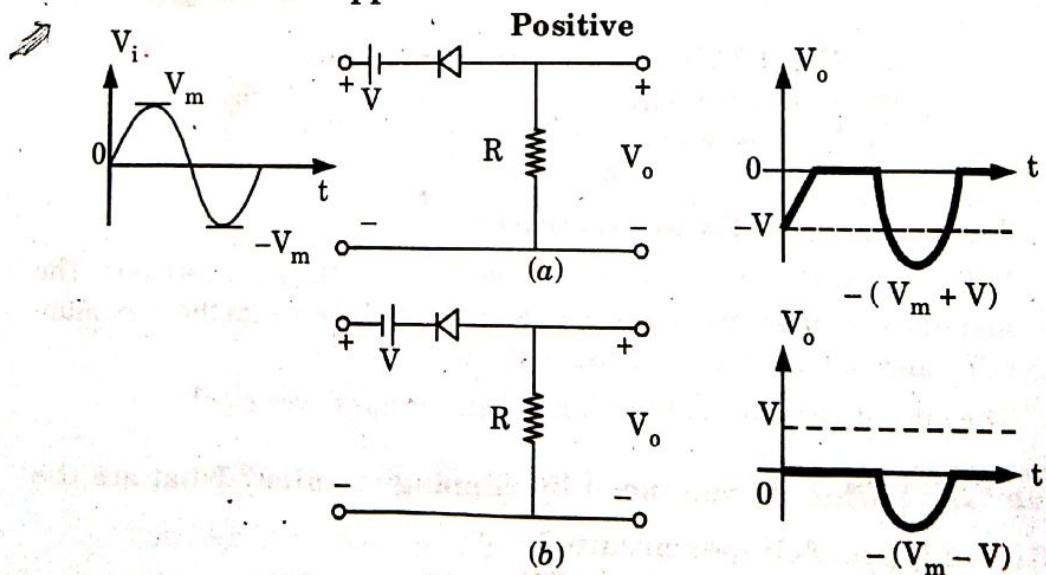


Fig. 1.3.1.

**ii. Biased series clippers :**



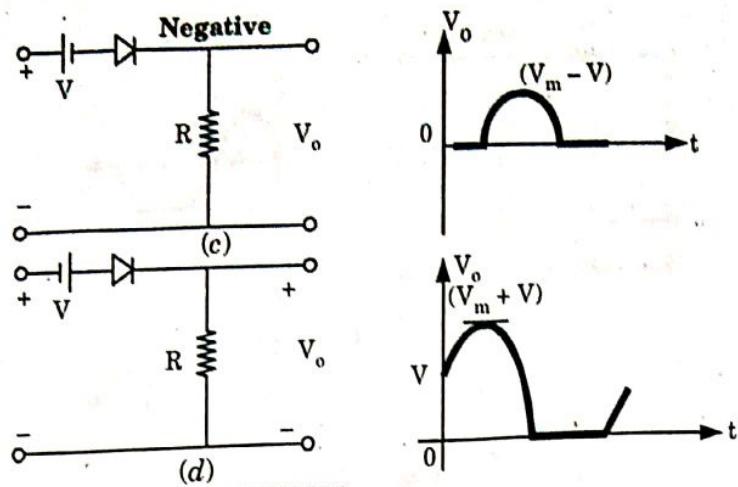


Fig. 1.3.2.

2. Parallel clippers (for ideal diodes) :  
i. Simple parallel clippers:

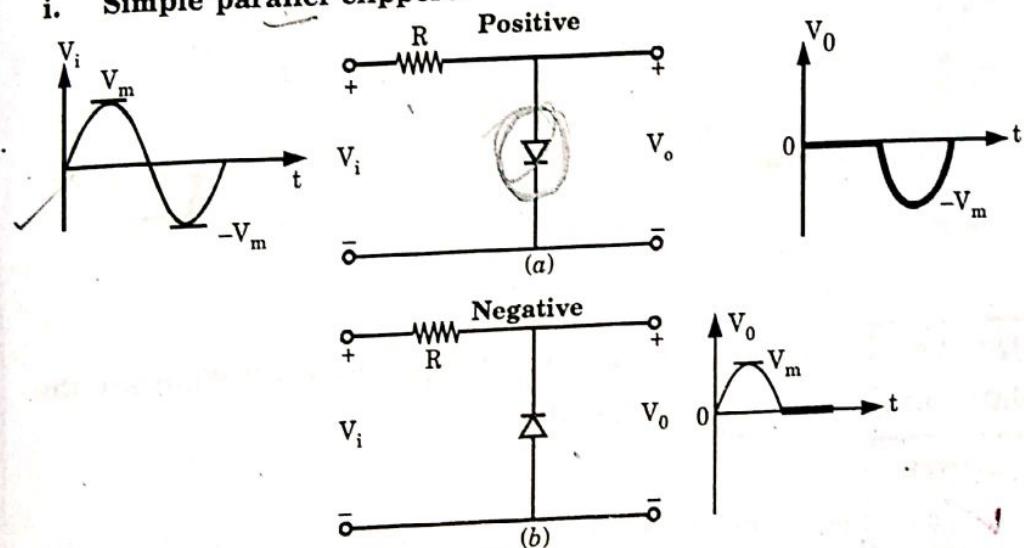
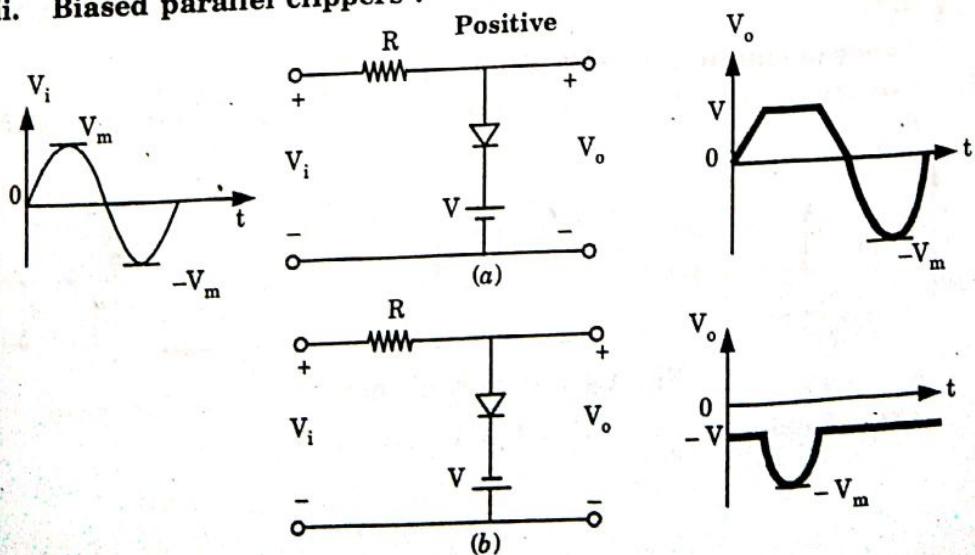


Fig. 1.3.3.

ii. Biased parallel clippers :



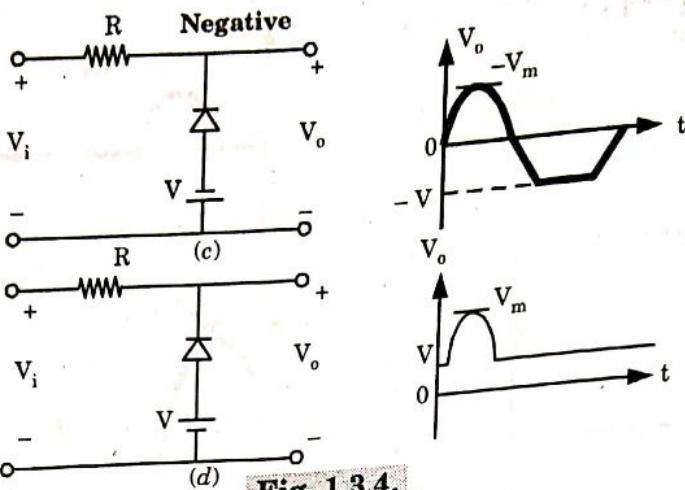


Fig. 1.3.4.

c. Combination clipper (Positive and Negative) :

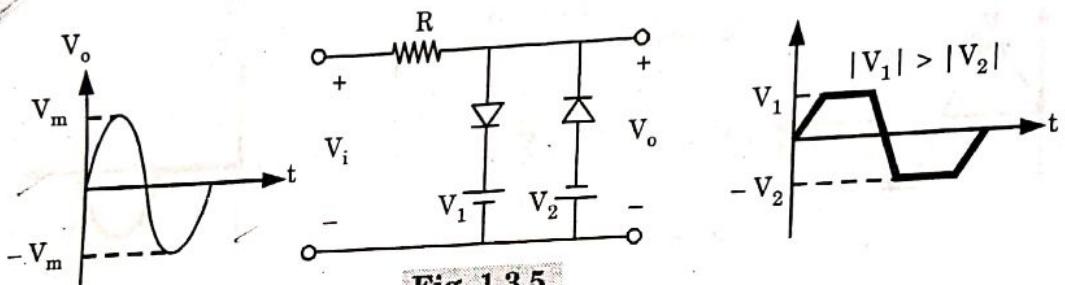


Fig. 1.3.5.

# ⚡ Que 1.4. What do you mean by clamper circuit? What are the different types of clamper circuits?

**Answer**

A clampling circuit is a device that 'clamps' a signal to a different DC level. A clampling circuit must have a diode, a resistance and a capacitor, an independent DC supply is also required to introduce an additional shift.

**Types of clamper circuit :** There are two types of clamper circuits.

1. **Positive Clamper :** It shifts the original signal in vertical upward direction.

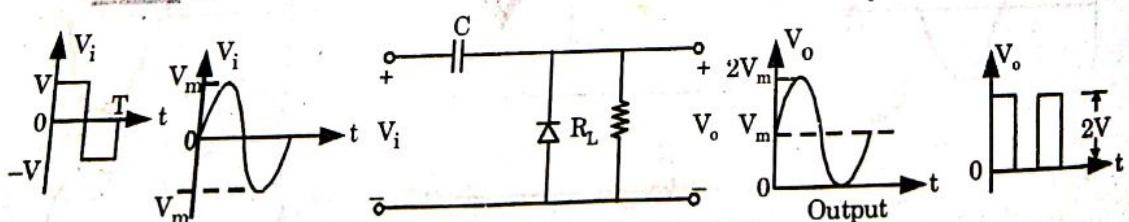


Fig. 1.4.1. Positive clamper.

Output voltage

$$V_o = V_m + V_c = V_m + V_m = 2V_m$$

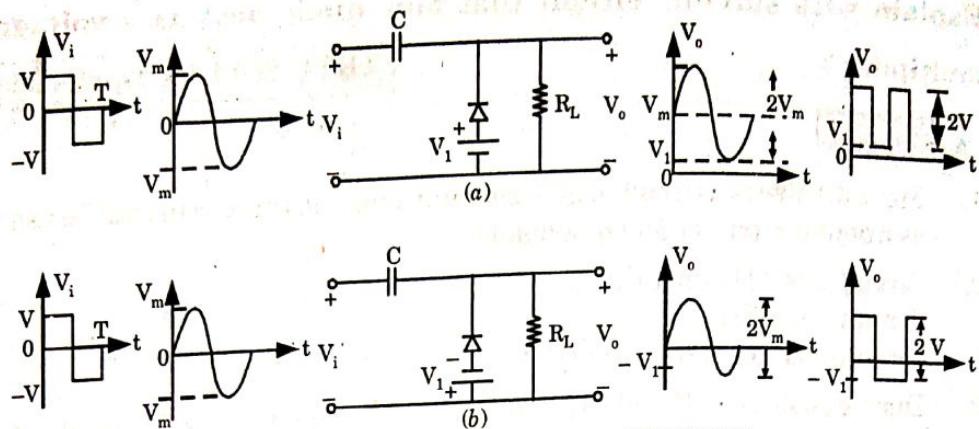
**Positive clamp with bias :**

Fig. 1.4.2. Positive clamp with positive biased,  
(b) Positive clamp with negative biased.

2. **Negative clamp** : It shifts the original signal in vertical downward direction.

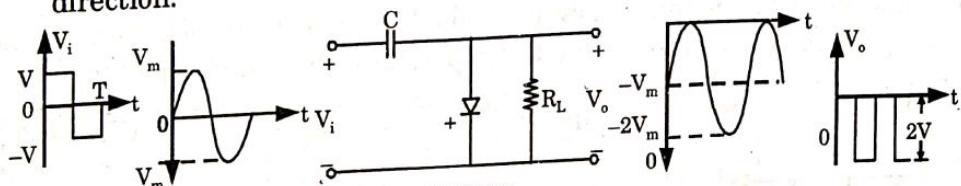


Fig. 1.4.3.

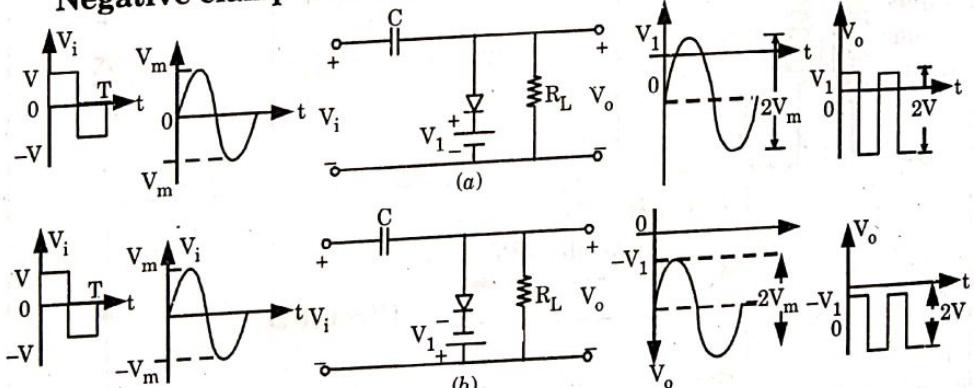
**Negative clamp with bias**

Fig. 1.4.4. (a) Negative clamp with positive bias,  
(b) Negative clamp with negative bias.

- Que 1.5.** Draw and discuss voltage tripler circuit.

AKTU 2016-17, Marks 05 →

OR

Describe with the help of circuit diagram working of voltage tripler.

AKTU 2015-16, Marks 05

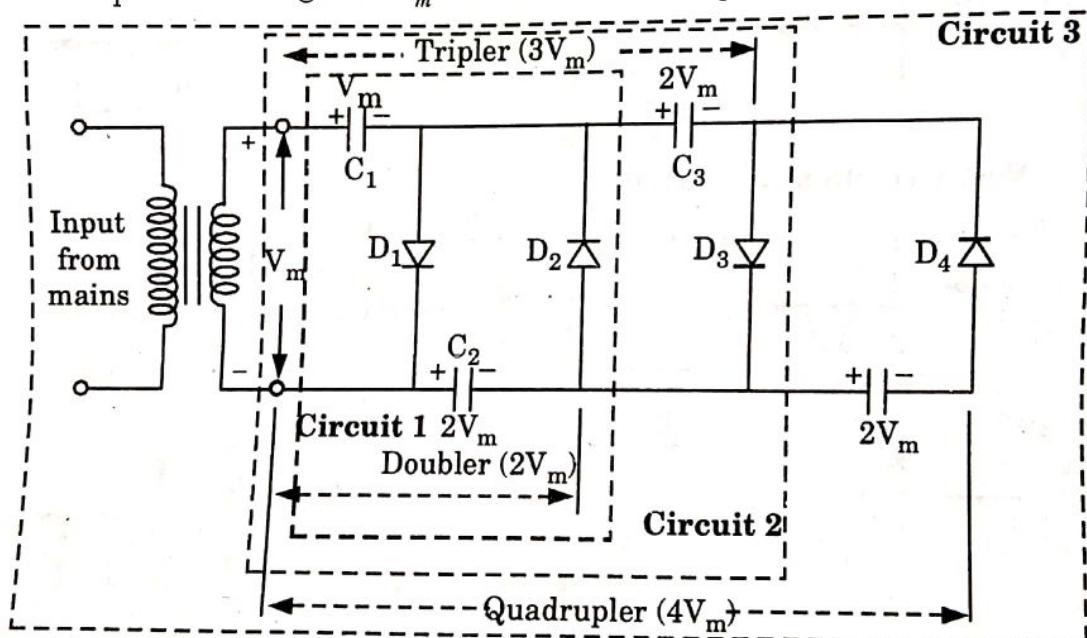
OR

Explain with suitable circuit that how diode acts as a voltage multiplier?

AKTU 2014-15, Marks 05

**Answer**

- Fig. 1.5.1 shows a circuit of general multiplier i.e. this circuit can be used as a doubler, tripler and quadrupler.
- Circuit-1 is a Doubler ( $2V_m$ ).  
Circuit-2 is a Tripler ( $3V_m$ ).  
Circuit-3 is a Quadrupler ( $4V_m$ ).
- During positive half cycle, the diode  $D_1$  is ON and it charges capacitor  $C_1$  to  $V_m$ .
- In the first negative half cycle, the diode  $D_2$  is ON and it charges  $C_2$  to  $2V_m$  ( $V_{C2} = V_m + V_{C1} = 2V_m$ ). In this cycle the charge on capacitor  $C_1$  starts discharging.
- In the second positive half cycle the diode  $D_1$  and  $D_3$  are ON, the capacitor  $C_1$  will be charged to  $V_m$  and the capacitor  $C_3$  will be charged to  $2V_m$ .



**Fig. 1.5.1. General circuit diagram of multiplier.**

$$V_{C3} = V_i + (-V_{C1}) + V_{C2} = V_m - V_m + 2V_m$$

$$V_{C3} = 2V_m \text{ (Voltage across } C_3\text{)}$$

- During second negative half-cycle, the diode  $D_2$  and diode  $D_4$  are ON. The voltage across capacitor is given as :

$$V_{C4} = V_i + (V_{C2}) + V_{C3} + V_{C1} = V_m - 2V_m + 2V_m + V_m$$

$$V_{C4} = 2V_m$$

- Now

$$\text{Voltage across } C_1 \rightarrow V_{C1} = V_m$$

$$\text{Voltage across } C_2 \rightarrow V_{C2} = 2V_m$$

- Voltage across  $C_3 \rightarrow V_{C3} = 2V_m$   
 Voltage across  $C_4 \rightarrow V_{C4} = 2V_m$
8. **Voltage doubler**: Taking output across  $C_2$ .  
 $V_o = V_{C2} = 2V_m$

9. **Voltage tripler**: Taking output across  $C_3$  and  $C_1$ .

$$V_1 = V_{C1} + V_{C3} = V_m + 2V_m = 3V_m$$

10. **Voltage quadrupler**: Taking output across  $C_2$  and  $C_4$   
 $V_o = V_{C2} + V_{C4} = 2V_m + 2V_m = 4V_m$

## PART-2

*Amplifier Models : Voltage Amplifier, Current Amplifier, Trans-conductance Amplifier and Trans-resistance Amplifier.*

### Questions-Answers

### Long Answer Type and Medium Answer Type Questions

- Que 1.6.** Discuss voltage amplifier model.

#### Answer

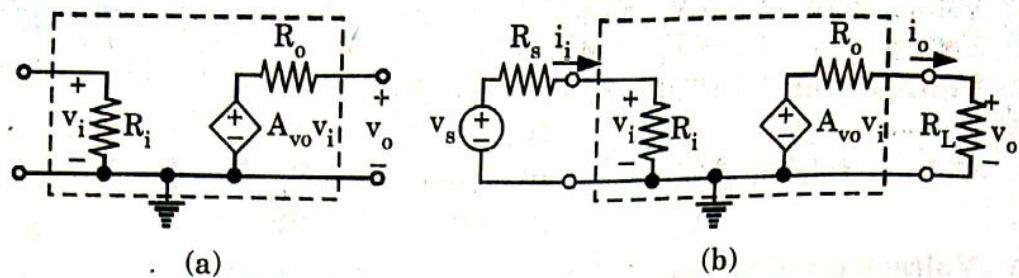
- Fig. 1.6.1(a) shows a circuit model for the voltage amplifier.
- The model consists of a voltage controlled voltage source having a gain factor  $A_{vo}$ , an input resistance and an output resistance  $R_o$ .
- In Fig. 1.6.1(b), the amplifier model fed with signal voltage source  $v_s$  having a resistance  $R_s$  and connected at the output to a load resistance  $R_L$ .
- The non-zero output resistance  $R_o$  causes only a fraction of  $A_{vo}v_i$  to appear across the output.
- Using the voltage-divider rule we obtain

$$v_o = A_{vo}v_i \frac{R_L}{R_L + R_o}$$

- Thus, the voltage gain is given by

$$A_v = \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \quad \dots(1.6.1)$$

- It follows that in order not to lose gain in coupling the amplifier output to a load, the output resistance  $R_o$  should be much smaller than the load resistance  $R_L$ .



**Fig. 1.6.1.** (a) Circuit model for the voltage amplifier.  
 (b) The voltage amplifier with input signal.

8. The finite input resistance  $R_i$  introduces another voltage-divider action at the input, with the result that only a fraction of the source signal  $v_s$  actually reaches the input terminals of the amplifier, that is

$$v_i = v_s \frac{R_i}{R_i + R_s} \quad \dots(1.6.2)$$

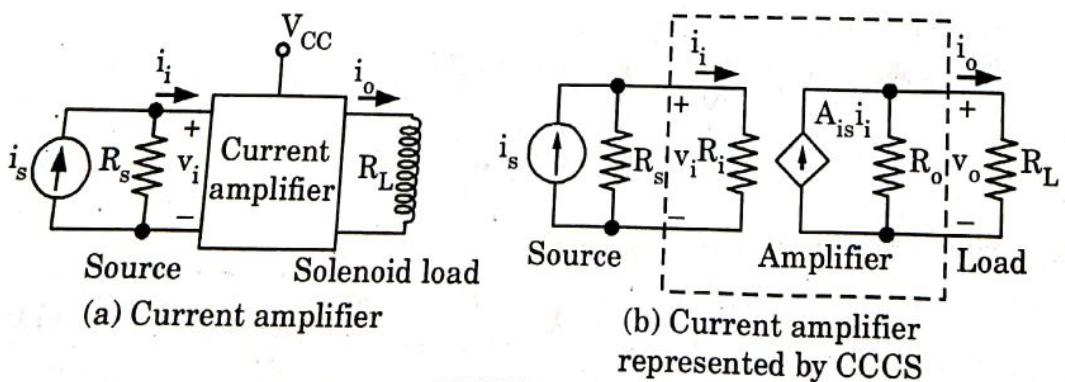
9. It follows that in order not to lose a significant portion of the input signal in coupling the signal source to the amplifier input, the amplifier must be designed to have an input resistance  $R_i$  much greater than the resistance of the signal source, i.e.,  $R_i \gg R_s$ .
10. The overall voltage gain ( $v_o/v_s$ ) can be found by combining eq. (1.6.1) and (1.6.2)

$$\frac{v_o}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o}$$

**Que 1.7.** Draw and explain circuit model of current amplifier.

**Answer**

1. An amplifier whose output current is proportional to its input current is called a current amplifier.



**Fig. 1.7.1.**

2. Its input is a current source, as shown in Fig. 1.7.1 (a), with a load resistance  $R_L$ . A current amplifier is represented by a current controlled current source (CCCS), as shown in Fig. 1.7.1 (b).

3.  $A_{is}$  is called the short-circuit current gain (or simply the current gain) with output terminals shorted.  $R_i$  is the input resistance, and  $R_o$  is the output resistance.
4. The output current  $i_o$  of the amplifier can be obtained by using the current divider rule :

$$i_o = A_{is} i_s \frac{R_o}{R_o + R_L} \quad \dots(1.7.1)$$

5. The input current  $i_i$  of the amplifier is related to the signal source current  $i_s$  by

$$i_i = \frac{R_s}{R_s + R_i} i_s \quad \dots(1.7.2)$$

6. Substituting  $i_i$  from eq. (1.7.2) into eq. (1.7.1), we get effective current gain  $A_i$ , which is defined as the ratio of  $i_o$  to  $i_s$ .

$$\text{i.e., } A_i = \frac{i_o}{i_s} = \frac{i_o}{i_i} \times \frac{i_i}{i_s} = \frac{A_{is} R_s R_o}{(R_s + R_i)(R_o + R_L)} = \frac{A_{is}}{(1 + R_i / R_s)(1 + R_L / R_o)} \quad \dots(1.7.3)$$

7. In eq. (1.7.3), if the values of input resistance  $R_i$  and load resistance  $R_L$  increase then reduce the effective current gain  $A_i$ .
8. A current amplifier should have an input resistance  $R_i$  much smaller than the source resistance  $R_s$  so that  $R_i \ll R_s$ .
9. The reduction in gain can also be minimized by designing an amplifier so that the ratio  $R_L/R_o$  is very small i.e.,  $R_o \gg R_L$ .
10. Therefore, an ideal current amplifier has  $R_o = \infty$  and  $R_i = 0$  so that there is no reduction in the current gain. That is,  $A_i = A_{is}$ , and eq. (1.7.3) becomes

$$i_o = A_{is} i_s \quad \dots(1.7.4)$$

**Que 1.8.** Explain the transconductance amplifier model.

**Answer**

1. An amplifier that receives a voltage signal as input and provides a current signal as output is called a transconductance amplifier.

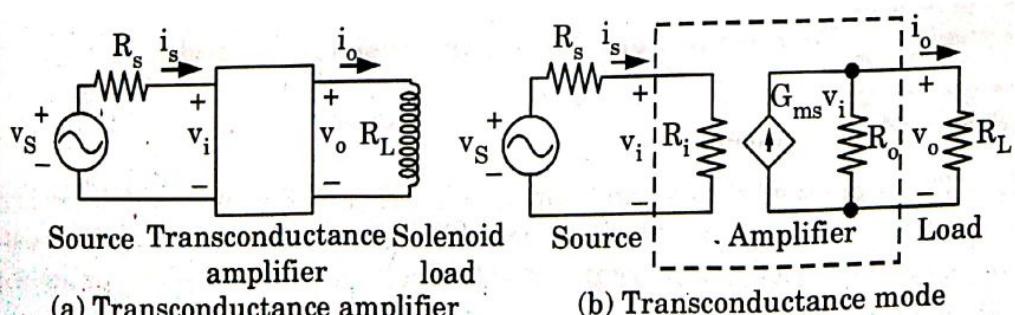


Fig. 1.8.1.

2. It can be represented by a voltage controlled current source (VCCS), as shown in Fig. 1.8.1(b).
3. The amplifier is connected between a voltage source  $v_s$  and a load resistance  $R_L$ .
4. Gain parameter  $G_{ms}$ , which is the ratio of the short-circuit output current to the input voltage, is called the short circuit transconductance.
5. From the current divider rule, the output current  $i_o$  is

$$i_o = G_{ms} v_i \frac{R_o}{R_o + R_L} \quad \dots(1.8.1)$$

6. The input voltage  $v_i$  of the amplifier is related to source voltage  $v_s$  by

$$v_i = \frac{R_i}{R_i + R_s} v_s \quad \dots(1.8.2)$$

7. Substituting  $v_i$  from eq. (1.8.2) into eq. (1.8.1) then transconductance gain  $G_m$  is

$$G_m = \frac{i_o}{v_s} = \frac{G_{ms} R_o R_i}{(R_o + R_L)(R_i + R_s)} = \frac{G_{ms}}{(1 + R_L / R_o)(1 + R_s / R_i)} \quad \dots(1.8.3)$$

8. The effective voltage gain  $A_v$  is,

$$\begin{aligned} A_v &= \frac{v_o}{v_s} = \frac{i_o R_L}{v_s} = \frac{v_o}{v_i} \times \frac{v_i}{v_s} = \frac{G_{ms} R_o R_L R_i}{(R_o + R_L)(R_i + R_s)} \\ &= \frac{G_{ms} R_L}{(1 + R_L / R_o)(1 + R_s / R_i)} \end{aligned} \quad \dots(1.8.4)$$

9. The source resistance  $R_s$  and the load resistance  $R_L$  reduce the effective transconductance gain  $G_m$ .
10. A transconductance amplifier should have a high input resistance  $R_i$  so that  $R_i \gg R_s$  and a very high output resistance  $R_o$  so that  $R_o \gg R_L$ .
11. Therefore, an ideal transconductance amplifier has  $R_o = \infty$  and  $R_i = \infty$  so that there is no reduction in the voltage gain. That is,  $G_m = G_{ms}$ , and eq. (1.8.3) becomes

$$i_o = G_{ms} v_s \quad \dots(1.8.5)$$

**Que 1.9.** Discuss in detail the trans-resistance model.

**Answer**

1. The input signal to a transimpedance (trans-resistance) amplifier is a current source, and its output is voltage source. Such an amplifier can be represented as a current-controlled voltage source (CCVS), as shown in Fig. 1.9.1.

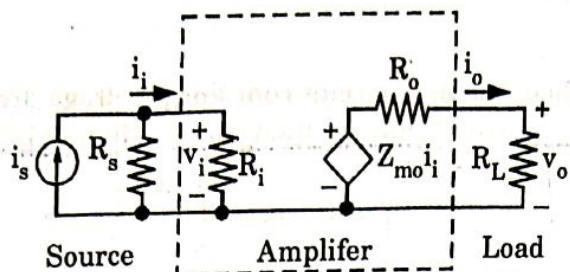


Fig. 1.9.1. Transimpedance amplifier.

2. The gain parameter  $Z_{mo}$  is the ratio of the open-circuit output voltage to the input current, and it is called the open circuit transimpedance.
3. The output voltage  $v_o$  is related to  $i_i$  by

$$v_o = \frac{Z_{mo} i_i R_L}{R_L + R_o} \quad \dots(1.9.1)$$

4. The input current  $i_i$  of the amplifier is related to  $i_s$  as follows :

$$i_i = \frac{R_s}{R_s + R_i} i_s \quad \dots(1.9.2)$$

5. Substituting  $i_i$  from eq. (1.9.2) into eq. (1.9.1) then effective transimpedance  $Z_m$ .

$$Z_m = \frac{v_o}{i_s} = \frac{Z_{mo} R_L R_s}{(R_L + R_o)(R_s + R_i)} = \frac{Z_{mo}}{(1 + R_o / R_L)(1 + R_i / R_s)} \quad \dots(1.9.3)$$

6. A transimpedance amplifier must have an input resistance  $R_i$  much smaller than the source resistance  $R_s$  and an output resistance  $R_o$  much smaller than the load resistance  $R_L$ .
7. An ideal transimpedance amplifier has  $R_i = 0$  and  $R_o = 0$ .

$$\text{i.e., } v_o = Z_{mo} i_s \quad \dots(1.9.4)$$

### PART-3

*Biasing Schemes for BJT and FET Amplifiers, Bias Stability.*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

- Que 1.10 Explain the operation of voltage divider bias circuit and write down the approximate equations of  $V_B$ ,  $I_E$ ,  $I_C$  and  $V_{CE}$ .

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**Answer**

1. In this method, the base circuit contains a voltage divider ( $R_1$  and  $R_2$ ). Because of this, the circuit is called voltage-divider bias (VDB).

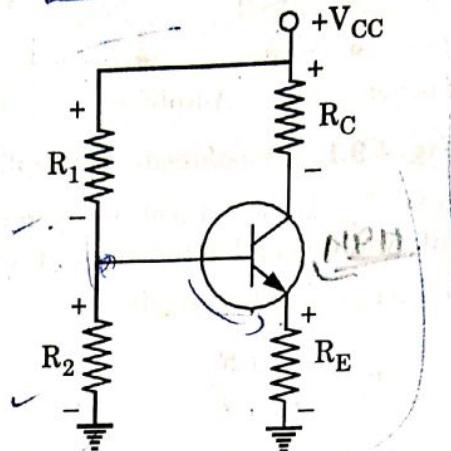


Fig. 1.10.1.

**Circuit analysis :**

1. In VDB circuit, the base current is much smaller than the current through the voltage divider.
2. Therefore, we can open the connection between the voltage divider and the base to get the equivalent circuit of Fig. 1.10.2(a).
3. In this circuit the output of the voltage divider is

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} = V_B$$

4. Ideally, this is the base-supply voltage as shown in Fig. 1.10.2(b).

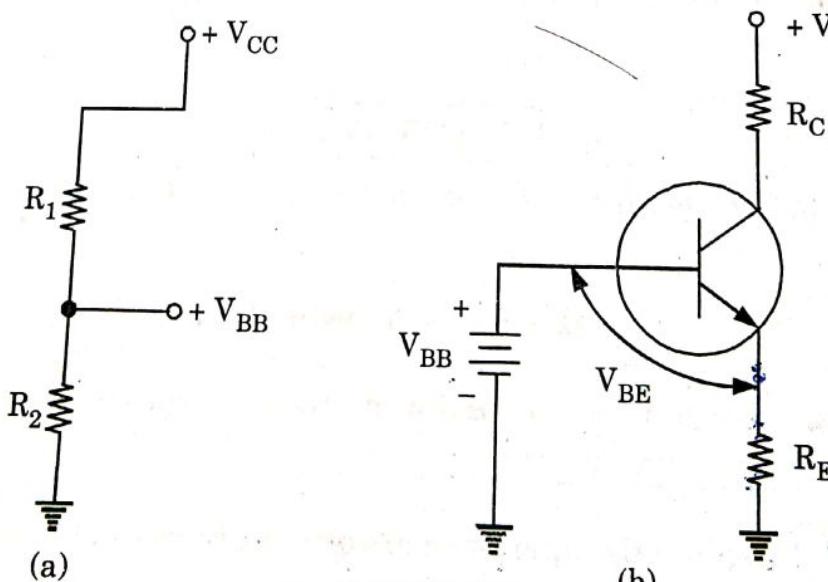


Fig. 1.10.2.

5. From Fig. 1.10.2(b)

$$V_E = V_{BB} - V_{BE}$$

$$M_C = I_C R_C$$

$$V = I R$$

$$I_E = \frac{V_E}{R_E}$$

$$I_C \approx I_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E \\ = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$I_C$  = Collector Current

$I_E$  = Emitter current approximately  
are same

Que 1.11. Explain collector feedback configuration.

Answer

1. Fig. 1.11.1 shows collector-feedback bias (also called self-bias).
2. Stabilizing the  $Q$  point, the basic idea is to feedback a voltage to the base in an attempt to neutralize any change in collector current.
3. For instance, suppose the collector current increases.
4. This decreases the collector voltage, which decreases the voltage across the base resistor.

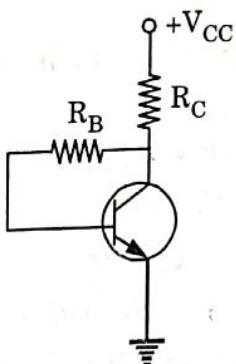


Fig. 1.11.1.

5. In turn, this decreases the base current which opposes the original increase in collector current.
6. The equations for analyzing collector feedback bias are :

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B / \beta_{DC}}$$

$$V_B = 0.7 \text{ V}$$

$$V_C = V_{CC} - I_C R_C$$

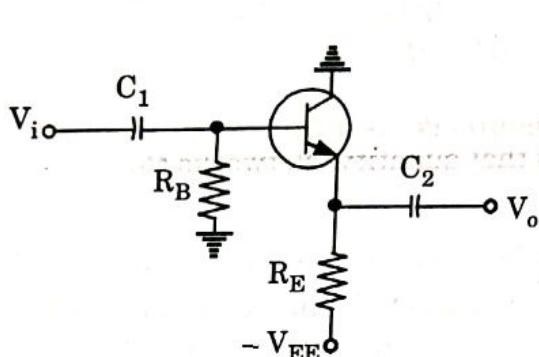
7. The  $Q$  point is usually set near the middle of the load line by using a base resistance of :

$$R_B = \beta_{DC} R_C$$

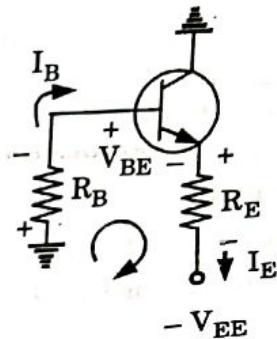
**Que 1.12.** Explain emitter follower configuration.

**Answer**

1. Here the output is taken from emitter terminal as shown in Fig. 1.12.1(a).



(a) Common-collector (emitter-follower) configuration.



(b) DC equivalent.

Fig. 1.12.1.

2. Applying Kirchhoff's voltage rule to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\text{and using } I_E = (\beta + 1) I_B$$

$$I_B R_B + (\beta + 1) I_B R_E = V_{EE} - V_{BE}$$

$$\text{so that } I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

3. For the output an application of Kirchhoff's voltage law will result in

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

$$\text{and } V_{CE} = V_{EE} - I_E R_E$$

**Que 1.13.** Explain bias stabilization.

**Answer**

1. The stability of a system is a measure of sensitivity of a network to variation in its parameters. In any amplifier employing a transistor the collector current  $I_C$  is sensitive to each of the following parameters :

- i.  $\beta$  increases with increase in temperature
- ii.  $V_{BE}$  decreases about 2.5 mV per degree Celsius ( $^{\circ}\text{C}$ ) increase in temperature.
- iii.  $I_{CO}$  (reverse saturation current) doubled in value for every  $10\text{ }^{\circ}\text{C}$  increase in temperature.

**Stability Factors :**

1. A stability factor  $S$  is defined for each of the parameters affecting bias stability as follows :

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

2. Here,  $\Delta$  signifies the change in that quantity. Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

$S(I_{CO})$ :

**Emitter-Bias Configuration :**

1.  $S(I_{CO}) = (\beta + 1) \frac{1 + R_B / R_E}{(\beta + 1) + R_B / R_E}$  ... (1.13.1)

2. For  $R_B / R_E \gg (\beta + 1)$ ,  
 $S(I_{CO}) = (\beta + 1)$  ... (1.13.2)

3. For  $R_B / R_E \ll 1$ ,

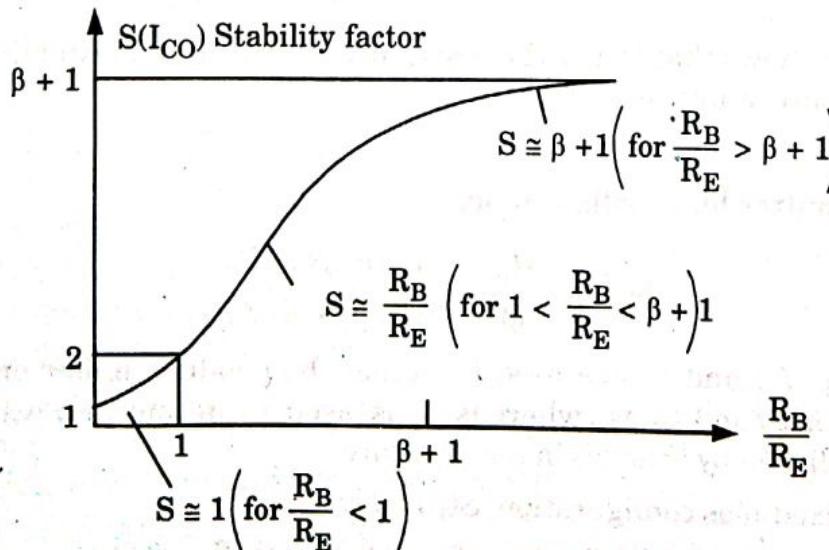
$$S(I_{CO}) = (\beta + 1) \frac{1}{(\beta + 1)} = 1 \quad \dots (1.13.3)$$

4. For the range where  $R_B / R_E$  ranges between 1 and  $(\beta + 1)$ , the stability factor will be determined by

$$S(I_{CO}) \approx \frac{R_B}{R_E} \quad \dots (1.13.4)$$

as shown in Fig. 1.13.1.

5. The result reveals that the emitter-bias configuration is quite stable when the ratio  $R_B / R_E$  is as small as possible and become stable when the same ratio approaches  $(\beta + 1)$ .



**Fixed Bias Configuration :**

For the fixed-bias configuration, if we multiply the top and bottom of eq. (1.13.1) by  $R_E$  and then put in  $R_E = 0 \Omega$ , the following eq. results

$$S(I_{CO}) = \beta + 1$$

**Voltage-Divider Bias Configuration :**

$$S(I_{CO}) = (\beta + 1) \frac{1 + R_{th} / R_E}{(\beta + 1) + R_{th} / R_E} \quad \dots(1.13.5)$$

**Feedback-Bias Configuration :**

$$S(I_{CO}) = (\beta + 1) \frac{1 + R_B / R_C}{(\beta + 1) + R_B / R_C} \quad \dots(1.13.6)$$

 **$S(V_{BE})$  :**

1. The stability factor is defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \quad \dots(1.13.7)$$

and results in the following equation for the emitter-bias configuration

$$S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E} \quad \dots(1.13.8)$$

2. If  $R_E = 0$  as it occurs for fixed-bias configuration

$$S(V_{BE}) = -\frac{\beta}{R_B} \quad \dots(1.13.9)$$

3. Eq. (1.13.8) can be written in the following form :

$$S(V_{BE}) = \frac{-\beta / R_E}{R_B / R_E + (\beta + 1)} \quad \dots(1.13.10)$$

4. If  $(\beta + 1) \gg R_B / R_E$

$$\text{then, } S(V_{BE}) \approx \frac{-\beta / R_E}{\beta + 1} \approx \frac{-\beta / R_E}{\beta} = -\frac{1}{R_E} \quad \dots(1.13.11)$$

which shows that larger the resistance  $R_E$ , lower is the stability factor and more stable is the system.

 **$S(\beta)$  :**

1. For emitter-bias configuration,

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C1}(1 + R_B / R_E)}{\beta_1(1 + \beta_2 + R_B / R_E)}$$

where,  $I_{C1}$  and  $\beta_1$  are used to define their values under one set of network conditions, whereas  $\beta_2$  is used to define new value of  $\beta$  established by changes in temperature

2. For fixed-bias configuration,  $S(\beta) = I_{C1} / \beta_1$ .
3. For the collector feedback configuration with  $R_E = 0 \Omega$

$$S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + R_C(1 + \beta_2))}$$

**Que 1.14.** Explain the self bias configuration of FET.

**Answer**

1. The self bias configuration eliminates the need of two DC supplies i.e., only drain supply is used and no gate supply is connected.
2. Fig. 1.14.1 shows the arrangement, a resistor  $R_s$  is connected in the source leg of the configuration. This is known as bias resistor.
3. The DC component of drain current  $I_D$  flowing through  $R_s$  makes a voltage drop across resistor  $R_s$ .
4. The capacitor  $C_s$  bypasses the AC component of drain current.

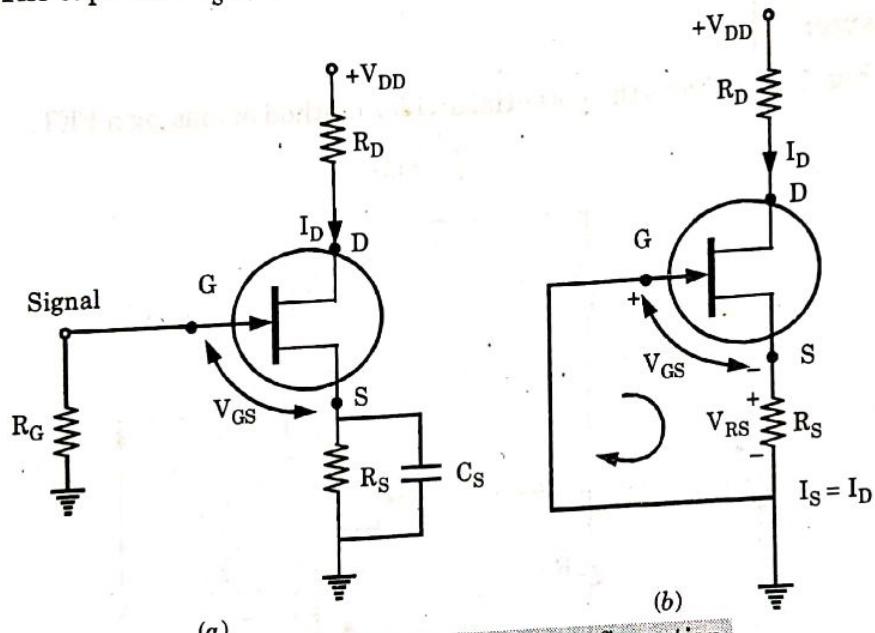


Fig. 1.14.1. Self bias configuration.

5. The addition of  $R_g$  in circuit does not upset the DC bias, but avoid the short-circuiting of the AC input voltage. Otherwise, the leakage current would build up static charge at the gate which could change the bias.
6.  $R_s$  also help to prevent any variation in FET drain current.
7. Let there be an increase in the drain current. This will increase the voltage drop across resistor  $R_s$  and this results in decrease of channel width. So, the drain current is reduced.
8. For DC analysis, the capacitors can be replaced by open circuit and the resistor  $R_g$  replaced by short-circuit equivalent. Since  $I_g = 0$  A. The equivalent circuit is shown in Fig. 1.14.1(b).

9. For the indicated loop, we have

$$-V_{GS} - V_{RS} = 0$$

$$V_{GS} = -V_{RS}$$

$$V_{GS} = -I_D R_S$$

10. The gate is kept at this much negative potential with respect to ground.

but

$$I_D = I_S$$

and

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

In addition

$$V_S = I_D R_S, V_G = 0V$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

**Que 1.15.** Draw and explain the voltage divider bias configuration of FET.

**Answer**

1. Fig. 1.15.1 shows the potential divider method of biasing a FET.

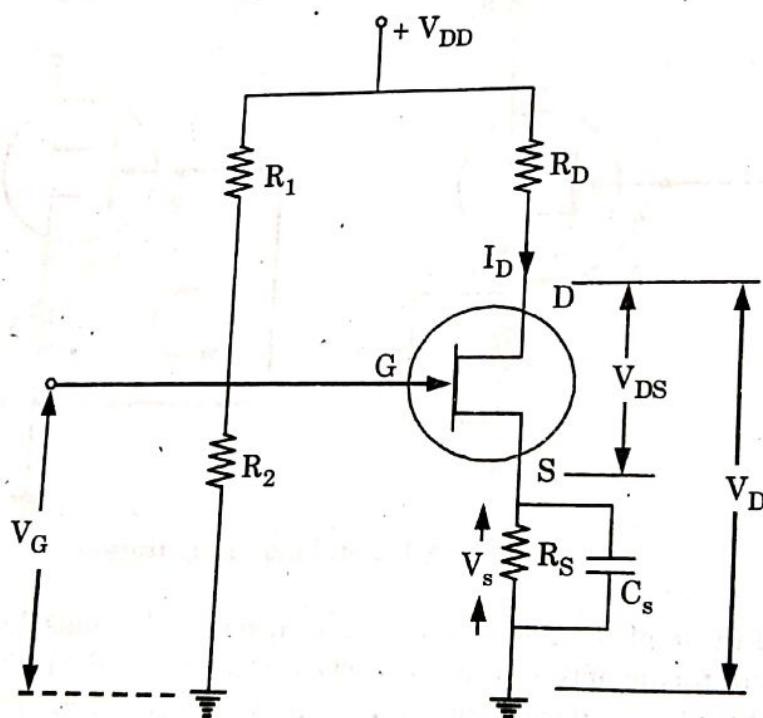


Fig. 1.15.1.

2. The name voltage divider is given due to the fact that resistors  $R_1$  and  $R_2$  form a voltage divider across drain supply  $V_{DD}$ . The voltage developed across  $R_2$  provides the necessary bias.
3. The gate voltage  $V_G$  is given by

$$V_G = \left[ \frac{V_{DD}}{R_1 + R_2} \right] R_2$$

4. The source voltage is given by

$$V_s = V_g - V_{gs}$$

$$I_d R_s = V_g - V_{gs}$$

$$V_{gs} = V_g - I_d R_s$$

5. The circuit is so designed that  $I_d R_s$  is larger than  $V_g$  so that  $V_{gs}$  is negative.

6. The operating point can be obtained as under :

i.  $I_d = \frac{V_s}{R_s} = \frac{V_g - V_{gs}}{R_s}$

ii.  $V_{ds} = V_{dd} - I_d (R_d + R_s)$

iii.  $V_d = V_{dd} - I_d R_d$

iv.  $V_s = I_d R_s$

v.  $I_{R1} = I_{R2} = \frac{V_{dd}}{R_1 + R_2}$

#### PART-4

*Various Configurations (Such as CE/CS, CB(CG, CC/CD) and Their Features.*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

- Que 1.16.** What are the types of transistor configurations ? Also draw the input and output characteristics of a BJT in the common base configuration.

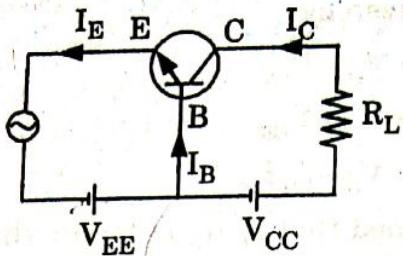
#### Answer

There are three types of transistor circuit configurations :

1. Common-base (CB)
2. Common-emitter (CE)
3. Common-collector (CC)

#### Common-base (CB) configuration :

1. In this configuration, the input signal is applied between emitter and base. The output is collected from collector and base as shown in Fig. 1.16.1.

**Fig. 1.16.1. Common-base npn transistor amplifier.****Current amplification factor ( $\alpha$ ) :**

- It is defined as the ratio of the collector current to the emitter current of a transistor when no signal is applied and is called DC alpha ( $\alpha_{DC}$ ).

$$\alpha_{DC} = \frac{I_C}{I_E}$$

- Simply  $\alpha_{DC}$  is  $\alpha$

Then  $\alpha = \frac{I_C}{I_E}$

- The transistor having high  $\alpha$  is better in the sense that collector current approaches the emitter current.

$$I_C = \alpha I_E \text{ and } I_B = I_E - I_C$$

$$I_B = I_E - \alpha I_E = I_E (1 - \alpha)$$

- Now, when signal is applied, the ratio of change in collector to emitter current at constant collector base voltage is defined as current amplification factor.

$$\alpha_{AC} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB} = \text{constant}}$$

Practically  $\alpha_{DC} = \alpha_{AC} = \alpha = 0.9$  to  $0.99$

- Total collector current  $I_C = \underbrace{\alpha I_E}_{\text{Majority}} + \underbrace{I_{CBO}}_{\text{Minority}}$

- The collector current can also be expressed as

$$I_C = \alpha (I_E + I_B) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left( \frac{\alpha}{1 - \alpha} \right) I_B + \left( \frac{1}{1 - \alpha} \right) I_{CBO}$$

- The relation between  $\alpha$  and  $\beta$  is given by

$$\alpha = \frac{\beta}{1 + \beta} \text{ or } 1 - \alpha = \frac{1}{1 + \beta}$$

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

### Characteristics of CB circuit :

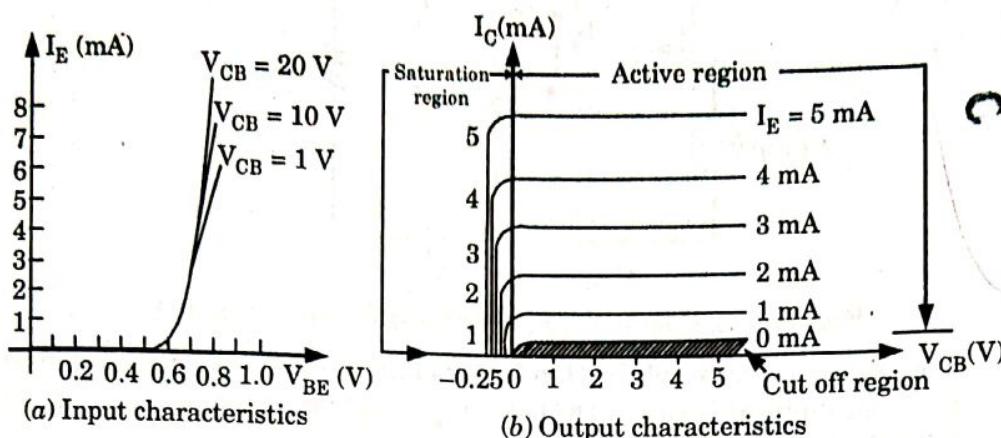


Fig. 1.16.2.

#### Input characteristics :

- There exists a cut in, offset or threshold voltage  $V_{BE}$  below which the current is very small.
- $I_E$  increases rapidly with small increase in  $V_{BE}$  i.e., input resistance is very small.

#### Output characteristics :

- In active region, the collector current is independent of collector voltage and depends upon emitter current but if  $V_{CB}$  increases beyond a certain value,  $I_C$  increases rapidly due to avalanche breakdown.  
In this region the base emitter function is forward biased whereas collector base function is reversed biased.
- In cut-off region, a small amount of collector current flows even when  $I_E = 0$ , i.e., leakage current  $I_{CBO}$ .  
Here emitter base and collector base junctions both are reversed biased.
- In saturation region, current  $I_C$  flows even if  $V_{CB} \approx 0$ .  
Here collector and emitter junctions both are forward biased.

**Que 1.17.** Draw and explain the input and output characteristics of common emitter configuration.

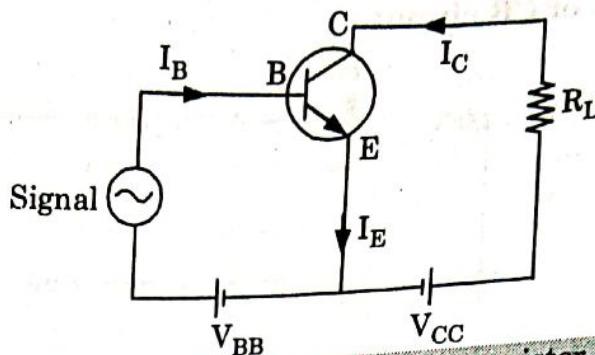
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OR

Draw the basic structure of a CE BJT and explain its principle of operation with neat diagrams along with its input output characteristics.

#### Answer

- In CE configuration, the input signal is applied between base and emitter and the output is taken from collector and emitter.
- As emitter is common to input and output circuits, hence the name common emitter configuration and is shown in Fig. 1.17.1



**Fig. 1.17.1. Common-emitter npn transistor amplifier.**

3. The base current amplification factor is the ratio of collector current to the base current is called DC beta ( $\beta_{DC}$ ) of a transistor, when no signal is applied.

$$\beta_{DC} = \beta = \frac{I_C}{I_B}$$

4. When signal is applied, the ratio of change in collector current to the change in base current is defined as current amplification factor.

$$\beta_{AC} = \beta = \frac{\Delta I_C}{\Delta I_B}$$

$$I_C = \beta I_B$$

$\beta$  is generally greater than 20 and ranges from 20 to 500. Hence, this configuration is frequently used when current gain as well as voltage gain is required.

5. Total collector current

$$I_C = \beta I_B + I_{CEO}$$

6. We know that  $I_E = I_B + I_C$

$$I_C = \alpha I_E + I_{CBO} = \alpha (I_B + I_C) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

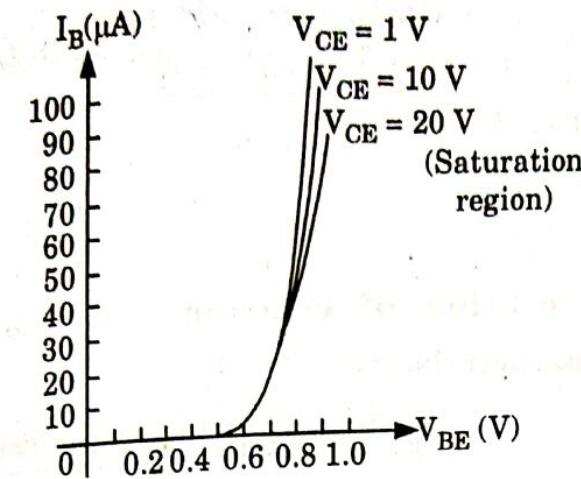
$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO}$$

7. On solving we get  $\beta = \frac{\alpha}{1 - \alpha}$  and  $I_{CEO} = \frac{1}{1 - \alpha} I_{CBO}$

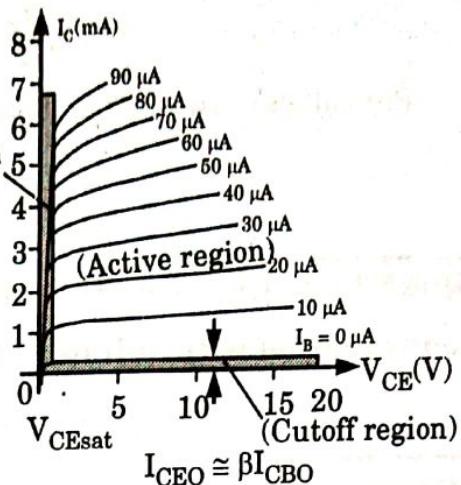
#### Characteristics of common emitter circuit :

##### **Input characteristic :**

1. The forward biased diode curve is expected because the base emitter section of transistor is a diode and it is forward biased.
2. In this case,  $I_B$  increases less rapidly with  $V_{BE}$  as compared to common base configuration i.e., input resistance of common emitter is higher than common base circuit.



(a) Input characteristics



(b) Output characteristics

Fig. 1.17.2.

**Output characteristics :**

1. In active region, for small values of base current, the effect of collector voltage over collector current is small while for large base current values effect increases. Thus, the current gain of this configuration is greater than unity.
2. When  $V_{CE}$  has very low value, the transistor is said to be saturated. The change in  $I_B$  does not produce a corresponding change in  $I_C$ .
3. In cut off region, a small amount of  $I_C$  flows even when  $I_B = 0$ . i.e.,  $I_{CEO}$  and the transistor is said to be cut-off.

**Que 1.18.** Establish the relation in between  $\gamma$ ,  $\beta$  and  $\alpha$ .

**Answer**

1. Total emitter current

$$I_E = I_B + I_C$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_B + (\alpha I_E + I_{CBO})$$

$$I_E (1 - \alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{(1 - \alpha)} + \frac{I_{CBO}}{(1 - \alpha)}$$

$$I_E = (1 + \beta) I_B + (1 + \beta) I_{CBO}$$

$$\frac{1}{1 - \alpha} = 1 + \beta$$

...(1.18.1)

2.  $\gamma = \frac{I_E}{I_B}$  and  $\alpha = \frac{I_C}{I_E}$

$$\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1 - (I_C/I_E)} = \frac{1}{1 - \alpha} \quad \dots(1.18.2)$$

4. Put values of eq. (1.18.1) in eq. (1.18.2)

$$\gamma = \frac{1}{1 - \alpha} = 1 + \beta$$

**Que 1.19.** Explain the operation of common collector configuration with suitable characteristics in detail.

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**Answer**

1. The circuit diagram for determining the static characteristics of an *npn* transistor in the common collector configuration is shown in Fig. 1.19.1.

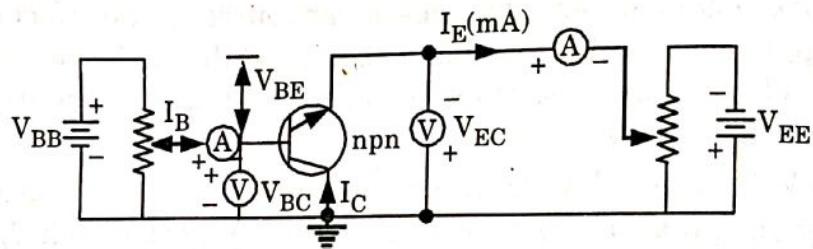


Fig. 1.19.1.

**Input characteristics :**

1. To determine the input characteristics,  $V_{EC}$  is kept at a suitable fixed value.
2. The base-collector voltage  $V_{BC}$  is increased in equal steps and the corresponding increase in  $I_B$  is noted.
3. This is repeated for different fixed values of  $V_{EC}$ . Plot of  $V_{BC}$  versus  $I_B$  for different values of  $V_{EC}$  is shown in Fig. 1.19.2.

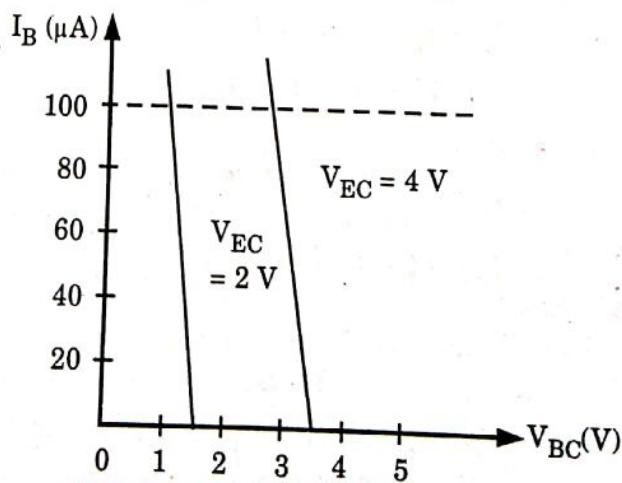


Fig. 1.19.2. Input characteristics.

**Output characteristics :**

1. The output characteristics shown in Fig. 1.19.3 are the plots of  $V_{EC}$  versus  $I_C$  for different values of  $I_B$ .

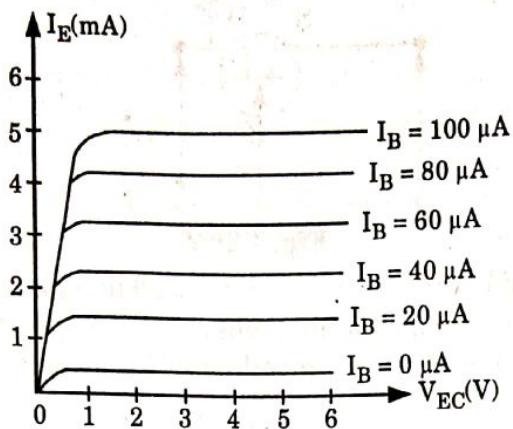


Fig. 1.19.3. Output characteristics.

**Que 1.20.** Discuss various configurations of FET with their features.

**Answer**

- There are three types of configuration.
- i. **Common source (CS) configuration :**
  1. In the CS configuration (similar to common emitter), the input is applied to the gate and its output is taken from the drain as shown in Fig. 1.20.1.
  2. This is the most common mode of operation of the FET due to its high input impedance and good voltage amplification.
  3. The common source mode is generally used for audio frequency amplifiers.
  4. The output signal is  $180^\circ$  out of phase with the input.

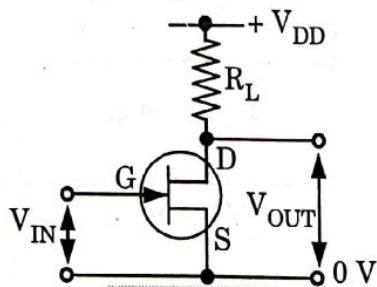
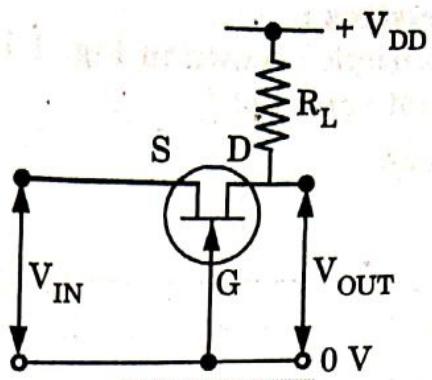


Fig. 1.20.1.

**Common Gate (CG) configuration :**

1. In the CG configuration (similar to common base), the input is applied to the source and its output is taken from the drain with the gate connected directly to ground (0 V) as shown in Fig. 1.20.2.
2. In this configuration, it has a low input impedance, but a high output impedance.

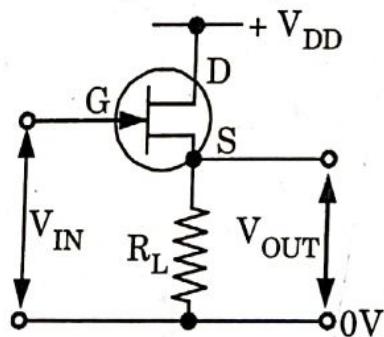


**Fig. 1.20.2.**

3. This type of FET configuration can be used in high frequency circuits or in impedance matching circuits where a low input impedance needs to be matched to a high output impedance. The output is in-phase with the input.

#### **Common Drain (CD) configuration :**

1. In the CD configuration (similar to common collector), the input is applied to the gate and its output is taken from the source.
2. The common drain or source follower configuration has a high input impedance and a low output impedance and near-unity voltage gain so therefore it is used in buffer amplifiers.
3. The voltage gain of the source follower configuration is less than unity, and the output signal is in-phase  $0^\circ$  with the input signal.
4. This type of configuration is referred to as common drain because there is no signal available at the drain connection, the voltage present,  $+V_{DD}$  just provides a bias. The output is in-phase with the input.



**Fig. 1.20.3.**

#### **PART-5**

*Small Signal Analysis, Low Frequency Transistor Models,  
Estimation of Voltage Gain, Input Resistance, Output Resistance etc.*

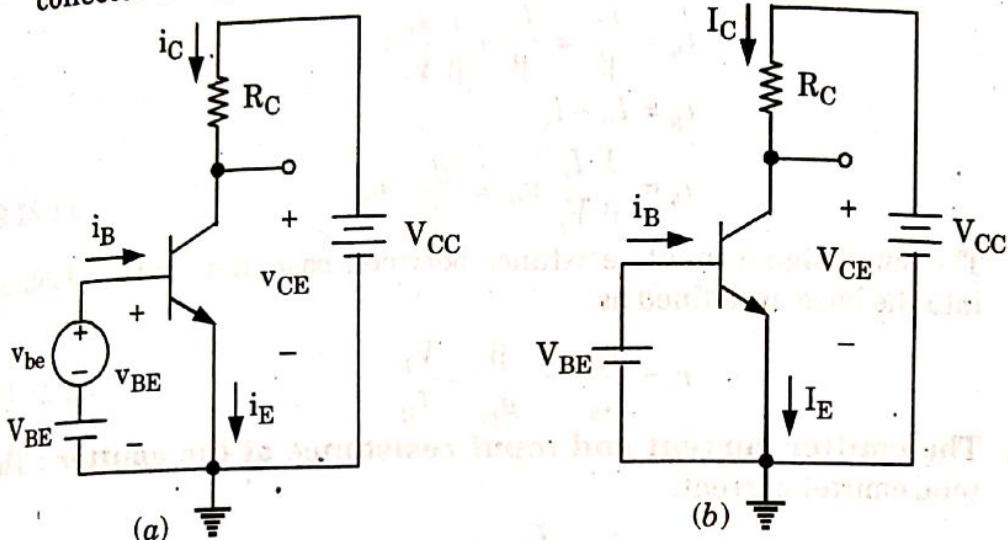
#### **Questions-Answers**

**Long Answer Type and Medium Answer Type Questions**

**Que 1.21:** Explain the small signal operation in BJT.

**Answer**

- Consider the conceptual circuit is shown in Fig. 1.21.1(a). Here the base-emitter junction is forward biased by a DC voltage  $V_{BE}$  and collector-base junction is reverse biased.



**Fig. 1.21.1. (a)** Conceptual circuit to illustrate the operation of the transistor as an amplifier; **(b)** The circuit of (a) for DC analysis.

- The input signal to be amplified is represented by the voltage source  $v_{be}$  that is superimposed on  $V_{BE}$ .
- For DC bias,  $v_{be}$  is zero. The circuit reduces as shown in Fig. 1.21.1(b), and following relationships are established :

$$I_C = I_S e^{V_{BE}/V_T} \quad \dots(1.21.1)$$

$$I_E = \frac{I_C}{\alpha} \quad \dots(1.21.2)$$

$$I_B = \frac{I_C}{\beta} \quad \dots(1.21.3)$$

$$V_C = V_{CE} = V_{CC} - I_C R_C \quad \dots(1.21.4)$$

- The collector current and the transconductance :** From

$$\text{Fig. 1.21.1(a)}, \quad v_{BE} = V_{BE} + v_{be}$$

$$\therefore i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}/V_T)} \cdot e^{(v_{be}/V_T)}$$

$$\text{using eq. (1.21.1), } i_C = I_C e^{v_{be}/V_T} \quad \dots(1.21.5)$$

if  $v_{be} \ll V_T$ ,

$$i_C = I_C \left( 1 + \frac{v_{be}}{V_T} \right) = I_C + \frac{I_C}{V_T} v_{be} \quad \dots(1.21.6)$$

thus, collector current composed of the DC bias value  $I_C$  and a small component  $i_c$ ,

$$i_c = \frac{I_C}{V_T} v_{be} = g_m v_{be} \quad \dots(1.21.7)$$

where,  $g_m = \frac{I_C}{V_T}$  = transconductance

- ii. **The base current and the input resistance at the base :** The total base current  $i_B$  using eq. (1.21.6) is given by

$$\begin{aligned} i_B &= \frac{i_c}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta} \frac{I_C}{V_T} v_{be} \\ i_B &= I_B + i_b \\ i_b &= \frac{1}{\beta} \frac{I_C}{V_T} v_{be} = \frac{g_m}{\beta} \cdot v_{be} \end{aligned} \quad \dots(1.21.9)$$

The small signal input resistance between base and emitter, looking into the base, is defined as,

$$r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{V_T}{I_B} \quad \dots(1.21.10)$$

- iii. **The emitter current and input resistance at the emitter :** The total emitter current,

$$\begin{aligned} i_E &= \frac{i_c}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha} \\ \text{and } i_E &= I_E + i_e \end{aligned}$$

$$\text{where, } i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be} \quad \dots(1.21.11)$$

The small signal resistance between base and emitter looking into the emitter is defined as,

$$r_e = \frac{v_{be}}{i_e} = \frac{V_T}{I_E} = \frac{\alpha}{g_m} = \frac{1}{g_m} \quad \dots(1.21.12)$$

The relationship between  $r_\pi$  and  $r_e$  can be found by eq. (1.21.10) and eq. (1.21.12), we get

$$v_{be} = i_b r_\pi = i_e r_e$$

$$\text{thus, } r_\pi = \left( \frac{i_e}{i_b} \right) r_e = (\beta + 1) r_e$$

- iv. **Voltage gain :**

From Fig. 1.21.1(a), the total collector voltage  $v_C$  will be

$$\begin{aligned} v_C &= V_{CC} - i_C R_C = V_{CC} - (I_C + i_c) R_C \\ &= (V_{CC} - I_C R_C) - i_c R_C = V_C - i_c R_C \end{aligned}$$

Here the quantity  $V_C$  is the DC bias voltage at the collector, and the signal voltage is given by

$$v_c = -i_c R_C = -g_m v_{be} R_C = -(g_m R_C) v_{be}$$

$$\text{thus, } A_v = \frac{v_c}{v_{be}} = -g_m R_C = -\frac{I_C R_C}{V_T} \quad \dots(1.21.13)$$

**Que 1.22.** Explain the hybrid- $\pi$  model of the *npn* transistor.

**Answer**

- Fig. 1.22.1, shows the expressions for the current increment ( $i_c$ ,  $i_b$ , and  $i_e$ ) obtained when a small signal  $v_{be}$  is applied.
- An equivalent circuit model for the BJT is shown in Fig. 1.22.2(a). This includes the input resistance looking into the base,  $r_\pi$ . The model obviously yields  $i_c = g_m v_{be}$  and  $i_b = v_{be}/r_\pi$ .
- At the emitter node we have,

$$i_e = \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}(1 + g_m r_\pi) = \frac{v_{be}}{r_\pi}(1 + \beta) = v_{be} \left( \frac{\frac{r_\pi}{1+\beta}}{r_\pi} \right) \quad \dots(1.22.1)$$

$$= v_{be} / r_e$$

- Expressing the current of the controlled source ( $g_m v_{be}$ ) in terms of the base current  $i_b$  as follows :

$$g_m v_{be} = g_m (i_b r_\pi) \quad \dots(1.22.2)$$

$$= (g_m r_\pi) i_b = \beta i_b$$

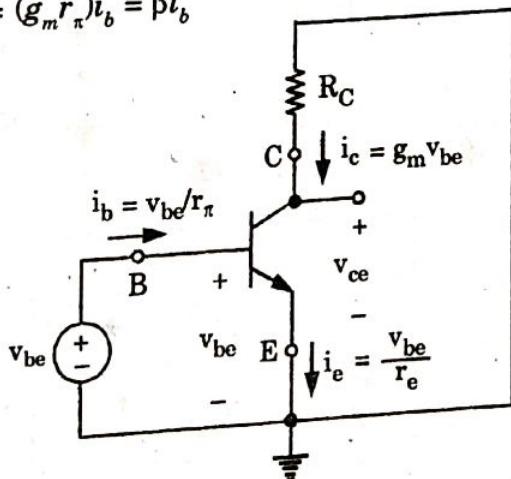


Fig. 1.22.1. The amplifier circuit with the DC sources ( $V_{BE}$  and  $V_{CC}$ ) eliminated (short circuited).

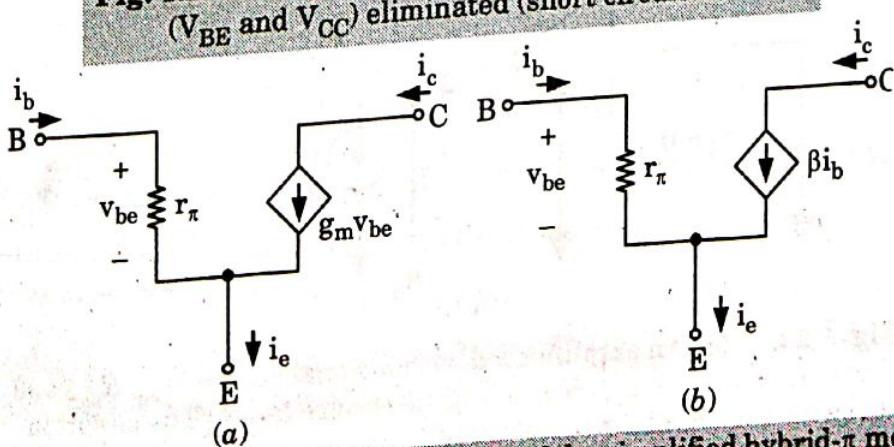


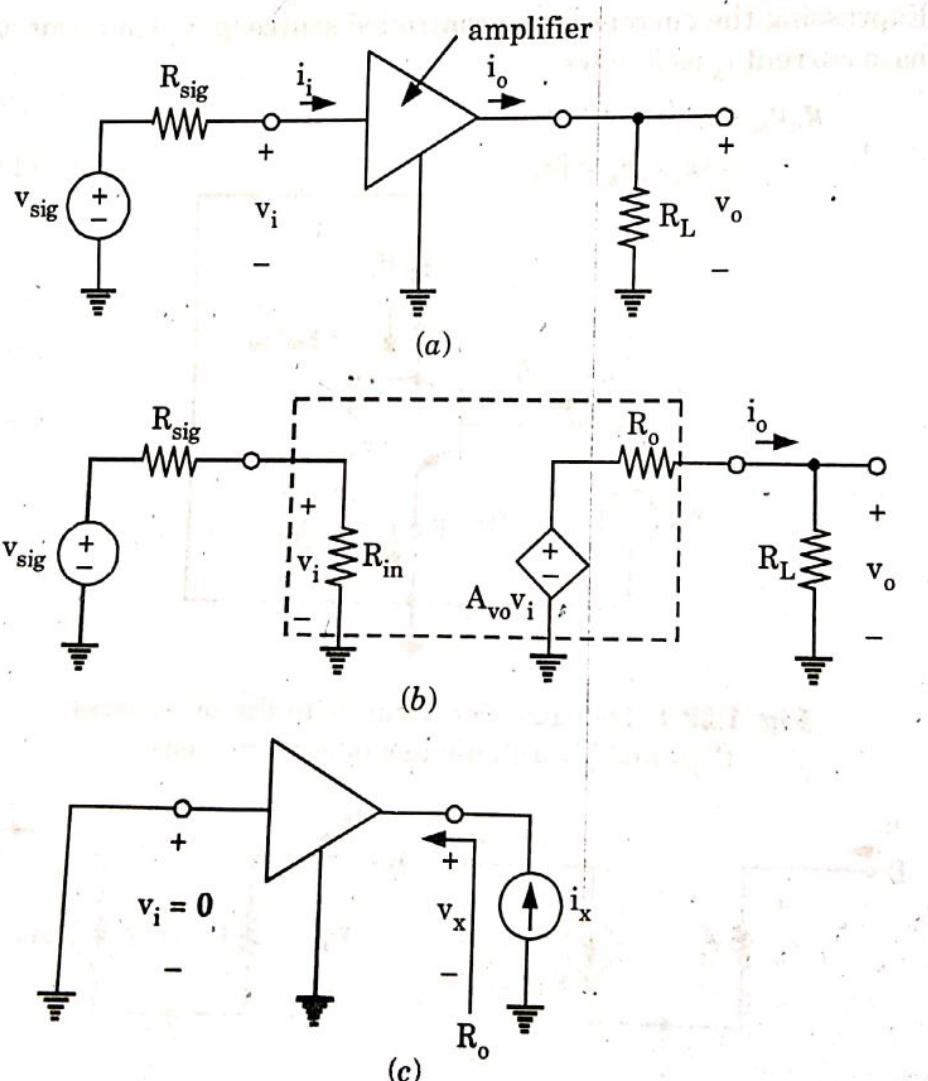
Fig. 1.22.2. Two slightly different versions of the simplified hybrid- $\pi$  model.

5. The result of eq. (1.22.2) in the alternative equivalent circuit model shown in Fig. 1.22.2(b). Hence the transistor is represented as a current-controlled current source, with the control current being  $i_b$ .
6. The two models of Fig. 1.22.2 are known as the hybrid- $\pi$  model. This is the most widely used model for the BJT.

**Que 1.23.** Draw the basic structure of single stage BJT amplifier and find out its characteristic parameters.

**Answer**

1. Fig. 1.23.1(a) shows an amplifier fed with a signal source having an open circuit voltage  $v_{sig}$  and an internal resistance  $R_{sig}$ . Fig. 1.23.1(b) shows the amplifier circuit with the amplifier block replaced by its equivalent circuit model.



**Fig. 1.23.1.** (a) An amplifier fed with a signal source ( $v_{sig}, R_{sig}$ ) and providing its output across a load resistance  $R_L$ . (b) The circuit in (a) with the amplifier represented by its equivalent circuit model. (c) Determining the output resistance  $R_o$  of the amplifier.

2. The input resistance  $R_{in}$  represents the loading effect of the amplifier input on the signal source.

$$R_{in} = \frac{v_i}{i_i}$$

$R_{in}$  and  $R_{sig}$  forms a voltage divider that reduces  $v_{sig}$  to the value  $v_i$

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig}$$

3. The second parameter for characterizing amplifier performance is the open circuit voltage gain  $A_{vo}$ , defined as

$$A_{vo} = \left. \frac{v_o}{v_i} \right|_{R_L = \infty}$$

4. The third and final parameter is the output resistance  $R_o$ . Observe from Fig. 1.23.1(c) that  $R_o$  is the resistance seen looking back into the amplifier output terminal with  $v_i$  set to zero.

$$R_o = \frac{v_x}{i_x}$$

Because  $R_o$  is determined with  $v_i = 0$ , its value does not depend on  $R_{sig}$ .

5. The controlled source  $A_{vo}v_i$  and the output resistance  $R_o$  represent the Thevenin's equivalent of the amplifier output circuit, and the output  $v_o$  will be

$$v_o = \frac{R_L}{R_L + R_o} A_{vo} v_i$$

6. Thus, the voltage gain of the amplifier,  $A_v$ , is

$$A_v = \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o}$$

7. The overall voltage gain  $G_v$ ,

$$G_v = \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} A_v$$

**Que 1.24.** Draw the small signal low frequency model of a BJT in CE configuration. Derive expression for the voltage gain of an emitter follower amplifier.

**Answer**

**Small signal low frequency model :**

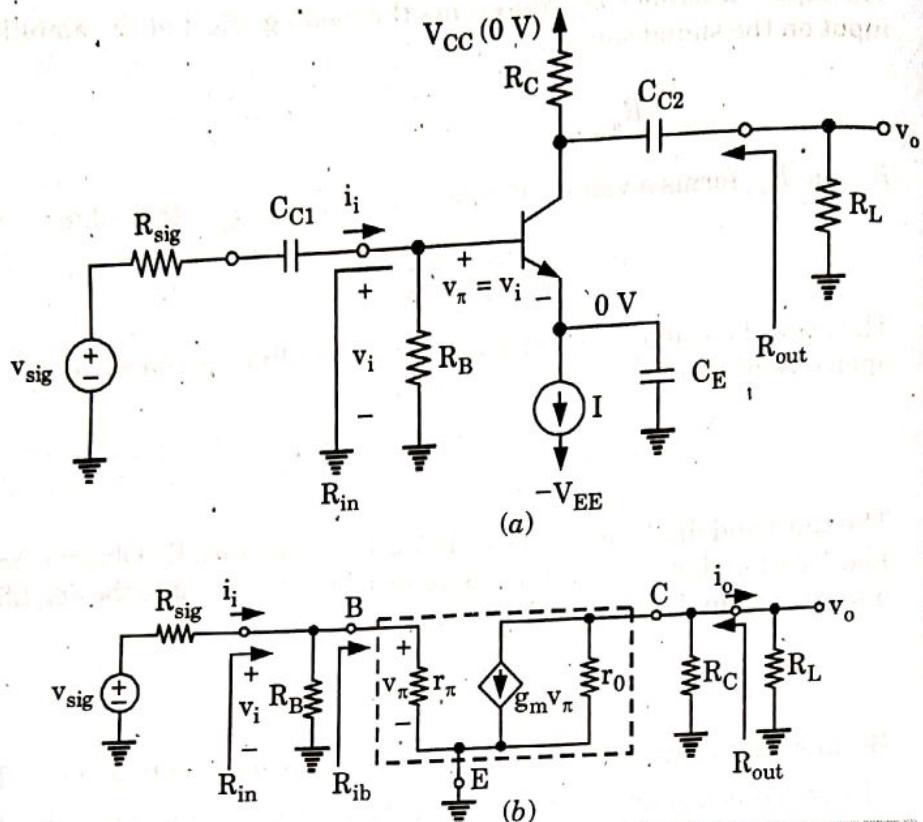


Fig. 1.24.1. (a) Small signal low frequency model of common emitter amplifier. (b) Equivalent circuit obtained by replacing the transistor with its hybrid- $\pi$  model.

#### Derivation :

- The equivalent circuit of emitter follower is given in Fig. 1.24.2(b). Collector is grounded with respect to the signal and  $V_{CC}$  is replaced by a short circuit.

$$i_o = -i_b - g_m v_{\pi} \quad \dots(1.24.1)$$

$$\text{and} \quad v_{\pi} = i_b r_{\pi} \quad \dots(1.24.2)$$

- Current gain,  $A_i = \frac{i_o}{i_b}$

Divide eq. (1.24.1) with  $i_b$ , we get

$$A_i = -1 - \frac{g_m v_{\pi}}{i_b} \quad [\because v_{\pi} = i_b r_{\pi}]$$

$$A_i = -(1 + g_m r_{\pi})$$

but  $\beta_o = g_m r_{\pi}$   
 where,  $\beta_o$  is the low frequency value of  $\beta$ .

$$A_i = \frac{i_o}{i_b} = -(1 + \beta_o) \quad \dots(1.24.3)$$

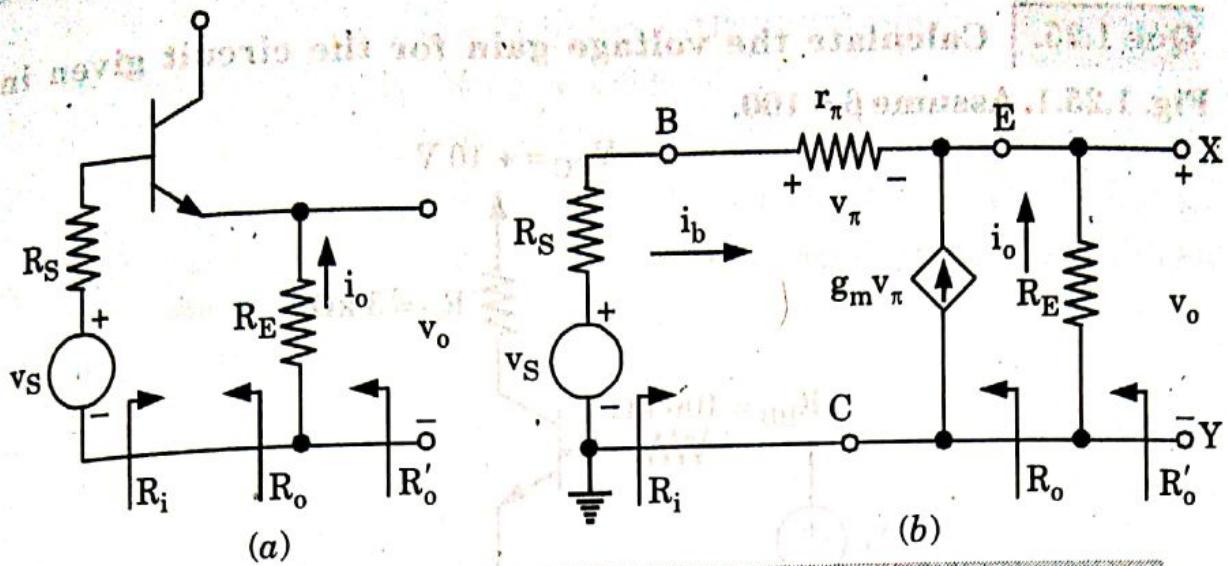


Fig. 1.24. (a) The common-collector (emitter follower) stage and  
(b) the low frequency equivalent circuit.

3. Input resistance,  $R_i = \frac{v_b}{i_b}$

4. From KVL for outer loop of Fig. 1.24.2(b),

$$v_b = i_b r_\pi - i_o R_E \quad \dots(1.24.4)$$

5. Substitute  $i_o$  from eq. (1.24.3), we get

$$v_b = i_b r_\pi + (\beta_o + 1) i_b R_E \quad \dots(1.24.5)$$

6. Divide eq. (1.24.5) by  $i_b$ , we get

$$\frac{v_b}{i_b} = R_i = r_\pi + (\beta_o + 1) R_E$$

7. The output voltage,

$$v_o = -i_o R_E = (1 + \beta_o) i_b R_E \quad \dots(1.24.6)$$

8. Since  $v_s = i_b R_S + v_b$

From eq. (1.24.4), eq. (1.24.6) can be written as,

$$v_s = i_b R_S + i_b r_\pi - i_o R_E$$

9. The voltage gain,

$$A_v = \frac{v_o}{v_s} = \frac{(1 + \beta_o) i_b R_E}{i_b R_S + i_b r_\pi - i_o R_E}$$

$$A_v = \frac{(1 + \beta_o) i_b R_E}{i_b [R_S + r_\pi + (1 + \beta_o) R_E]}$$

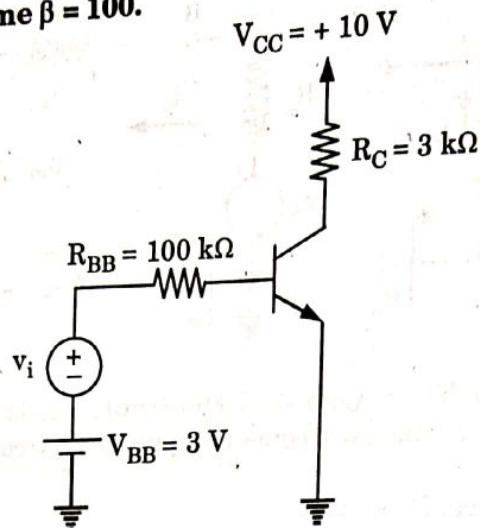
$$= \frac{(1 + \beta_o) R_E}{R_S + r_\pi + (1 + \beta_o) R_E} \quad \dots(1.24.7)$$

10. Putting,  $R_i = r_\pi + (1 + \beta_o) R_E$  in eq. (1.24.7), we get

$$A_v = \frac{(1 + \beta_o) R_E}{R_S + R_i}$$

**Que 1.25.** Calculate the voltage gain for the circuit given in

**Fig. 1.25.1.** Assume  $\beta = 100$ .



**Fig. 1.25.1.**

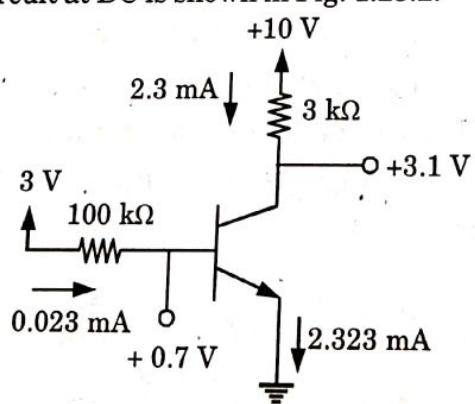
**AKTU 2014-15, Marks 10**

**Answer**

**Given :**  $\beta = 100$

**To Find :**  $\frac{v_o}{v_i}$

1. To determine the quiescent operating point, assume  $v_i = 0$ . Analysis of circuit at DC is shown in Fig. 1.25.2.



**Fig. 1.25.2.**

2. The DC base current will be

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}} = \frac{3 - 0.7}{100 \text{ k}\Omega} = 0.023 \text{ mA}$$

3. The DC collector current will be

$$I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA}$$

4. The DC voltage at the collector will be

$$\begin{aligned} V_C &= V_{CC} - I_C R_C \\ &= +10 - 2.3 \times 3 = +3.1 \text{ V} \end{aligned}$$

5. Since  $V_B = +0.7 \text{ V}$ , it follows that in the quiescent the transistor will be operating in the active mode.

#### Small signal parameters :

1. Fig. 1.25.3 shows small signal model of given circuit shown in Fig. 1.25.1.

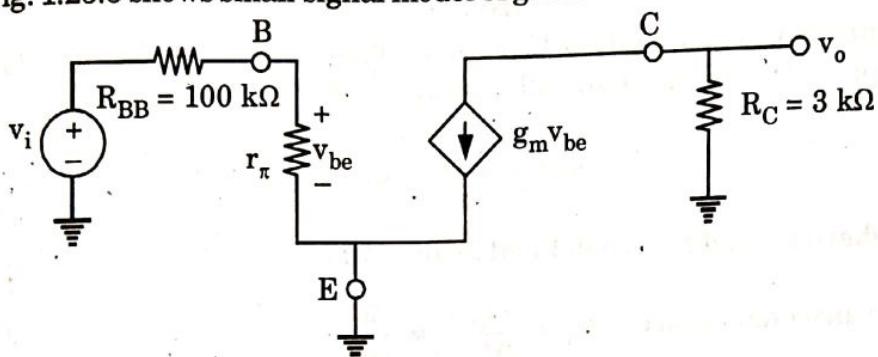


Fig. 1.25.3.

$$2. g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V}$$

$$3. r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega$$

4. From Fig. 1.25.3,

$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}} = v_i \frac{1.09}{101.09} = 0.011 v_i$$

5. The output voltage  $v_o$  is given by

$$\begin{aligned} v_o &= -g_m v_{be} R_C \\ &= -92 \times 0.011 v_i \times 3 = -3.04 v_i \end{aligned}$$

6. Thus, the voltage gain will be

$$\frac{v_o}{v_i} = -3.04$$

Negative sign shows phase reversal.

**Que 1.26.** Explain small-signal model of FET.

**Answer**

1. If  $i_D$  is taken as the dependent variable, then

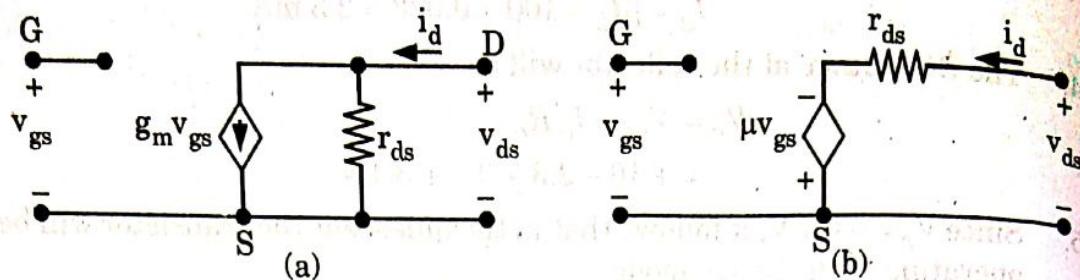


Fig. 1.26.1. Small-signal model for the CS FET.

$$i_D = f(v_{GS}, v_{DS}) \quad \dots(1.26.1)$$

2. For small excursions (AC signals) about the  $Q$  point,  $\Delta i_D = i_d$ , thus, application of the chain rule to (1.26.1) leads to

$$i_d = \Delta i_D \approx di_D = g_m v_{gs} + \frac{1}{r_{ds}} v_{ds} \quad \dots(1.26.2)$$

where  $g_m$  and  $r_{ds}$  are defined as follows :

$$\text{Transconductance } g_m \equiv \left. \frac{\partial i_D}{\partial V_{GS}} \right|_Q \approx \left. \frac{\Delta i_D}{\Delta v_{GS}} \right|_Q \quad \dots(1.26.3)$$

$$\text{Source-drain resistance } r_{ds} \equiv \left. \frac{\partial v_{DS}}{\partial i_D} \right|_Q \approx \left. \frac{\Delta v_{DS}}{\Delta i_D} \right|_Q \quad \dots(1.26.4)$$

3. As long as the JFET is operated in the pinchoff region,  $i_G = i_g = 0$ , so that the gate acts as an open circuit.
4. This, along with eq. (1.26.2), leads to the current-source equivalent circuit of Fig. 1.26.1. Either of these models may be used in analyzing an amplifier, but one may be more efficient than the other in a particular circuit.

**Que 1.27.** Show that the transconductance  $g_m$  of JFET is related to drain current  $I_{DS}$  by

$$g_m = \frac{2}{|V_p|} \sqrt{I_{DSS} I_{DS}}$$

**Answer**

1. As we know, the saturation drain current,  $I_{DS}$  is given by

$$I_{DS} = I_{DSS} \left( 1 - \frac{V_{GS}}{V_p} \right)^2 \quad \dots(1.27.1)$$

where  $V_p$  is pinch-off voltage and  $I_{DSS}$  is the value of  $I_{DS}$  when  $V_{GS} = 0$ .

2. Differentiating eq. (1.27.1) with respect to  $V_{GS}$ , we get

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2 \left( 1 - \frac{V_{GS}}{V_p} \right) \left( -\frac{1}{V_p} \right)$$

3. We know that,  $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$ ,  $V_{DS}$  is constant

$$g_m = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right) \quad \dots(1.27.2)$$

4. From eq. (1.27.1), we have

$$\left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

5. Substituting this value in eq. (1.27.2), we get

$$g_m = \frac{-2I_{DSS}}{V_P} \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

$$g_m = \frac{-2}{V_P} \sqrt{\frac{(I_{DSS})^2 I_{DS}}{I_{DSS}}} = \frac{2}{|V_P|} \sqrt{I_{DSS} I_{DS}}$$

[ $\because V_P$  may be positive or negative]

**Que 1.28.** Draw common source (CS) amplifier and find expressions for voltage gain, input impedance and output impedance.

**Answer**

Circuit diagram of common-source amplifier :

**Voltage gain  $A_V$ :**

- In this amplifier,  $R_s$  is used to set the Q-point but is bypassed by  $C_s$  for mid frequency operation.
- From small signal equivalent circuit, the output voltage

$$V_o = \frac{-R_D}{R_D + r_d} (\mu V_{gs})$$

where  $V_{gs} = V_i$ , input voltage.

- Hence, voltage gain,

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d}$$

Here, minus sign indicates a  $180^\circ$  phase shift between  $V_i$  and  $V_o$ .

**Input impedance :**

- From Fig. 1.28.1(b) the input impedance is

$$Z_i = R_g$$

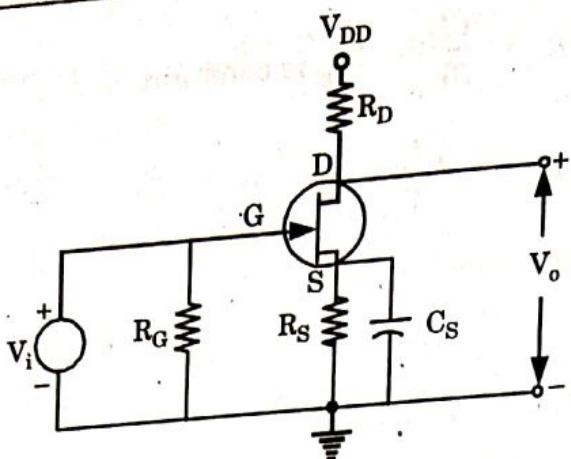


Fig. 1.28.1. (a) Common source amplifier.

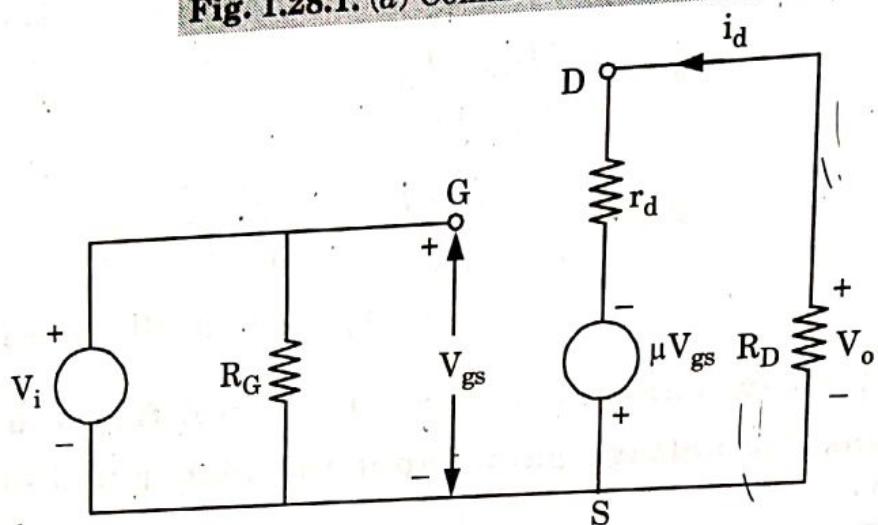


Fig. 1.28.1. (b) Small signal equivalent circuit of CS amplifier.

#### Output impedance :

1. Output impedance is the impedance measured at output terminals with  $V_i = 0$ .
2. In Fig. 1.28.1(b), if  $V_i = 0$ ;  $V_{gs} = 0$ .  
then  $\mu V_{gs} = 0$
3. Now, output impedance is given by  
$$Z_o = r_d || R_D$$
4. Normally,  
$$r_d \gg R_D$$
  
$$\therefore Z_o \approx R_D$$

#### PART-6

Design Procedure For Particular Specifications,  
Low Frequency Analysis of Multistage Amplifier.

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 1.29.** Explain the cascade amplifiers. Write advantages of multistage over single stage amplifier.

**Answer**

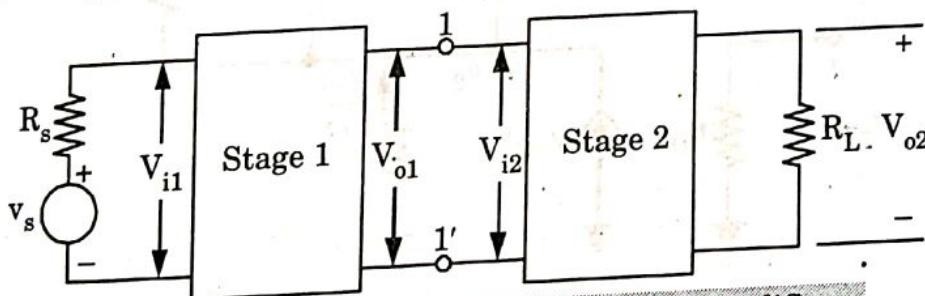
1. A multistage amplifier using two or more single stage common emitter amplifier is called as cascaded amplifier.
2. Fig. 1.29.1 shows the block diagram of two stage cascaded amplifier. These stages are connected such that the output of the first stage is connected to the input of the second stage.
3. As shown in the Fig. 1.29.1  $V_{i1}$  is the input of the first stage and  $V_{o2}$  is the output of the second stage.
4. Therefore,  $V_{o2}/V_{i1}$  is the overall voltage gain of two stage amplifier and it can be given as,

$$A_v = \frac{V_{o2}}{V_{i1}} = \frac{V_{o2}}{V_{i2}} \frac{V_{i2}}{V_{i1}}$$

We know that,  $V_{o1} = V_{i2}$

$$A_v = \frac{V_{o2}}{V_{i2}} \frac{V_{o1}}{V_{i1}}$$

So that, we can say the voltage gain of multistage amplifier is the product of voltage gains of the individual stages.



**Fig. 1.29.1. Block diagram of two cascade amplifier.**

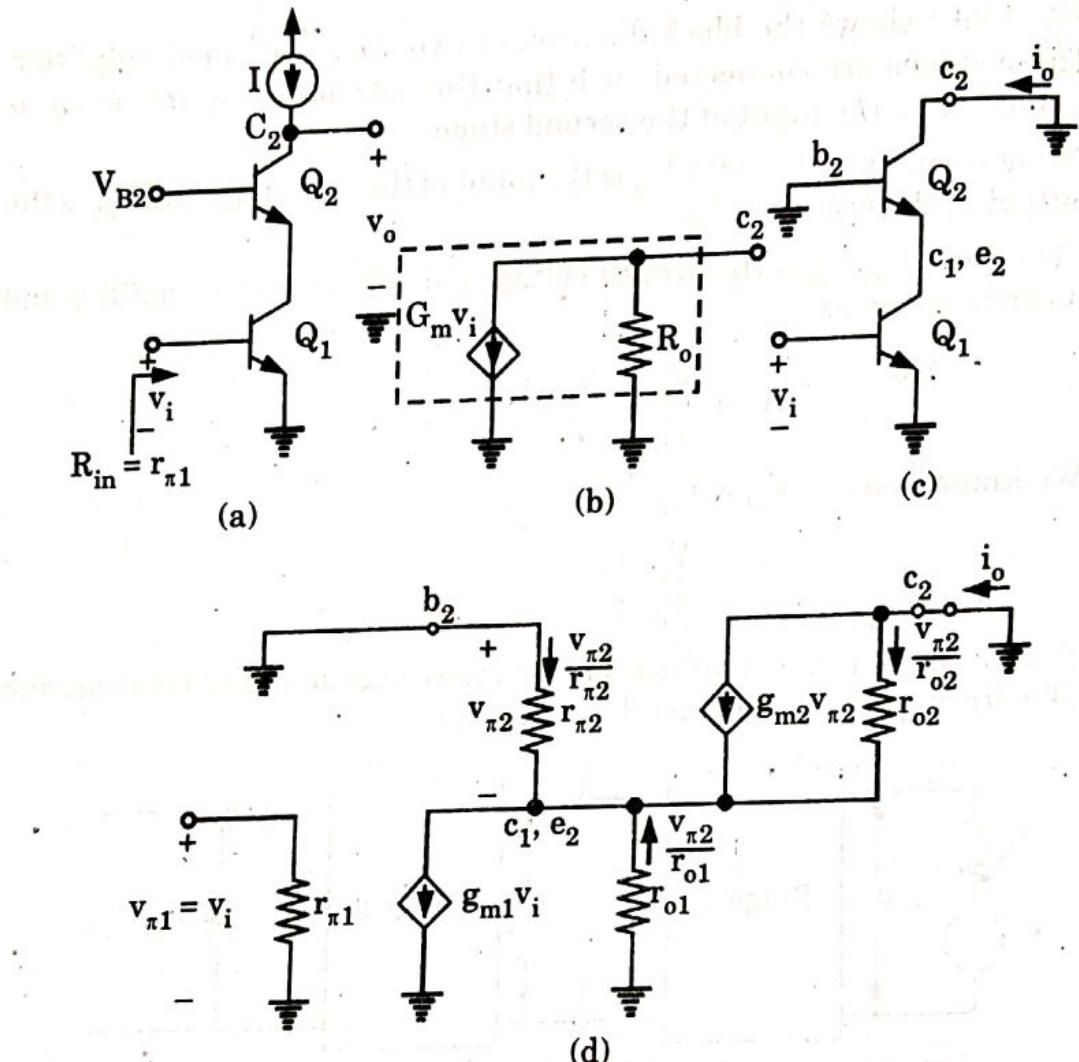
**Advantages :**

1. The gain that is realized by a single-stage circuit may not be sufficient for the particular purpose.
2. In addition, the input and output resistances may not be the correct magnitudes for the intended application.
3. To overcome these limitations, two or more stages can be connected in cascade; thus, the output of one stage is connected to the input of the next stage.

**Que 1.30.** Draw and explain the BJT cascode amplifier.

**Answer****The BJT cascode :**

1. Fig. 1.30.1(a) shows the BJT cascode amplifier with an ideal current-source load. Voltage  $V_{B2}$  is a DC bias voltage for the CB cascode transistor  $Q_2$ .



**Fig. 1.30.1.** (a) A BJT cascode amplifier with an ideal current-source load; (b) small-signal equivalent-circuit representation of the output of the cascode amplifier; (c) the cascode amplifier with the output short-circuited to ground, and (d) equivalent circuit representation of (c).

2.  $G_m$  is the short-circuit transconductance and can be determined from the circuit in Fig. 1.30.1(c).
3. The transconductance  $G_m$  can be determined as

$$G_m = \frac{i_o}{v_i}$$

Replacing  $Q_1$  and  $Q_2$  with their hybrid- $\pi$  equivalent models gives rise to the circuit in Fig. 1.30.1(d).

4. The voltage at the node ( $c_1, e_2$ ) is seen to be  $-v_{\pi 2}$ . Thus we can write a node equation for ( $c_1, e_2$ ) as

$$g_{m2}v_{\pi 2} + \frac{v_{\pi 2}}{r_{o1}} + \frac{v_{\pi 2}}{r_{o2}} + \frac{v_{\pi 2}}{r_{\pi 2}} = g_{m1}v_i$$

5. Since  $g_{m2} \gg (1/r_{\pi 2})$ ,  $1/r_{o1}$  and  $1/r_{o2}$ , we can neglect all the terms beyond the first on the left-hand side to obtain

$$g_{m2}v_{\pi 2} = g_{m1}v_i$$

6. Next, we write a node equation at  $c_2$ ,

$$i_o = g_{m2}v_{\pi 2} + \frac{v_{\pi 2}}{r_{o2}}$$

and again neglect the second term on the right-hand side to obtain

$$i_o = g_{m2}v_{\pi 2}$$

7. Using eq. (1.30.1) result in

$$i_o = g_{m1}v_i$$

Thus,  $G_m = g_{m1}$

8. To obtain  $R_o$ , we set  $v_i = 0$ , which result in  $Q_1$  being reduced to its output resistance  $r_{o1}$ , which appears in the emitter lead of  $Q_2$  as shown in Fig. 1.30.2(a). Here we have applied a test voltage  $v_x$  and will determine  $R_o$  as

$$R_o = \frac{v_x}{i_x}$$

9. The voltage at the emitter node,  $-v_{\pi 2}$ , can be found as

$$-v_{\pi 2} = i_x(r_{o1} || r_{\pi 2}) \quad \dots(1.30.2)$$

10. Next we write a loop equation around the  $c_2 - e_2 - \text{ground}$  loop as

$$v_x = (i_x - g_{m2}v_{\pi 2})r_{o2} + i_x(r_{o1} || r_{\pi 2})$$

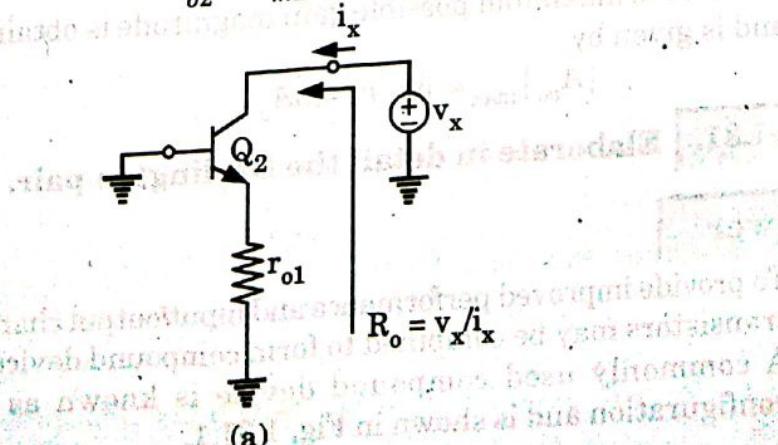
Substituting for  $v_{\pi 2}$  from eq. (1.30.2) and collecting terms, we find

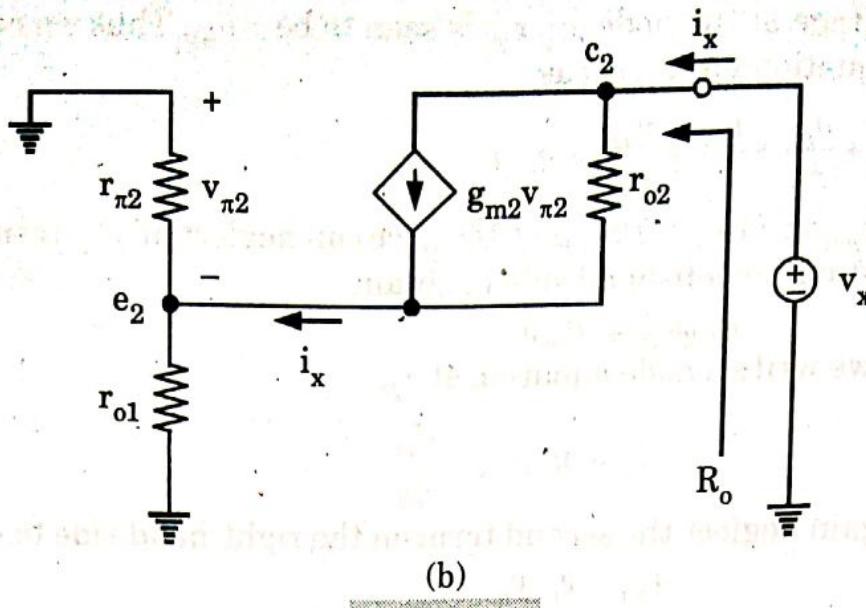
$$R_o = v_x/i_x \text{ as}$$

$$R_o = r_{o2} + (r_{o1} || r_{\pi 2}) + (g_{m2}r_{o2})(r_{o1} || r_{\pi 2}) \quad \dots(1.30.3)$$

which can be written as

$$\begin{aligned} R_o &= r_{o2} + (g_{m2}r_{o2} + 1)(r_{o1} || r_{\pi 2}) \\ &= r_{o2} + (g_{m2}r_{o2})(r_{o1} || r_{\pi 2}) \end{aligned} \quad \dots(1.30.4)$$





(b)

Fig. 1.30.2.

11. Since  $g_{m2}(r_{o1} \parallel r_{\pi 2}) \gg 1$ , we can neglect the first term on the right-hand side of eq. (1.30.4)

$$R_o = (g_{m2}r_{o2})(r_{o1} \parallel r_{\pi 2})$$

12. Because  $(r_{o1} \parallel r_{\pi 2})$  will always be lower than  $r_{\pi 2}$ , it follows that the maximum possible value of  $R_o$  is

$$\begin{aligned} R_o|_{\max} &= g_{m2}r_{o2}r_{\pi 2} \\ &= (g_{m2}r_{\pi 2})r_{o2} = \beta_2 r_{o2} \end{aligned} \quad \dots(1.30.5)$$

Thus the maximum output resistance realizable by cascoding is  $\beta_2 r_{o2}$ .

13. Having determined  $G_m$  and  $R_o$ , we can now find the open circuit voltage gain of the bipolar cascode as

$$A_{vo} = \frac{v_o}{v_i} = -G_m R_o$$

Thus,

$$A_{vo} = -g_{m1}(g_{m2}r_{o2})(r_{o1} \parallel r_{\pi 2}) \quad \dots(1.30.6)$$

For the case  $g_{m1} = g_{m2}$ ,  $r_{o1} = r_{o2} = r_o$

$$A_{vo} = -(g_m r_o)[(g_m(r_o \parallel r_\pi))] \quad \dots(1.30.7)$$

which will be less than  $(g_m r_o)$  in magnitude.

14. In fact, the maximum possible gain magnitude is obtained when  $r_o \gg r_\pi$  and is given by

$$|A_{vo}|_{\max} = \beta g_m r_o = \beta A_o$$

**Que 1.31.** Elaborate in detail the Darlington pair.

### Answer

- To provide improved performance and input/output characteristics, single transistors may be combined to form compound devices.
- A commonly used compound device is known as the Darlington configuration and is shown in Fig. 1.31.1.

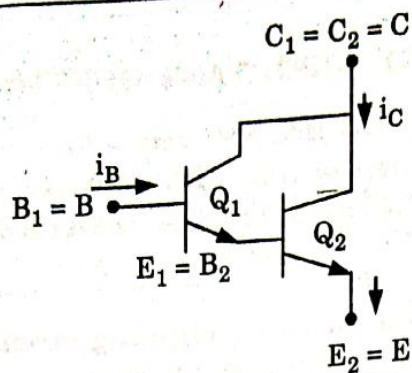


Fig. 1.31.1.

3. In this representation, two *n*p*n* BJTs are cascaded and are behaviorally equivalent to a single *n*p*n* transistor.
4. This single compound device possesses desirable characteristics such as high input impedance, low output impedance and high current gain; but does have the disadvantages of an almost doubled  $V_{BE}$  (overall  $V_{BE}$  for the pair is 1.2 V to 1.4 V instead of the 0.6 V to 0.7 V for single silicon BJTs).
5. A Darlington pair may also be created using two *p*n*p* devices, particularly in discrete circuit design, or through the use of an *n*p*n* and a *p*n*p*.
6. The resulting compound device may be considered a single transistor and, will be used in either the CE or CC configuration.
7. Assuming  $r_{01}$  and  $r_{02}$  are very large so that they may be neglected, and that  $\beta_1$  and  $\beta_2$  are both much greater than one (*i.e.*,  $\beta_1 = \alpha_1 + 1$  and  $\beta_2 = \alpha_2 + 1$ ), the AC small signal model of the *n*p*n* version of the Darlington pair is shown in Fig. 1.32.2.

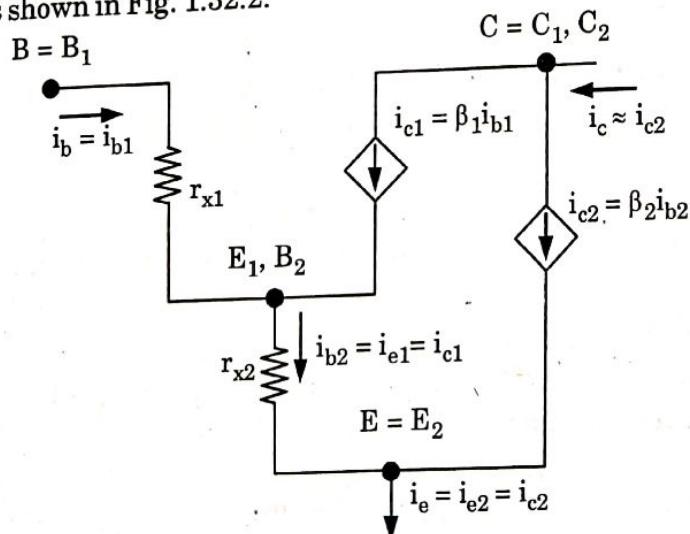


Fig. 1.31.2.

8. By making the assumption that emitter currents are approximately equal to collector currents (*i.e.*,  $\alpha_1 = \alpha_2 = 1$ ) :
$$i_e = i_{e2} = \beta_2 i_{b2} = \beta_2 i_{e1} = \beta_2 \beta_1 i_{b1},$$
9. We can see that the combination looks like a single high  $\beta$  ( $\beta = \beta_1 \beta_2$ ) transistor.

## VERY IMPORTANT QUESTIONS

*Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.*

**Q. 1. What do you mean by clipping circuits ? What are the different types of clipper circuits ?**

**Ans:** Refer Q. 1.3.

**Q. 2. Draw and discuss voltage tripler circuit.**

**Ans:** Refer Q. 1.5.

**Q. 3. Explain the operation of voltage divider bias circuit and write down the approximate equations of  $V_B$ ,  $I_E$ ,  $I_C$  and  $V_{CE}$ .**

**Ans:** Refer Q. 1.10.

**Q. 4. Draw and explain the input and output characteristics of common emitter configuration.**

**Ans:** Refer Q. 1.17.

**Q. 5. Explain the operation of common collector configuration with suitable characteristics in detail.**

**Ans:** Refer Q. 1.19.

**Q. 6. Explain the hybrid- $\pi$  model of the  $npn$  transistor.**

**Ans:** Refer Q. 1.22.

**Q. 7. Draw the basic structure of single stage BJT amplifier and find out its characteristic parameters.**

**Ans:** Refer Q. 1.23.

**Q. 8. Draw the small signal low frequency model of a BJT in CE configuration. Derive expression for the voltage gain of an emitter follower amplifier.**

**Ans:** Refer Q. 1.24.

**Q. 9. Show that the transconductance  $g_m$  of JFET is related to drain current  $I_{DS}$  by**

$$g_m = \frac{2}{|V_P|} \sqrt{I_{DSS} I_{DS}}$$

**Ans:** Refer Q. 1.27.

**Q. 10. Draw and explain the BJT cascode amplifier.**

**Ans:** Refer Q. 1.30.



**PART- 1***High Frequency Transistor Models.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 2.1.** Draw the equivalent circuit of BJT at high frequency and derive the expression for upper cut-off frequency.

**OR**

Draw the high frequency equivalent circuit for the typical *RC* coupled common emitter amplifier.

**AKTU 2014-15, Marks 05**

**Answer**

1. High frequency equivalent circuit for *CE* configuration is shown in Fig. 2.1.1(a).
2. The equivalent circuit of Fig. 2.1.1(a) can be simplified by utilizing Thevenin's theorem at the input side and by combining the three parallel resistances at the output side.
3. Thevenin's theorem simplifies the resistive network at the input side to a signal generator  $V'_{\text{sig}}$  and a resistance  $R'_{\text{sig}}$

where, 
$$V'_{\text{sig}} = V_{\text{sig}} \frac{R_B}{R_B + R_{\text{sig}}} \frac{r_\pi}{r_\pi + r_x + (R_{\text{sig}} \parallel R_B)} \quad \dots(2.1.1)$$

$$R'_{\text{sig}} = r_\pi \parallel [r_x + (R_B \parallel R_{\text{sig}})] \quad \dots(2.1.2)$$

4.  $V_o$  can be approximately given by

$$V_o = -g_m V_R' L = -g_m R'_L V_\pi \quad \dots(2.1.3)$$

where  $R'_L = r_o \parallel R_C \parallel R_L$

5. The current  $I_\mu$  can be found from

$$\begin{aligned} I_\mu &= sC_\mu(V_\pi - V_o) \\ &= sC_\mu[V_\pi - (-g_m R'_L V_\pi)] \\ &= sC_\mu(1 + g_m R'_L)V_\pi \end{aligned}$$

6. Now, in Fig. 2.1.1(b), the left hand side of the circuit, at  $XX'$ , knows of the existence of  $C_\mu$  only through the current  $I_\mu$ . Therefore we can replace  $C_\mu$  by an equivalent capacitance  $C_{\text{eq}}$  between  $B'$  and ground as long as  $C_{\text{eq}}$  draws a current equal to  $I_\mu$ , i.e.,

$$sC_{\text{eq}} V_\pi = I_\mu = sC_\mu(1 + g_m R'_L)V_\pi$$

$$C_{\text{eq}} = C_\mu(1 + g_m R'_L)$$

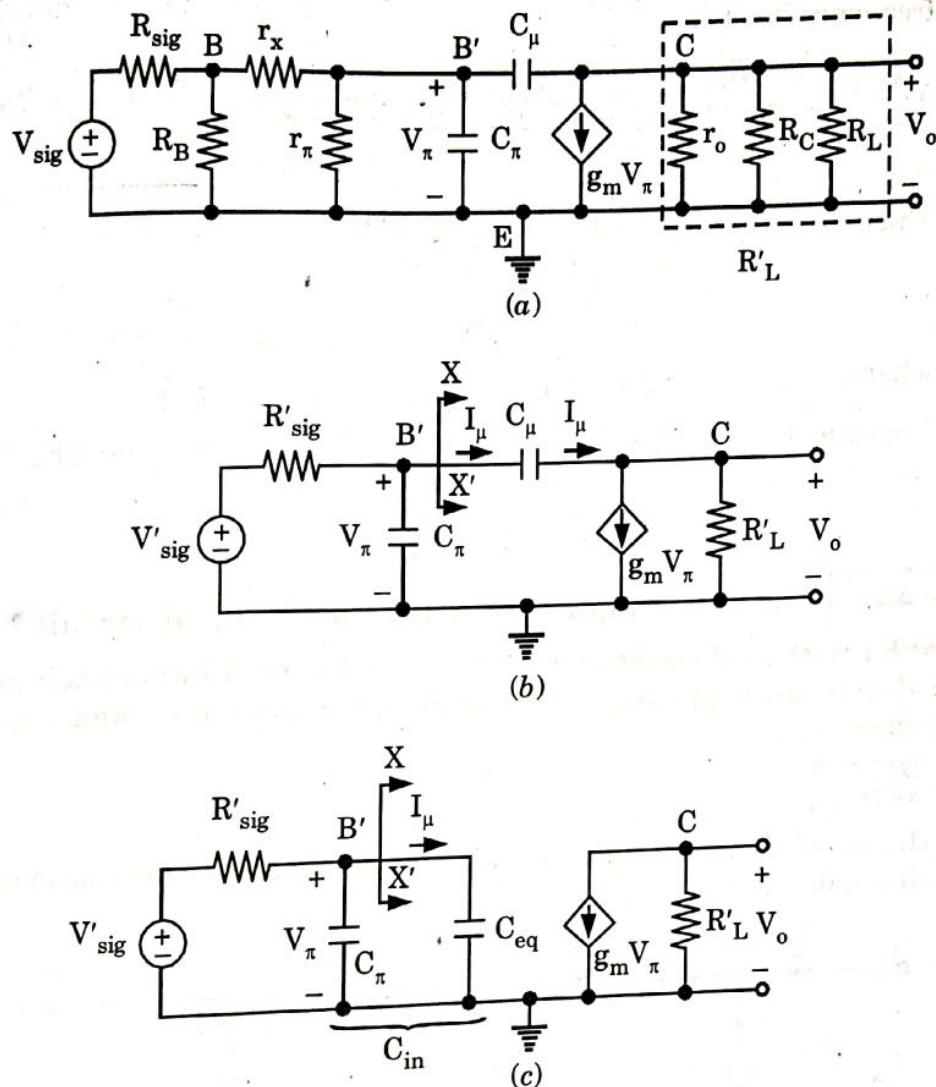


Fig. 2.1.1.

7.  $C_{eq}$  is used to simplify the equivalent circuit at the input side to that shown in Fig. 2.1.1(c). Therefore we can express  $V_\pi$  in terms of  $V'_{sig}$  as

$$V_\pi = V'_{sig} \frac{1}{1 + s/\omega_0} \quad \dots(2.1.4)$$

where,  $\omega_0$  is the corner frequency of STC (single time constant) network composed of  $C_{in}$  and  $R'_{sig}$ ,

$$\omega_0 = 1/C_{in} R'_{sig}$$

where,  $C_{in}$  is the total input capacitance at  $B'$ ,

$$C_{in} = C_\pi + C_{eq} = C_\pi + C_\mu (1 + g_m R'_L)$$

and  $R'_{sig}$  is the effective source resistance, given by eq. (2.1.2).

8. Combining eq. (2.1.3), (2.1.4) and (2.1.1) give the voltage gain in the high frequency band as

$$\frac{V_o}{V_{\text{sig}}} = - \left[ \frac{R_B}{R_B + R_{\text{sig}}} \frac{r_n g_m R'_L}{r_n + r_x + (R_{\text{sig}} \parallel R_B)} \right] \left( \frac{1}{1 + \frac{s}{\omega_o}} \right) \quad \dots(2.1.5)$$

Thus,  $\frac{V_o}{V_{\text{sig}}} = \left( \frac{A_M}{1 + \frac{s}{\omega_o}} \right)$

where,  $A_M = - \left[ \frac{R_B}{R_B + R_{\text{sig}}} \frac{r_n g_m R'_L}{r_n + r_x + (R_{\text{sig}} \parallel R_B)} \right]$

from which we deduce that the upper 3-dB frequency  $f_H$  must be

$$f_H = \frac{\omega_o}{2\pi} = \frac{1}{2\pi C_{\text{in}} R'_{\text{sig}}}$$

**Que 2.2.** Draw the high frequency small signal circuit of a MOSFET with load resistance using the effect of Miller capacitance. Also derive an expression for the Miller capacitance and cut-off frequency ( $f_T$ ).

### Answer

1. High frequency small signal circuit of a MOSFET with load resistance is shown in Fig. 2.2.1.

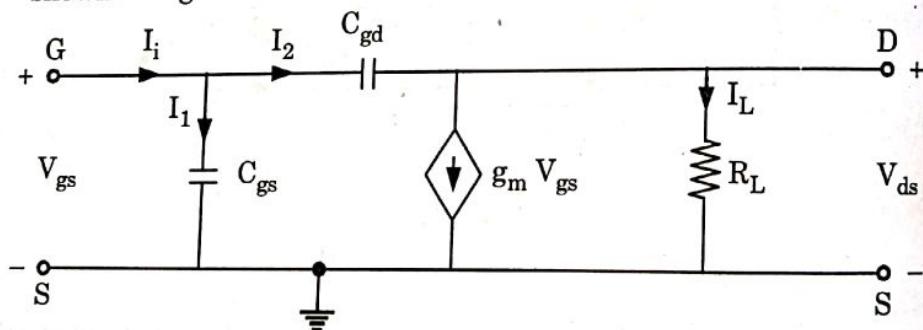


Fig. 2.2.1.

2. To obtain the expression for current gain, apply KCL at input node.

$$I_i = I_1 + I_2$$

$$I_i = j\omega C_{gs} V_{gs} + j\omega C_{gd} (V_{gs} - V_{ds}) \quad \dots(2.2.1)$$

3. Apply KCL at output node, we get

$$I_2 = g_m V_{gs} + I_L$$

$$\therefore j\omega C_{gd} (V_{gs} - V_{ds}) = g_m V_{gs} + \frac{V_{ds}}{R_L} \quad \dots(2.2.2)$$

$$\therefore g_m V_{gs} + \frac{V_{ds}}{R_L} + j\omega C_{gd} (V_{ds} - V_{gs}) = 0 \quad \dots(2.2.3)$$

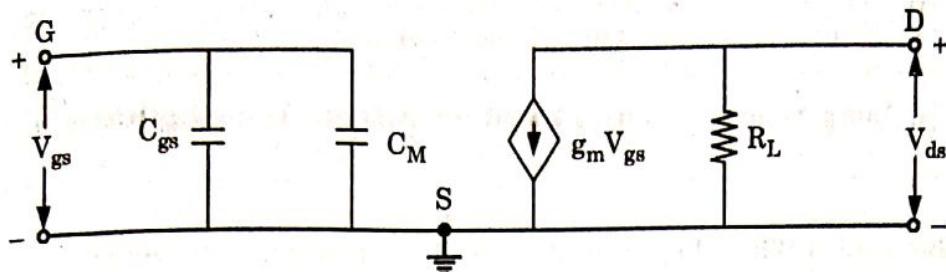


Fig. 2.2.2.

4. From eq. (2.2.1) and eq. (2.2.3)

$$I_i = j\omega \left\{ C_{gs} + C_{gd} \left[ \frac{1 + g_m R_L}{1 + j\omega R_L C_{gd}} \right] \right\} V_{gs} \quad \dots(2.2.4)$$

But generally  $(\omega R_L C_{gd}) \ll 1$ , hence we can neglect this term, therefore,

$$I_i = j\omega \{ [C_{gs} + C_{gd}] (1 + g_m R_L) \} V_{gs} \quad \dots(2.2.5)$$

5. From Fig. 2.2.2, Miller capacitance  $C_M$  can be defined as

$$C_M = C_{gd} (1 + g_m R_L) \quad \dots(2.2.6)$$

6. The input current  $I_i$  can be expressed as

$$I_i = j\omega (C_{gs} + C_M) V_{gs}$$

**Cut-off frequency :** The cut-off frequency of MOSFET ( $f_T$ ) is defined as the frequency at which the current gain magnitude is unity or when the input current  $I_i$  is equal to  $I_d$ .

$$\text{But, } I_i = j\omega (C_{gs} + C_M) V_{gs}$$

$$I_d = g_m V_{gs}$$

$$|A_i| = \left| \frac{I_d}{I_i} \right| = \frac{g_m V_{gs}}{\omega (C_{gs} + C_M) V_{gs}}$$

$$|A_i| = \frac{g_m}{2\pi f (C_{gs} + C_M)}$$

At

$$f = f_T, |A_i| = 1$$

$$1 = \frac{g_m}{2\pi f_T (C_{gs} + C_M)}$$

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_M)} = \frac{g_m}{2\pi C_G}$$

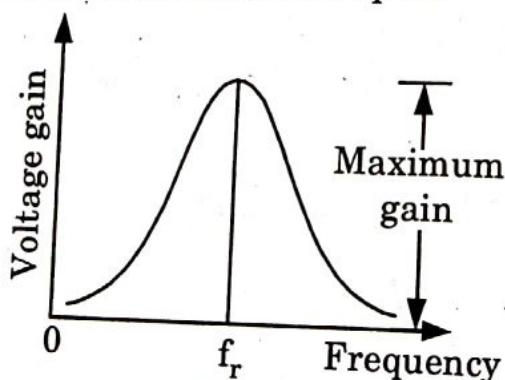
$$\text{where, } C_{gs} + C_M = C_G$$

## PART-2

*Frequency Response of Single Stage and Multistage Amplifier,  
Cascode Amplifier.*

**Que 2.3.****What do you understand by frequency response ?****Answer**

1. The voltage gain of an amplifier varies with signal frequency. It is because reactance of the capacitors in the circuit changes with signal frequency and hence affects the output voltage.
2. The curve between voltage gain and signal frequency of an amplifier is known as frequency response.
3. Fig. 2.3.1 shows the frequency response of a typical amplifier. The gain of the amplifier increases as the frequency increase from zero till it becomes maximum at  $f_r$ , called resonant frequency. If the frequency of signal increases beyond  $f_r$ , the gain decreases.
4. The performance of an amplifier depends to a considerable extent upon its frequency response. While designing an amplifier, appropriate steps must be taken to ensure that gain is essentially uniform over some specified frequency range.
5. For instance, in case of an audio amplifier, which is used to amplify speech or music, it is necessary that all the frequencies in the sound spectrum (i.e., 20 Hz to 20 kHz) should be uniformly amplified otherwise speaker will give a distorted sound output.

**Fig. 2.3.1.****Que 2.4.****Explain the frequency response of common emitter configuration.****Answer**

1. Fig. 2.4.1 shows the frequency response of a typical RC coupled amplifier.
2. Bandwidth of the amplifier is given by,

$$BW = f_H - f_L$$

where,

$f_H$  = Upper cut-off frequency

$f_L$  = Lower cut-off frequency

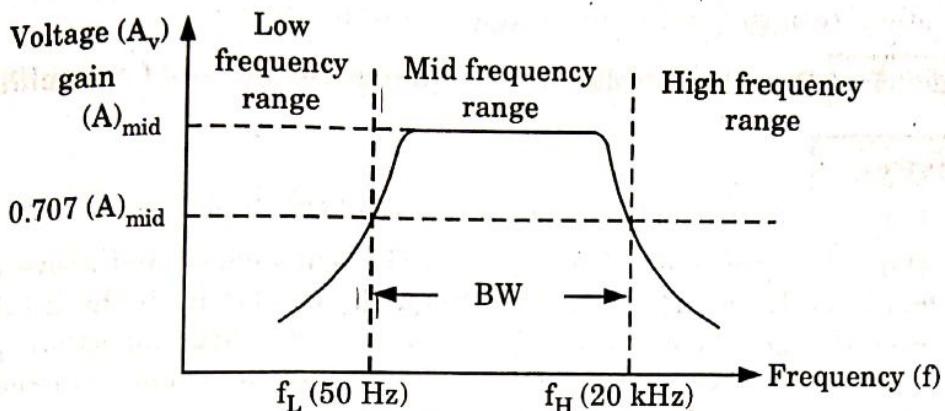


Fig. 2.4.1.

3. These two frequencies are also referred to as half-power frequencies since gain or output voltage drops to 70.7 % of maximum value and this represents a power level of one-half the power at the reference frequency in mid frequency region.
4. It is clear that voltage gain drops off at low (< 50 Hz) and high (> 20 kHz) frequencies whereas it is uniform over mid frequency range (50 Hz to 20 kHz).
5. This behaviour of the amplifier is briefly explained as follows :
  - i. **At low frequencies (< 50 Hz) :**
    1. The reactance of coupling capacitor  $C_C$  is quite high and hence very small part of signal will pass from one stage to the next stage.
    2. Moreover,  $C_E$  cannot shunt the emitter resistance  $R_E$  effectively because of its large reactance at low frequencies. These two factors cause a falling of voltage gain at low frequencies.
  - ii. **At high frequencies (> 20 kHz) :**
    1. The reactance of  $C_C$  is very small and it behaves as a short circuit. This increases the loading effect of next stage and serves to reduce the voltage gain.
    2. Moreover, at high frequency, capacitive reactance of base emitter junction is low which increases the base current. This reduces the current amplification factor  $\beta$ .
    3. Due to these two reasons, the voltage gain drops off at high frequency.
  - iii. **At mid frequencies (50 Hz to 20 kHz) :**
    1. The voltage gain of the amplifier is constant. The effect of coupling capacitor in this frequency range is such so as to maintain a uniform voltage gain.
    2. Thus, as the frequency increases in this range, reactance of  $C_C$  decreases which tends to increase the gain.

3. However, at the same time, lower reactance means higher loading of first stage and hence lower gain. These two factors almost cancel each other, resulting in a uniform gain at mid-frequency.

**Que 2.5.** Draw and explain the frequency response of CS amplifier.

**Answer**

- Fig. 2.5.1 shows the frequency response of CS amplifier.
- Here the gain falls off at signal frequencies below and above the midband. The gain falls off in low frequency band is due to the fact that even though all capacitors ( $C_{c1}$ ,  $C_{c2}$  and  $C_s$ ) are large capacitors ( $\mu\text{F}$ ) range as the signal frequency is reduced, their impedances increase, and they are no longer behave as short circuit.
- On the other hand, the gain falls off in the high frequency band as a result of  $C_{gs}$  and  $C_{gd}$  which though small (in pF), their impedances at high frequency decreases thus can no longer be considered as open circuits.
- The amplifier bandwidth or 3-dB bandwidth is defined as,

$$\text{BW} = f_H - f_L$$

$$\text{if } f_L \ll f_H, \quad \text{BW} = f_H$$

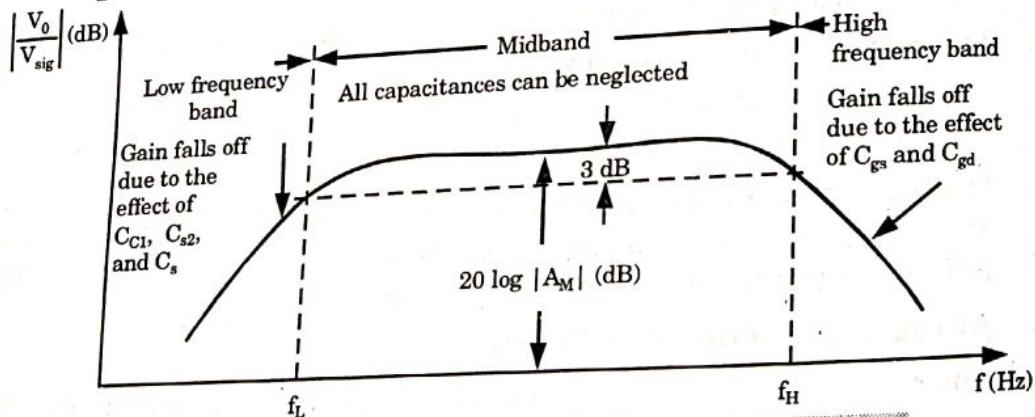


Fig. 2.5.1. Frequency response of the CS amplifier.

- The figure of merit for the amplifier is its gain bandwidth product which is defined as :

$$\text{GB} = |A_M| \text{ BW}$$

**Que 2.6.** Write the different coupling scheme of multistage amplifier. Explain frequency response of RC coupled amplifier in two-stage CE configuration.

**Answer**

There are three types of coupling scheme of multistage amplifier :

- Direct coupling.
- Transfer coupling.

## iii. RC coupling.

1. In RC coupling, a resistor and a capacitor are used as a coupling device. The capacitor connects the output of one stage to the input of next stage to pass AC signal and to block the DC bias voltages. The amplifier using RC coupling is called the RC coupled amplifier.
2. A two-stage RC coupled amplifier using *npn* transistors in CE configuration is shown in Fig. 2.6.1.
3. The two *npn* transistors are identical and have a common power supply  $V_{CC}$ .

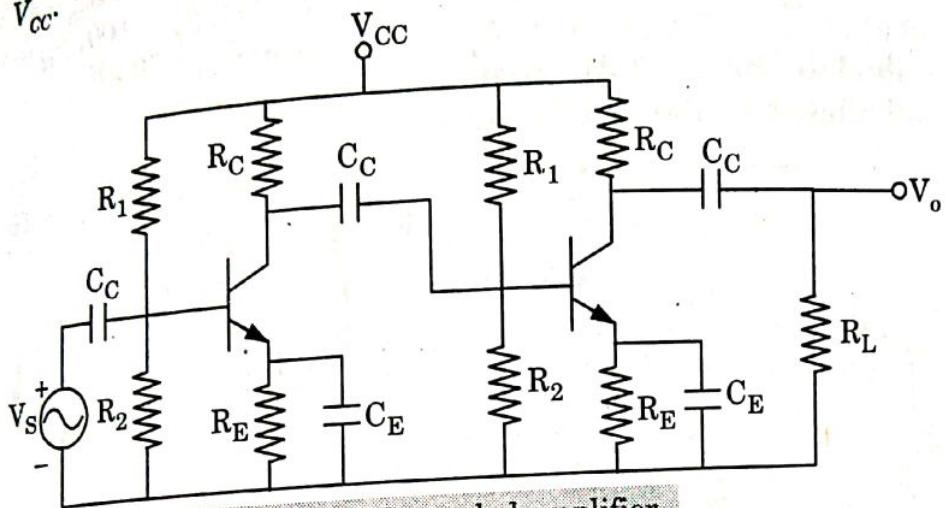


Fig. 2.6.1. RC coupled amplifier.

4.  $R_1$ ,  $R_2$  and  $R_E$  are the biasing resistors used separately for the two stages. Voltage divider biasing is being used.
5. Due to the use of coupling capacitors, the DC voltages will not be coupled from one stage to the other. Therefore, the quiescent point of the next stage will not be affected due to coupling. Thus due to RC coupling the DC operating point in any stage remain unaffected.
6. RC network gives a wide band frequency response without introduction of peaks at any frequencies. Therefore, RC coupling can be used for audio frequency amplifiers.

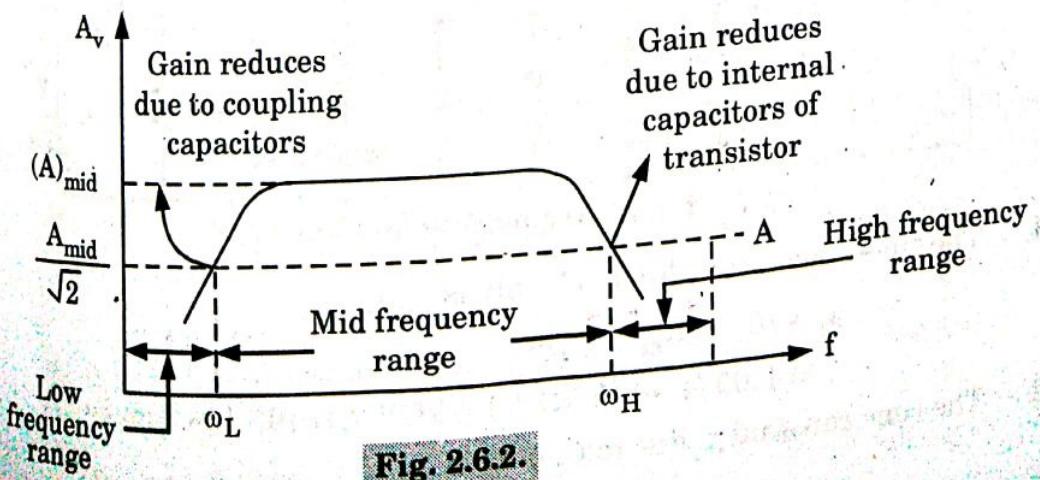


Fig. 2.6.2.

- The frequency response drops off at low frequencies due to the coupling capacitors and at high frequencies due to shunting effects of internal capacitors of the transistor.
- Due to reduction in gain at low frequencies. The RC coupled amplifiers are not suitable for amplification of low frequency signals.

**Que 2.7.** Find the frequency response of a two-stage CE-CE BJT

amplifier as shown in Fig. 2.7.1. The circuit parameters are  $C_{\pi 1} = C_{\pi 2} = 15 \text{ pF}$ ,  $C_{\mu 1} = C_{\mu 2} = 1 \text{ pF}$ ,  $g_{m1} = g_{m2} = 57.14 \text{ mS}$ ,  $R_s = 200 \Omega$ ,  $R_{11} = 22 \text{ k}\Omega$ ,  $R_{21} = 47 \text{ k}\Omega$ ,  $R_{C1} = 8 \text{ k}\Omega$ ,  $R_{E1} = 5 \text{ k}\Omega$ ,  $R_{12} = 22 \text{ k}\Omega$ ,  $R_{22} = 47 \text{ k}\Omega$ ,  $R_{C2} = 8 \text{ k}\Omega$ ,  $R_{E2} = 5 \text{ k}\Omega$ ,  $R_L = 5 \text{ k}\Omega$ ,  $r_{\pi 1} = r_{\pi 2} = 1.4 \text{ k}\Omega$ ,  $\beta_{f1} = 100$ ,  $\beta_{f2} = 150$ ,  $C_1 = 10 \mu\text{F}$ ,  $C_2 = 5 \mu\text{F}$ ,  $C_3 = 10 \mu\text{F}$ ,  $C_{E1} = 50 \mu\text{F}$ , and  $C_{E2} = 50 \mu\text{F}$ .

- Calculate the low 3-dB frequency  $f_L$ .
- Calculate the high 3-dB frequency  $f_H$ .

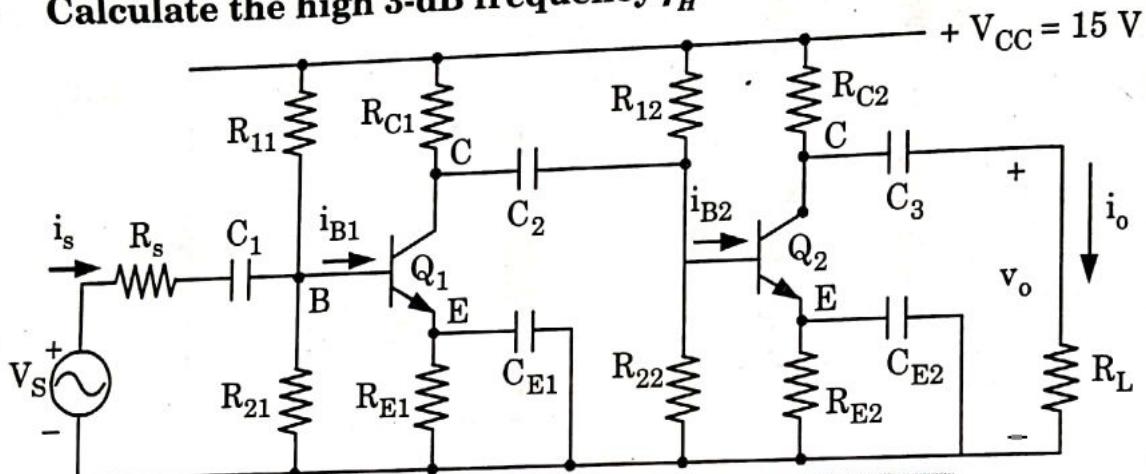


Fig. 2.7.1. Two-stage CE-CE BJT amplifier.

### Answer

- The low-frequency AC equivalent circuit is shown in Fig. 2.7.2. We have

$$R_{B1} = R_{11} \parallel R_{21} = 22 \text{ k}\Omega \parallel 47 \text{ k}\Omega = 15 \text{ k}\Omega$$

and

$$R_{B2} = R_{12} \parallel R_{22} = 22 \text{ k}\Omega \parallel 47 \text{ k}\Omega = 15 \text{ k}\Omega$$

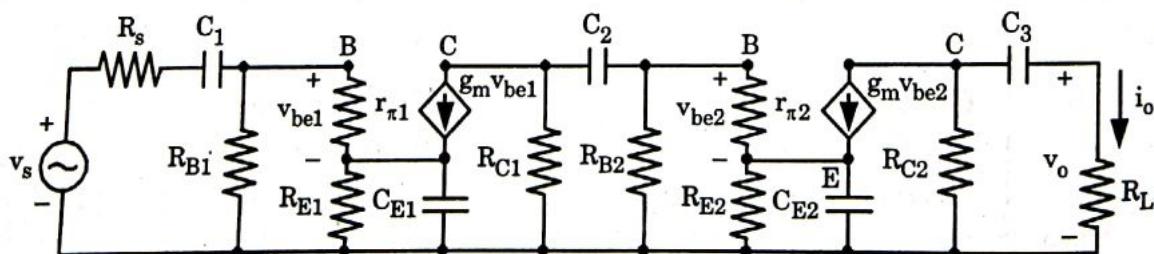


Fig. 2.7.2. Low-frequency equivalent circuit

- The time constant  $\tau_1$  due to  $C_1$  only is

$$\begin{aligned} \tau_1 &= [R_s + (R_{B1} \parallel r_{\pi 1})]C_1 \\ &= [200 \Omega + (15 \text{ k}\Omega \parallel 1.4 \text{ k}\Omega)] \times 10 \mu\text{F} = 14.8 \text{ ms} \end{aligned}$$

- The time constant  $\tau_2$  due to  $C_2$  only is

$$\begin{aligned}\tau_2 &= [R_{C1} + (R_{B2} \parallel r_{\pi 2})]C_2 \\ &= [8 \text{ k}\Omega + (15 \text{ k}\Omega \parallel 1.4 \text{ k}\Omega)] \times 5 \mu\text{F} = 46.4 \text{ ms}\end{aligned}$$

3. The time constant  $\tau_3$  due to  $C_3$  only is,

$$\tau_3 = [R_{C2} + R_L]C_3 = [8 \text{ k}\Omega + 5 \text{ k}\Omega] \times 10 \mu\text{F} = 130 \text{ ms}$$

4. The time constant  $\tau_4$  due to  $C_{E1}$  only is,

$$\begin{aligned}\tau_4 &= \left[ R_{E1} \parallel \frac{r_{\pi 1} + (R_s \parallel R_{B1})}{1 + \beta_{f1}} \right] C_{E1} \\ &= \left[ 5 \text{ k}\Omega \parallel \frac{1.4 \text{ k}\Omega + (200 \Omega \parallel 15 \text{ k}\Omega)}{1 + 100} \right] \times 50 \mu\text{F} = 0.79 \text{ ms}\end{aligned}$$

5. The time constant  $\tau_5$  due to  $C_{E2}$  only is,

$$\begin{aligned}\tau_5 &= \left[ R_{E2} \parallel \frac{r_{\pi 2} + (R_{C1} \parallel R_{B2})}{1 + \beta_{f2}} \right] C_{E2} \\ &= \left[ 5 \text{ k}\Omega \parallel \frac{1.4 \text{ k}\Omega + (8 \text{ k}\Omega \parallel 15 \text{ k}\Omega)}{1 + 150} \right] \times 50 \mu\text{F} = 2.17 \text{ ms}\end{aligned}$$

$$\text{As, } f_L = \frac{1}{2\pi} \sum_{k=1}^n \frac{1}{\tau_k}$$

6. The low 3-dB frequency  $f_L$  is,

$$f_L = \frac{1}{2\pi} \left[ \frac{1}{14.8 \text{ ms}} + \frac{1}{46.4 \text{ ms}} + \frac{1}{130 \text{ ms}} + \frac{1}{0.79 \text{ ms}} + \frac{1}{2.17 \text{ ms}} \right] = 290.2 \text{ Hz}$$

b. The high-frequency equivalent circuit shown in Fig. 2.7.3.

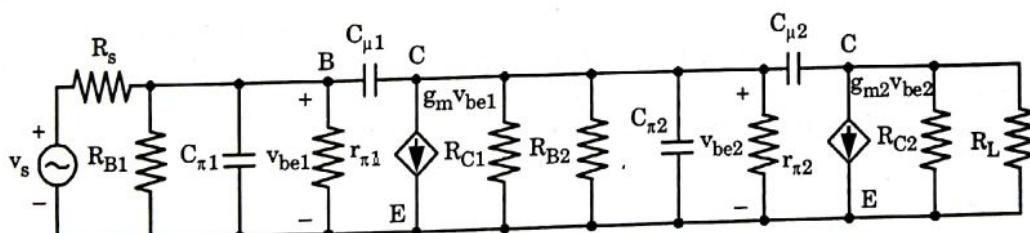


Fig. 2.7.3. High-frequency equivalent circuit.

1. If we assume  $R_{\pi 1}$  is Thevenin's equivalent resistance faced by  $C_{\pi 1}$  with  $C_{\mu 1}$ ,  $C_{\mu 2}$ , and  $C_{\pi 2}$  open-circuited, the time constant  $\tau_{\pi 1}$  can be found from

$$\begin{aligned}\tau_{\pi 1} &= R_{\pi 1}C_{\pi 1} = [r_{\pi 1} \parallel (R_s \parallel R_{B1})]C_{\pi 1} \\ &= [1.4 \text{ k}\Omega \parallel (200 \Omega \parallel 15 \text{ k}\Omega)] \times 15 \text{ pF} = 2.6 \text{ ns}\end{aligned}$$

2. If  $R_{\pi 2}$  is Thevenin's equivalent resistance faced by  $C_{\pi 2}$  with  $C_{\mu 1}$ ,  $C_{\mu 2}$ , and  $C_{\pi 1}$  open-circuited, the time constant  $\tau_{\pi 2}$  can be found from

$$\tau_{\pi 2} = R_{\pi 2}C_{\pi 2} = (r_{\pi 2} \parallel (R_{B2} \parallel R_{C1}))C_{\pi 2}$$

$$= [1.4 \text{ k}\Omega \parallel (15 \text{ k}\Omega \parallel 8 \text{ k}\Omega)] \times 15 \text{ pF} = 16.6 \text{ ns}$$

3. With  $C_{\mu 2}$ ,  $C_{\pi 1}$  and  $C_{\pi 2}$  open-circuited, the effective load resistance of  $C_{\mu 1}$  is

$$R_{L1(\text{eff})} = r_{\pi 2} \parallel R_{B2} \parallel R_{C1} = 1.4 \text{ k}\Omega \parallel 15 \text{ k}\Omega \parallel 8 \text{ k}\Omega = 1.1 \text{ k}\Omega$$

and its effective input resistance of  $C_{\mu 1}$  is

$$R_{\pi 1(\text{eff})} = r_{\pi 1} \parallel R_s \parallel R_{B1} = 1.4 \text{ k}\Omega \parallel 200 \text{ }\Omega \parallel 15 \text{ k}\Omega = 173 \text{ }\Omega$$

As  $R_{eq} = R_L + R_i(1 + g_m R_L)$

4. The time constant ( $\tau_{\mu 1}$ ) presented to  $C_{\mu 1}$  is

$$\begin{aligned} \tau_{\mu 1} &= [R_{L1(\text{eff})} + R_{\pi 1(\text{eff})}(1 + g_{m1} R_{L1(\text{eff})})] C_{\mu 1} \\ &= [1.1 \text{ k}\Omega + 173 \times (1 + 57.14 \text{ m}\Omega \times 1.1 \text{ k}\Omega)] \times 1 \text{ pF} = 12.2 \text{ ns} \end{aligned}$$

5. With  $C_{\mu 1}$ ,  $C_{\pi 1}$ , and  $C_{\pi 2}$  open-circuited, the effective load resistance of  $C_{\mu 2}$  is

$$R_{L2(\text{eff})} = R_L \parallel R_{C2} = 5 \text{ k}\Omega \parallel 8 \text{ k}\Omega = 3.08 \text{ k}\Omega$$

and its effective input side resistance of  $C_{\mu 2}$  is

$$R_{\pi 2(\text{eff})} = r_{\pi 2} \parallel R_{B2} \parallel R_{C1} = R_{L1(\text{eff})} = 1.4 \text{ k}\Omega \parallel 15 \text{ k}\Omega \parallel 8 \text{ k}\Omega = 1.1 \text{ k}\Omega$$

6. The time constant presented to  $C_{\mu 2}$  is

$$\begin{aligned} \tau_{\mu 2} &= [R_{L2(\text{eff})} + R_{\pi 2(\text{eff})}(1 + g_{m2} R_{L2(\text{eff})})] C_{\mu 2} \\ &= [3.08 \text{ k}\Omega + 1.1 \text{ k}\Omega \times (1 + 57.14 \text{ m}\Omega \times 3.08 \text{ k}\Omega)] \times 1 \text{ pF} \\ &= 197.8 \text{ ns} \end{aligned}$$

7. The high 3-dB frequency  $f_H$  is

$$f_H = \frac{1}{2\pi \sum_{j=1}^n \tau_j}$$

$$f_H = \frac{1}{2\pi} \left[ \frac{1}{\tau_{\pi 1} + \tau_{\pi 2} + \tau_{\mu 1} + \tau_{\mu 2}} \right]$$

$$= \frac{1}{2\pi} \left[ \frac{10^9}{2.6 + 16.6 + 12.2 + 197.8} \right] = 694.4 \text{ kHz}$$

**Que 2.8.** What is the cascode amplifier?

**Answer**

1. A common gate (common base) amplifier stage in cascade with a common source (common emitter) amplifier stage, is known as the cascode configuration.
2. The basic idea behind the cascode amplifier is to combine the high input resistance and large transconductance achieved in a common source (common-emitter) amplifier with the current buffering property and the superior high-frequency response of the common gate (common-base) circuit.
3. The cascode amplifier can be designed to obtain a wider bandwidth but equal DC gain as compared to the common source (common-emitter) amplifier.

4. It can be designed to increase the DC gain while leaving the gain-bandwidth product unchanged.

**PART-3**

*Various Classes of Operation (Class A, B, AB, C), Their Power Efficiency and Linearity Issues.*

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 2.9.** Explain transfer characteristics of class A output stage.  
Also draw signal waveforms.

**Answer****Transfer Characteristic :**

1. An emitter follower (Class A)  $Q_1$  biased with a constant current  $I$  supplied by transistor  $Q_2$ .
2. The emitter current  $i_{E1} = I + i_L$ , the bias current  $I$  must be greater than the largest negative load current; otherwise,  $Q_1$  cuts off and class A operation will no longer be maintained.
3. The transfer characteristic of the emitter follower of Fig. 2.9.1 is described by

$$v_o = v_I - v_{BE1}$$

where  $v_{BE1}$  depends on the emitter current  $i_{E1}$  and thus on the load current  $i_L$ .

4. If we neglect the relatively small changes in  $v_{BE1}$ , the linear transfer curve shown in Fig. 2.9.2 results.

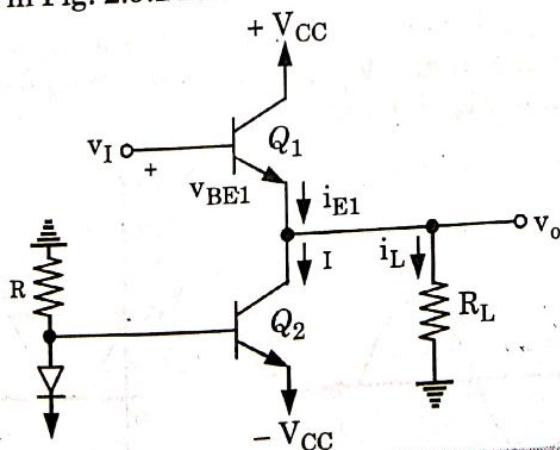
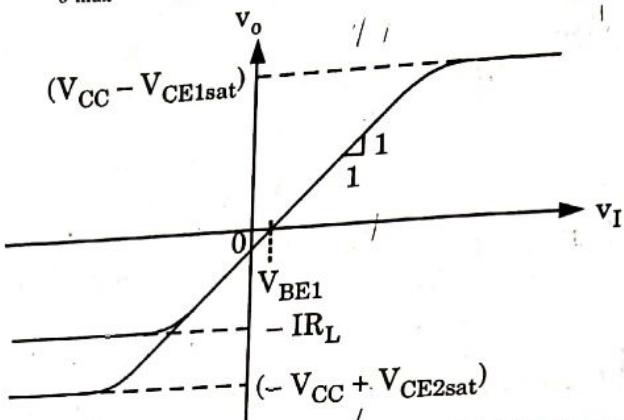


Fig. 2.9.1. An emitter follower ( $Q_1$ ) biased with a constant current  $I$  supplied by transistor  $Q_2$ .

5. As indicated, the positive limit of the linear region is determined by the saturation of  $Q_1$ , thus

$$v_{o \max} = V_{CC} - V_{CE1sat}$$



**Fig. 2.9.2.** Transfer characteristic of the emitter follower.

6. In the negative direction, depending on the values of  $I$  and  $R_L$ , the limit of the linear region is determined either by  $Q_1$  turning off,

$$v_{o \min} = -IR_L$$

or by  $Q_2$  saturating,

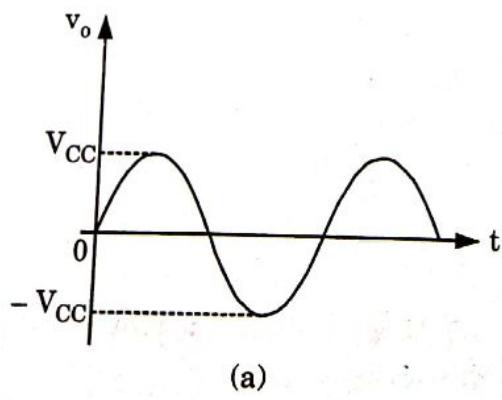
$$v_{o \min} = -V_{CC} + V_{CE2sat} \quad \dots(2.9.1)$$

7. The absolutely lowest output voltage is that given by eq. (2.9.1) and is achieved provided the bias current  $I$  is greater than the magnitude of the corresponding load current,

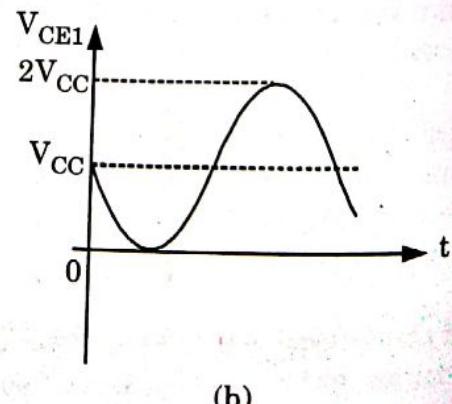
$$I \geq \frac{|-V_{CC} + V_{CE2sat}|}{R_L}$$

#### Signal waveforms :

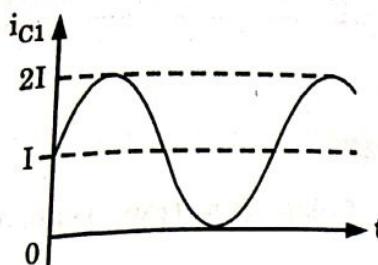
1. Consider the operation of the emitter-follower circuit of Fig. 2.9.1 for sine wave input.
2. Neglecting  $V_{CEsat}$ , then the bias current  $I$  is properly selected, the output voltage can swing from  $-V_{CC}$  to  $+V_{CC}$  with the quiescent value being zero, as shown in Fig. 2.9.3(a).



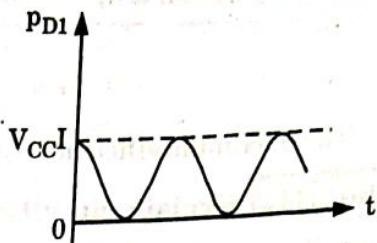
(a)



(b)



(c)



(d)

**Fig. 2.9.3.**

3. Fig. 2.9.3(b) shows the corresponding waveform of  $v_{CE1} = V_{CC} - v_o$ .
4. The bias current  $I$  is selected to allow a maximum negative load current of  $V_{CC}/R_L$ , the collector current of  $Q_1$  will have the waveform shown in Fig. 2.9.3(c).
5. Fig. 2.9.3(d) shows the waveform of the instantaneous power dissipation in  $Q_1$ ,

$$p_{D1} = v_{CE1} i_{C1}$$

**Que 2.10.** Derive power-conversion efficiency of class A output stage.

**Answer**

1. The power-conversion efficiency of an output stage is defined as

$$\eta = \frac{\text{Load power } (P_L)}{\text{Supply power } (P_S)} \quad \dots(2.10.1)$$

2. Assuming that the output voltage is a sinusoid with the peak value  $\hat{V}_o$ , the average load power will be

$$P_L = \frac{(\hat{V}_o / \sqrt{2})^2}{R_L} = \frac{1}{2} \frac{\hat{V}_o^2}{R_L} \quad \dots(2.10.2)$$

3. Since the current in  $Q_2$  is constant ( $I$ ), the power drawn from the negative supply is  $V_{CC}I$ . The average current in  $Q_1$  is equal to  $I$ , and thus the average power drawn from the positive supply is  $V_{CC}I$ . Thus the total average supply power is

$$\dots(2.10.3)$$

$$P_S = 2V_{CC}I$$

4. Equation (2.10.2) and (2.10.3) can be combined to yield

$$\eta = \frac{1}{4} \frac{\hat{V}_o^2}{IR_L V_{CC}} = \frac{1}{4} \left( \frac{\hat{V}_o}{IR_L} \right) \left( \frac{\hat{V}_o}{V_{CC}} \right)$$

5. Since  $\hat{V}_o \leq V_{CC}$  and  $\hat{V}_o \leq IR_L$ , maximum efficiency is obtained when

$$\hat{V}_o = V_{CC} = IR_L$$

The maximum efficiency attainable is 25 %.

**Que 2.11.** Explain circuit operation of class B output stage. Also draw its transfer characteristics.

**Answer**

- Figure 2.11.1 shows a class B output stage. It consists of a complementary pair of transistors (an *npn* and a *pnp*) connected in such a way that both cannot conduct simultaneously.

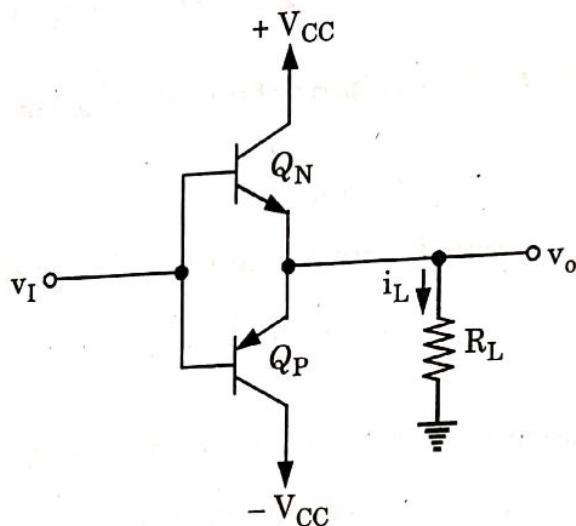
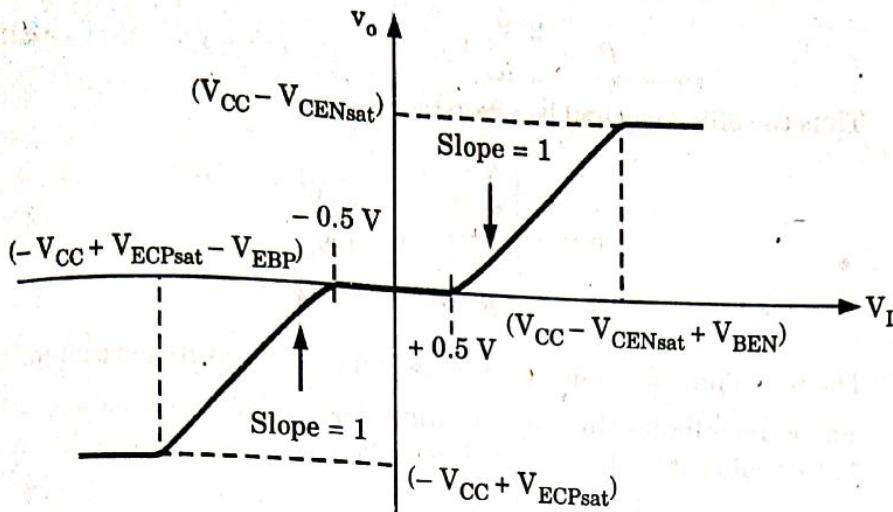


Fig. 2.11.1. A class B output stage.

- When the input voltage  $v_I$  is zero, both transistors are cut off and the output voltage  $v_o$  is zero.
- As  $v_I$  goes positive and exceeds about 0.5 V,  $Q_N$  conducts and operates as an emitter follower. In this case,  $v_o$  follows  $v_I$  (*i.e.*,  $v_o = v_I - v_{BE}$ ) and  $Q_N$  supplies the load current.
- Meanwhile, the emitter-base junction of  $Q_P$ , will be reverse-biased by the  $V_{BE}$  of  $Q_N$ , which is approximately 0.7 V. Thus  $Q_P$  will be cut off.
- If the input goes negative by more than about 0.5 V,  $Q_P$  turns ON and acts as an emitter follower. Again  $v_o$  follows  $v_I$  (*i.e.*,  $v_o = v_I + v_{EB}$ ), but in this case  $Q_P$  supplies the load current and  $Q_N$  will be cut off.
- The circuit operates in a push-pull fashion,  $Q_N$  pushes (sources) current into the load when  $v_I$  is positive, and  $Q_P$  pulls (sinks) current from the load when  $v_I$  is negative.

**Transfer Characteristic :**

- The transfer characteristic of the class B stage is shown in Fig. 2.11.2.



**Fig. 2.11.2.** Transfer characteristic for the class B output stage.

2. There exists a range of  $v_i$  centered around zero where both transistors are cut off and  $v_o$  is zero. This dead band results in the crossover distortion.
3. The effect of crossover distortion will be most pronounced when the amplitude of the input signal is small.
4. Crossover distortion in audio power amplifiers gives rise to unpleasant sounds.

**Que 2.12.** Derive power conversion efficiency of class B output stage.

**Answer**

1. To calculate the power-conversion efficiency,  $\eta$ , of the class B stage, we neglect the crossover distortion and consider the case of an output sinusoid of peak amplitude  $\hat{V}_o$ .
  2. The average load power will be
- $$P_L = \frac{1}{2} \frac{\hat{V}_o^2}{R_L} \quad \dots(2.12.1)$$
3. The current drawn from each supply will consist of half-sine waves of peak amplitude  $(\hat{V}_o / R_L)$ . Thus the average current drawn from each of the two power supplies will be  $\hat{V}_o / \pi R_L$ .
  4. The average power drawn from each of the two power supplies will be the same,

$$P_{S+} = P_{S-} = \frac{1}{\pi} \frac{\hat{V}_o}{R_L} V_{cc} \quad \dots(2.12.2)$$

and the total supply power will be

$$P_s = \frac{2}{\pi} \frac{\hat{V}_o}{R_L} V_{cc} \quad \dots(2.12.3)$$

5. Thus the efficiency will be given by

$$\eta = \frac{\left( \frac{1}{2} \frac{\hat{V}_o^2}{R_L} \right)}{\left( \frac{2}{\pi} \frac{\hat{V}_o}{R_L} V_{cc} \right)} = \frac{\pi}{4} \frac{\hat{V}_o}{V_{cc}} \quad \dots(2.12.4)$$

6. The maximum efficiency is obtained when  $\hat{V}_o$  is at its maximum. This maximum is limited by the saturation of  $Q_N$  and  $Q_P$  to  $V_{cc} - V_{CEsat} \approx V_{cc}$ . At this value of peak output voltage, the power conversion efficiency is

$$\eta_{max} = \pi/4 = 78.5 \% \quad \dots(2.12.5)$$

**Que 2.13.** Explain the operation of class AB output stage with its transfer characteristics.

**Answer**

1. A bias voltage  $V_{BB}$  is applied between the bases of  $Q_N$  and  $Q_P$ . For  $v_I = 0$ ,  $v_o = 0$ , and a voltage  $V_{BB}/2$  appears across the base-emitter junction of each of  $Q_N$  and  $Q_P$ .
2. Assuming matched devices,

$$i_N = i_P = I_Q = I_S e^{V_{BB}/2V_T} \quad \dots(2.13.1)$$

3. When  $v_I$  goes positive by a certain amount, the voltage at the base of  $Q_N$  increases by the same amount and the output becomes positive at an almost equal value,

$$v_o = v_I + \frac{V_{BB}}{2} - v_{BEN} \quad \dots(2.13.2)$$

4. The positive  $v_o$  causes a current  $i_L$  to flow through  $R_L$ , and thus  $i_N$  must increase i.e.,

$$i_N = i_P + i_L \quad \dots(2.13.3)$$

The increase in  $i_N$  will be accompanied by a corresponding increase in  $v_{BEN}$ .

5. Since the voltage between the two bases remains constant at  $V_{BB}$ , the increase in  $v_{BEN}$  will result in an equal decrease in  $v_{EBP}$  and hence in  $i_P$ . The relationship between  $i_N$  and  $i_P$  can be derived as follows,

$$v_{BEN} + v_{EBP} = V_{BB}$$

$$V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S}$$

$$i_N i_P = I_Q^2 \quad \dots(2.13.4)$$

- Eq. (2.13.3) and (2.13.4) can be combined and we get

6.  $i_N^2 - i_L i_N - I_Q^2 = 0 \quad \dots(2.13.5)$
7. For positive output voltages, the load current is supplied by  $Q_N$ , which acts as the output emitter follower. Meanwhile,  $Q_P$  will be conducting a current that decreases as  $v_o$  increases, for large  $v_o$  the current in  $Q_P$  can be ignored altogether.
8. For negative input voltages the opposite occurs, the load current will be supplied by  $Q_P$ , which acts as the output emitter follower, while  $Q_N$  conducts a current that gets smaller as  $v_I$  becomes more negative. Eq. (2.13.4), relating  $i_N$  and  $i_P$ , holds for negative inputs as well.
9. We conclude that the class AB stage operates in much the same manner as the class B circuit, with one important exception. For small  $v_I$ , both transistors, and as  $v_I$  is increased or decreased, one of the two transistors takes over the operation.
10. Since the transition is a smooth one, crossover distortion will be almost totally eliminated. Fig. 2.13.1 shows the transfer characteristic of the class AB stage.

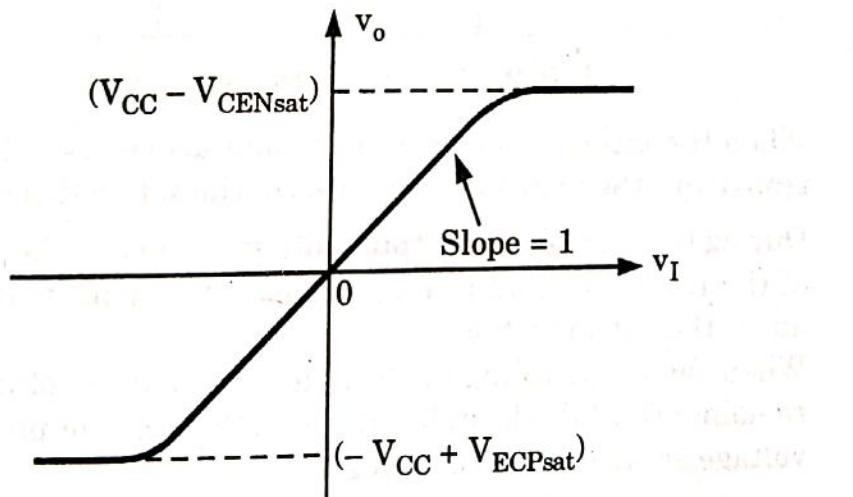


Fig. 2.13.1. Transfer characteristic of the class AB stage.

**Que 2.14.** Why is class C amplifier's efficiency higher than that of class A amplifier?

**Answer**

1. Class A power amplifier is biased in the active region to produce a linear output signal with minimal distortion. However, due to this biasing arrangement, the transistor remains ON even for no input signal.

2. In the class C amplifier, the transistor is biased such that it remains OFF for no-signal conditions and operates in the saturation region when an input signal is present.
3. When the transistor is OFF, the current through it is very small and hence the transistor dissipates negligible power.
4. Similarly, when the transistor operates in saturation, the voltage across it is very small, and again the power dissipation is small.
5. Therefore, in the class C amplifier, as the transistor dissipates less power, its efficiency is higher than that of the class A amplifier.

**Que 2.15.** Describe class C output stage with its input and output waveforms. Also write its power conversion efficiency.

**Answer**

1. The schematic diagram of a class C amplifier is shown in Fig. 2.15.1.
2. The input and the waveforms at the collector terminal are shown in Fig. 2.15.2.

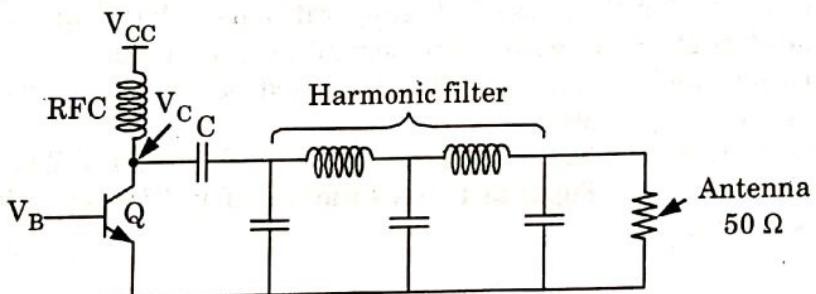


Fig. 2.15.1. The class C output stage.

3. When the input signal is positive and above the cut-in voltage of the transistor, the transistor operates in the saturation region.
4. During this period, the output voltage is equal to the saturation voltage of the transistor and remains constant as long as the input signal is above the cut-in voltage.
5. When the input voltage is less than the cut-in voltage, the transistor remains off, while the induced emf in the inductor provides the collector voltage as shown in Fig. 2.15.2.

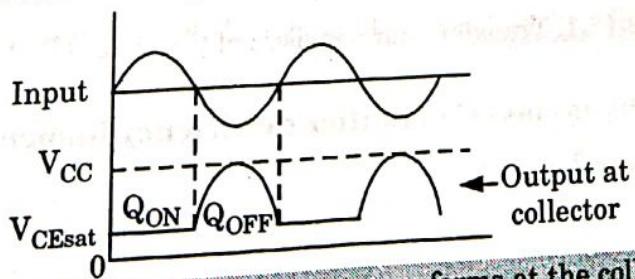


Fig. 2.15.2. Input and output waveforms at the collector terminal of the class C amplifier.

6. This output voltage is fed to the low-pass filter as shown in Fig. 2.15.1. The low-pass filter suppresses the high-frequency harmonics present at the collector and produces output similar to the input signal.

**Efficiency:**  
The efficiency of the class C amplifier is given by

$$h = \frac{P_{AC}}{P_{DC}} = \frac{(V_{CC} - V_{CE\text{sat}}) I_{DC}}{V_{CC} I_{DC}} = \left(1 - \frac{V_{CE\text{sat}}}{V_{CC}}\right)$$

As  $V_{CE\text{sat}}$  is very small as compared to  $V_{CC}$ , the efficiency of the class C amplifier is very high; it can achieve above 90 % efficiency

#### PART-4

*Feedback Topologies : Voltage Series, Current Series, Voltage Shunt, Current Shunt.*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 2.16.** What are the four basic feedback topologies of amplifier ?

OR

Write short notes on (i) series-series topology (ii) shunt-series topology.

AKTU 2016-17, Marks 15

#### Answer

The four basic feedback topologies are as follows :

##### i. Voltage amplifier (series-shunt):

- It can also be called as voltage controlled voltage source and shown in Fig. 2.16.1. In this,

$$V_o = A_v V_s$$

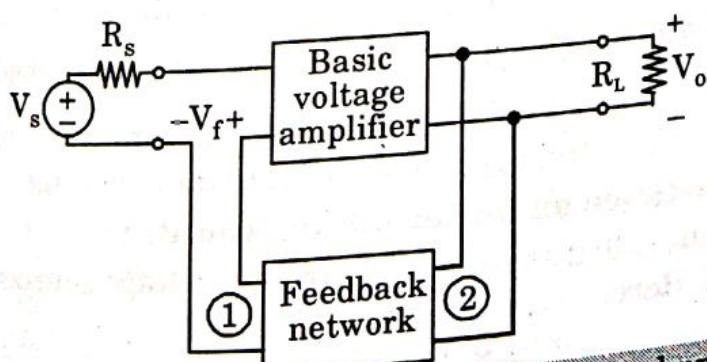


Fig. 2.16.1. Voltage-mixing, voltage-sampling (series-shunt) topology.

2. The output voltage is directly proportional to input voltage and the proportionality factor is independent of magnitudes of the source and load resistance.

**ii. Current amplifier (shunt-series) :**

1. It can also be called as current controlled current source and shown in Fig. 2.16.2. Here,

$$I_o = A_i I_s$$

2. In this amplifier, the output quantity is a current, thus the feedback signal is in current form. The output current is directly proportional to input current.

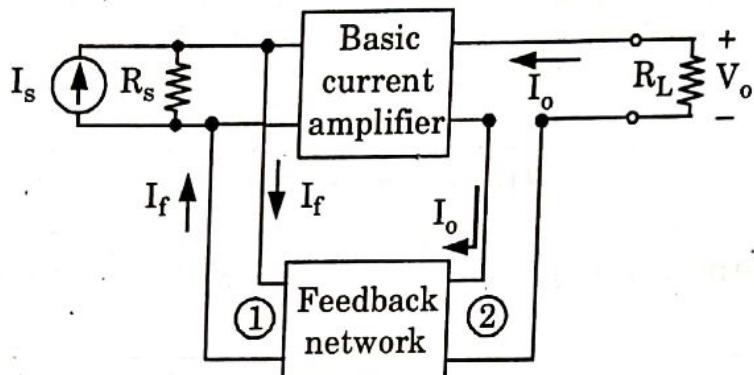


Fig. 2.16.2. Current-mixing, current-sampling (shunt-series) topology.

**iii. Transconductance amplifier (series-series) :**

1. It can also be called as voltage controlled current source and shown in Fig. 2.16.3. Here,

$$I_o = G_m V_s$$

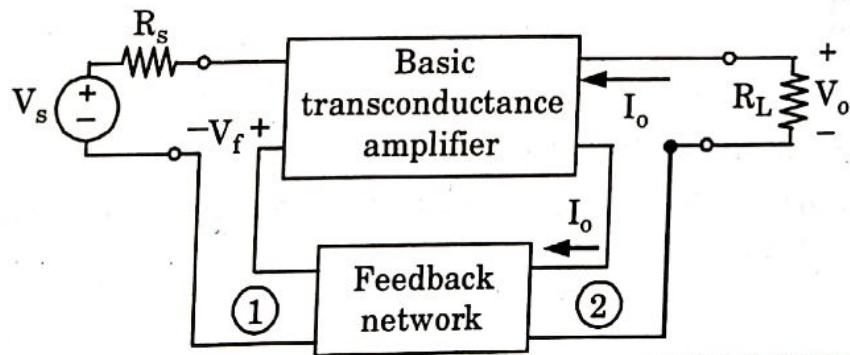


Fig. 2.16.3. Voltage-mixing, current-sampling (series-series) topology.

2. The voltage is given as input and the current is taken as output and the output current is directly proportional to input voltage.

**iv. Transresistance amplifier (shunt-shunt) :**

1. It can also be called as current controlled voltage source and shown in Fig. 2.16.4. Here,

$$V_o = R_m I_s$$

2. The current source acts as input and voltage is taken as output and the output voltage is directly proportional to input current.

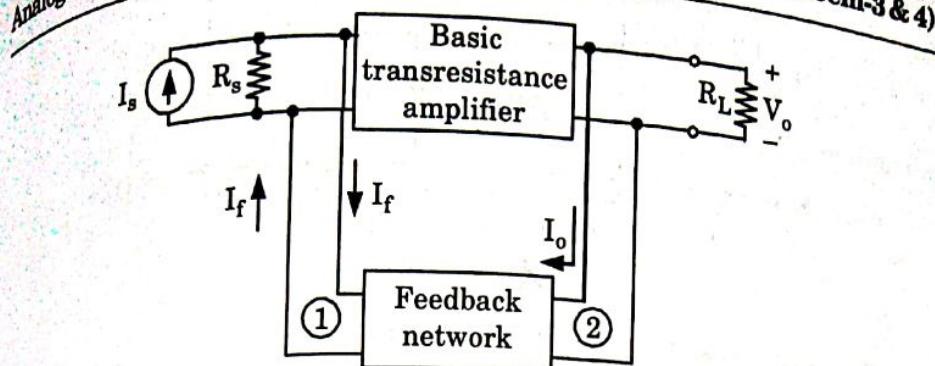


Fig. 2.16.4. Current-mixing, voltage-sampling (shunt-shunt) topology.

**Que 2.17.** Draw the circuit diagram of series-shunt feedback amplifier and explain the working operation.

**Answer**

1. The ideal structure of the series-shunt feedback amplifier is shown in Fig. 2.17.1(a). The circuit has an input resistance  $R_i$ , a voltage gain  $A$ , and an output resistance  $R_o$ .
2. The closed-loop voltage gain  $A_f$  is given by

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + A\beta}$$

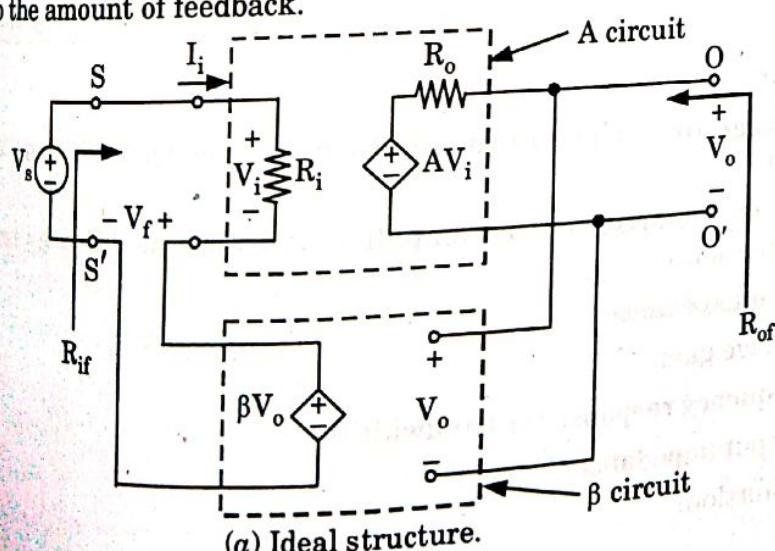
3. The equivalent circuit model of the series-shunt feedback amplifier is shown in Fig. 2.17.1(b).  $R_{if}$  and  $R_{of}$  denote the input and output resistance with feedback.

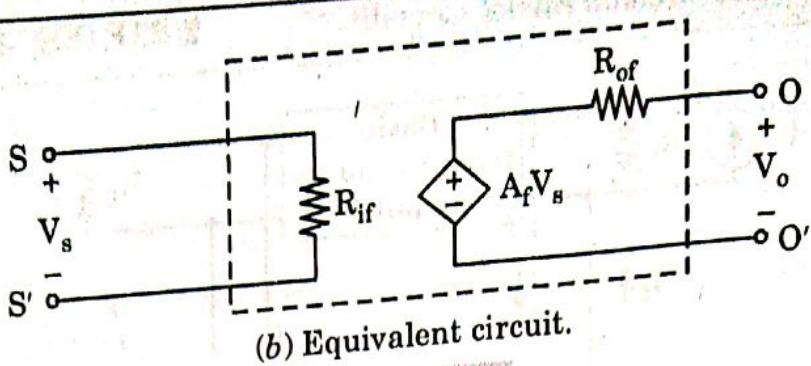
4.  $R_{if}$  can be given as

$$R_{if} = \frac{V_s}{I_i} = \frac{V_s}{V_i/R_i} = R_i \frac{V_s}{V_i} = R_i \frac{V_i + \beta A V_i}{V_i}$$

$$R_{if} = R_i(1 + A\beta)$$

5. The negative feedback increases the input resistance by a factor equal to the amount of feedback.





**Fig. 2.17.1.**

6. The output resistance  $R_{of}$  can be given as

$$R_{of} = \frac{V_t}{I}$$

where,

$V_t$  = test voltage at the output

$$I = \frac{V_t - AV_t}{R_o} = \frac{V_t + A\beta V_t}{R_o}$$

$$(\because V_i = -V_f = -\beta V_o = -\beta V_t)$$

and

$$R_{of} = \frac{R_o}{1 + A\beta}$$

The negative feedback in this case reduces the output resistance by a factor equal to the amount of feedback.

**Que 2.18.** Explain the series-series (current-series) feedback amplifier.

OR

Derive the input and output resistance of a transconductance and voltage amplifier.

**AKTU 2014-15, Marks 05**

OR

List five characteristics of an amplifier which are modified by negative feedback.

**AKTU 2014-15, Marks 05**

**AKTU 2016-17, Marks 10**

### Answer

**Voltage or series shunt amplifier :** Refer Q. 2.17, Page 2-23E, Unit-2.

1. The characteristics of an amplifier which are modified by negative feedback are :
  - i. Input impedance.
  - ii. Voltage gain.
  - iii. Frequency response (or bandwidth).
  - iv. Output impedance.
  - v. Distortion.

- Series-series or transconductance feedback amplifier :**
- Fig. 2.18.1(a) shows the ideal structure for the series-series feedback amplifier.
  - The circuit has an input resistance  $R_i$ , a short-circuit transconductance,  $A = I_o / V_i$ , and an output resistance  $R_o$ .

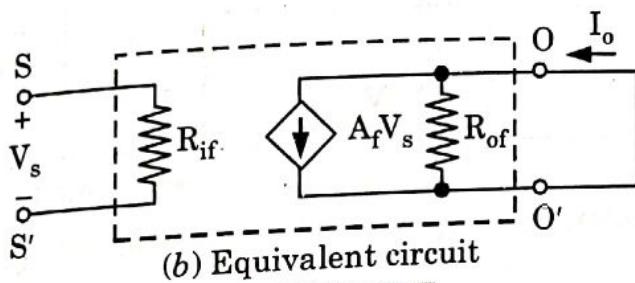
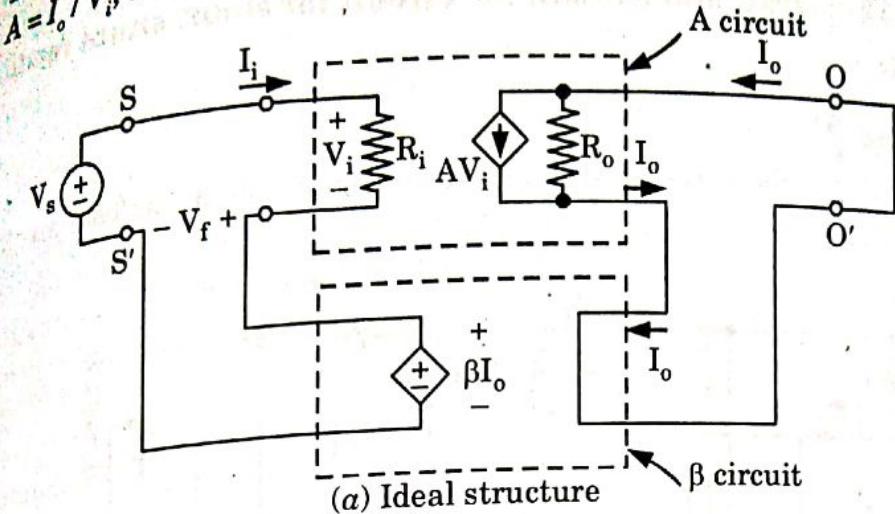


Fig. 2.18.1.

- The closed-loop voltage gain  $A_f$  is given by

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + A\beta}$$

- The input resistance,  $R_{if}$ , with feedback is given as

$$\begin{aligned} R_{if} &= \frac{V_s}{I_i} = \frac{V_s}{V_i / R_i} \\ &= R_i \frac{V_s}{I_i} = R_i \frac{V_i + V_f}{V_i} = R_i \frac{V_i + A\beta V_i}{V_i} \end{aligned}$$

$$R_{if} = R_i (1 + A\beta)$$

The negative feedback increases the input resistance by a factor equal to the amount of feedback.

- The output resistance,  $R_{of}$  with feedback can be given as

$$R_{of} = V/I_t$$

where,

$I_t$  = test current at output

$$V = (I_t - AV_i)R_o = (I_t + A\beta I_t)R_o \quad (\because V_i = -V_f = -\beta I_o = -\beta I_t)$$

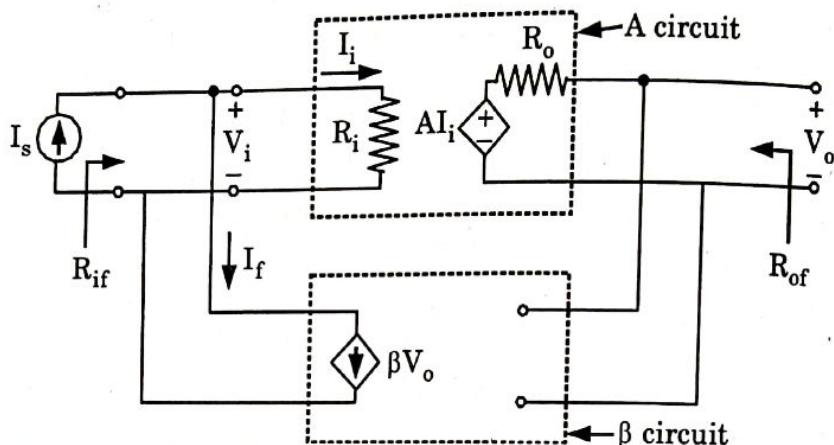
Hence,  $R_{of} = (1 + A\beta)R_o$

6. The negative feedback increases the output resistance by a factor equal to the amount of feedback.

**Que. 2.19.** Draw and explain the circuit for shunt-shunt feedback amplifier.

**Answer**

1. Fig. 2.19.1 shows the ideal structure for a shunt-shunt feedback amplifier.



**Fig. 2.19.1.** Ideal structure for the shunt-shunt feedback amplifier.

2. Here  $R_i$  is the input resistance,  $A$  is transresistance and  $R_o$  is output resistance.  $\beta$  is the conductance.
3. The closed-loop gain  $A_f$  is defined

$$A_f = V_o / I_s$$

and is given by

$$A_f = \frac{A}{1 + A\beta}$$

4. The input resistance with feedback is given by

$$\begin{aligned} R_{if} &= \frac{V_i}{I_s} = \frac{I_i R_i}{I_s} = \frac{I_i R_i}{I_i + I_f} \\ &= \frac{I_i R_i}{I_i + \beta A I_i} = \frac{R_i}{1 + A\beta} \end{aligned}$$

5. The output resistance with feedback is given by

$$R_{of} = V_t / I$$

$V_t$  = test voltage at output.

where,

$$I = \frac{V_t - AI_i}{R_o} = \frac{V_t + A\beta V_t}{R_o} = \frac{V_t (1 + A\beta)}{R_o}$$

$(\because I_i = -I_f = -\beta V_o = -\beta V_t)$

$$R_{of} = \frac{R_o}{1 + A\beta}$$

Hence,

**Que 2.20.** Draw and explain the circuit for shunt-series feedback amplifier.

**Answer**

1. Fig. 2.20.1 shows the ideal structure of the shunt-series feedback amplifier. The closed-loop gain,  $A_f$ , is given by

$$A_f = \frac{I_o}{I_s} = \frac{A}{1 + A\beta}$$

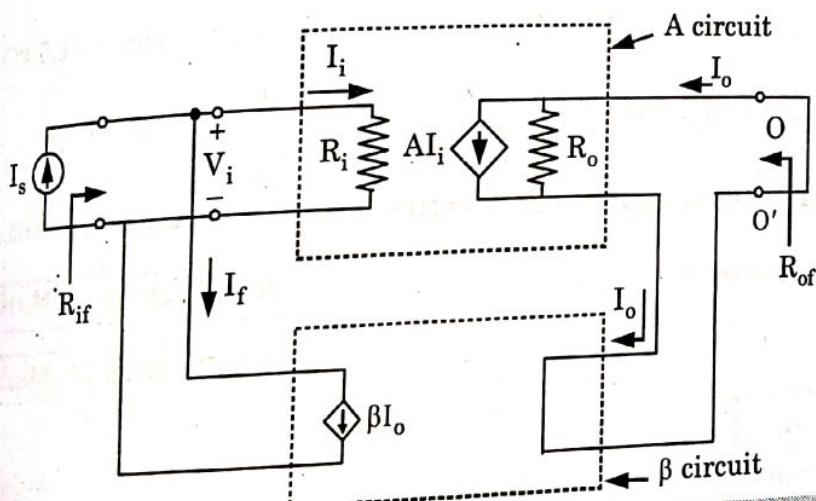


Fig. 2.20.1. Ideal structure for the shunt-series feedback amplifier.

2. The input resistance with feedback is given by

$$R_{if} = \frac{V_i}{I_s} = \frac{I_i R_i}{I_i + I_f} = \frac{I_i R_i}{I_i + \beta I_o}$$

$$= \frac{I_i R_i}{I_i + \beta A I_i} = \frac{R_i}{1 + A\beta}$$

$$R_{if} = \frac{R_i}{1 + A\beta}$$

3. The output resistance with feedback is given by

where,  $R_{of} = V/V_t$   
 $I_t = \text{test current at output.}$

$$V = (I_t - AI_i) R_o = (I_t + A\beta I_t) R_o \quad (\because I_i = -I_f = -\beta I_o = -\beta I_t)$$

4. Hence,  $R_{of} = R_o (1 + A\beta)$

**Que 2.21.** Calculate the voltage gain, input and output resistance of voltage-series feedback amplifier having  $A_v = 300$ ,  $R_i = 1.5 \text{ k}\Omega$ ,  $R_o = 50 \text{ k}\Omega$  and  $\beta = 1/15$ .

AKTU 2014-15, Marks 05

### Answer

**Given :**  $A_v = 300$ ,  $R_i = 1.5 \text{ k}\Omega$ ,  $R_o = 50 \text{ k}\Omega$  and  $\beta = 1/15$

**To Find :** Voltage gain ( $A_{vf}$ ), Input resistance ( $R_{if}$ ), Output resistance ( $R_{of}$ ).

$$1. \text{ Voltage gain, } A_{vf} = \frac{A_v}{1 + \beta A_v} = \frac{300}{1 + (300/15)} = 14.28$$

$$2. \text{ Input resistance, } R_{if} = R_i(1 + A_v \beta) = 1.5 [1 + (300/15)] = 31.5 \text{ k}\Omega$$

$$3. \text{ Output resistance, } R_{of} = \frac{R_o}{1 + \beta A_v} = \frac{50}{1 + (300/15)} = 2.380 \text{ k}\Omega$$

**Que 2.22.** Describe the properties of series-shunt and shunt-shunt feedback amplifier.

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AKTU 2016-17, Marks 10

### Answer

#### Properties of series-shunt amplifier :

1. It stabilizes the voltage gain.
2. High input impedance, i.e.,  $R_{if} = R_i (1 + A\beta)$ .
3. Low output impedance, i.e.,  $R_{of} = \frac{R_o}{1 + A\beta}$ .

#### Properties of shunt-shunt amplifier :

1. Low input impedance, i.e.,  $R_{if} = \frac{R_i}{1 + A\beta}$ .
2. Low output impedance, i.e.,  $R_{of} = \frac{R_o}{1 + A\beta}$ .
3. It stabilizes the output voltage.

**Que 2.23.** Draw a comparison table for the different characteristics and types of feedback network used.

**Answer**

S.No.	Characteristics	Types of feedback network			
		voltage series	voltage shunt	current series	current shunt
1.	Voltage gain	decreases	decreases	decreases	decreases
2.	Bandwidth	increases	increases	increases	increases
3.	Input resistance	increases by a factor of $(1 + A\beta)$	decreases by a factor of $(1 + A\beta)$	increases by a factor of $(1 + A\beta)$	decreases by a factor of $(1 + A\beta)$
4.	Output resistance	decreases by a factor of $(1 + A\beta)$	decreases by a factor of $(1 + A\beta)$	increases by a factor of $(1 + A\beta)$	increases by a factor of $(1 + A\beta)$
5.	Harmonic distortion	decreases	decreases	decreases	decreases
6.	Noise	decreases	decreases	decreases	decreases

**PART-5**

Effect of Feedback on Gain, BW etc, Calculation with Practical Circuits.

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 2.24.** What is the effect of feedback on gain and bandwidth?

**Answer**

- Consider an amplifier whose high frequency response is characterized by a single pole. Its gain at mid and high frequencies can be expressed as

$$A(s) = \frac{A_M}{1 + s/\omega_H}$$

where  $A_M$  denotes the midband gain and  $\omega_H$  is the upper 3-dB frequency.

2. Application of negative feedback, with a frequency independent factor  $\beta$ , around this amplifier results in a closed loop gain  $A_f(s)$  given by

$$A_f(s) = \frac{A_M / (1 + A_M \beta)}{1 + s / \omega_H (1 + A_M \beta)}$$

3. Thus, the feedback amplifier will have a midband gain of  $A_M / (1 + A_M \beta)$  and an upper 3-dB frequency  $\omega_{Hf}$  given by

$$\omega_{Hf} = \omega_H (1 + A_M \beta)$$

4. Similarly, it can be shown that if the open loop gain is characterized by a dominant low frequency pole giving rise to a lower 3-dB frequency  $\omega_L$ , then the feedback amplifier will have a lower 3-dB frequency  $\omega_{Lf}$ ,

$$\omega_{Lf} = \frac{\omega_L}{1 + A_M \beta}$$

5. The amplifier bandwidth is increased by the same factor by which its midband gain is decreased, maintaining the gain bandwidth product at a constant value.

**Que 2.25.** An amplifier has a midband gain of 125 and a bandwidth of 250 kHz. (a) If 4 % negative feedback is introduced. Find the new bandwidth and gain. (b) If the bandwidth is to be restricted to 1 MHz, find the feedback ratio.

**Answer**

**Given :** Midband gain,  $A = 125$ , Bandwidth, (BW) = 250 kHz.

**To Find :** a. New bandwidth and gain when 4 % negative feedback.  
b. Feedback ratio when BW = 1 MHz

a.  $\beta = 0.04$ ,

$$\begin{aligned} \text{BW}_f &= (1 + A\beta) \text{ BW} \\ &= (1 + 125 \times 0.04) \times 250 \times 10^3 \text{ Hz} \\ &= 1.5 \text{ MHz} \end{aligned}$$

$$\text{Gain with feedback, } A_f = \frac{A}{1 + A\beta} = \frac{125}{1 + 125 \times 0.04} = \frac{125}{6} = 20.83$$

b.

$$\begin{aligned} \text{BW}_f &= (1 + A\beta) \text{ BW} \\ 1 \times 10^6 &= (1 + 125\beta') \times 250 \times 10^3 \end{aligned}$$

$$\begin{aligned} (1 + 125\beta') &= \frac{1 \times 10^6}{250 \times 10^3} \\ (1 + 125\beta') &= 4 \end{aligned}$$

$$\begin{aligned} \beta' &= \frac{3}{125} = 0.024 \\ \beta' &= 2.4 \% \end{aligned}$$

**Ques 2.26.** Analyze the circuit of Fig. 2.26.1 to determine the small signal voltage gain  $V_o / V_s$ , the input resistance  $R_{in}$ , and the output resistance  $R_{out} = R_{of}$ . The transistor has  $\beta = 100$ .

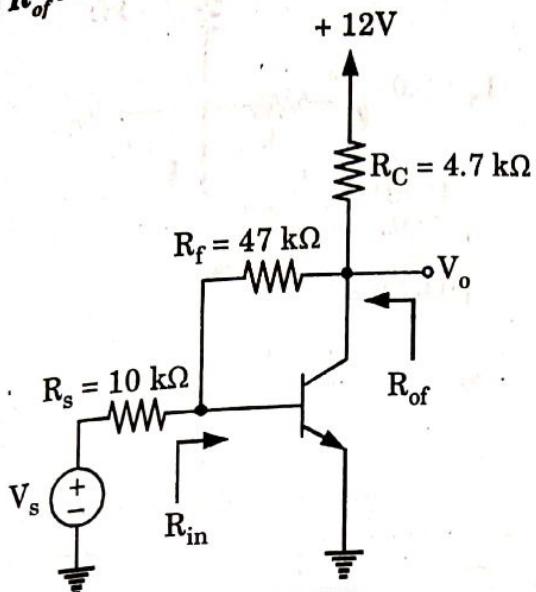


Fig. 2.26.1.

**Answer**

1. The DC analysis is illustrated in Fig. 2.26.2(a), from which we can write

$$V_C = 0.7 + (I_B + 0.07)47 = 3.99 + 47I_B \quad \dots(2.26.1)$$

$$\text{and } \frac{12 - V_C}{4.7} = (\beta + 1)I_B + 0.07 \quad \dots(2.26.2)$$

2. After solving eq. (2.26.1) and eq. (2.26.2) then we get  $I_B = 0.015 \text{ mA}$ ,  $I_C = 1.5 \text{ mA}$ , and  $V_C = 4.7 \text{ V}$ .

3. The small signal analysis is shown in Fig. 2.26.2(c), we get

$$V_\pi = I_i(R_s \parallel R_f \parallel r_\pi)$$

$$V_o = -g_m V_\pi (R_f \parallel R_C)$$

$$r_\pi = \frac{V_T}{I_B} = \frac{0.025}{0.015} = 1.66 \text{ k}\Omega$$

$$R_i = R_s \parallel R_f \parallel r_\pi = 1.4 \text{ k}\Omega$$

$$R_o = R_C \parallel R_f = 4.27 \text{ k}\Omega$$

$$g_m = \frac{I_c}{V_T} = 60 \text{ mS}$$

$$A = \frac{V_o}{I_i} = -g_m (R_f \parallel R_C) (R_s \parallel R_f \parallel r_\pi)$$

$$= -358.7 \text{ k}\Omega$$

4. Thus

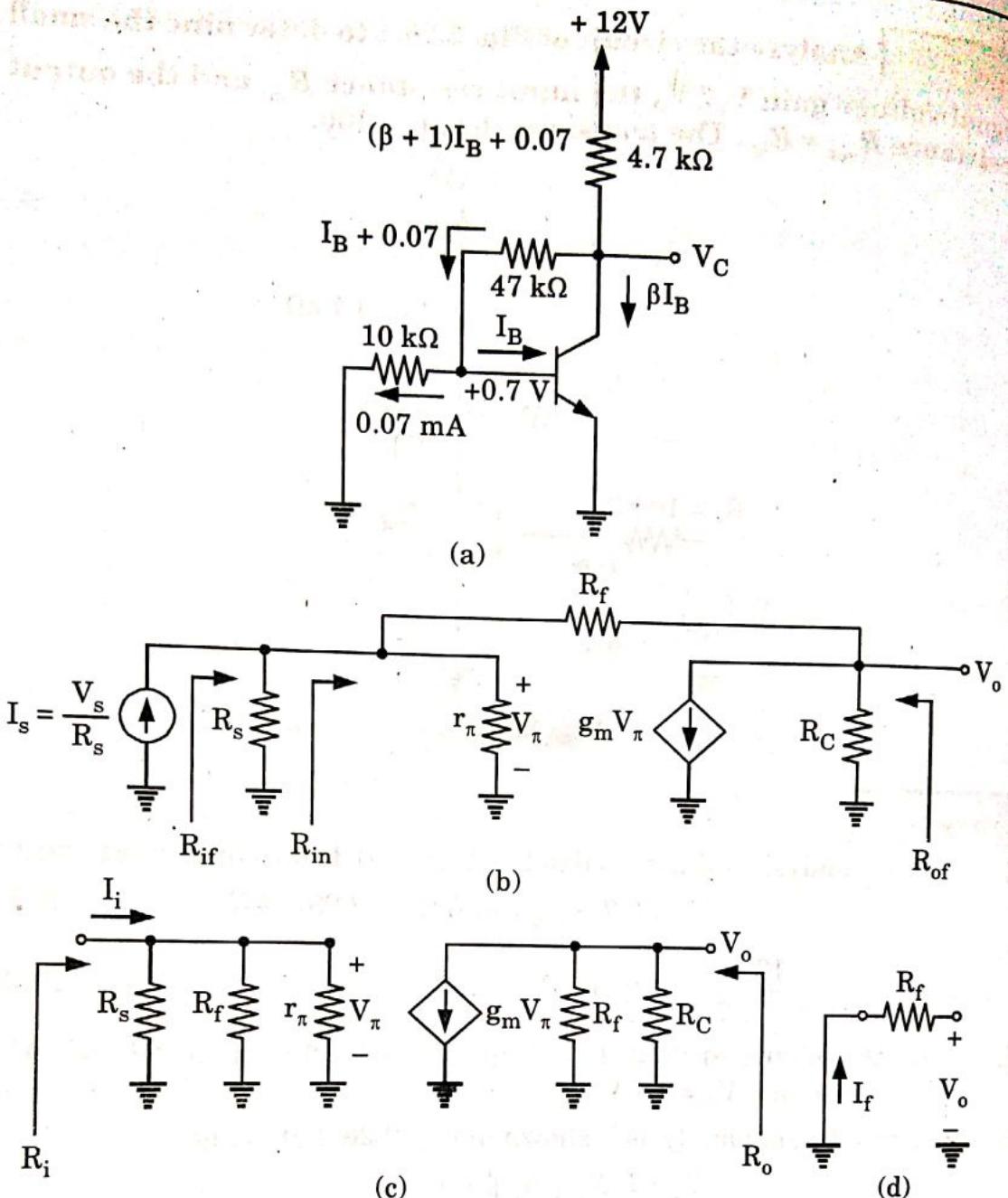


Fig. 2.26.2.

5. The circuit for determining  $\beta$  is shown in Fig. 2.26.2(d), from which obtain

$$\beta = \frac{I_f}{V_o} = -\frac{1}{R_f} = -\frac{1}{47 \text{ k}\Omega}$$

6. We can now obtain  $A_f$  (for the circuit in Fig. 2.26.2(b)) as

$$A_f = \frac{V_o}{I_s} = \frac{A}{1 + A\beta}$$

$$\frac{V_o}{I_s} = \frac{-358.7}{1 + 358.7 / 47} = \frac{-358.7}{8.63} = -41.6 \text{ k}\Omega$$

1. Thus

$$\frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{-41.6}{10} = -4.16 \text{ V/V}$$

8. The input resistance and output resistance with feedback in Fig. 2.26.2(b) is given by,

$$R_{if} = \frac{R_i}{1 + A\beta} = \frac{1.4}{8.63} = 162.2 \Omega$$

$$R_{of} = \frac{R_o}{1 + A\beta} = \frac{4.27}{8.63} = 495 \Omega$$

### PART-6

*Concept of Stability, Gain Margin, Phase Margin.*

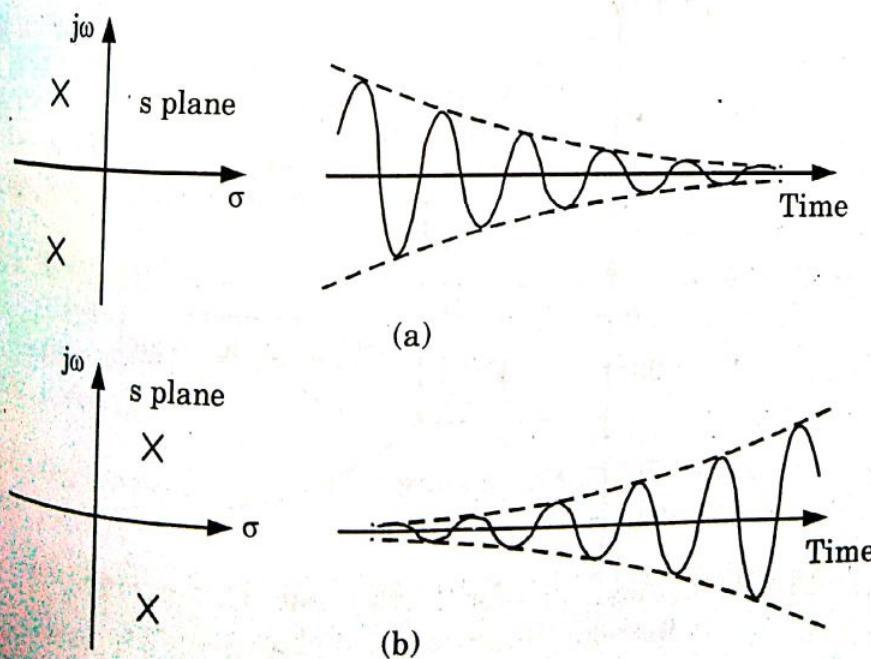
#### Questions-Answers

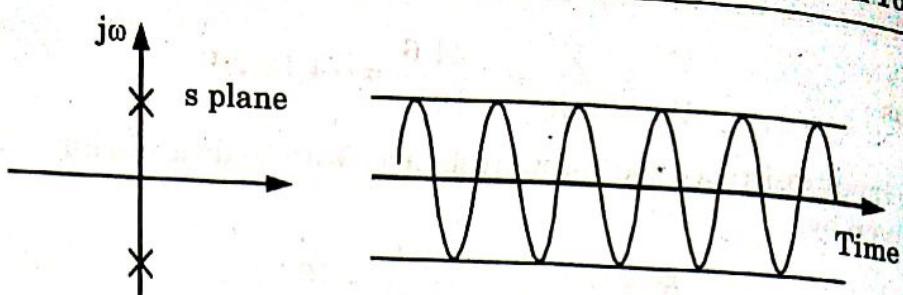
#### Long Answer Type and Medium Answer Type Questions

**Que 2.27.** Explain the relationship between stability and pole location.

#### Answer

- For an amplifier or any other system to be stable, its poles should lie in the left half of the  $s$ -plane.
- A pair of complex conjugate poles on the  $j\omega$  axis gives rise to sustained sinusoidal oscillations.





(c)

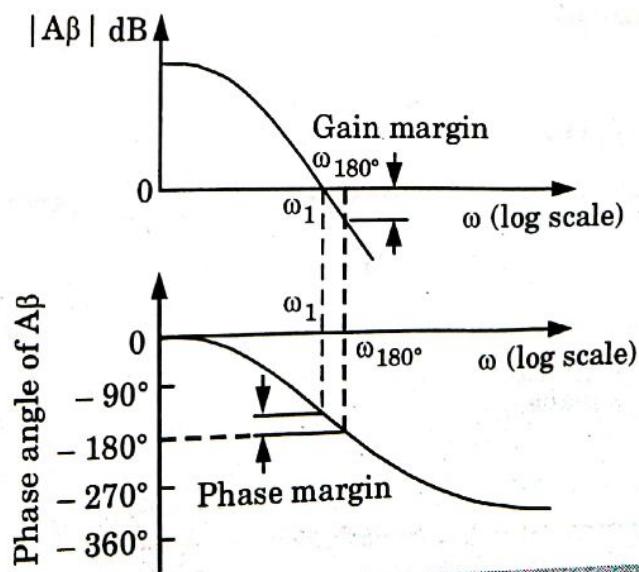
**Fig. 2.27.1.** Relationship between pole location and transient response.

3. Poles in the right half of the s plane give rise to growing oscillations.
4. Consider an amplifier with a pole pair at  $s = \sigma_o \pm j\omega_n$ .
5. If the poles are in the left half of the s plane, then  $\sigma_o$  will be negative and the oscillations will decay exponentially toward zero, as shown in Fig. 2.27.1(a), indicating that the system is stable.
6. If the poles are in the right half-plane, then  $\sigma_o$  will be positive, and the oscillation will grow exponentially as shown in Fig. 2.27.1(b).
7. If the poles are on the  $j\omega$ -axis, then  $\sigma_o$  will be zero and the oscillations will be sustained, as shown in Fig. 2.27.1(c).

**Que 2.28.** What is the effect of gain margin and phase margin on stability ?

**Answer**

1. A feedback amplifier is or is not stable by examining its loop gain  $A\beta$  as a function of frequency.
2. The use of a Bode plot for  $A\beta$  is shown in Fig. 2.28.1.
3. The feedback amplifier whose loop gain is plotted in Fig. 2.28.1 will be stable, since at the frequency of  $180^\circ$  phase shift,  $\omega_{180}$ , the magnitude of the loop gain is less than unity (negative dB).



**Fig. 2.28.1.** Bode plot for the loop gain  $A\beta$  illustrating the definitions of the gain and phase margins.

4. The difference between the value of  $|A\beta|$  at  $\omega_{180}$  and unity, called the gain margin, is usually expressed in decibels.
5. The gain margin represents the amount by which the loop gain can be increased while stability is maintained.
6. Another way to determine the stability and to express its degree is to examine the Bode plot at the frequency for which  $|A\beta| = 1$ , which is the point at which the magnitude plot crosses the 0-dB line.
7. If at this frequency the phase angle is less (in magnitude) than  $180^\circ$ , then the amplifier is stable.
8. The difference between the phase angle at this frequency and  $180^\circ$  is termed the phase margin.
9. On the other hand, if at the frequency of unity loop-gain magnitude, the phase lag is in excess of  $180^\circ$ , the amplifier will be unstable.

### VERY IMPORTANT QUESTIONS

*Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.*

Q.1. Draw the equivalent circuit of BJT at high frequency and derive the expression for upper cut-off frequency.

**Ans.** Refer Q. 2.1.

Q.2. Draw the high frequency small signal circuit of a MOSFET with load resistance using the effect of Miller capacitance. Also derive an expression for the Miller capacitance and cut-off frequency ( $f_T$ ).

**Ans.** Refer Q. 2.2.

Q.3. Explain the frequency response of common emitter configuration.

**Ans.** Refer Q. 2.4.

Q.4. Write the different coupling scheme of multistage amplifier. Explain frequency response of RC coupled amplifier in two-stage CE configuration.

**Ans.** Refer Q. 2.6.

Q.5. Derive power-conversion efficiency of class A output stage.

**Ans.** Refer Q. 2.10.

Q.6. Why is class C amplifier's efficiency higher than that of class A amplifier?

## Questions-Answers

## Long Answer Type and Medium Answer Type Questions

**Que 3.1.** What is the basic principle of sinusoidal oscillators ? Explain Barkhausen criterion.

**Answer**

1. Sinusoidal oscillators are electronic circuits that produce oscillations of sinusoidal nature. They work on the principle of Barkhausen criterion.
2. The basic structure of sinusoidal oscillator consists of an amplifier and a frequency-selective network connected in a positive feedback loop, shown in Fig. 3.1.1.
3. The gain with feedback is given by,

$$A_f(s) = \frac{A(s)}{1 - A(s)\beta(s)} \quad \dots(3.1.1)$$

Here loop gain is

$$L(s) = A(s)\beta(s) \quad \dots(3.1.2)$$

and the characteristic equation,  $1 - L(s) = 0$

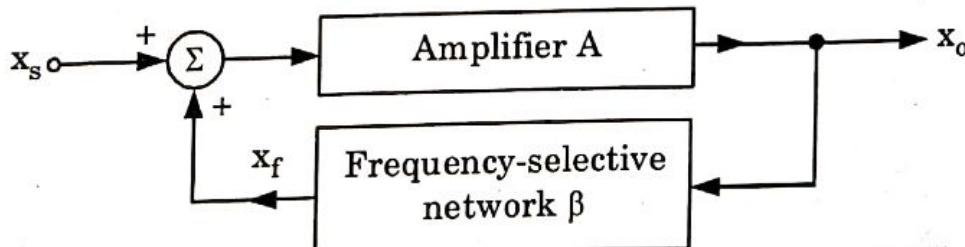


Fig. 3.1.1. The basic structure of a sinusoidal oscillator.

4. If at a specific frequency  $f_o$ , the loop gain  $A\beta$  is equal to unity, it follows from eq. (3.1.1) that  $A_f$  will be infinite. That is, at this frequency the circuit will have finite output for zero input signal. Such a circuit is an oscillator.
5. Thus the condition for the feedback loop of Fig. 3.1.1 to provide sinusoidal oscillations of frequency  $\omega_o$  is

$$L(j\omega_o) = A(j\omega_o)\beta(j\omega_o) = 1$$

That is, at  $\omega_o$  the phase of the loop gain should be zero and the magnitude of the loop gain should be unity. This is known as the Barkhausen criterion.

6. For this loop, (Fig. 3.1.1) to produce and sustain an output  $x_o$  with no input applied ( $x_s = 0$ ), the feedback signal  $x_f$  is,

$$x_f = \beta x_o$$

should be sufficiently large that when multiplied by  $A$  it produces  $x_o$ , that is,

$$Ax_f = x_o$$

i.e.,

$$A\beta x_o = x_o$$

...(3.1.3)

which results in

$$A\beta = 1$$

...(3.1.4)

7. Thus, the Barkhausen criterion defines two basic requirements for oscillations:

- i. Total phase shift in the closed loop is  $0^\circ$  or  $360^\circ$ .
- ii. The magnitude of loop gain, i.e.,  $|A\beta| = 1$ .

## PART-2

*RC Oscillators (Phase Shift, Wien Bridge etc.).*

### Questions-Answers

### Long Answer Type and Medium Answer Type Questions

- Que 3.2.** Draw the circuit of an *RC* phase-shift oscillator using op-amp and derive frequency and condition of oscillation for *RC* phase-shift oscillator.

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**OR**

Write the disadvantages of *RC* phase-shift oscillator. Draw the circuit diagram of *RC* phase-shift oscillator and derive the expression for frequency.

### Answer

1. The *RC* phase-shift oscillator consisting of an op-amp serving as the amplifier stage, and the cascaded *RC* network acting as the feedback circuit is shown in Fig. 3.2.1.
2. The op-amp is used in inverting configuration, and it produces  $180^\circ$  phase-shift at the output.
3. The cascaded *RC* networks connected in the feedback network path provide an additional phase-shift of  $180^\circ$ . Therefore, the total phase-shift around the loop is achieved to be  $360^\circ$  (or  $0^\circ$ ).

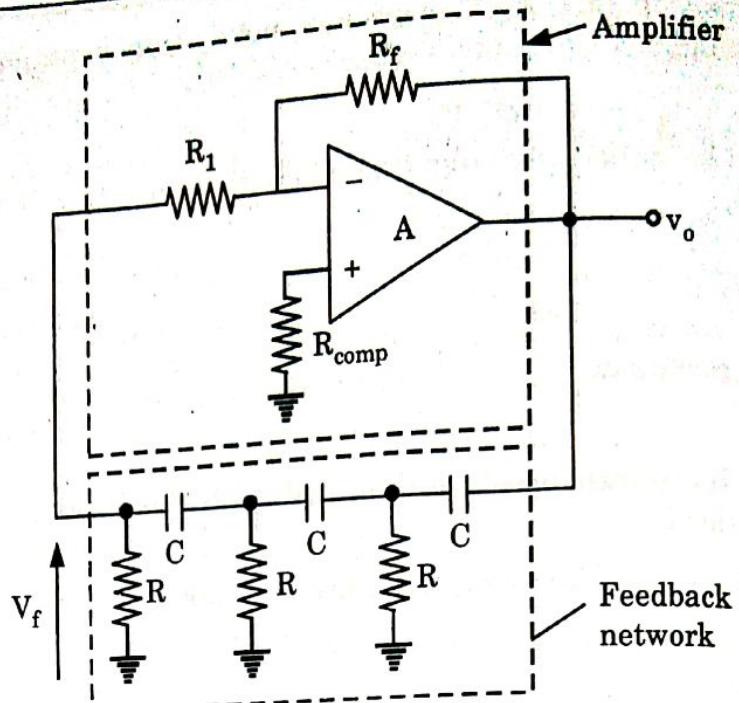


Fig. 3.2.1. RC phase-shift oscillator.

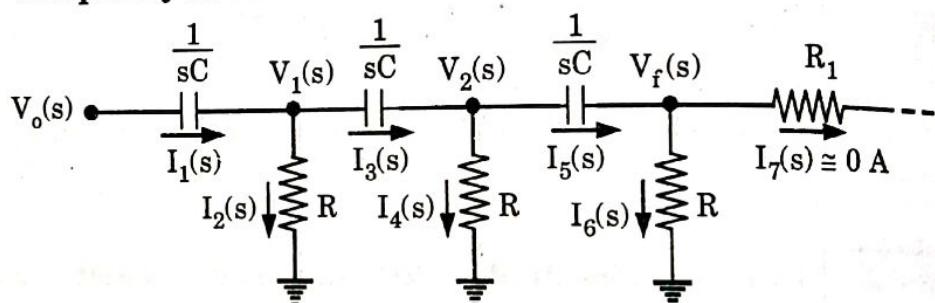
**Frequency of oscillation :**

Fig. 3.2.2. RC network of the phase-shift oscillator in s-domain.

1. Applying Kirchhoff's current law at node  $V_1(s)$  as shown in Fig. 3.2.2 and we have

$$I_1(s) = I_2(s) + I_3(s)$$

$$\frac{V_o(s) - V_1(s)}{(1/sC)} = \frac{V_1(s)}{R} + \frac{V_1(s) - V_2(s)}{(1/sC)}$$

Thus,

$$V_1(s) = \frac{[V_o(s) + V_2(s)]RCs}{2RCs + 1} \quad \dots(3.2.1)$$

2. Similarly, at node  $V_2(s)$ ,

$$I_3(s) = I_4(s) + I_5(s)$$

$$\frac{V_1(s) - V_2(s)}{(1/sC)} = \frac{V_2(s)}{R} + \frac{V_2(s) - V_f(s)}{(1/sC)}$$

Solving for  $V_1(s)$ , we get

$$V_1(s) = \frac{(2RCs + 1)V_2(s)}{RCs} - V_f(s) \quad \dots(3.2.2)$$

When  $R_1 \gg R$ ,  $I_5 \approx I_6$  and  $V_f(s) = V_2(s) \frac{R}{\left(R + \frac{1}{sC}\right)}$

Therefore,

$$V_2(s) = \frac{(RCs + 1)}{RCs} V_o(s) \quad \dots(3.2.3)$$

Substituting eq. (3.2.3) and eq. (3.2.1) in eq. (3.2.2) result in

$$\frac{RCsV_o(s)}{2RCs + 1} + \frac{(RCs + 1)V_f(s)}{2RCs + 1} = \frac{(2RCs + 1)(RCs + 1)V_f(s)}{(RCs)^2} - V_f(s)$$

Simplifying for  $\frac{V_f(s)}{V_o(s)}$ , we get

$$\beta = \frac{V_f(s)}{V_o(s)} = \frac{R^3 C^3 s^3}{R^3 C^3 s^3 + 6R^2 C^2 s^2 + 5RCs + 1} \quad \dots(3.2.4)$$

The voltage gain of the op-amp is

$$A = \frac{V_o(s)}{V_f(s)} = -\frac{R_f}{R_1} \quad \dots(3.2.5)$$

We know that for any oscillator, the necessary condition for the oscillation is  $A\beta = 1$ . Therefore, using eq. (3.2.4) and (3.2.5), we obtain

$$A\beta = -\frac{R_f}{R_1} \frac{R^3 C^3 s^3}{R^3 C^3 s^3 + 6R^2 C^2 s^2 + 5RCs + 1} = 1 \quad \dots(3.2.6)$$

Substituting  $s = j\omega_o$  in eq. (3.2.6), we obtain

$$\left(-\frac{R_f}{R_1}\right)(-j\omega_o^3 R^3 C^3) = (-j\omega_o^3 R^3 C^3) - 6\omega_o^2 R^2 C^2 + j5\omega_o R C + 1 \quad \dots(3.2.7)$$

Equating the real parts of eq. (3.2.7), we get

$$0 = -6\omega_o^2 R^2 C^2 + 1 \quad \dots(3.2.8)$$

$$\omega_o^2 = \frac{1}{6R^2 C^2} \quad \dots(3.2.9)$$

or

$$f_o = \frac{1}{2\pi\sqrt{6RC}}$$

Equating the imaginary parts of eq. (3.2.7), we get

$$\left(-\frac{R_f}{R_1}\right)(-j\omega_o^3 R^3 C^3) = -j\omega_o^3 R^3 C^3 + 5j\omega_o R C$$

$$\text{i.e., } \frac{-R_f}{R_1} = 1 - \frac{5}{\omega_o^2 R^2 C^2}$$

9. Substituting for  $\omega_o^2$  from eq. (3.2.9),

$$\left| \frac{R_f}{R_1} \right| = |1 - 30| = 29 \text{ or } R_f = 29 R_1 \quad \dots(3.2.10)$$

Therefore, the gain of the amplifier should be at least 29, and the total phase-shift around the loop should be exactly  $360^\circ$ .

### Disadvantages of phase-shift oscillator :

1. It is difficult for the circuit to start oscillations as a feedback is generally small.
2. The circuit gives small output.

**Que 3.3.** Write a short note on ring oscillator.

### Answer

1. Ring oscillator is an example of phase-shift oscillator. It is used in digital integrated circuit for clock generation.
2. The ring oscillator consists of odd number of inverters connected in a ring as shown in Fig. 3.3.1. The load of each inverter is a capacitor.

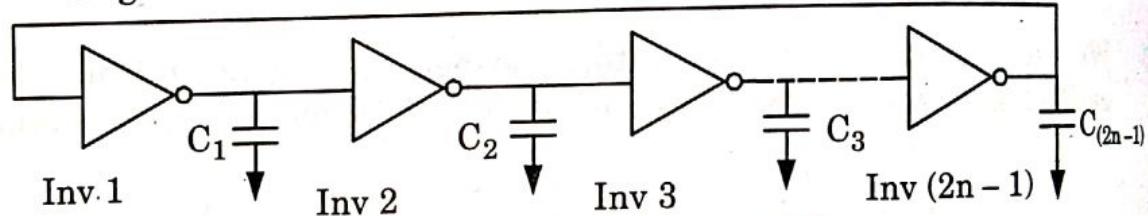


Fig. 3.3.1. Ring oscillator.

3. It is known that every inverter provides a  $180^\circ$  phase shift between input and output.
4. If the inverters and the associated load capacitors generate a net phase shift at the last inverter output in multiples of  $360^\circ$ , then the feedback signal is in phase with the input and the oscillations can be sustained.
5. Since the output of an inverter is a pulse, the ring oscillator generates pulses.
6. The frequency of this pulse generator is decided by the propagation delay per inverter stage and the number of such (odd) stages.

**Que 3.4.** In a *RC* phase-shift oscillator,  $R = 100 \text{ k}\Omega$  and  $C = 600 \text{ pF}$ . Find the frequency of oscillation of the oscillator.

### Answer

**Given :**  $R = 100 \text{ k}\Omega$ ,  $C = 600 \text{ pF}$

**To Find :**  $f_o$

Frequency of  $RC$  phase-shift oscillator,

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

$$= \frac{1}{2\pi \times 100 \times 10^3 \times 600 \times 10^{-12} \sqrt{6}}$$

$$= 1082.91 \text{ Hz}$$

$$= 1.082 \text{ kHz}$$

Que 3.5.

Write a short note on the Wien bridge oscillator.

Answer

- Fig. 3.5.1 shows Wien bridge oscillator. The circuit consists of an op-amp connected in the non-inverting configuration, with a closed loop gain  $\left(1 + \frac{R_2}{R_1}\right)$ . In the feedback path, an  $RC$  network is connected.
- There are two feedback paths in Fig. 3.5.1, positive feedback through  $Z_p$  and  $Z_s$ , whose components determine the frequency of oscillation, and negative feedback through  $R_1$  and  $R_2$ , whose elements affect the amplitude of oscillation and set the gain of the op-amp stage.

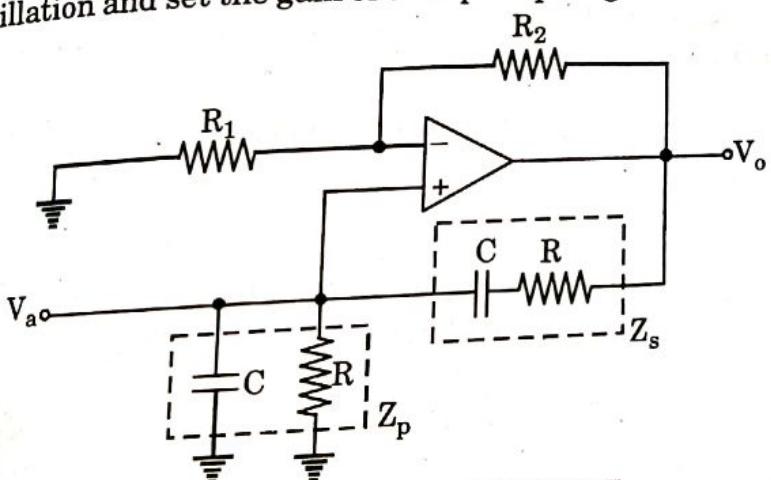


Fig. 3.5.1. Wien-bridge oscillator.

- The loop gain can be easily obtained as

$$L(s) = \left[1 + \frac{R_2}{R_1}\right] \left[ \frac{Z_p}{Z_p + Z_s} \right] \quad \dots(3.5.1)$$

where,

$$Z_p = \frac{R \times \frac{1}{sC}}{R + \frac{1}{sC}} = \frac{R}{1 + sRC}, \quad Z_s = R + \frac{1}{sC} = \frac{sRC + 1}{sC}$$

- Putting values of  $Z_p$  and  $Z_s$ , in eq. (3.5.1)

$$L(s) = \frac{1 + R_2/R_1}{3 + sCR + 1/sCR}$$

Putting  $s = j\omega$ ,

$$L(j\omega) = \frac{1 + R_2/R_1}{3 + j\omega CR - \frac{j}{\omega CR}}$$

5. Loop gain will be real number at one frequency given by

$$\omega_o CR = \frac{1}{\omega_o CR}$$

$$\omega_o = \frac{1}{CR} \Rightarrow f_o = \frac{1}{2\pi RC}$$

6. To obtain sustained oscillation at  $\omega_o$ , we should set the magnitude of the loop gain to unity. This can be achieved by selecting

$$R_2/R_1 = 2$$

**Que 3.6.** Draw a circuit diagram of Wien bridge oscillator and derive an expression of frequency of oscillation. Calculate the frequency of oscillation for given values of  $R_1 = R_2 = 200 \text{ k}\Omega$ ,  $C_1 = C_2 = 200 \text{ pF}$ .

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### Answer

**Wien bridge oscillator :** Refer Q. 3.5, Page 3-7E, Unit-3.

**Numerical :**

Given :  $R_1 = R_2 = 200 \text{ k}\Omega$ ,  $C_1 = C_2 = 200 \text{ pF}$

To Find :  $f_o$ .

$$f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 200 \times 10^3 \times 200 \times 10^{-12}} \\ = 0.03978 \times 10^5 \text{ Hz} = 3.978 \text{ kHz}$$

### PART-3

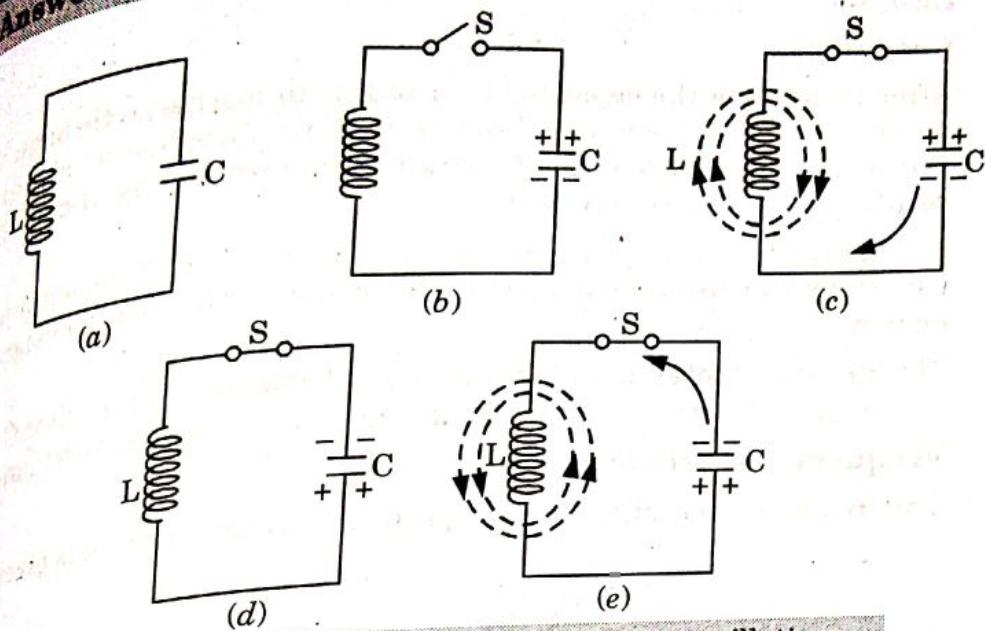
*LC Oscillators (Hartley, Colpitt, Clapp etc.).*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 3.7.** Explain the operation of LC tank circuit.

AKTU 2016-17, Marks 7.5

**Answer**

**Fig. 3.7.1.** LC tank circuit for generating oscillations.

The inductor  $L$  stores electromagnetic energy in it when current flows through it. If voltage is applied to the capacitor  $C$ , it stores electrostatic energy in its electric field.

**Case I :** Refer to Fig. 3.7.1(b), suppose the capacitor  $C$  is charged from DC voltage with the polarities as shown. Now the capacitor  $C$  has voltage across it, hence it stores electrostatic energy across it.

**Case II :**

- As the switch  $S$  is closed, the capacitor  $C$  discharges through the inductor  $L$  due to flow of electrons as shown in Fig. 3.7.1(c). Due to this current flow, magnetic field gets set around the inductor coil  $L$ . This magnetic field stores electromagnetic energy.
- The current increases slowly to maximum value and the capacitor is discharged fully.
- When the capacitor  $C$  gets discharged fully, the electrical energy (electrostatic energy) across it is completely converted into magnetic field energy (electromagnetic energy) around the inductor coil  $L$ .

**Case III :**

- As the capacitor  $C$  gets discharged completely, the magnetic field around the inductor coil starts to collapse resulting to develop counter emf.
- Due to this counter emf, current flows in the same direction as per Lenz law. Due to this, the capacitor gets charge with opposite polarity as shown in Fig. 3.7.1(d).

3. As the capacitor  $C$  gets charged fully, the electromagnetic energy around the inductor coil has now converted into electrostatic energy in the capacitor.

**Case IV :**

1. After recharging the capacitor  $C$ , it begins to discharge through the inductor coil  $L$  but current flows in opposite direction as shown in Fig. 3.7.1(e). This sequence of charging and discharging of capacitor results into alternating current.
2. The energy is alternately stored in the electric field of capacitor (i.e., electrostatic energy) and magnetic field of inductor (i.e., electromagnetic energy).
3. This process of interchanging the energy between the capacitor  $C$  and the inductor  $L$  is repeated resulting to generate electrical oscillations.

**Frequency of oscillations :**

The frequency of oscillations ( $f_o$ ) produced by tank circuit is given by

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

**Que 3.8.** Explain Colpitts oscillator.

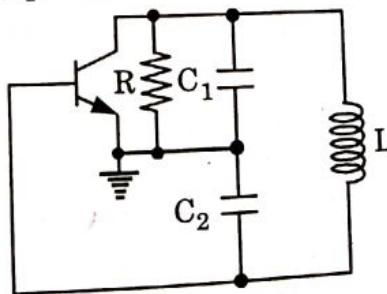
**OR**

Derive the expression for the loop gain and frequency of oscillation for Colpitts oscillator.

**AKTU 2014-15, Marks 10**

**Answer**

1. The schematic of Colpitts oscillator is shown in Fig. 3.8.1.

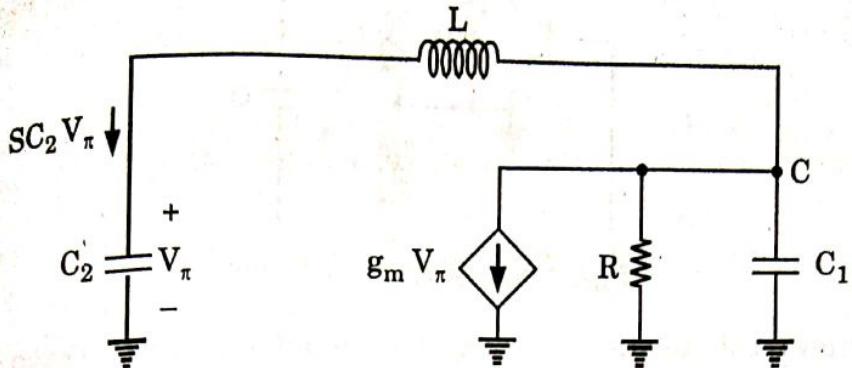


**Fig. 3.8.1.**

2. Colpitts oscillator utilizes a parallel  $LC$  circuit connected between collector and base (or between drain and gate if a FET is used) with a fraction of the tuned-circuit voltage fed to the emitter.
3. This feedback is achieved by the way of a capacitive divider in the Colpitts oscillator circuit.
4. For Colpitts oscillator, the frequency of operation is given by

$$\omega_o = 1/\sqrt{L \left( \frac{C_1 C_2}{C_1 + C_2} \right)}$$

**Derivation for loop gain and frequency of operation :**



**Fig. 3.8.2. Equivalent circuit of the Colpitts oscillator.**

1. Apply KCL at node C gives

$$sC_2V_\pi + g_m V_\pi + \left( \frac{1}{R} + sC_1 \right) (1 + s^2LC_2)V_\pi = 0 \quad \dots(3.8.1)$$

2. Since  $V_\pi \neq 0$  (oscillations have started), it can be eliminated, and eq. (3.8.1) can be rearranged in the form

$$s^3LC_1C_2 + s^2(LC_2/R) + s(C_1 + C_2) + \left( g_m + \frac{1}{R} \right) = 0 \quad \dots(3.8.2)$$

Substituting  $s = j\omega$  gives,

$$\left( g_m + \frac{1}{R} - \frac{\omega^2 LC_2}{R} \right) + j[\omega(C_1 + C_2) - \omega^3 LC_1C_2] = 0 \quad \dots(3.8.3)$$

3. For oscillations, to start, both the real and imaginary parts must be zero. Equating the imaginary part of eq. (3.8.3) to zero gives the frequency of oscillation as

$$\omega_o = 1/\sqrt{L \left( \frac{C_1 C_2}{C_1 + C_2} \right)} \quad \dots(3.8.4)$$

which is the resonance frequency of the tank circuit.

4. Equating the real part of eq. (3.8.3) to zero together with using eq. (3.8.4) gives condition of oscillation as

$$C_2/C_1 = g_m R \quad \dots(3.8.5)$$

**Que 3.9.**

**Explain Hartley oscillator. AKTU 2016-17, Marks 7.5**

**Answer**

1. The schematic of Hartley oscillator is shown in Fig. 3.9.1.

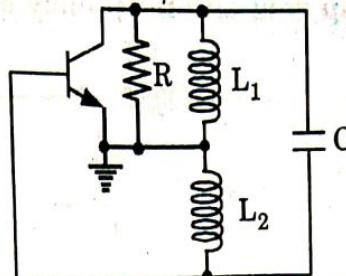


Fig. 3.9.1. Hartley oscillator.

2. Hartley oscillator utilizes a parallel LC circuit connected between collector and base with a fraction of the tuned-circuit voltage fed to the emitter.
3. This feedback is achieved by the way of an inductive divider in the Hartley oscillator circuit.
4. For Hartley oscillator, the frequency of operation is given by

$$\omega_0 = 1/\sqrt{(L_1 + L_2)C}$$

**Derivation for loop gain and frequency of operation :**

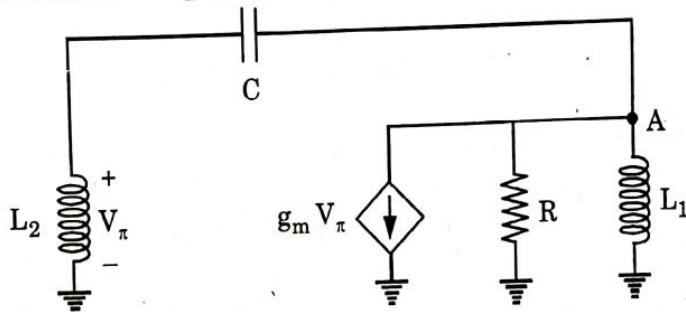


Fig. 3.9.2. Equivalent circuit of the Hartley oscillator.

1. Apply KCL at node A

$$\frac{V_A}{R} + \frac{V_A}{sL_1} + g_m V_\pi + \frac{V_A}{sL_2 + \frac{1}{sC}} = 0 \quad \dots(3.9.1)$$

$$V_\pi = \frac{sL_2}{sL_2 + \frac{1}{sC}} V_A \quad \dots(3.9.2)$$

2. Substituting eq. (3.9.2) in eq. (3.9.1)

$$V_A \left[ \frac{1}{R} + \frac{1}{sL_1} + \frac{s^2 g_m L_2 C}{s^2 L_2 C + 1} + \frac{sC}{s^2 L_2 C + 1} \right] = 0 \quad \dots(3.9.3)$$

3. Substituting  $s = j\omega$  in eq. (3.9.3) gives

$$\left( \frac{1}{R} - \frac{\omega^2 g_m L_2 C}{1 - \omega^2 L_2 C} \right) + j \left( \frac{\omega C}{1 - \omega^2 L_2 C} - \frac{1}{\omega L_1} \right) = 0 \quad \dots(3.9.4)$$

4. Equating the imaginary part of eq. (3.9.4) to zero gives the frequency of oscillation as

$$\omega_o = 1/\sqrt{(L_1 + L_2)C} \quad \dots(3.9.5)$$

5. Equating the real part of eq. (3.9.4) to zero together with using eq. (3.9.5) gives the condition of oscillation as

$$g_m R = \frac{L_1}{L_2}$$

**Que 3.10.**

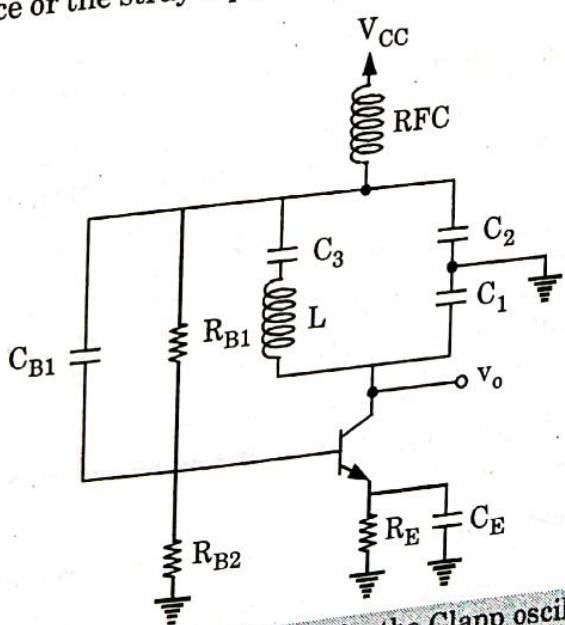
Explain Clapp oscillator.

OR

What is the drawback of Colpitts oscillator? How it can be removed by Clapp oscillator?

**Answer**

1. The drawback of the Colpitts oscillator is that its frequency stability is very poor.
2. To overcome this drawback, the inductor  $L$  is replaced by a series combination of inductor  $L$  and capacitor  $C_3$ , with a very small value of  $C_3$  compared to either  $C_1$  or  $C_2$ .
3. As  $C_3 \ll C_1, C_2$ , the stability of the circuit is improved because the frequency of oscillation is only dependent on  $C_3$  and not on any other capacitance or the stray capacitance of the transistor.



**Fig. 3.10.1.** Complete circuit for the Clapp oscillator.

4. Fig. 3.10.1 shows the modified Colpitts oscillator, which is known as the Clapp oscillator, where a capacitor  $C_3$  has been added in series with the inductor.
5. For the Colpitts oscillator, the frequency of oscillation is given by

$$\omega_o = \frac{1}{\sqrt{L \left( \frac{C_1 C_2}{C_1 + C_2} \right)}}$$

6. Assuming that all the three capacitors are in series, the frequency of oscillation for the Clapp oscillator becomes

$$\omega_o = \frac{1}{\sqrt{LC}}$$

where,  $\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$

7. We know that  $C_3 \ll C_1, C_2$ . Hence,

$$C \approx C_3$$

$$\therefore \omega_o = \frac{1}{\sqrt{LC_3}}$$

**Que 3.11.** Which type of feedback is seen in Wien bridge oscillator? Compare the performances of  $RC$  oscillators and  $LC$  oscillators.

### Answer

**Feedback in Wien bridge oscillator :** Refer Q. 3.5, Page 3-7E, Unit-3.

S.No.	RC oscillators	LC oscillators
1.	$RC$ oscillators are used for generating frequencies upto 1 MHz.	$LC$ oscillators are used for generating frequencies higher than 1 MHz.
2.	$RC$ networks are used.	$LC$ networks are used.
3.	Wien-bridge oscillator, phase-shift oscillators etc. are some $RC$ oscillators.	Crystal tuned, Colpitts oscillators etc. are some $LC$ oscillators.
4.	It has large degree of distortion.	It has less degree of distortion.
5.	It creates non-linearity.	It does not create non-linearity.
6.	Tuned circuit is absent because $RC$ oscillator generates only low frequencies.	Tuned circuit or tank circuit is used because the oscillators are difficult to tune over large frequencies.
7.	It has low quality factor.	It has high quality factor.

**PART-4***Non-Sinusoidal Oscillators.***CONCEPT OUTLINE**

Blocking oscillator and multivibrator are relaxation oscillator.

**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 3.12.** Draw the circuit diagram for monostable multivibrator with operational amplifier. Explain its operation. Derive the expression for its time period.

**OR**

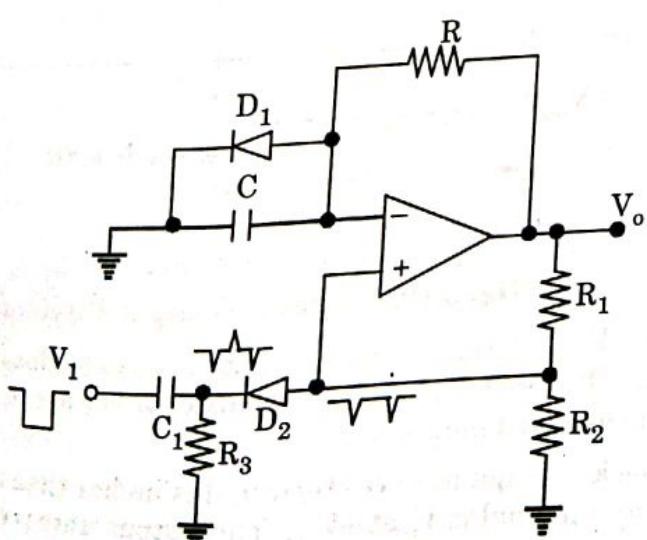
What do you mean by non-sinusoidal oscillators ?

**Answer**

**Non-sinusoidal or relaxation oscillators :** The oscillators which produce square waves, triangular waves, pulses or sawtooth waves are known as relaxation oscillators.

**Circuit diagram for monostable multivibrator :**

- Fig. 3.12.1 shows the circuit diagram of monostable multivibrator. A diode  $D_1$  clamps the capacitor voltage to 0.7 V when the output is at  $+V_{sat}$ .



**Fig. 3.12.1.**

2. The negative going pulse signal of magnitude  $V_1$  (triggering signal) passing through the differentiator  $R_3C_1$  and diode  $D_2$  produces a negative going triggering pulse and is applied to the (+) input terminal.

#### Operation :

- For monostable operation, the trigger pulse width  $T_p$  should be much less than  $T$ , the pulse width of the monostable multivibrator.
- The diode  $D_2$  is used to avoid malfunctioning by blocking the positive spikes that may be present at the differentiated trigger input.
- Fig. 3.12.2 shows the trigger and output waveform.

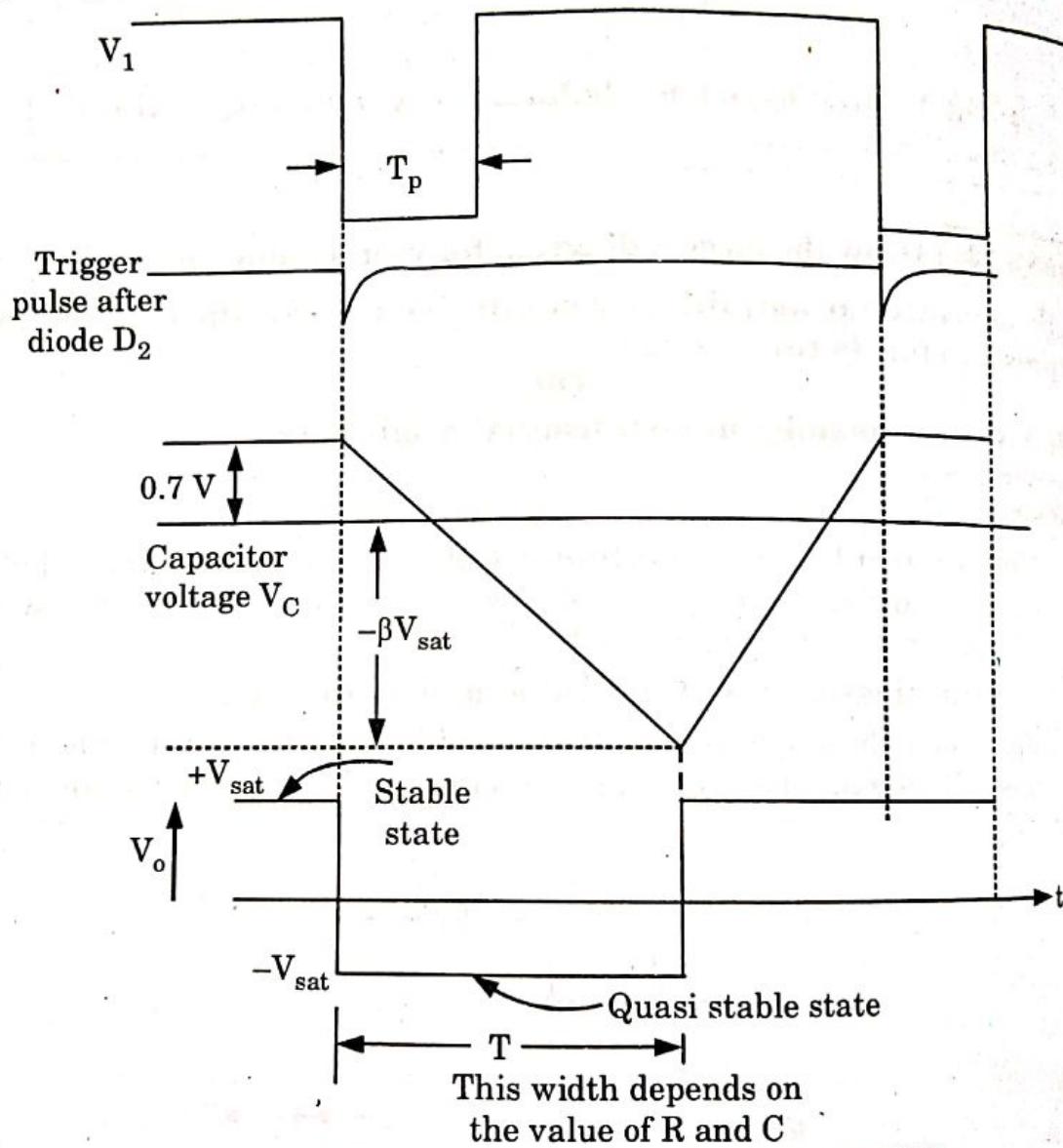


Fig. 3.12.2. Input and output waveform

- When  $V_o$  is  $+V_{\text{sat}}$ , voltage divider  $R_1$  and  $R_2$  gives feedback  $+\beta V_{\text{sat}}$  to the (+ve) input. The diode  $D_1$  clamps the capacitor voltage to  $0.7 \text{ V}$  (because the diode is forward biased).
- The feedback voltage at (+ve) terminal is higher than (-ve) terminal therefore op-amp holds  $V_o$  at  $+V_{\text{sat}}$ . This output state is called as stable state.

6. If the negative spike (trigger signal) is applied to (+ve) of op-amp which is higher than the voltage at (-ve) terminal. The combination of feedback voltage and negative trigger voltage will be pulled below the voltage at (-ve) input.
7. Once the (+ve) input becomes negative with respect to the (-ve) input,  $V_o$  switches to  $-V_{sat}$ . With this change, the one-shot is now in its timing state. This state is an unstable state.
8. Due to  $V_o = -V_{sat}$ , the diode  $D_1$  is reverse biased and the capacitor  $C$  charges. The (-ve) input becomes more and more negative with respect to ground. When the capacitor voltage is more than (+ve) terminal,  $V_o$  switches to  $+V_{sat}$ .

### Expression for time period :

1. The general solution for a signal time constant low pass  $RC$  circuit with  $V_i$  and  $V_f$  as initial and final value is

$$V_o = V_f + (V_i - V_f) e^{-t/RC}$$

2. For the circuit,  $V_f = -V_{sat}$  and  $V_i = V_D$  (diode forward voltage)

The output  $V_C$  is

$$V_C = -V_{sat} + (V_D + V_{sat}) e^{-t/RC} \quad \dots(3.12.1)$$

If the time constant  $T = RC$  and when  $t = T$

$$V_C = -\beta V_{sat}$$

$$V_C = \frac{R_2}{R_1 + R_2} (-V_{sat})$$

where

$$\beta = \frac{R_2}{R_1 + R_2}$$

Therefore

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat}) e^{-t/RC}$$

After simplification, the pulse widths is obtained as

$$T = RC \ln \frac{(1 + V_D / V_{sat})}{1 - \beta} \quad \dots(3.12.2)$$

If  $V_{sat} \gg V_D$  and  $R_1 = R_2$  so that  $\beta = 0.5$  then

$$T = 0.69 RC \quad \dots(3.12.3)$$

**Ques 3.13.** Explain astable multivibrator with its waveform.

**Answer**

Square wave generator is also called as astable multivibrator or free running oscillator.

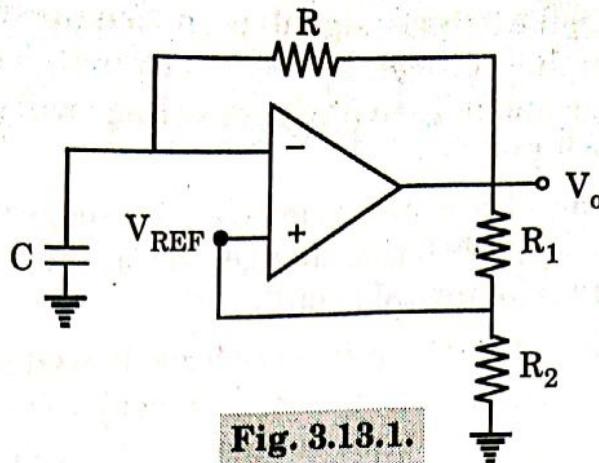


Fig. 3.13.1.

2. Circuit of square wave generator is as shown in Fig. 3.13.1. The principle of generation of square wave output is to force an op-amp to operate in the saturation region.
3. A fraction of output is fed back to the (+ve) input terminal. This fraction is given by

$$\beta = \frac{R_2}{R_1 + R_2}$$

4. Thus, the reference voltage is  $\beta V_o$  and may take values as  $+ \beta V_{sat}$  or  $- \beta V_{sat}$ . The output is also fed back to the (-ve) input terminal after integrating by means of a low-pass  $RC$  combination. When (-ve) input terminal voltage exceeds  $V_{REF}$ , switching takes place resulting in square wave output.
5. Now, consider the waveform shown in Fig. 3.13.2. When the output is at  $+ V_{sat}$ , capacitor  $C$  starts charging through  $R$ . Voltage at (+ve) input terminal is  $+ \beta V_{sat}$ . Now as the charge on  $C$  rises above this reference voltage  $+ \beta V_{sat}$ , output switches to  $- V_{sat}$ .

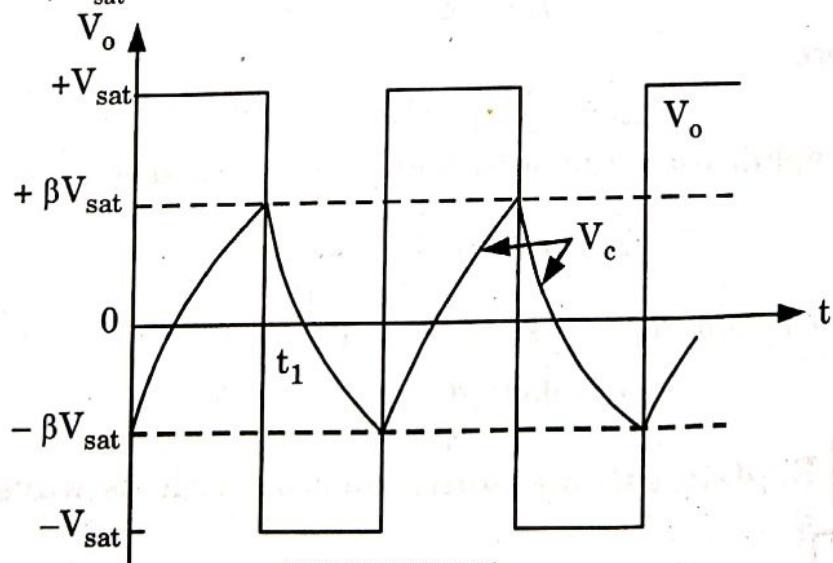


Fig. 3.13.2.

6. At this instant, voltage on the capacitor is  $+ \beta V_{sat}$ , hence it starts discharging through  $R$  i.e., charges towards  $- V_{sat}$ . When output voltage switches to  $- V_{sat}$ , the capacitor charges more negatively until its voltage just exceeds  $- \beta V_{sat}$ .
7. The output switches back to  $+ V_{sat}$  and hence the cycle repeats itself.
8. Now, voltage across the capacitor, as a function of time is given by

As,  
and

$$V_c(t) = V_{final} + (V_{initial} - V_{final}) e^{-t/RC}$$

$$V_{final} = \pm V_{sat}$$

$$V_{initial} = -\beta V_{sat}$$

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/RC}$$

$$V_c(t) = V_{sat} - V_{sat}(1 + \beta) e^{-t/RC}$$

9. At  $t = t_1$ , voltage across capacitor reaches to  $\pm \beta V_{sat}$ , therefore,
- $$V_c(t_1) = \beta V_{sat} = V_{sat} - V_{sat}(1 + \beta) e^{-t_1/RC}$$

After solving,  $t_1 = RC \ln\left(\frac{1+\beta}{1-\beta}\right)$

This is only half of the total period.

$$\therefore \text{Total time period} = 2t_1 = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

**Que 3.14.** Explain the generation of square and triangular waveforms from astable multivibrator operation using Op-Amp. Also find expression of the time period for both cases.

AKTU 2014-15, Marks 10

AKTU 2016-17, Marks 15

OR

Draw and explain the circuit of triangular wave generator. How square wave can be obtained using this triangular wave.

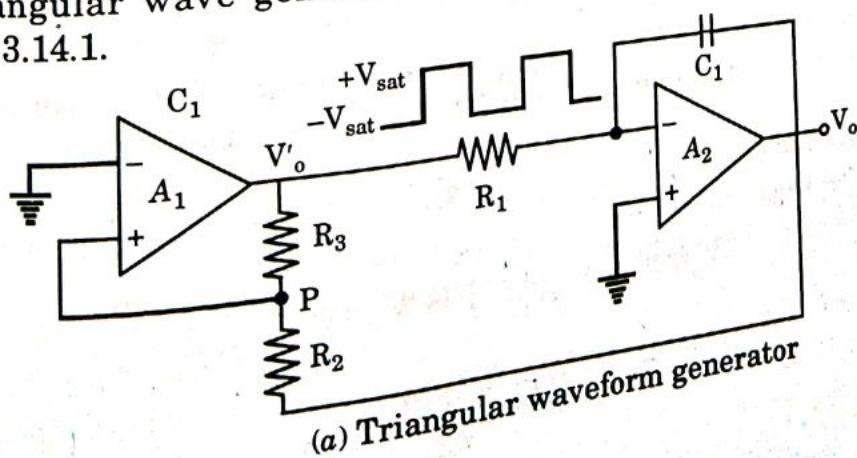
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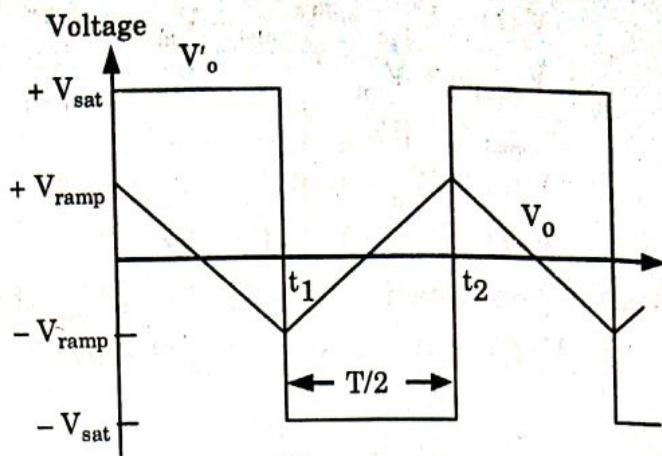
**Answer**

**Generation of square waveforms :** Refer Q. 3.13, Page 3-17E, Unit-3.

**Generation of triangular waveforms :**

1. A triangular wave can be simply obtained by integrating a square wave.
2. Triangular wave generator along with waveforms is shown in Fig. 3.14.1.





(b) Waveforms.

**Fig. 3.14.1.**

### Working :

1. Assume output of comparator  $A_1$  is at  $\pm V_{\text{sat}}$  so output of integrator will be a negative going ramp as shown in Fig. 3.14.1(b).
2. When the negative going ramp reaches to  $-V_{\text{ramp}}$ , the output of  $A_1$  switches from  $+V_{\text{sat}}$  to  $-V_{\text{sat}}$ . The sequence then repeats to give triangular wave at the output of  $A_2$ .
3. The frequency of triangular waveform can be calculated as follows :
  - i. The effective voltage at point  $P$  during the time when output of  $A_1$  is at  $+V_{\text{sat}}$  level is given by,

$$-V_{\text{ramp}} + \frac{R_2}{R_2 + R_3} [+V_{\text{sat}} - (-V_{\text{ramp}})] \quad \dots(3.14.1)$$

- ii. At  $t = t_1$ , the voltage at point  $P$  becomes equal to zero. Therefore from eq. (3.14.1)

$$-V_{\text{ramp}} = -\frac{R_2}{R_3} (+V_{\text{sat}}) \quad \dots(3.14.2)$$

- iii. Similarly, at  $t = t_2$ , when the output of  $A_1$  switches from  $-V_{\text{sat}}$  to  $+V_{\text{sat}}$ ,

$$V_{\text{ramp}} = \frac{-R_2}{R_3} (-V_{\text{sat}}) = \frac{R_2}{R_3} (V_{\text{sat}})$$

- iv. Therefore, peak to peak amplitude of the triangular wave is

$$V_o(pp) = +V_{\text{ramp}} - (-V_{\text{ramp}}) = 2 \frac{R_2}{R_3} V_{\text{sat}} \quad \dots(3.14.3)$$

- v. The output switches from  $-V_{\text{ramp}}$  to  $+V_{\text{ramp}}$  in half the time period  $T/2$ . Putting the values in the basic integrator equation,

$$\begin{aligned} V_o &= -\frac{1}{RC} \int v_i dt \\ V_o(pp) &= -\frac{1}{R_1 C_1} \int_0^{T/2} (-V_{\text{sat}}) dt = \frac{V_{\text{sat}}}{R_1 C_1} \left( \frac{T}{2} \right) \\ \text{or, } T &= 2R_1 C_1 \frac{V_o(pp)}{V_{\text{sat}}} \end{aligned} \quad \dots(3.14.4)$$

v. Putting the value of  $V_o(pp)$  from eq. (3.14.3), we get,  $T = \frac{4R_1C_1R_2}{R_3}$

Hence the frequency of oscillation  $f_o$  is,  $f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}$

**Generation of square wave using triangular wave :**

A square wave can be obtained by differentiating a triangular wave.

### VERY IMPORTANT QUESTIONS

*Following questions are very important. These questions may be asked in your SESSIONALS as well as UNIVERSITY EXAMINATION.*

Q. 1. What is the basic principle of sinusoidal oscillators ? Explain Barkhausen criterion.

Ans. Refer Q. 3.1.

Q. 2. Draw the circuit of an  $RC$  phase-shift oscillator using op-amp and derive frequency and condition of oscillation for  $RC$  phase-shift oscillator.

Ans. Refer Q. 3.2.

Q. 3. Draw a circuit diagram of Wien bridge oscillator and derive an expression of frequency of oscillation. Calculate the frequency of oscillation for given values of  $R_1 = R_2 = 200 \text{ k}\Omega$ ,  $C_1 = C_2 = 200 \text{ pF}$ .

Ans. Refer Q. 3.6.

Q. 4. Explain the operation of  $LC$  tank circuit.

Ans. Refer Q. 3.7.

Q. 5. Derive the expression for the loop gain and frequency of oscillation for Colpitts oscillator.

Ans. Refer Q. 3.8.

Q. 6. Explain Hartley oscillator.

Ans. Refer Q. 3.9.

Q. 7. Draw the circuit diagram for monostable multivibrator with operational amplifier. Explain its operation. Derive the expression for its time period.

Ans. Refer Q. 3.12.

Q. 8. Explain the generation of square and triangular waveforms from astable multivibrator operation using Op-Amp. Also find expression of the time period for both cases.

Ans. Refer Q. 3.14.



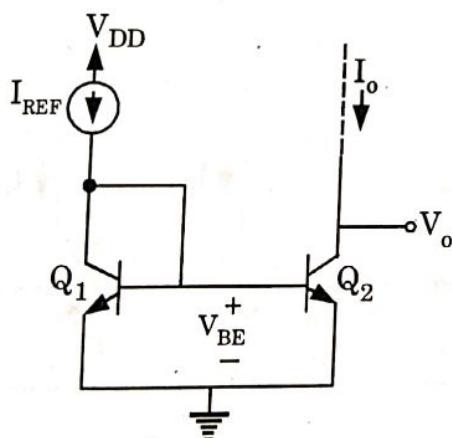
**PART-1***Current Mirror : Basic Topology and its Variants.***Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 4.1.** Draw the simple BJT current mirror circuit and deduce the expression for current transfer ratio using matched transistors.

**Answer**

1. The basic BJT current mirror is shown in Fig. 4.1.1.
2. Consider  $\beta$  is high and neglect base current.  $I_{REF}$  is passed through  $Q_1$  and the corresponding voltage is  $V_{BE}$ .  $V_{BE}$  is applied voltage between base and emitter of  $Q_2$ .
3. Now,  $Q_2$  is matched to  $Q_1$ , i.e., same relative area of emitter-base junction and having equal collector current..

$$I_o = I_{REF}$$



**Fig. 4.1.1.** The basic BJT current mirror.

1. Here  $Q_2$  is in active mode until  $V_o$  is 0.3 V or higher than emitter voltage.
2. For obtaining the current transfer ratio, it is required to consider  $m$  times relative area of emitter-base junction (EBJ).

$$I_o = m I_{REF}$$

The current transfer ratio,

$$\frac{I_o}{I_{REF}} = \frac{I_{s2}}{I_{s1}} = \frac{\text{Area of EBJ of } Q_2}{\text{Area of EBJ of } Q_1}$$

From the node equation at collector of  $Q_1$ ,

$$I_{REF} = I_C + 2I_C/\beta \\ = I_C(1 + 2/\beta)$$

Since,

$$\frac{I_o}{I_{REF}} = \frac{I_C}{I_C(1+2/\beta)} = \frac{1}{1+2/\beta}$$

**Que 4.2.** Discuss the operation and significance of a multiple output transistor mirror.

**Answer**

1. The diode-resistor combination of a simple current source or a current mirror which establishes current  $I_{REF}$ , that is, used to bias multiple amplifier stages. Such a circuit is called a current repeater or a multiple current source or multiple output transistor mirror.
2. The reference current  $I_{REF}$  is supplied by the diode-connected transistor  $Q$  for establishing the emitter-base reference voltage  $V_{EB}$ . The  $V_{EB}$  generated is used for biasing the transistors  $Q_1$  through  $Q_3$ .
3. Different values of  $I_{C1}$ ,  $I_{C2}$ , and  $I_{C3}$  can be obtained by correspondingly scaling the emitter areas of  $Q_1$ ,  $Q_2$  and  $Q_3$ .
4. In Fig. 4.2.1, assuming equal emitter areas, the collector currents of the various transistors are given by  $I_{C1} = I_{C2} = I_{C3} = I_{REF}$ .

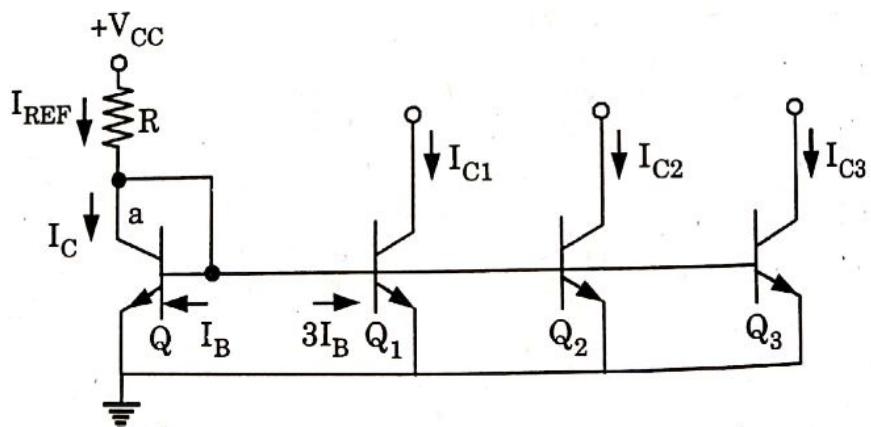


Fig. 4.2.1. Multiple current source.

5. At the collector node  $a$  of transistor  $Q$ ,  $I_{REF} = I_B + I_C + NI_B$  where,  $N$  is the number of multiple current sources.
6. If there are three identical transistors  $Q_1$ ,  $Q_2$  and  $Q_3$ , we have  $N = 3$ . Therefore,

$$I_{REF} = I_C + (1 + 3)I_B = I_C + \left(\frac{1+3}{\beta}\right)I_C$$

7. When  $N$  numbers of such multiple current sources are required, we have

$$I_{REF} = I_C + \left( \frac{1+N}{\beta} \right) I_C = I_C \left( 1 + \left( \frac{1+N}{\beta} \right) \right)$$

Therefore,

$$I_C = I_{REF} \times \frac{\beta}{\beta + N + 1}$$

**Significance :** Multiple copies of  $I_{REF}$  can be generated at different location by simply applying the idea of current mirror to more transistors.

**Que 4.3.** What do you understand by the base current mirror? How does it provide improvement over simple current mirror circuit? Explain with the help of a neat circuit diagram.

AKTU 2015-16, Marks 10

OR

Why we need BJT base current compensation mirror circuit? Draw the circuit and express relation between  $I_{REF}$  and  $I_o$  for same.

AKTU 2016-17, Marks 10

### Answer

1. A bipolar current mirror with a current transfer ratio is less dependent on  $\beta$  than that of simple current mirror.

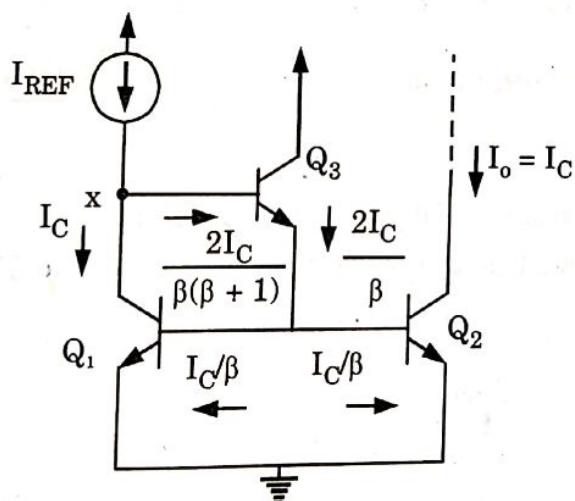


Fig. 4.3.1. A current mirror with base current compensation.

2. This reduces dependency on  $\beta$  and is achieved by using transistor  $Q_3$ . The  $Q_3$  supplies the base current to the  $Q_1$  and  $Q_2$ .
3. The sum of base currents is divided by  $(\beta_3 + 1)$ , resulting in much smaller error current, that has to be supplied by  $I_{REF}$ .
4. Let us assume  $Q_1$  and  $Q_2$  are matched and having equal collector current. A node equation at node  $x$  gives

$$I_{REF} = I_c \left[ 1 + \frac{2}{\beta(\beta+1)} \right]$$

5. As,

The current transfer ratio of the mirror will be

$$\frac{I_o}{I_{REF}} = \frac{2}{1 + \beta(\beta + 1)} \approx \frac{1}{1 + 2/\beta^2}$$

Eq. (4.3.1) shows that the error due to finite  $\beta$  has been reduced from  $2/\beta$  to  $2/\beta^2$ . ...(4.3.1)

6. However, the output resistance ( $r_o$ ) remains approximately equal to that of simple mirror.
7. If  $I_{REF}$  is not present, then we connect node  $x$  to the power supply  $V_{CC}$  through resistor  $R$ , then

$$I_{REF} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R}$$

**Need:**

1. In simple current mirror circuit, a mismatch between  $I_{REF}$  and  $I_o$  caused by the unavoidable presence of base current for the two transistors flowing through  $R$ .
2. With high-gain transistors the difference is small and sometimes negligible, but sometimes it must be recognized and minimized.
3. To reduce the base current flowing through  $R$ , compensation is required. This is done by adding a third transistor as shown in Fig. 4.3.1.

**Que 4.4.** Explain the working of basic MOSFET current source

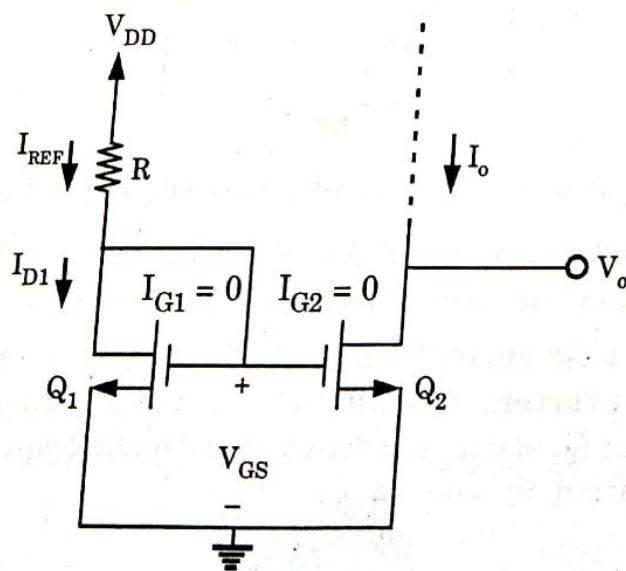
and current steering circuits.

**AKTU 2014-15, Marks 05**

**Answer**

**Working of basic MOSFET current source :**

1. Fig. 4.4.1 shows the basic circuit diagram of MOSFET constant current source.



**Fig. 4.4.1. MOSFET constant current source.**

2. The circuit is driven by the transistor  $Q_1$ .  $Q_1$  is operating in saturation mode as the drain is shorted to its gate. The current equation is given as,

$$I_{D1} = \frac{1}{2} K'_n \left( \frac{W}{L} \right)_1 (V_{GS} - V_t)^2 \quad \dots(4.4.1)$$

3. Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

4. Similarly for  $Q_2$

$$I_o = I_{D2} = \frac{1}{2} K'_n \left( \frac{W}{L} \right)_2 (V_{GS} - V_t)^2 \quad \dots(4.4.2)$$

5. From eq. (4.4.1) and (4.4.2)

$$\frac{I_o}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

6. The connections of  $Q_1$  and  $Q_2$  provides the output current  $I_o$  in relation with  $I_{REF}$  by the aspect ratios of the transistors.

#### Working of current-steering circuit :

1. A constant DC current is generated at one location and then replicated at various other locations for biasing the various amplifier stages through a process known as current steering. Current mirror can be used to implement this current steering function. Fig. 4.4.2 shows the current steering circuit.
2. Here  $Q_1$  together with  $R$  determine the reference current  $I_{REF}$ . Transistors  $Q_1$ ,  $Q_2$ , and  $Q_3$  form a two-output current mirror, ... (4.4.3)

$$I_2 = I_{REF} \frac{(W/L)_2}{(W/L)_1}$$

$$I_3 = I_{REF} \frac{(W/L)_3}{(W/L)_1}$$

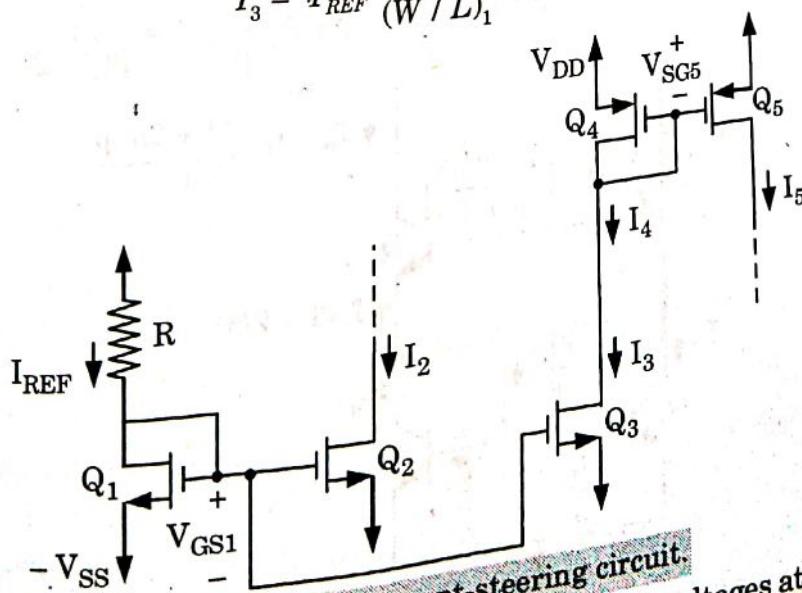


Fig. 4.4.2. A current-steering circuit.

3. To ensure operation in the saturation region, the voltages at the drains of  $Q_2$  and  $Q_3$  are constrained as follows :

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{GS1} - V_{tn}$$

or, equivalently,

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{OV1} \quad \dots(4.4.4)$$

where  $V_{OV1}$  is the overdrive voltage at which  $Q_1$ ,  $Q_2$ , and  $Q_3$  are operating.  $\dots(4.4.5)$

4. The current  $I_3$  is fed to the input side of a current mirror formed by PMOS transistors  $Q_4$  and  $Q_5$ . This mirror provides

$$I_5 = I_4 \frac{(W/L)_5}{(W/L)_4} \quad \dots(4.4.6)$$

where  $I_4 = I_3$ .

5. To keep  $Q_5$  in saturation, its drain voltage should be

$$V_{D5} \leq V_{DD} - |V_{OV5}| \quad \dots(4.4.7)$$

where  $V_{OV5}$  is the overdrive voltage at which  $Q_5$  is operating.

### Que 4.5. Explain Wilson current mirror.

#### Answer

1. Wilson current mirror is the modification of basic bipolar mirror with reduced  $\beta$  dependency and increased output resistance.
2. The analysis to determine the effect of finite  $\beta$  on current transfer ratio is shown in Fig. 4.5.1.

$$\begin{aligned} \frac{I_o}{I_{REF}} &= \frac{I_C \left(1 + \frac{2}{\beta}\right) \frac{\beta}{(\beta+1)}}{I_C \left[1 + \frac{\left(1 + \frac{2}{\beta}\right)}{(\beta+1)}\right]} \\ &= \frac{\beta+2}{\beta+1 + \frac{\beta+2}{\beta}} = \frac{\beta+2}{\beta+2 + \frac{2}{\beta}} = \frac{1}{1 + \frac{2}{\beta(\beta+2)}} \approx \frac{1}{1 + \frac{2}{\beta^2}} \end{aligned}$$

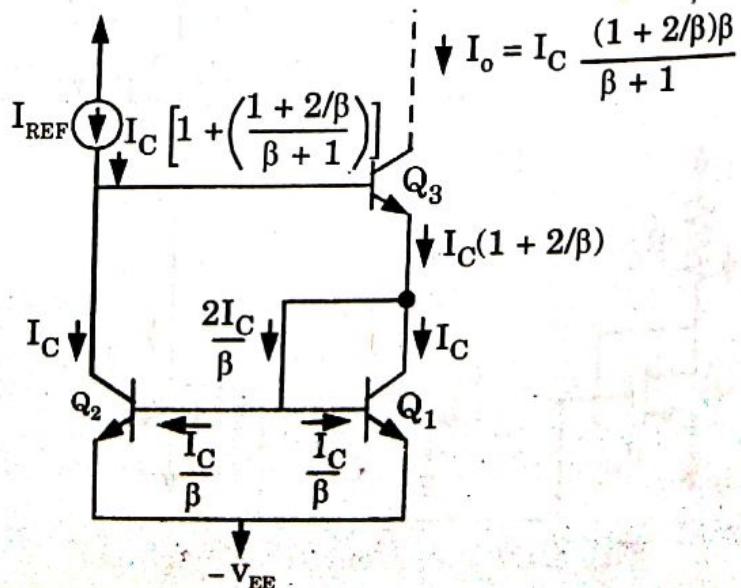
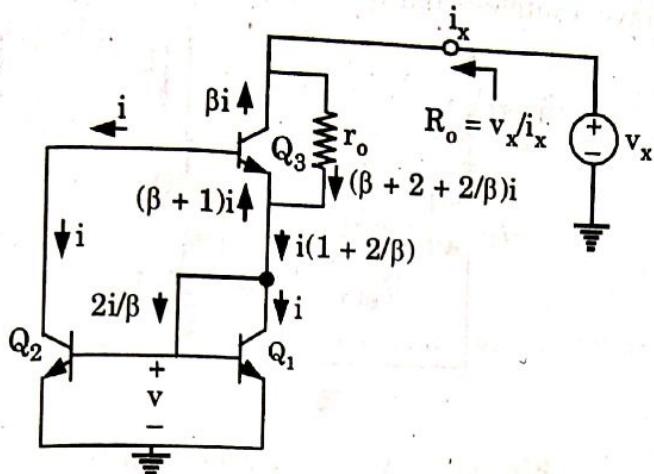


Fig. 4.5.1. Analysis to determine the current transfer ratio.

3. The collector emitter voltage of  $Q_1$  and  $Q_2$  are not equal and introduces a current offset error. Analysis to determine the output resistance of the Wilson mirror is shown in Fig. 4.5.2.



**Fig. 4.5.2. Analysis for output resistance.**

$$i_x = 2i \left(1 + \frac{1}{\beta}\right)$$

$$v = i \left(1 + \frac{1}{\beta}\right) r_e$$

$$v_x = \left(\beta + 2 + \frac{2}{\beta}\right) i r_o + i r_e \left(1 + \frac{1}{\beta}\right)$$

$$R_o = \frac{v_x}{i_x} \approx \frac{\beta r_o}{2}$$

**Que 4.6.** Explain Widlar current source.

**Answer**

- Fig. 4.6.1 shows a Widlar current source which is particularly suitable for low value of currents.
- The circuit differs from the basic current mirror only in the resistance  $R_E$ , that is included in the emitter lead of  $Q_2$ .
- A voltage difference is produced across resistor  $R_E$ , so that  $B-E$  voltage of  $Q_2$  is less than the  $B-E$  voltage of  $Q_1$ .
- A smaller  $B-E$  voltage produces a small collector current, which in turn means that the load current  $I_o$  is less than the reference current  $I_{REF}$ .
- Neglecting base currents,

$$V_{BE1} = V_T \ln \left( \frac{I_{REF}}{I_s} \right) \quad \dots(4.6.1)$$

$$I_o / I_{REF} = \frac{(W/L)_2}{(W/L)_1} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} = \frac{(W/L)_2}{(W/L)_1}$$

Hence, there is no error in the current gain.

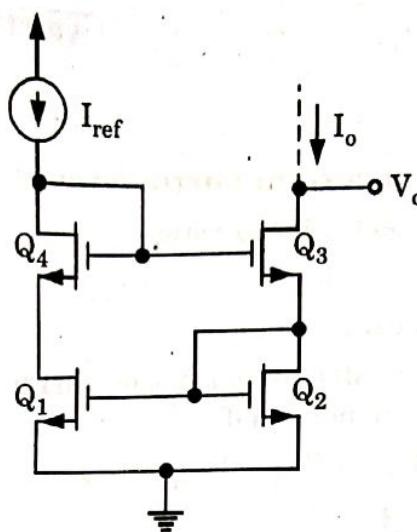


Fig. 4.8.2. Improved Wilson current mirror.

**Que 4.9.** The parameter of the three transistor CM (current mirror) are  $V_{CC} = 9\text{ V}$ ,  $V_{EE} = 0$ ,  $R_1 = 12\text{ k}\Omega$ ,  $V_{BE(ON)} = 0.7\text{ V}$ ,  $\beta = 75$ ,  $V_A = \infty$ . Calculate the value of current  $I_{REF}$ ,  $I_o$ ,  $I_{C1}$ ,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$ ,  $I_{E3}$ .

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**Answer**

Given :  $V_{CC} = 9\text{ V}$ ,  $V_{EE} = 0$ ,  $R_1 = 12\text{ k}\Omega$ ,  $V_{BE(ON)} = 0.7\text{ V}$ ,  $\beta = 75$ ,  $V_A = \infty$ .

To Calculate :  $I_{REF}$ ,  $I_o$ ,  $I_{C1}$ ,  $I_{B1}$ ,  $I_{B2}$ ,  $I_{B3}$ ,  $I_{E3}$ .

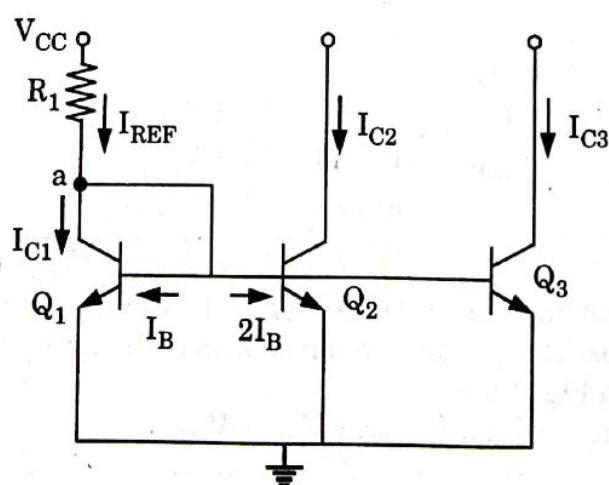


Fig. 4.9.1.

- From Fig. 4.9.1, we can write

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R_1}$$

$$I_{REF} = \frac{9\text{ V} - 0.7\text{ V}}{12\text{ k}\Omega} = 0.691\text{ mA} \quad \dots(4.9.1)$$

Here,  
At node 'a',

$$I_{REF} = I_C + I_B + 2I_B$$

$$I_{REF} = I_C + 3I_B \quad \dots(4.9.2)$$

$$= I_C \left( 1 + \frac{3}{\beta} \right)$$

$$0.691 \times 10^{-3} = I_C \left( 1 + \frac{3}{75} \right)$$

$$I_C = \frac{0.691 \times 10^{-3}}{1.04} = 0.664\text{ mA}$$

$$I_C = I_{C1} = I_{C2} = I_{C3} = 0.664\text{ mA}$$

3. In eq. (4.9.2), substitute the value of  $I_C$ , we get,

$$I_B = \frac{0.691\text{ mA} - 0.664\text{ mA}}{3} = 0.009\text{ mA}$$

$$I_E = I_B + I_C = 0.009 + 0.664 = 0.673\text{ mA}$$

$$I_{E1} = I_{E2} = I_{E3} = I_E$$

**Que 4.10.** Determine  $I_{C1}, I_{C2}, I_{C3}$  for the circuit shown in Fig. 4.10.1.

Assume  $\beta = 125$ .

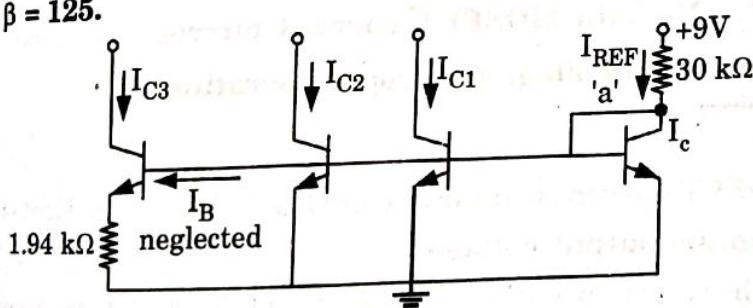


Fig. 4.10.1.

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**Answer**

1. We know,

$$I_{REF} = \frac{9\text{ V} - 0.7\text{ V}}{30\text{ k}\Omega} = 0.277\text{ mA}$$

2. Also at node 'a'

$$I_{REF} = I_C + 3I_B \quad (\text{Assume } I_{B3} \text{ of Widlar source negligible})$$

$$= I_C \left( 1 + \frac{3}{\beta} \right)$$

$$I_C = I_{REF} \left( \frac{\beta}{3 + \beta} \right)$$

Putting the values of  $\beta$  and  $I_{REF}$  and solving, we get

$$I_C = I_{C1} = I_{C2} = 0.271 \text{ mA}$$

3. Calculate  $I_{C3}$ , using equation

$$\left( \frac{1}{\beta} + 1 \right) I_{C3} R_E = V_T \ln \left( \frac{I_{C1}}{I_{C3}} \right)$$

$$1.94 = \frac{0.025}{I_{C3} \left( 1 + \frac{1}{125} \right)} \ln \frac{0.271}{I_{C3}} \quad \dots(4.10.1)$$

After solving the eq. (4.10.1) we obtain

$$I_{C3} = 0.0287 \text{ mA}$$

## PART-2

*V-I Characteristics, Output Resistance and Minimum Sustainable Voltage (V<sub>ON</sub>), Maximum Usable Load.*

### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 4.11.** Explain MOSFET current mirror and also find the minimum output voltage for proper operation.

#### Answer

**MOSFET current mirror :** Refer Q. 4.4, Page 4–5E, Unit-4.

**Minimum output voltage :**

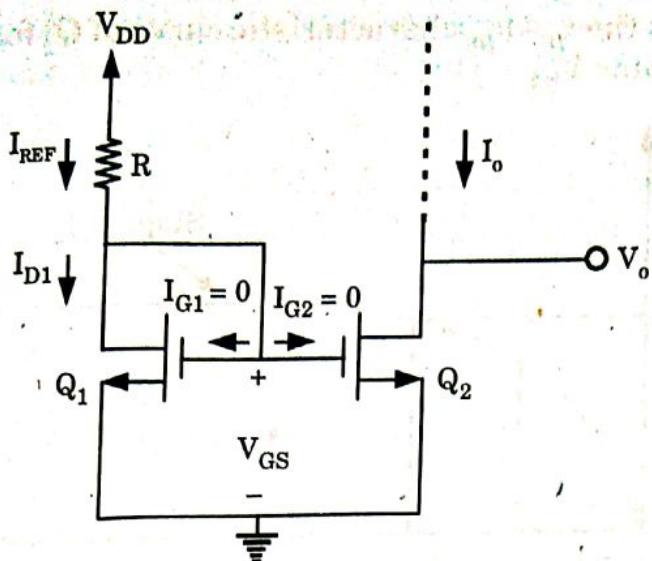
- For the operation of the current source of Fig. 4.11.1, we assumed  $Q_2$  to be operating in saturation.
- This is essential if  $Q_2$  is to supply a constant-current output.
- To ensure that  $Q_2$  is saturated, the circuit to which the drain of  $Q_2$  is to be connected must establish a drain voltage  $V_o$  that satisfied the relationship

$$V_o \geq V_{GS} - V_t$$

- Equivalently in terms of the overdrive voltage  $V_{ov}$  of  $Q_1$  and  $Q_2$ ,

$$V_o \geq V_{ov}$$

- In other words, the current source will operate properly with an output voltage  $V_o$  as low as  $V_{ov}$ , which is a few tenth of a volt.

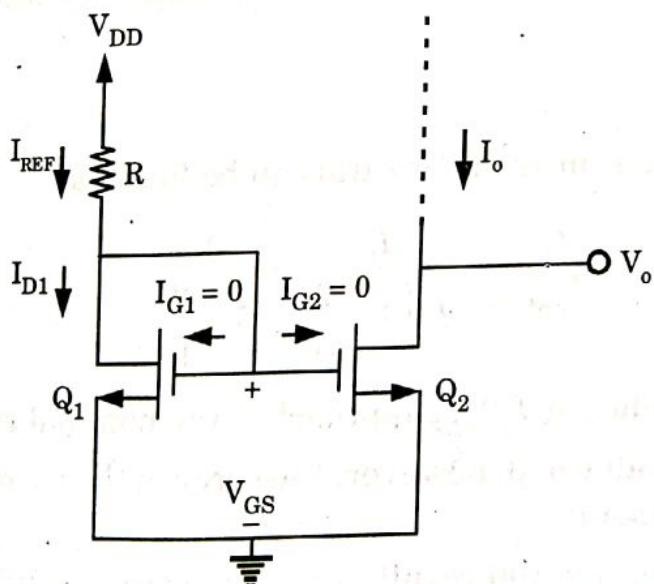


**Fig. 4.11.1.** MOSFET constant current source.

**Que 4.12.** Describe the effect of output voltage ( $V_o$ ) on output current ( $I_o$ ) of MOS current mirror and also find the output resistance.

**Answer**

1. Channel-length modulation can have a significant effect on the operation of the current source.
2. Consider, for simplicity, the case of identical devices  $Q_1$  and  $Q_2$ .



**Fig. 4.12.1.** MOSFET constant current source.

3. The drain current of  $Q_2$ ,  $I_o$ , will equal the current in  $Q_1$ ,  $I_{REF}$ , at the value of  $V_o$  that causes the two devices to have the same  $V_{DS}$ , that is, at  $V_o = V_{GS}$ .
4. As  $V_o$  is increased above this value,  $I_o$  will increase according to the incremental output resistance  $r_{o2}$  of  $Q_2$ .

5. Fig. 4.12.1 is the  $i_D - v_{DS}$  characteristic curve of  $Q_2$  for  $v_{GS}$  equal to the particular value  $V_{GS}$ .

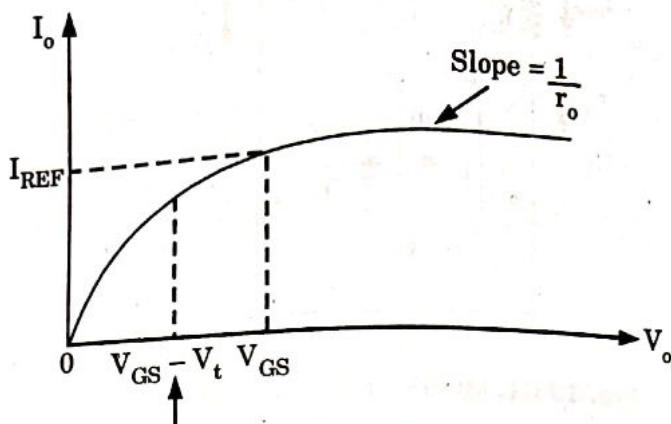


Fig. 4.12.1. Output characteristic of the current source.

6. A finite output resistance  $r_o$ ,

$$r_o = \frac{\Delta V_o}{\Delta I_o} = r_{o2} = \frac{V_{A2}}{I_o} \quad \dots(4.12.1)$$

where  $I_o$  is saturation current and  $V_{A2}$  is the Early voltage of  $Q_2$ .

**Que 4.13.** What is the effect of  $\beta$  and output resistance ( $r_o$ ) on the BJT current mirror? Also find the output resistance ( $r_o$ ) of the current mirror.

**Answer**

1.  $I_o = I_C$ , the current transfer ratio can be found as

$$\frac{I_o}{I_{REF}} = \frac{I_C}{I_C \left(1 + \frac{2}{\beta}\right)} = \frac{1}{1 + \frac{2}{\beta}} \quad \dots(4.13.1)$$

As  $\beta$  approaches  $\infty$ ,  $I_o/I_{REF}$  approaches the nominal value of unity.

2. For typical value of  $\beta$ , however, the error in the current transfer ratio can be significant.
3. For instance,  $\beta = 100$  results in a 2 % error in the current transfer ratio.
4. The BJT mirror has a finite output resistance  $r_o$ ,

$$r_o \equiv \frac{\Delta V_o}{\Delta I_o} = r_{o2} = \frac{V_{A2}}{I_o} \quad \dots(4.13.2)$$

where  $V_{A2}$  and  $r_{o2}$  are the Early voltage and the output resistance, respectively, of  $Q_2$ .

5. Taking both the finite  $\beta$  and the finite  $R_o$  into account, we can express the output current of a BJT mirror with a nominal current transfer ratio  $m$  as

$$I_o = I_{REF} \left( \frac{m}{1 + \frac{m+1}{\beta}} \right) \left( 1 + \frac{V_o - V_{BE}}{V_{A2}} \right) \quad \dots(4.13.3)$$

### PART-3

*Differential Amplifier : Basic Structure and Principle of Operation.*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

- Que 4.14.** Draw and explain basic structure of BJT differential amplifier.

#### Answer

1. The differential amplifier circuit has two separate inputs and two separate outputs and that the emitters are connected together.
2. It also consists of two separate voltage supplies.

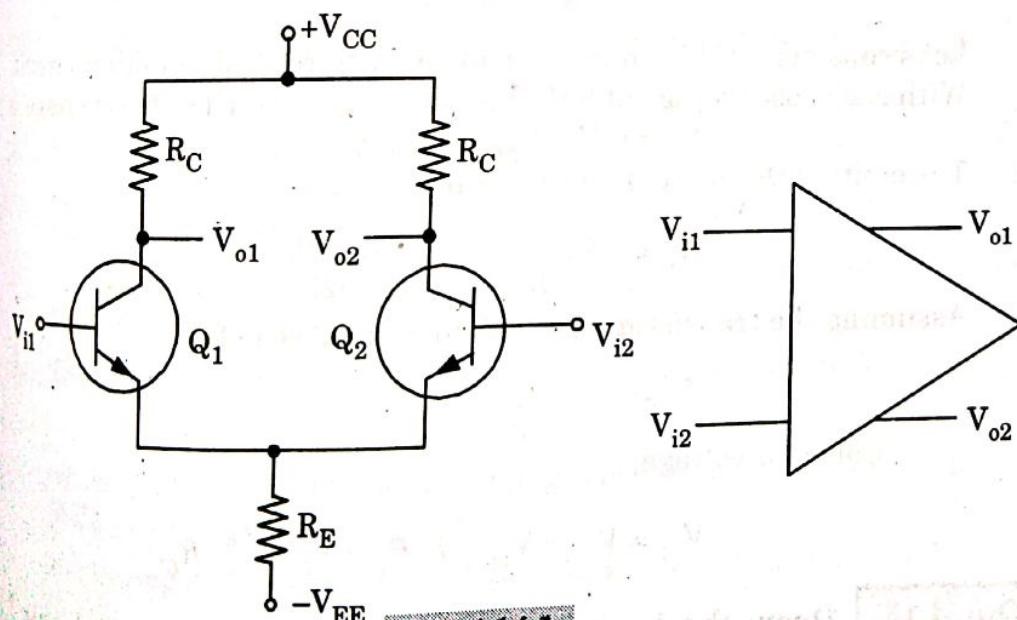


Fig. 4.14.1.

3. In differential amplifier circuit, the input signal operates both transistors in single-ended operation due to the common emitter connection, resulting in output from both collectors.

4. In double-ended operation, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.
5. In common-mode operation the common input signal results in opposite signals at each collector, these signals cancel each other so that the resulting output signal is zero.
6. The main feature of the differential amplifier is the very large gain when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs.

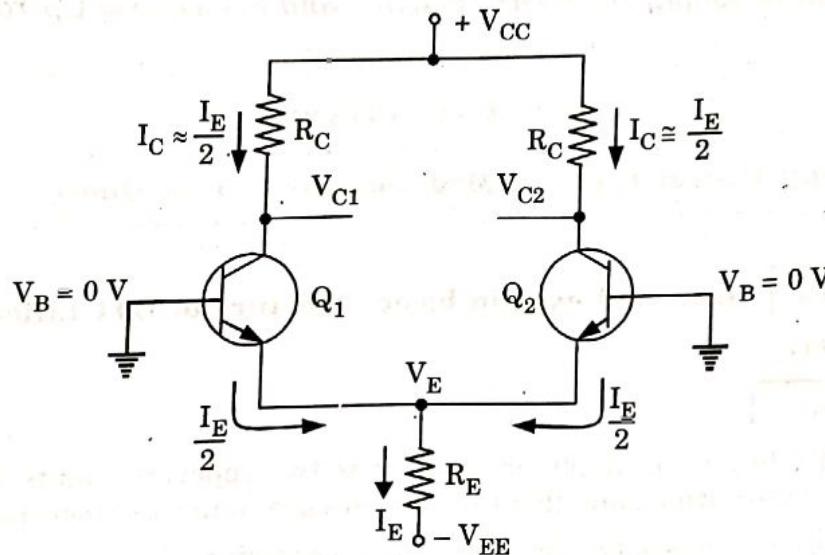


Fig. 4.14.2.

7. Let's consider DC bias operation of the differential amplifier circuit. With each base voltage at 0 V, the common emitter DC bias voltage is  

$$V_E = 0 \text{ V} - V_{BE} = -0.7 \text{ V}$$
8. The emitter DC bias current is then,

$$I_E = \frac{V_E - (-V_{EE})}{R_E} \approx \frac{V_{EE} - 0.7 \text{ V}}{R_E}$$

9. Assuming the transistors are well matched, we get

$$I_{C1} = I_{C2} = \frac{I_E}{2}$$

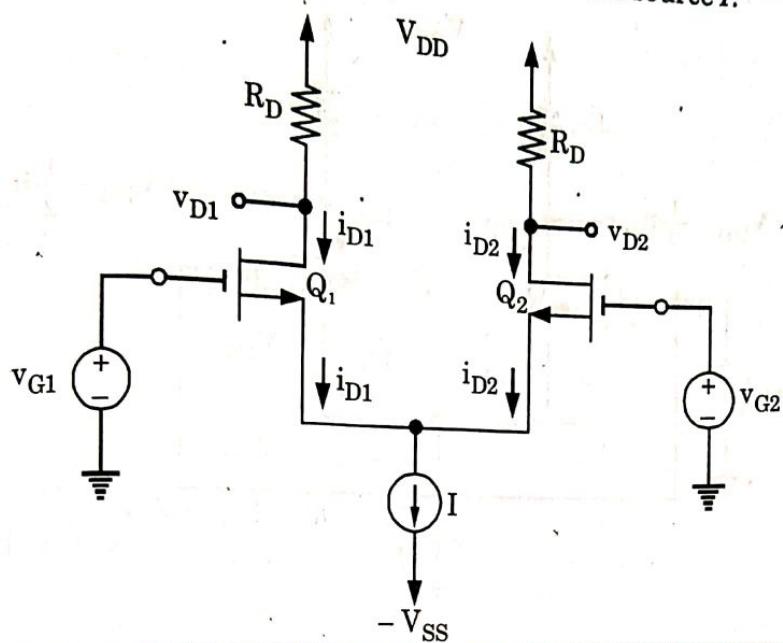
$\therefore$  Collector voltage,

$$V_{C1} = V_{C2} = V_{CC} - I_C R_C = V_C - \frac{I_E}{2} R_C$$

**Que 4.15.** Draw the basic structure of MOS differential pair ?  
 Explain their operation with common-mode input voltage.

**Answer****The MOS differential pair:**

- Fig. 4.15.1 shows the basic MOS differential-pair configuration.
- It consists of two matched transistor,  $Q_1$  and  $Q_2$ , whose sources are joined together and biased by a constant-current source  $I$ .

**Fig. 4.15.1. The Basic MOS differential-pair configuration.**

- Each drain is connected to the positive supply through a resistance  $R_D$ .

**Operation with a common-mode input voltage :**

- Consider a case of the two gate terminals joined together and connected to a voltage  $v_{CM}$ , called the common-mode voltage, as shown in Fig. 4.15.2, where  $v_{G1} = v_{G2} = v_{CM}$ .
- Since  $Q_1$  and  $Q_2$  are matched, it follows from symmetry that the current  $I$  will divide equally between the two transistors.
- Thus,  $i_{D1} = i_{D2} = I/2$ , and the voltage at the source  $v_S$ , will be

$$v_S = v_{CM} - V_{GS}$$

where  $V_{GS}$  is the gate-to-source voltage corresponding to a drain current of  $I/2$ .

- Neglecting channel-length modulation,  $V_{GS}$  and  $I/2$  are related by

$$\frac{I}{2} = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2$$

or in terms of the overdrive voltage  $V_{OV}$

$$V_{OV} = V_{GS} - V_t$$

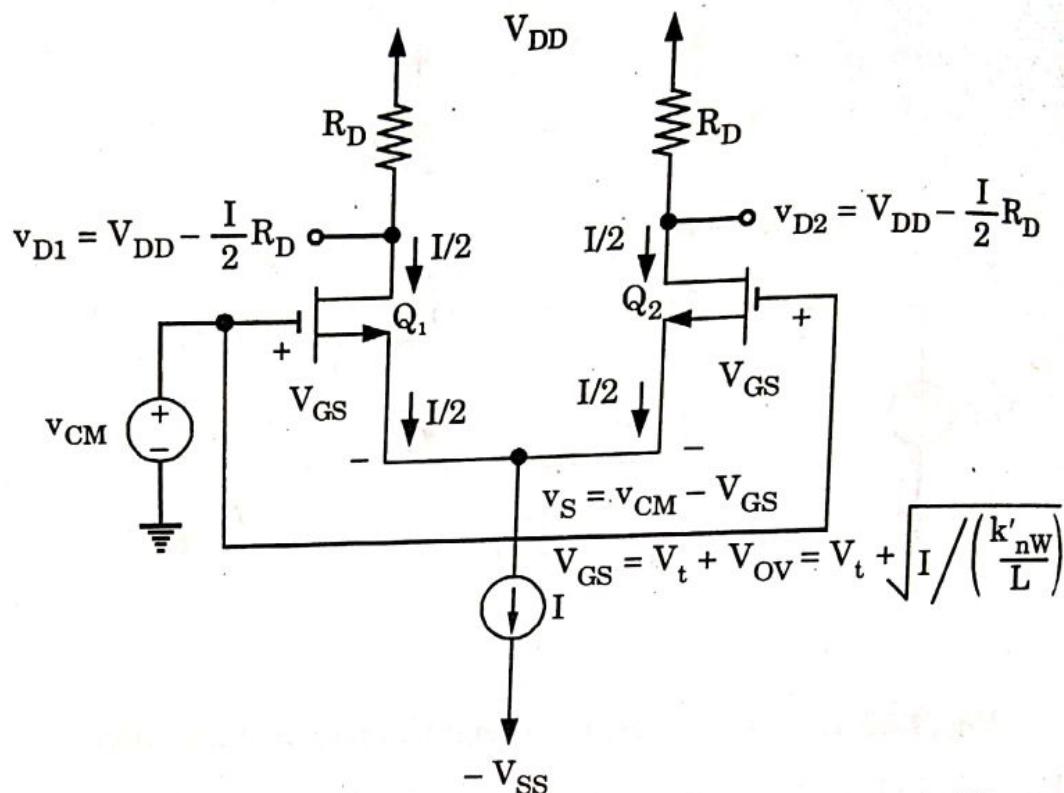
$$\frac{I}{2} = \frac{1}{2} k'_n \frac{W}{L} V_{OV}^2$$

$$V_{ov} = \sqrt{I / k'_n (W / L)}$$

5. The voltage at each drain will be,

$$v_{D1} = v_{D2} = V_{DD} - \frac{I}{2} R_D$$

6. Thus, the difference in voltage between the two drains will be zero.



**Fig. 4.15.2.** The MOS differential-pair with a common-mode input voltage  $v_{CM}$ .

7. Now, let us vary the value of the common-mode voltage  $v_{CM}$ .
8. As long as  $Q_1$  and  $Q_2$  remain in the saturation region, the current  $I$  will divide equally between  $Q_1$  and  $Q_2$  and the voltages at the drains will not change.
9. Thus, the differential pair does not respond to (*i.e.*, it rejects) common-mode input signals.

**Que 4.16.** Explain the operation of MOS differential pair when differential input voltage is applied.

**Answer**

1. We apply a difference or differential input voltage by grounding the gate of  $Q_2$  (*i.e.*, setting  $v_{G2} = 0$ ) and applying a signal  $v_{id}$  to the gate of  $Q_1$ , as shown in Fig. 4.16.1.

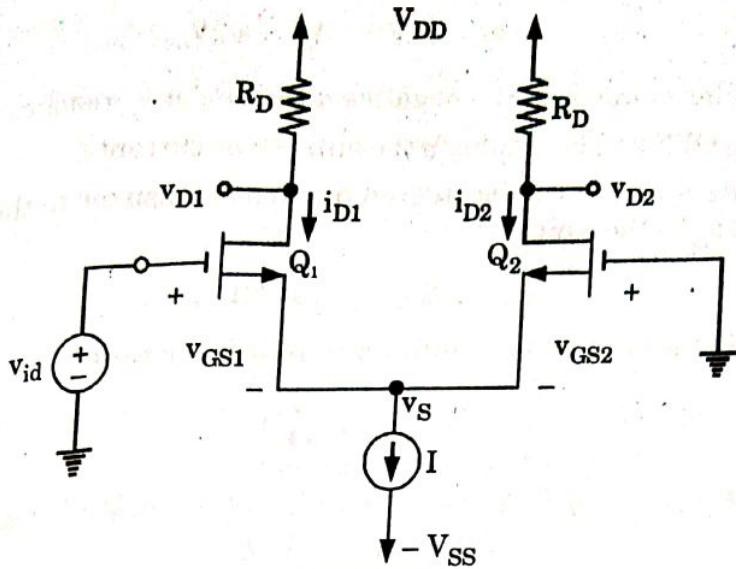


Fig. 4.16.1.

2. Since  $v_{id} = v_{GS1} - v_{GS2}$ , if  $v_{id}$  is positive,  $v_{GS1}$  will be greater than  $v_{GS2}$  and hence,  $i_{D1}$  will be greater than  $i_{D2}$  and the difference output voltage  $(v_{D2} - v_{D1})$  will be positive.
3. When  $v_{id}$  is negative,  $v_{GS1}$  will be lower than  $v_{GS2}$ ,  $i_{D1}$  will be smaller than  $i_{D2}$ , and correspondingly  $v_{D1}$  will be higher than  $v_{D2}$ . In other words, the difference or differential output voltage  $(v_{D2} - v_{D1})$  will be negative.
4. The differential pair responds to difference-mode or differential input signals by providing a corresponding differential output signal between the two drains.
5. It is useful to inquire about the value of  $v_{id}$  that causes the entire bias current  $I$  to flow in any one of the two transistors.
6. In the positive direction,  $v_{GS1}$  reaches the value that corresponds to  $i_{D1} = I$ , and  $v_{GS2}$  is reduced to a value equal to the threshold voltage  $V_t$ , at which point  $v_s = -V_t$ .
7. The value of  $v_{GS1}$  can be found from

$$I = \frac{1}{2} \left( k' \frac{W}{L} \right) (v_{GS1} - V_t)^2$$

as

$$v_{GS1} = V_t + \sqrt{2I/k'_n(W/L)}$$

$$= V_t + \sqrt{2}V_{ov}$$

where  $V_{ov}$  is the overdrive voltage corresponding to a drain current of  $I/2$ .

8. Thus, the value of  $v_{id}$  at which the entire bias current  $I$  is steered into  $Q_1$  is

$$v_{id\max} = v_{GS1} + v_s$$

9. In a similar manner, in the negative direction, as  $v_{id}$  reaches  $-\sqrt{2}V_{ov}$ ,  $Q_1$  turns OFF and  $Q_2$  conducts the entire bias current  $I$ .
10. Thus, the current  $I$  can be steered from one transistor to the other by varying  $v_{id}$  in the range  $-\sqrt{2}V_{ov} \leq v_{id} \leq \sqrt{2}V_{ov}$ , which defines the range of differential-mode operation.

#### PART-4

*Calculation of Differential Gain, Common Mode Gain, CMRR and ICMR.*

#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 4.17.** Write short note on input common mode range (ICMR) of MOS differential amplifier.

#### Answer

1. ICMR is the range of  $V_{CM}$  over which the differential pair operates properly.
2. The highest value of  $V_{CM}$  is limited by the requirement that  $Q_1$  and  $Q_2$  remain in saturation, thus

$$V_{CM\max} = V_t + V_{DD} - \frac{I}{2} R_D \quad \dots(4.17.1)$$

3. The lowest value of  $v_{CM}$  is determined by the need to allow for a sufficient voltage across current source  $I$  for it to operate properly.
4. If a voltage  $V_{CS}$  is needed across the current source, then

$$V_{CM\min} = -V_{SS} + V_{CS} + V_t + V_{ov} \quad \dots(4.17.2)$$

**Que 4.18.** Find the differential gain of the MOS differential amplifier.

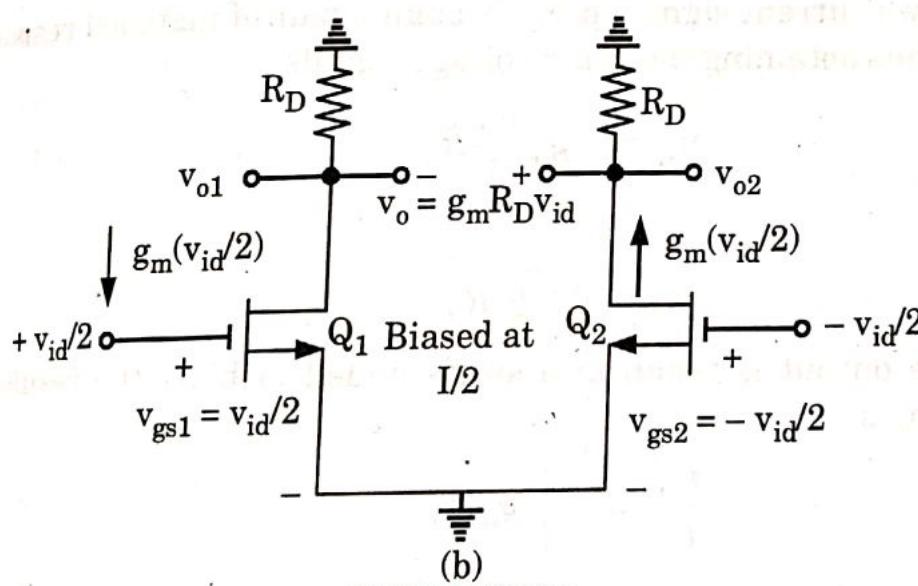
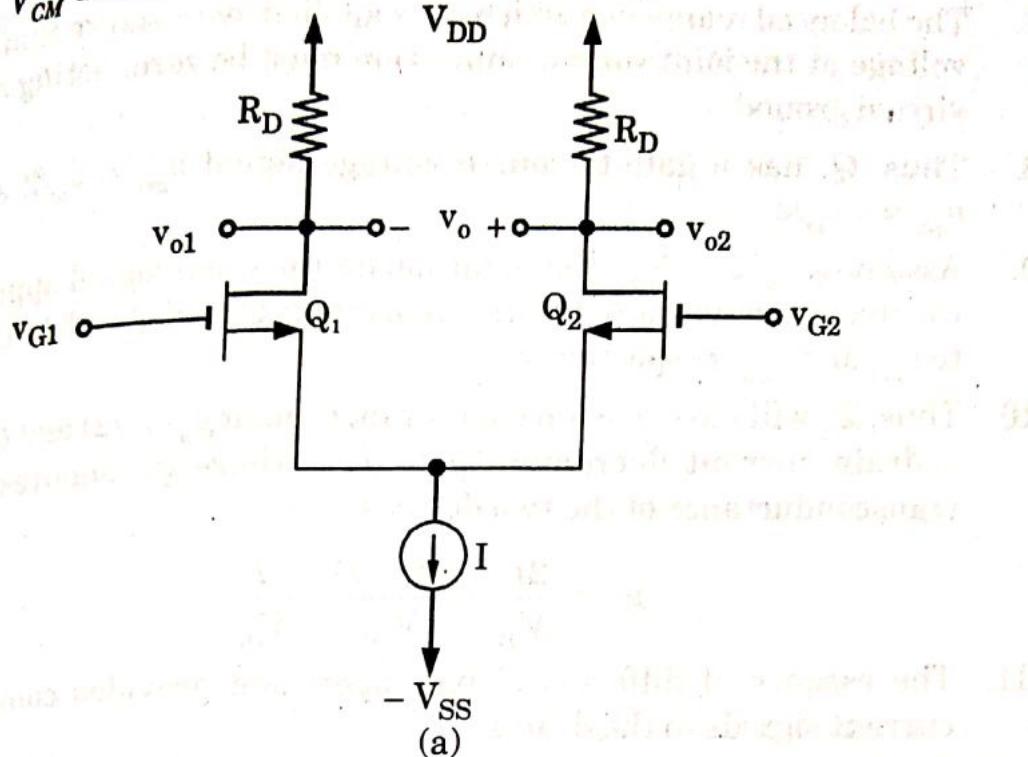
#### Answer

1. Fig. 4.18.1(a) shows the MOS differential amplifier with input voltages

$$v_{G1} = V_{CM} + \frac{1}{2} v_{id}$$

and

Here,  $V_{CM}$  denotes a common-mode DC voltage



**Fig. 4.18.1.**

2. The differential input signal  $v_{id}$  is applied in a complementary (or balanced) manner; that is,  $v_{G1}$  is increased by  $v_{id}/2$  and  $v_{G2}$  is decreased by  $v_{id}/2$ .
  3. As indicated in Fig. 4.18.1(a) the amplifier output can be taken either between one of the drains and ground or between the two drains.  
Now analyze the small-signal operation of the differential amplifier of Fig. 4.18.1(a) to determine its voltage gain in response to the differential input signal  $v_{id}$ .
- In Fig. 4.18.1(b), the power supplies grounded, the bias current sources removed, and  $V_{CM}$  eliminated.

6. We will neglect the effect of the MOSFET  $r_o$ , and the body effect. Each of  $Q_1$  and  $Q_2$  is biased at a DC current of  $I/2$  and is operating at an overdrive voltage  $V_{ov}$ .
7. The balanced manner in which  $v_{id}$  is applied, we observe that the signal voltage at the joint source connection must be zero, acting as a sort of virtual ground.
8. Thus,  $Q_1$  has a gate-to-source voltage signal  $v_{gs1} = v_{id}/2$  and  $Q_2$  has  $v_{gs2} = -v_{id}/2$ .
9. Assuming  $v_{id}/2 \ll V_{ov}$ , the condition for the small-signal approximation, the changes resulting in the drain current of  $Q_1$  and  $Q_2$  will be proportional to  $v_{gs1}$  and  $v_{gs2}$ , respectively.
10. Thus,  $Q_1$  will have a drain current increment  $g_m(v_{id}/2)$  and  $Q_2$  will have a drain current decrement  $g_m(v_{id}/2)$ , where  $g_m$  denotes the equal transconductance of the two devices.

$$g_m = \frac{2I_D}{V_{ov}} = \frac{2(I/2)}{V_{ov}} = \frac{I}{V_{ov}}$$

11. The essence of differential pair operation provides complementary current signals in the drains.
12. The two current signals pass through a pair of matched resistors,  $R_D$ , and thus obtaining the drain voltage signals.

$$v_{o1} = -g_m \frac{v_{id}}{2} R_D$$

and

$$v_{o2} = g_m \frac{v_{id}}{2} R_D$$

13. If the output is taken in a single ended fashion, the resulting gain becomes

$$\frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_D$$

$$\frac{v_{o2}}{v_{id}} = \frac{1}{2} g_m R_D$$

14. Alternatively, if the output is taken differentially the gain becomes

$$A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

**Que 4.19.** Determine the common mode gain and common mode rejection ratio which arise due to mismatch in drain terminal resistance ( $R_D$ ).

Answer

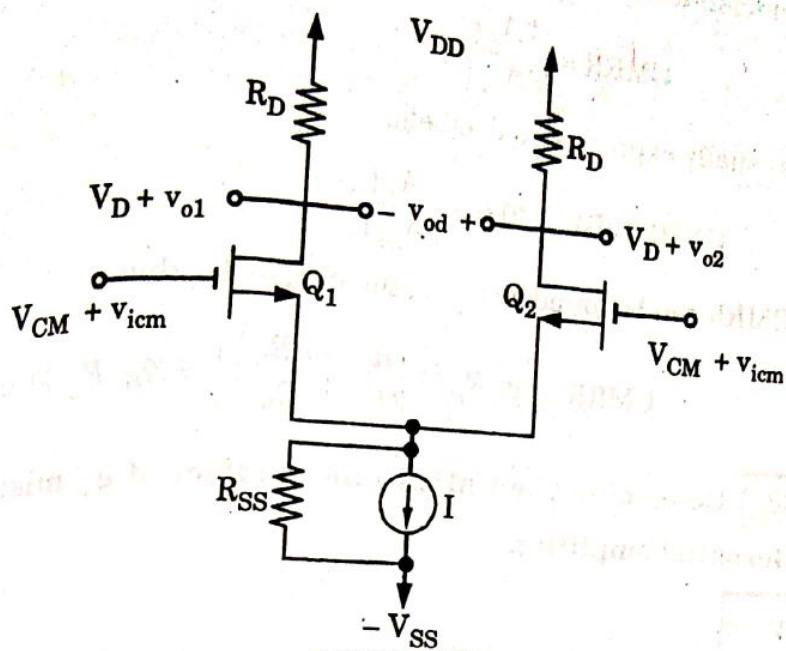


Fig. 4.19.1.

- When the two drain resistances exhibit a mismatch  $\Delta R_D$ , the common-mode voltages at the two drains will no longer be equal.
- Rather, if the load of  $Q_1$  is  $R_D$  and that of  $Q_2$  is  $(R_D + \Delta R_D)$ , the drain signal voltages arising from  $v_{icm}$  will be

$$v_{o1} = -\frac{R_D}{2R_{SS}} v_{icm}$$

and

$$v_{o2} = -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm}$$

- Thus,

$$v_{od} = v_{o2} - v_{o1} = -\frac{\Delta R_D}{2R_{SS}} v_{icm}$$

and we can find the common-mode gain  $A_{cm}$  as

$$A_{cm} = \frac{v_{od}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}}$$

which can be expressed in the alternate form

$$A_{cm} = -\left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right)$$

- It follows that a mismatch in the drain resistance causes the differential amplifier to have a finite common-mode gain.
- A measure of the effectiveness of the differential amplifier in amplifying differential-mode signals and rejecting common-mode interference is the ratio of the magnitude of its differential gain  $|A_d|$  to the magnitude of its common-mode gain  $|A_{cm}|$ .

6. The common-mode rejection ratio (CMRR) is,

$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|}$$

and is usually expressed in decibels,

$$\text{CMRR (dB)} = 20 \log \frac{|A_d|}{|A_{cm}|}$$

7. The CMRR can be found as the ratio of  $A_d$  to  $A_{cm}$  thus

$$\text{CMRR} = g_m R_D \left[ \frac{R_D}{2R_{SS}} \left( \frac{\Delta R_D}{R_D} \right) \right] = (2g_m R_{SS}) / (\Delta R_D / R_D)$$

**Que 4.20.** Determine the CMRR due to effect of  $g_m$  mismatch in MOS differential amplifier.

**Answer**

1. For the purpose of finding the effect of a  $g_m$  mismatch on CMRR, let

$$g_{m1} = g_m + \frac{1}{2} \Delta g_m \quad \dots(4.20.1)$$

$$g_{m2} = g_m - \frac{1}{2} \Delta g_m \quad \dots(4.20.2)$$

Solving eq. (4.20.1) and eq. (4.20.2) then we get,

$$g_{m1} - g_{m2} = \Delta g_m \quad \dots(4.20.3)$$

2. The equivalent circuit is shown in Fig. 4.20.1, shows that the voltages between gate and source for the two transistors are equal (and equal to  $v_{icm} - v_s$ ). Thus,

$$i_1 (1/g_{m1}) = i_2 (1/g_{m2}) \quad \dots(4.20.4)$$

$$\text{Now } i_1 + i_2 = i_1 \left( 1 + \frac{g_{m2}}{g_{m1}} \right) \quad \dots(4.20.5)$$

3. Now the voltage between the gate of  $Q_1$  and ground which is equal to  $v_{icm}$  can be expressed as

$$v_{icm} = i_1/g_{m1} + (i_1 + i_2)R_{SS}$$

$$= i_1 / g_{m1} + i_1 \left( 1 + \frac{g_{m2}}{g_{m1}} \right) R_{SS}$$

which can be rearranged to obtain  $i_1$  in terms of  $v_{icm}$  as

$$i_1 = \frac{g_{m1} v_{icm}}{1 + (g_{m1} + g_{m2}) R_{SS}} \quad \dots(4.20.6)$$

4. We can then use eq. (4.20.4) together with eq. (4.20.6) to express  $i_2$  as

$$i_2 = \frac{g_{m2} v_{icm}}{1 + (g_{m1} + g_{m2}) R_{SS}} \quad \dots(4.20.7)$$

6. The voltages  $v_{o1}$  and  $v_{o2}$  can be obtained as,

$$v_{o1} = -i_1 R_D = -\frac{g_{m1} R_D}{1 + (g_{m1} + g_{m2}) R_{SS}} v_{icm} \quad \dots(4.20.8)$$

$$v_{o2} = -i_2 R_D = -\frac{g_{m2} R_D}{1 + (g_{m1} + g_{m2}) R_{SS}} v_{icm} \quad \dots(4.20.9)$$

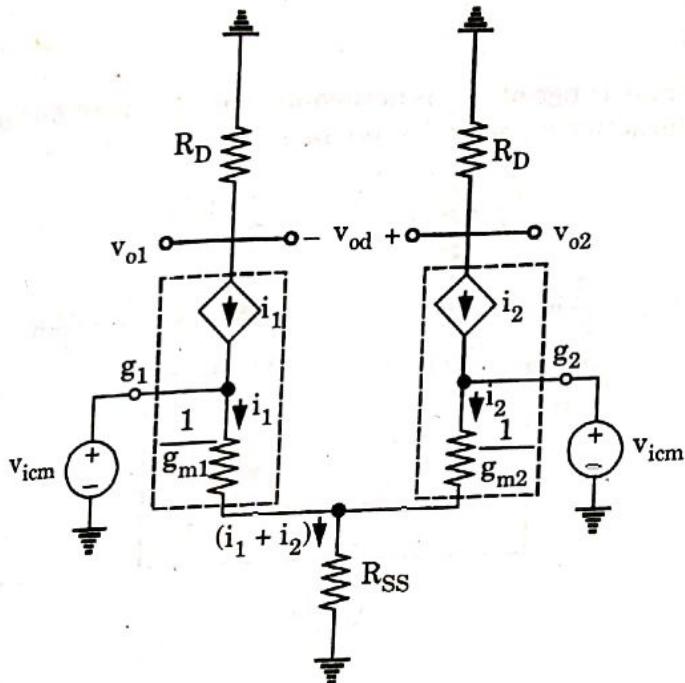


Fig. 4.20.1.

6. The differential output voltage  $v_{od}$  is obtained as,

$$v_{od} = v_{o2} - v_{o1} = \frac{(g_{m1} - g_{m2}) R_D}{1 + (g_{m1} + g_{m2}) R_{SS}} v_{icm} \quad \dots(4.20.10)$$

substituting for  $g_{m1}$  and  $g_{m2}$  from eq. (4.20.1) and eq. (4.20.2), respectively, gives

$$v_{od} = \frac{\Delta g_m R_D}{1 + 2g_m R_{SS}} v_{icm} \quad \dots(4.20.11)$$

7. Thus the common-mode gain resulting from a mismatch  $\Delta g_m$  can be expressed as

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = \frac{\Delta g_m R_D}{1 + 2g_m R_{SS}} v_{icm} \quad \dots(4.20.12)$$

which can be approximated by

$$A_{cm} \approx \left( \frac{R_D}{2R_{SS}} \right) \left( \frac{\Delta g_m}{g_m} \right) \quad \dots(4.20.13)$$

8. And the corresponding CMRR will be

$$\text{CMRR} = g_m R_D \left/ \left[ \frac{R_D}{2R_{SS}} \left( \frac{\Delta g_m}{g_m} \right) \right] \right. = (2g_m R_{SS}) \left/ \left( \frac{\Delta g_m}{g_m} \right) \right. \quad \dots(4.20.14)$$

**Que 4.21.** What is input common-mode range (ICMR) of BJT differential amplifier?

**Answer**

1. The allowable range of  $V_{CM}$  is determined at the upper end by  $Q_1$  and  $Q_2$  leaving the active mode and entering saturation.

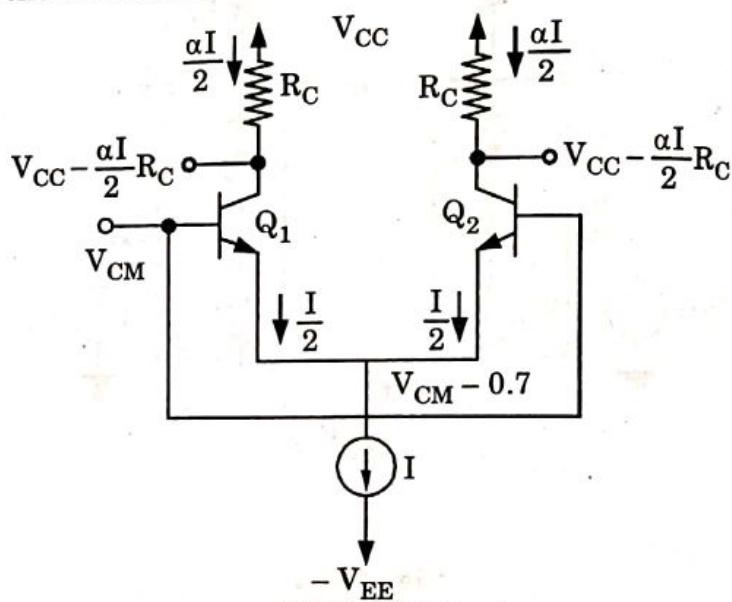


Fig. 4.21.1.

2. Thus,  $V_{CM\max} = V_C + 0.4 = V_{CC} - \alpha \frac{I}{2} R_C + 0.4$
3. The lower end of the  $V_{CM}$  range is determined by the need to provide a certain minimum voltage  $V_{CS}$  across the current source  $I$  to ensure its proper operation.
4. Thus,  $V_{CM\min} = -V_{EE} + V_{CS} + V_{BE}$

**Que 4.22.** Draw the circuit diagram of BJT differential amplifier when small differential input signal  $v_{id}$  is applied. Also find the differential gain.

**Answer**

1. Fig. 4.22.1 shows the BJT differential pair with a difference voltage signal  $v_{id}$  applied between the two bases.

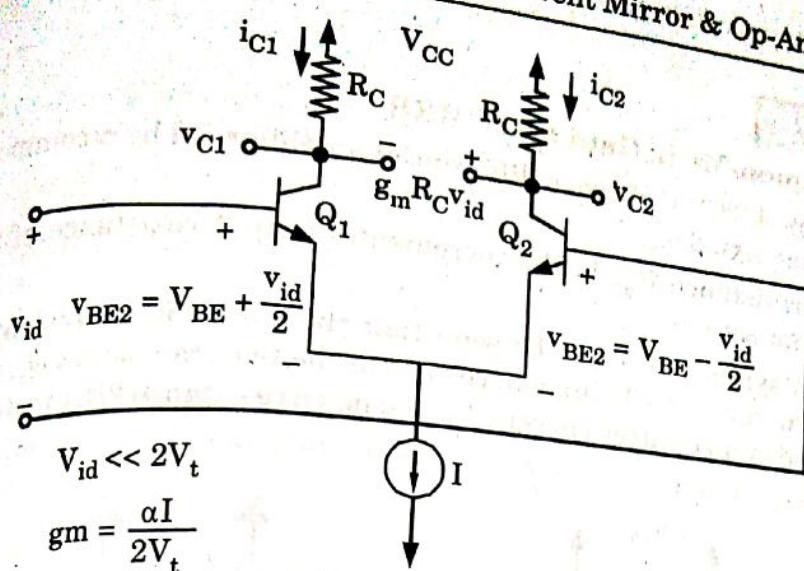


Fig. 4.22.1.

**Differential voltage gain :**

1 For small difference input voltage the collector currents are given by

$$i_{C1} = I_c + g_m (v_{id}/2)$$

$$i_{C2} = I_c - g_m (v_{id}/2)$$

where,

$$I_c = \alpha I / 2$$

2 Thus the total voltages at the collectors will be

$$v_{C1} = (V_{cc} - I_c R_C) - g_m R_C (v_{id}/2)$$

$$v_{C2} = (V_{cc} - I_c R_C) + g_m R_C (v_{id}/2)$$

3 The quantities in parentheses are simply the DC voltage at each of the two collectors.

4 The differential gain of the differential amplifier will be,

$$A_d = \frac{v_{c1} - v_{c2}}{v_{id}} = -g_m R_C$$

i On the other hand, if we take the output single-ended (between the collector of  $Q_1$  and ground), then the differential gain will be given by,

$$A_d = \frac{v_{c1}}{v_{id}} = -\frac{1}{2} g_m R_C$$

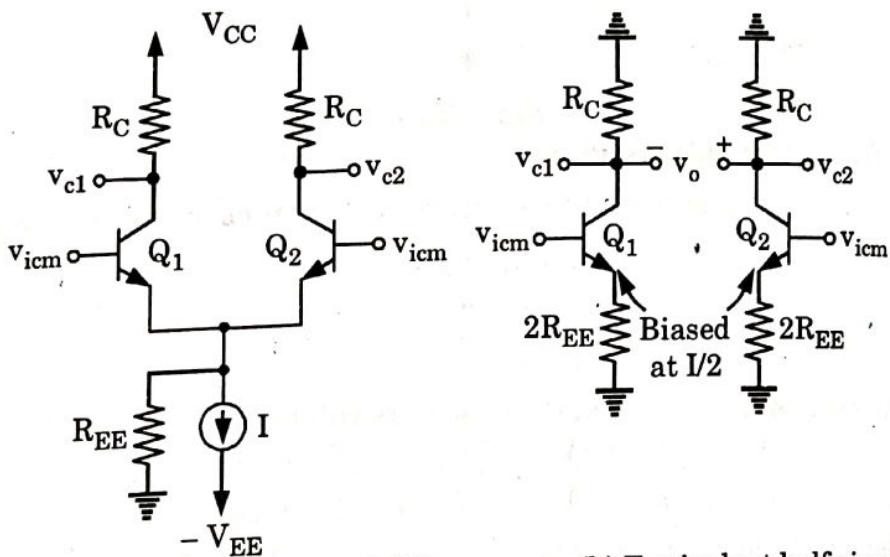
For the differential amplifier with resistances in the emitter leads the differential gain with the output is taken differentially is given by,

$$A_d = -\frac{\alpha(2R_C)}{2r_e + 2R_e} \approx -\frac{R_C}{r_e + R_e}$$

Q. 423. Write in detail about the common-mode gain and CMRR of the BJT differential amplifier. Elaborate the effect of mismatch in the collector resistance.

**Answer****Common-Mode Gain and CMRR :**

- Figure 4.23.1(a) shows a differential amplifier fed by a common-mode voltage signal  $v_{icm}$ .
- The resistance  $R_{EE}$  is the incremental output resistance of the bias current source.
- From symmetry it can be seen that the circuit is equivalent to that shown in Fig. 4.23.1(b), where each of the two transistors  $Q_1$  and  $Q_2$  is biased at an emitter current  $I/2$  and has a resistance  $2R_{EE}$  in its emitter lead.

(a) The differential amplifier fed by a common-mode voltage signal  $v_{icm}$ .

(b) Equivalent half-circuits for common-mode calculations.

**Fig. 4.23.1.**

- Thus, the common-mode output voltage  $v_{c1}$  will be

$$v_{c1} = -v_{icm} \frac{\alpha R_C}{2R_{EE} + r_e} = -v_{icm} \frac{\alpha R_C}{2R_{EE}} \quad \dots(4.23.1)$$

- At the other collector we have an equal common-mode signal  $v_{c2}$ ,

$$v_{c2} = -v_{icm} \frac{\alpha R_C}{2R_{EE}} \quad \dots(4.23.2)$$

- If the output is taken differentially, then the output common-mode voltage  $v_o = (v_{c1} - v_{c2})$  will be zero and the common-mode gain also will be zero.
- On the other hand, if the output is taken single-ended, the common mode gain  $A_{cm}$  will be finite and given by

$$A_{cm} = -\frac{\alpha R_C}{2R_{EE}}$$

- Since in this case the differential gain is

$$A_d = \frac{1}{2} g_m R_c$$

9. The common-mode rejection ratio (CMRR) will be,

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right| = g_m R_{EE} \quad \dots(4.23.4)$$

10. Normally the CMRR is expressed in decibels,

$$\text{CMRR} = 20 \log \left| \frac{A_d}{A_{cm}} \right| \quad \dots(4.23.5)$$

### Effect of mismatch of $R_c$ :

1. Let the collector of  $Q_1$  have a load resistance  $R_c$ , and  $Q_2$  have a load resistance  $R_c + \Delta R_c$ .

2. It follows that

$$v_{c1} = -v_{icm} \frac{\alpha R_c}{2R_{EE} + r_e}$$

$$v_{c2} = -v_{icm} \frac{\alpha(R_c + \Delta R_c)}{2R_{EE} + r_e}$$

Thus, the signal at the output due to the common-mode input signal will be,

$$v_o = v_{c1} - v_{c2} = v_{icm} \frac{\alpha \Delta R_c}{2R_{EE} + r_e}$$

and the common-mode gain will be,

$$A_{cm} = \frac{\alpha \Delta R_c}{2R_{EE} + r_e} = \frac{\Delta R_c}{2R_{EE}}$$

This expression can be rewritten as,

$$A_{cm} = \frac{R_c}{2R_{EE}} \frac{\Delta R_c}{R_c} \quad \dots(4.23.7)$$

Compare the common-mode gain in eq. (4.23.7) with the single-ended output in eq. (4.23.3). The common-mode gain is much smaller in the case of differential output.

The input signals  $v_1$  and  $v_2$  to a differential amplifier usually contain a common-mode component,  $v_{icm}$ ,

$$v_{icm} \equiv \frac{v_1 + v_2}{2}$$

and a differential component  $v_{id}$ ,

$$v_{id} \equiv v_1 - v_2$$

Thus, the output signal will be given by

$$v_o = A_d(v_1 - v_2) + A_{cm} \left( \frac{v_1 + v_2}{2} \right)$$

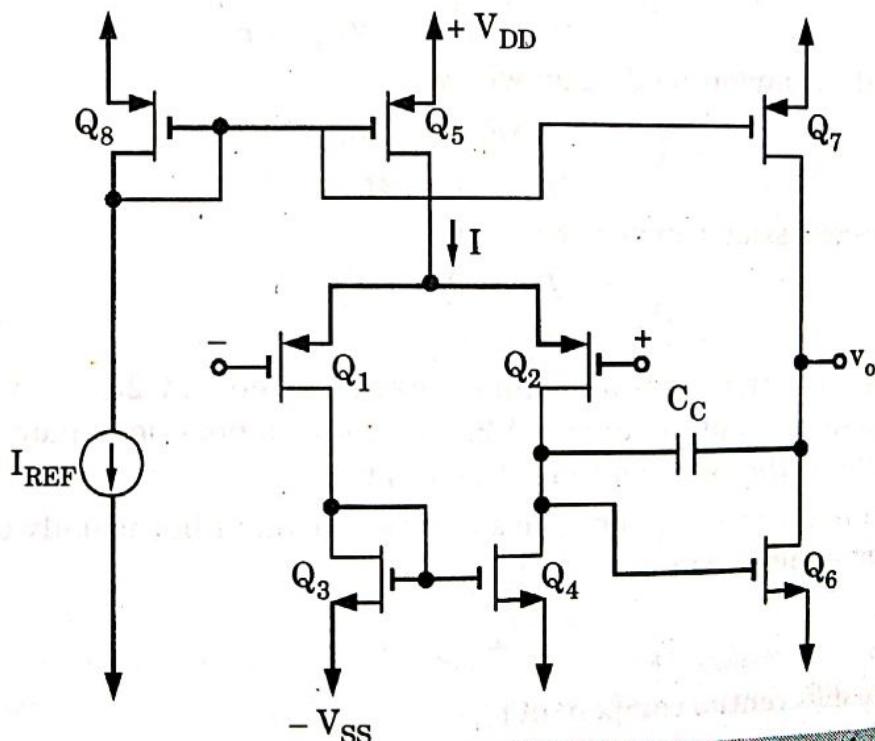
## Questions-Answers

## Long Answer Type and Medium Answer Type Questions

**Que 4.24.** Draw the circuit diagram of two-stage CMOS Op-Amp and also give details of differential amplifier used in it.

**Answer**

1. The circuit consists of two gain stages : The first stage is formed by the differential pair  $Q_1 - Q_2$  together with its current mirror load  $Q_3 - Q_4$ .
2. This differential amplifier circuit provides a voltage gain that is typically in the range of 20 V/V to 60 V/V, as well as performing conversion from differential to single ended form.



**Fig. 4.24.1.** The basic two-stage CMOS Op-Amp configuration.

3. The differential pair is biased by current source  $Q_5$ , which is one of the two output transistors of the current mirror formed by  $Q_8, Q_5$ , and  $Q_7$ .
4. The current mirror is fed by a reference current  $I_{REF}$ , which can be generated by simply connecting a precision resistor to the negative supply voltage  $-V_{SS}$ .

5. The second gain stage consists of the common-source transistor  $Q_6$  and its current source load  $Q_7$ .
6. The second stage typically provides a gain of 50 V/V to 80 V/V.
7. In addition, it takes part in the process of frequency compensating the Op-Amp.
8. The CMOS Op-Amp circuit of Fig. 4.24.1 can exhibit a systematic output DC offset voltage.
9. It was found that the DC offset can be eliminated by sizing the transistors so as to satisfy the following constraint :

$$\frac{(W/L)_6}{(W/L)_4} = 2 \frac{(W/L)_7}{(W/L)_5}$$

**Que 4.25.** Draw 741 Op-Amp block diagram and equivalent circuit and tell its ideal characteristics.

**Answer**

1. The block diagram of typical Op-Amp is shown in Fig. 4.25.1.

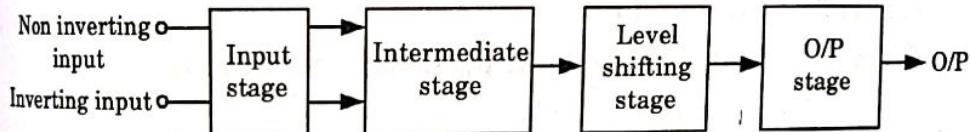


Fig. 4.25.1. Block diagram of Op-Amp.

2. The equivalent circuit of Op-Amp is shown in Fig. 4.25.2.

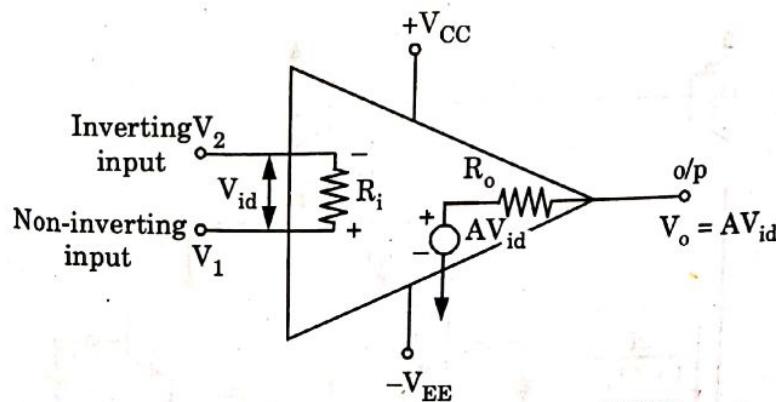


Fig. 4.25.2. Equivalent circuit of Op-Amp.

3. An ideal Op-Amp exhibit following electrical characteristics :

- i. Infinite voltage gain,  $A_v = \infty$ .
- ii. Infinite input resistance,  $R_i = \infty$ .
- iii. Zero output resistance,  $R_o = 0$ .
- iv. Zero output voltage when input voltage is zero.
- v. Infinite bandwidth.

**Que 4.26.** Explain the DC analysis of input stage of 741 IC Op-Amp.

**Answer**

- Transistor  $Q_{11}$  is biased by  $I_{REF}$ , and the voltage developed across it is used to bias  $Q_{10}$ , which has a series emitter resistance  $R_4$ .

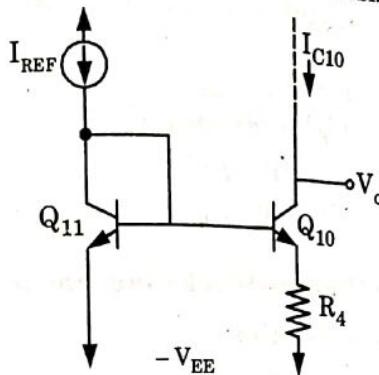


Fig. 4.26.1. The Widlar current source that biases the input stage.

- This part of the circuit is shown in Fig. 4.26.1 and can be recognized as the Widlar current source.
- From the circuit, and assuming  $\beta_{10}$  to be large, we have

$$V_{BE11} - V_{BE10} = I_{C10}R_4$$

$$\text{Thus, } V_T = \ln\left(\frac{I_{REF}}{I_{C10}}\right) = I_{C10}R_4 \quad \dots(4.26.1)$$

where it has been assumed that  $I_{C10} = I_{C11}$ .

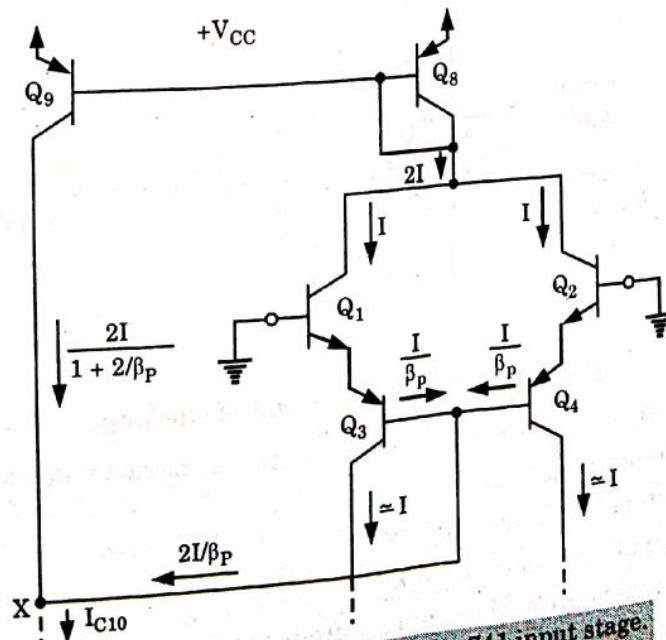


Fig. 4.26.2. The DC analysis of the 741 input stage.

4. Substituting the known values for  $I_{REF}$  and  $R_4$ , eq. (4.26.1) can be solved by trial and error to determine  $I_{C10}$ .

5. Having determined  $I_{C10}$ , we proceed to determine the DC current in each of the input-stage transistors. Part of the input stage is redrawn in Fig. 4.26.2. From symmetry,

$$I_{C1} = I_{C2} = I$$

6. If the *npn*  $\beta$  is high, then

$$I_{E3} = I_{E4} \approx I$$

and the base currents of  $Q_3$  and  $Q_4$  are equal, with a value of  $I/(\beta_p + 1) \approx I/\beta_p$ , where  $\beta_p$  denotes  $\beta$  of the *pnp* devices.

7. The current mirror formed by  $Q_8$  and  $Q_9$  is fed by an input current of  $2I$ , we can express the output current of the mirror as

$$I_{C9} = \frac{2I}{1 + 2/\beta_p}$$

8. We can write a node equation for node  $X$  in Fig. 4.26.2 and thus determine the value of  $I$ . If  $\beta_p > 1$ , then this node equation gives

$$2I = I_{C10}$$

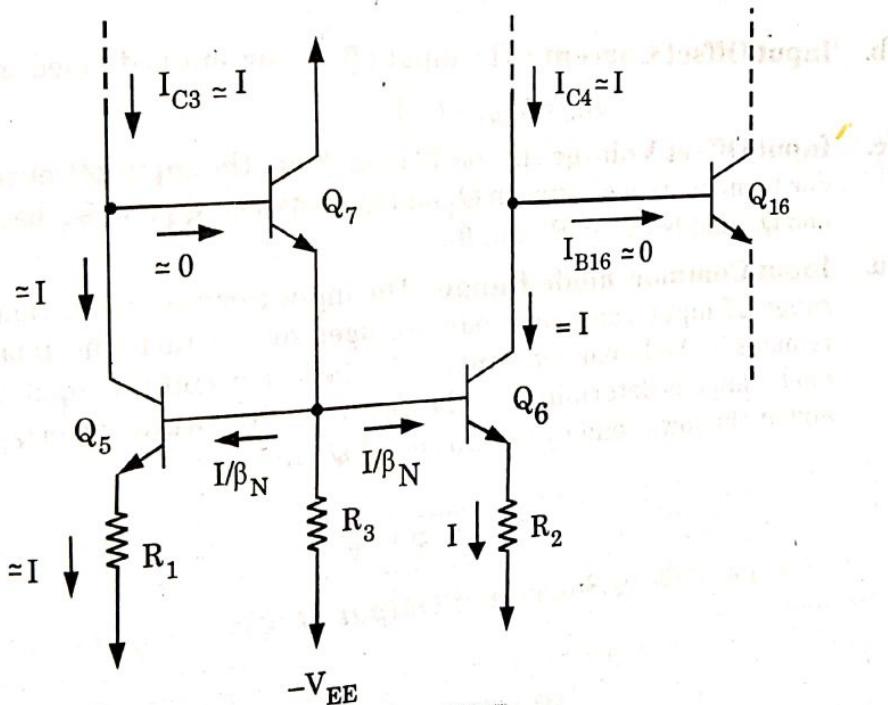


Fig. 4.26.3.

9. Fig. 4.26.3 shows the remainder of the 741 input stages. This part of the circuit is fed by  $I_{C3} = I_{C4} = I$ . Transistors  $Q_5$  and  $Q_6$  are identical and have equal resistances  $R_1$  and  $R_2$  in their emitters,

$$I_{C5} = I_{C6}$$

Now if the base currents of  $Q_7$  and  $Q_{16}$  can be neglected, then

$$I_{C5} \approx I_{C3} = I \quad \dots(4.26.3)$$

and

$$I_{C6} = I_{C4} = I \quad \dots(4.26.4)$$

10. Thus both the symmetry of  $Q_5$  and  $Q_6$  and the node equations at their collectors force their currents to be equal and to equal  $I$ .
11. The bias current of  $Q_7$  can be determined from

$$I_{C7} \approx I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3} \quad \dots(4.26.5)$$

where  $\beta_N$  denote  $\beta$  of the *npn* transistors. To determine  $V_{BE6}$  we use the transistor exponential relationship and write

$$V_{BE6} = V_T \ln \frac{I}{I_S}$$

- a. **Input Bias Current :** The input bias current of an Op-Amp is defined as

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

For the 741 we obtain,  $I_B = \frac{I}{\beta_N}$

- b. **Input Offset Current :** The input offset current is defined as

$$I_{OS} = |I_{B1} - I_{B2}|$$

- c. **Input Offset Voltage :** In the 741 Op-Amp, the input offset voltage is due to mismatches between  $Q_1$  and  $Q_2$ , between  $Q_3$  and  $Q_4$ , between  $Q_5$  and  $Q_6$ , and between  $R_1$  and  $R_2$ .

- d. **Input Common-mode Range :** The input common-mode range is the range of input common-mode voltages over which the input stage remains in the linear active mode. In the 741 circuit the input common-mode range is determined at the upper end by saturation of  $Q_1$  and  $Q_2$ , and at the lower end by saturation of  $Q_3$  and  $Q_4$ .

## PART-6

*Design of Gain Stages and Output Stages, Compensation.*

### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 4.27.** Explain the DC analysis of second stage and output stage of 741 IC Op-Amp.

**Answer****A. Second-Stage :**

1. If we neglect the base current of  $Q_{23}$  from Op-Amp circuit then the collector current of  $Q_{17}$  is approximately equal to the current supplied by current source  $Q_{13B}$ .

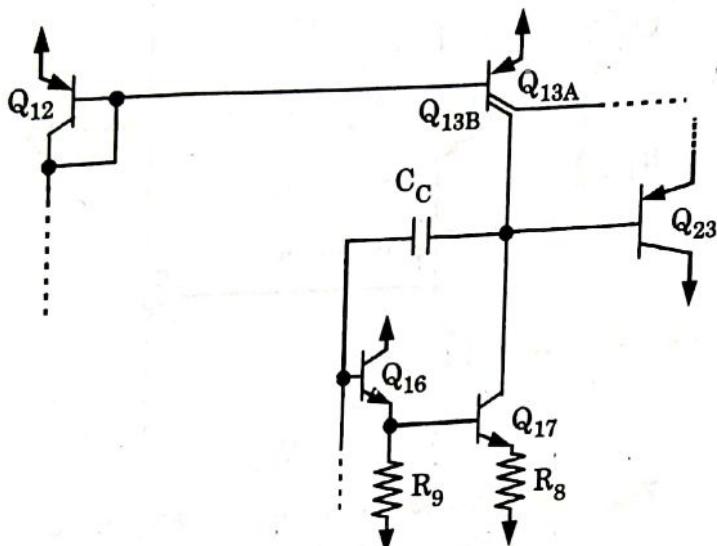


Fig. 4.27.1.

2. Because  $Q_{13B}$  has a scale current 0.75 times that of  $Q_{12}$ , its collector current will be  $I_{C13B} = 0.751 I_{REF}$ , where we have assumed that  $\beta_p > 1$ .  
 3. At this current level the base-emitter voltage for  $Q_{17}$  is

$$V_{BE17} = V_T \ln \frac{I_{C17}}{I_s}$$

4. The collector current of  $Q_{16}$  can be determined from

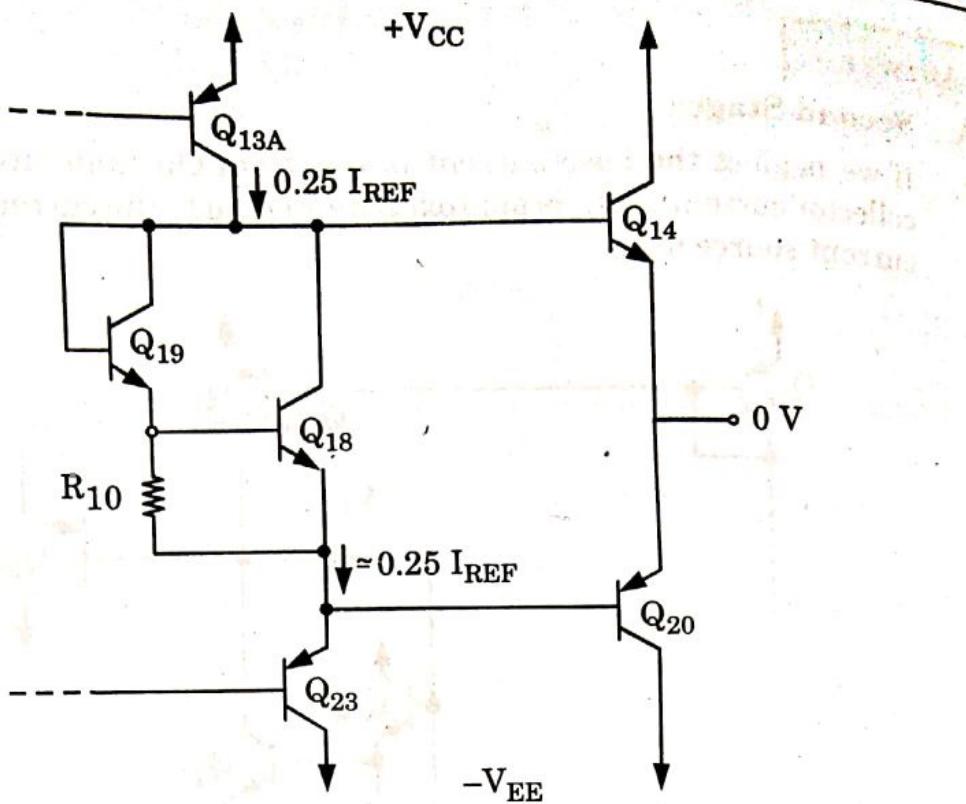
$$I_{C16} = I_{E16} = I_{B17} + \frac{I_{E17}R_8 + V_{BE17}}{R_9}$$

**B. Output-stage Bias :**

1. Fig. 4.27.2 shows the output stage of the 741.  
 2. Current source  $Q_{13A}$  delivers a current of  $0.25 I_{REF}$  (because  $I_S$  of  $Q_{13A}$  is 0.25 times the  $I_S$  of  $Q_{12}$ ) to the network composed of  $Q_{18}$ ,  $Q_{19}$  and  $R_{10}$ .  
 3. If we neglect the base current of  $Q_{14}$  and  $Q_{20}$ , then the emitter current of  $Q_{23}$  will also be equal to  $0.25 I_{REF}$ . Thus,  

$$I_{C23} = I_{E23} = 0.25 I_{REF}$$
  
 4. Thus, we can assume that the base current of  $Q_{23}$  is negligible compared to  $I_{C17}$ .  
 5. The voltage drop across the base-emitter junction of  $Q_{19}$  can be determined as

$$V_{BE19} = V_T \ln \frac{I_{C19}}{I_s}$$



**Fig. 4.27.2.** The 741 output stage without the short-circuit protection devices.

6. Voltage drop,

$$V_{BB} = V_{BE18} + V_{BE19}$$

7. Since  $V_{BB}$  appears across the series combination of the base-emitter junctions of  $Q_{14}$  and  $Q_{20}$ , we can write

$$V_{BB} = V_T \ln \frac{I_{C14}}{I_{S14}} + V_T \ln \frac{I_{C20}}{I_{S20}}$$

**Que 4.28.** Explain the frequency response of two-stage CMOS Op-Amp using the  $C_c$  compensation capacitance.

**Answer**

1. The equivalent circuit is shown in Fig 4.28.1. Capacitance  $C_1$  is the total capacitance between the output node of the first stage and ground, thus

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6} \quad \dots(4.28.1)$$

2. Capacitance  $C_2$  represents the total capacitance between the output node of the Op-Amp and ground and includes whatever load capacitance  $C_L$  that the amplifier is required to drive, thus

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L \quad \dots(4.28.2)$$

3.  $C_L$  is larger than the transistor capacitances, with the result that  $C_2$  becomes much larger than  $C_1$ .

4.  $C_{gd6}$  should be shown in parallel with  $C_c$  but has been ignored because  $C_c$  is usually much larger.

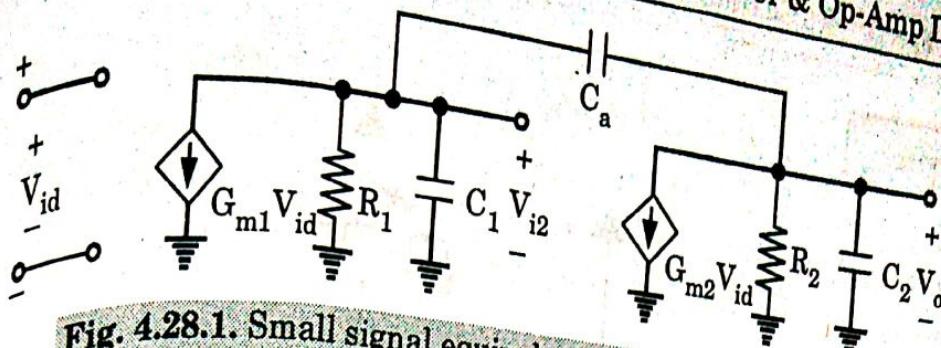


Fig. 4.28.1. Small signal equivalent circuit for the Op-Amp.

5. It was found that it has two poles and a positive real-axis zero with the following approximate frequencies :

$$f_{P1} \approx \frac{1}{2\pi R_1 G_{m2} R_2 C_C}, \quad f_{P2} \approx \frac{G_{m2}}{2\pi C_2}$$

$$f_z \approx \frac{G_{m2}}{2\pi C_C}$$

6. Here,  $f_{P1}$  is the dominant pole formed by the interaction of Miller-multiplied  $C_C$  [i.e.,  $(1 + G_{m2} R_2) C_C = G_{m2} R_2 C_C$ ] and  $R_1$ .  
 7. To achieve the goal of a uniform - 20 dB/decade gain rolloff down to 0 dB, the unity-gain frequency  $f_t$ ,

$$f_t = |A_v| f_{P1} = \frac{G_{m1}}{2\pi C_C}$$

must be lower than  $f_{P2}$  and  $f_z$ , thus the design must satisfy the following two conditions :

$$\frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2}$$

and

$$G_{m1} < G_{m2}$$

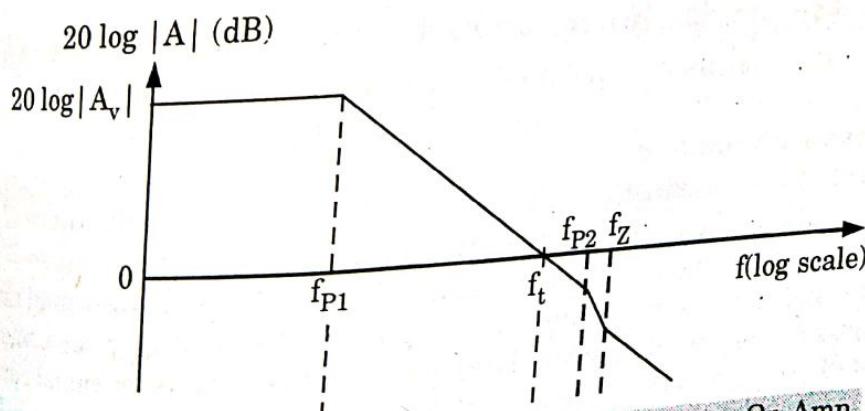
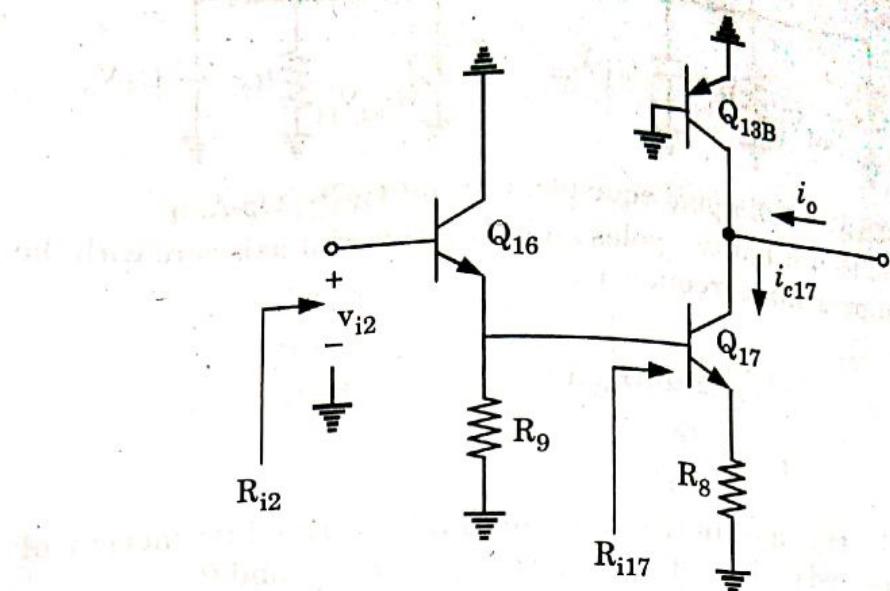


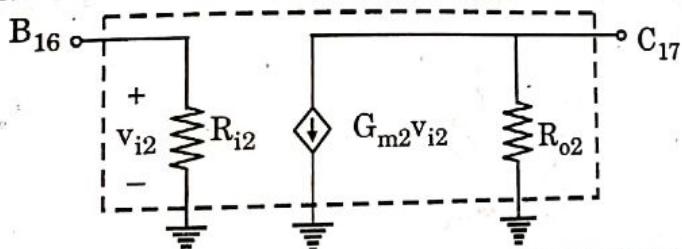
Fig. 4.28.2. Typical frequency response of the two-stage Op-Amp.

- Que 4.29. Determine the small-signal model of the second stage of the 741 Op-Amp.

AKTU 2017-18, Marks 05

**Answer****Fig. 4.29.1.** The 741 second stage.

1. Fig. 4.29.1 shows the 741 second stage Op-Amp prepared for small-signal analysis. Now we analyze the second stage to determine the values of the parameters of the equivalent circuit shown in Fig. 4.29.2.

**Fig. 4.29.2.** Small-signal equivalent-circuit model of the second stage.

1. **Input resistance :** The input resistance  $R_{i2}$  can be found by  

$$R_{i2} = (\beta_{16} + 1) \{ r_{e16} + [R_9 \parallel (\beta_{17} + 1)(r_{e17} + R_8)] \}$$
2. **Transconductance :**
- i. From the equivalent circuit of Fig. 4.29.2, the transconductance  $G_{m2}$  is the ratio of the short-circuit output current to the input voltage.
  - ii. Short-circuiting the output terminal of the second stage to ground makes the signal current through the output resistance of  $Q_{13B}$  zero, and the output short-circuit current becomes equal to the collector signal current of  $Q_{17}$  ( $i_{c17}$ ). This can be related to  $v_{i2}$  as follows :

$$i_{c17} = \frac{\alpha v_{b17}}{r_{e17} + R_8}$$

$$v_{b17} = v_{i2} \frac{(R_9 \parallel R_{i17})}{(R_9 \parallel R_{i17}) + r_{e16}}$$

$$R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8)$$

where we have neglected  $r_{o16}$  because  $r_{o16} \gg R_9$ .

iii. These equations can be combined to obtain,  $G_{m2} \equiv \frac{i_{e17}}{v_{i2}}$

### 3. Output resistance :

- To determine the output resistance  $R_{o2}$  of the second stage in Fig. 4.29.1 we ground the input terminal and find the resistance looking back into the output terminal.
- So,  $R_{o2}$  is given by  $R_{o2} = (R_{o13B} \parallel R_{o17})$  where  $R_{o13B}$  is the resistance looking into the collector  $Q_{13B}$  while its base and emitter are connected to ground and  $R_{o17}$  is the resistance looking into the collector of  $Q_{17}$ .

**Que 4.30.** Discuss the frequency response of 741 Op-Amp.

### Answer

- The system employs the Miller compensation technique.
- A capacitor ( $C_c$ ) of about 30 pF is connected in the negative feedback path of the second stage.
- An estimation of frequency of poles can be obtained as

$$C_{in} = C_c(1 + |A_2|)$$

$A_2$  = Gain of second stage

- Let  $A_2 = -515$  then  $C_{in} = 15480 \text{ pF}$

Since, this value of capacitor is large so we neglect all other capacitances between the base and ground of transistor.

- The total resistance,

$$R_t = (R_{o1} \parallel R_{i2}) \quad [ \because R_{o1} = 6.7 \text{ M}\Omega, R_{i2} = 4 \text{ M}\Omega ] \\ = (6.7 \text{ M}\Omega \parallel 4 \text{ M}\Omega) = 2.5 \text{ M}\Omega$$

- The dominant pole has a frequency  $f_p$ ,  $f_p = \frac{1}{2\pi C_{in} R_t} = 4.1 \text{ Hz}$

- Calculate all the values of poles and a Bode plot is shown in Fig. 4.30.2

$$f_t = A_o f_{3dB} = 243147 \times 4.1$$

$$f_t \approx 1 \text{ MHz}$$

where,  $f_t$  is unity-gain bandwidth.

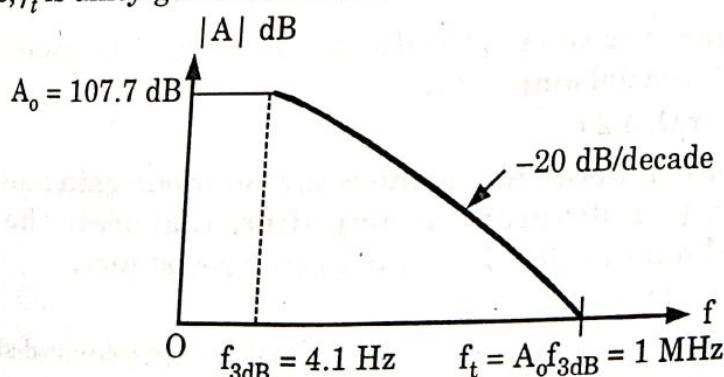


Fig. 4.30.1. Bode plot for the IC 741 gain.

Bode plot signifies that the phase shift at  $f_t$  is  $-90^\circ$  and thus phase margin is  $90^\circ$ . This phase margin is sufficient to provide stable operation of closed-loop amplifiers with any value of feedback factor  $\beta$ .

## PART - 1

*Op-amp applications : Review of Inverting and Non-inverting Amplifiers.*

### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 5.1.** Draw and derive relationship for op-amp as closed loop non-inverting amplifier circuit. AKTU 2016-17, Marks 05

OR

Derive an expression for voltage gain of inverting and non-inverting ideal operational amplifier configurations. AKTU 2017-18, Marks 07

### Answer

#### Inverting Op-Amp :

- Fig. 5.1.1 shows the basic inverting amplifier with input resistance  $R_1$  and feedback resistance  $R_f$ .

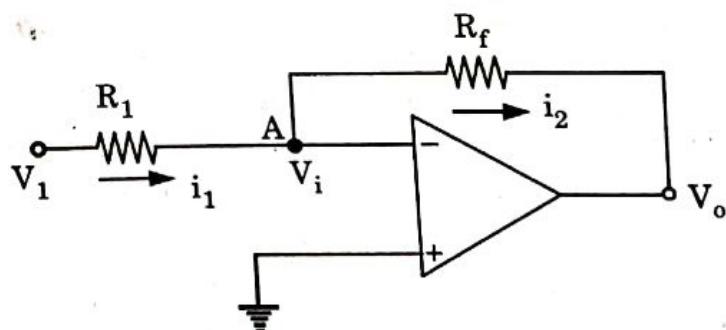


Fig. 5.1.1. Inverting amplifier.

- The current  $i_1$  flowing through  $R_1$  is given by,

$$i_1 = \frac{V_1 - V_i}{R_1} = \frac{V_1}{R_1} \quad (\because V_i = 0 \text{ due to virtual ground})$$

and

$$i_2 = \frac{V_i - V_o}{R_f} = \frac{-V_o}{R_f}$$

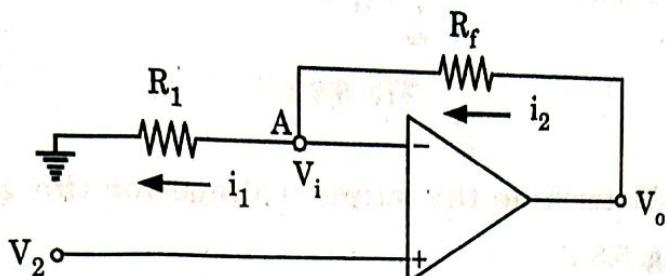
- At point A,

$$\frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

$$A_v = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

**Non-inverting amplifier :**

1. The circuit for non-inverting amplifier is shown in Fig. 5.1.2.

**Fig. 5.1.2. Non-inverting amplifier**

2. The currents  $i_1$  and  $i_2$  are given as :

$$i_1 = \frac{V_2}{R_1} \text{ and } i_2 = \frac{V_o - V_2}{R_f} \quad (\because V_i = V_2 \text{ due to virtual ground})$$

3. Applying KCL at point A,

$$(-i_1) + i_2 = 0 \quad -\frac{V_2}{R_1} + \frac{V_o - V_2}{R_f} = 0$$

$$\frac{V_o}{R_f} = \frac{V_2}{R_1} + \frac{V_2}{R_f} = V_2 \left( \frac{1}{R_1} + \frac{1}{R_f} \right)$$

$$\frac{V_o}{V_2} = \frac{R_1 + R_f}{R_1} = \left( 1 + \frac{R_f}{R_1} \right)$$

$$A_v = \left( 1 + \frac{R_f}{R_1} \right)$$

**Que 5.2.** Design and draw an inverting amplifier using op-amp  
with a gain of -5 and  $R_i = 10 \text{ k}\Omega$ .

AKTU 2016-17, Marks 05

**Answer**

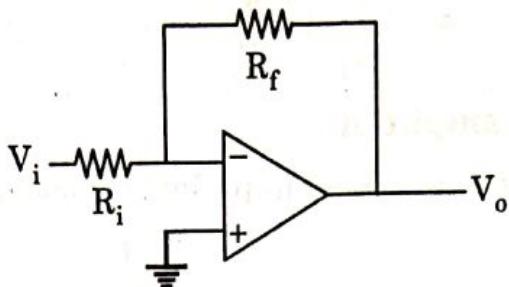
Gain,

$$A_v = -5$$

$$R_i = 10 \text{ k}\Omega$$

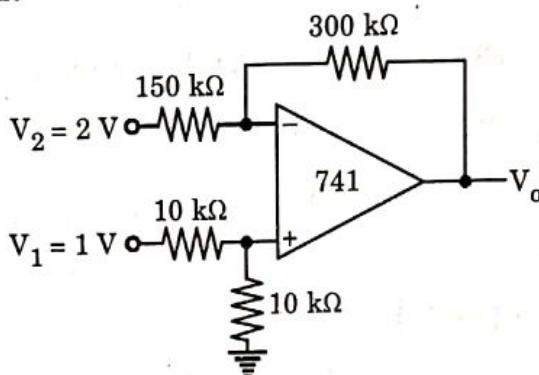
$$A_v = \frac{-R_f}{R_i} = -5$$

$$R_f = 5 \times R_i = 5 \times 10 = 50 \text{ k}\Omega$$



**Fig. 5.2.1.**

**Que 5.3.** Determine the output voltage for the given circuit shown in Fig. 5.3.1.



**Fig. 5.3.1.**

**AKTU 2014-15, Marks 05**

**AKTU 2017-18, Marks 3.5**

**Answer**

1. We can get  $V_o$  by superposition method,
2. Let  $V_1 = 1 \text{ V}$  and  $V_2$  is at ground, so output due to  $V_1$ ,  $V_{o1}$ , will be due to input at non-inverting terminal,

$$V_{o1} = \left(1 + \frac{300}{150}\right) \left(\frac{10}{(10+10)}\right) = \frac{1}{2} \times \frac{450}{150} = \frac{3}{2} = 1.5 \text{ V}$$

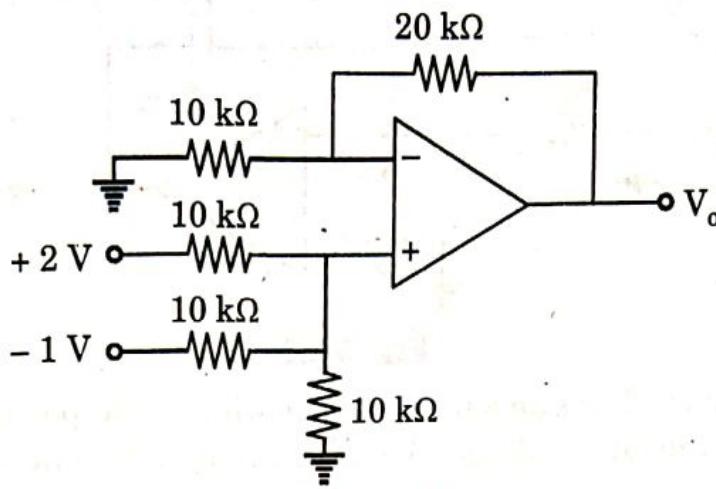
3. Let  $V_2 = 2 \text{ V}$  and  $V_1$  is at ground, so output due to  $V_2$ ,  $V_{o2}$  will be due to input at inverting terminal,

$$V_{o2} = - \frac{300}{150} \times 2 = -4 \text{ V}$$

4. Now total output,  $V_o = V_{o1} + V_{o2}$

$$V_o = +1.5 - 4 = -2.5 \text{ V}$$

**Que 5.4.** Find the output voltage for the given Fig. 5.4.1.



**Fig. 5.4.1.**

**Answer**

1. This circuit will be solved using superposition principle.
2. Considering only + 2 V voltage source :

$$V'_o = \left(1 + \frac{20}{10}\right) V'_1 = (1 + 2) \left(\frac{5 \times 2}{10 + 5}\right) = 2 \text{ V}$$

3. Considering only - 1 V voltage source :

$$V''_o = \left(1 + \frac{20}{10}\right) V''_1 = (1 + 2) \left(\frac{5 \times -1}{10 + 5}\right) = -1 \text{ V}$$

4. Total output voltage,  $V = V'_o + V''_o = 2 - 1 = 1 \text{ V}$

**PART-2**

*Integrator and Differentiator, Summing Amplifier.*

**Questions-Answers**

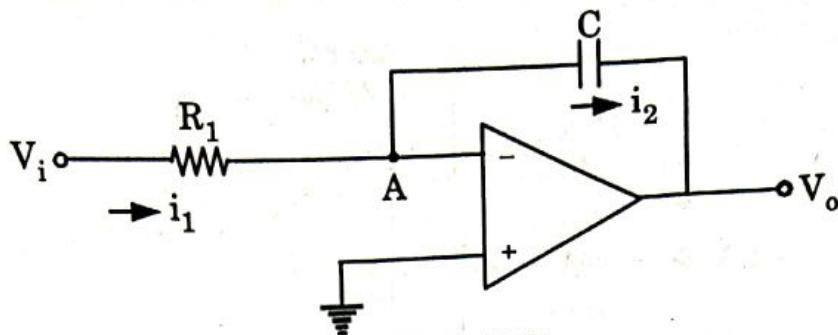
**Long Answer Type and Medium Answer Type Questions**

**Que 5.5.** Describe in detail account on integrator and differentiator with suitable circuit. **AKTU 2014-15, Marks 10**

**Answer**

**Integrator :**

1. The circuit of integrator is shown in Fig. 5.5.1.



**Fig. 5.5.1.**

2. This circuit produces an output voltage which is proportional to the time integral of the input voltage. Due to this reason it is known as integrator.
3. The integrator is an inverting op-amp in which feedback resistor  $R_f$  has been replaced by a capacitor  $C$ .
4. Feedback through capacitor forces a virtual ground to exist at the inverting input terminal.
5. The capacitive reactance  $X_c$  can be expressed as :

$$i_1 = \frac{V_i}{R_1} \text{ and } i_2 = \frac{dq_2}{dt} = C \frac{d(V_A - V_o)}{dt}$$

6. At point A,

$$\frac{V_i}{R_1} = -C \frac{d V_o}{dt}$$

$$dV_o = \frac{-1}{R_1 C} V_i dt$$

$$V_o(t) = -\frac{1}{R_1 C} \int V_i(t) dt \quad \dots(5.5.1)$$

The eq. (5.5.1) shows that the output is the integral of the input with an inversion and scale multiplier of  $1/R_1 C$ .

#### Differentiator :

1. The function of a differentiator is to give an output voltage which is proportional to the rate of change of input voltage.
2. The circuit of a differentiator is shown in Fig. 5.5.2.
3. When we feed linearly increasing voltage to the differentiator, we get a constant DC output. So it is an inverse mathematical operation to that of an integrator.

4. At point A,

$$V_i = \frac{q}{C}$$

$$\frac{dV_i}{dt} = \frac{1}{C} \frac{dq}{dt} = \frac{i}{C} \text{ where } i = \frac{dq}{dt} \quad \dots(5.5.2)$$

$$V_o = -iR \quad \dots(5.5.3)$$

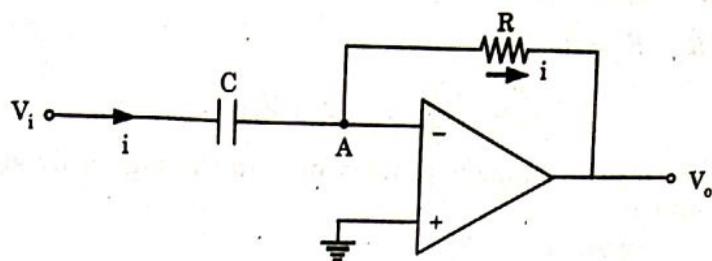


Fig. 5.5.2.

5. Put the value of  $i$  from eq. (5.5.2) in eq. (5.5.3)

$$V_o = -CR \frac{dV_i}{dt} \quad \dots(5.5.4)$$

6. The eq. (5.5.4) shows that the output voltage  $V_o$  is equal to a constant ( $-CR$ ) times the time derivative of the input voltage  $V_i$ .

**Que 5.6.** Explain summing amplifier using op-amp.

**AKTU 2015-16, Marks 03**

**Answer**

1. Fig. 5.6.1 shows the three input summer circuit. This circuit provides a means of algebraically summing three input voltages, each multiplied by a constant gain factor.

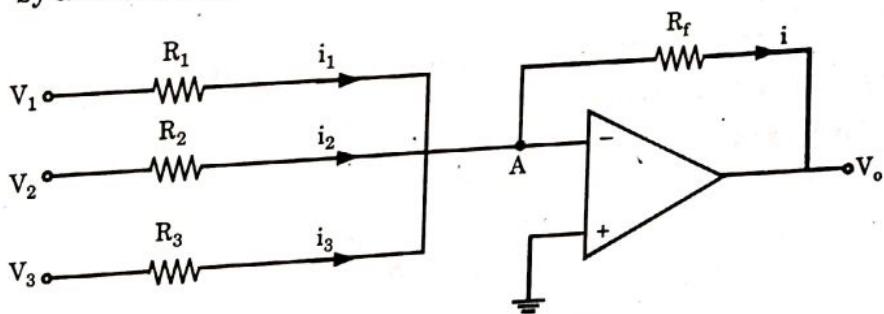


Fig. 5.6.1. Summer circuit.

2. At point A (virtual ground), the different currents are given as :

$$i_1 = \frac{V_1}{R_1}, i_2 = \frac{V_2}{R_2}, i_3 = \frac{V_3}{R_3} \text{ and } i = -\frac{V_o}{R_f}$$

3. Applying KCL at point A, we get,

$$i_1 + i_2 + i_3 - i = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

$$V_o = - \left[ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

4. If  $R_1 = R_2 = R_3 = R$ , then

$$V_o = -\frac{R_f}{R} [V_1 + V_2 + V_3]$$

5. Thus the output voltage is proportional to the algebraic sum of three input voltages.

Again, if  $R_f = R$ ,

$$V_o = -[V_1 + V_2 + V_3]$$

- Que 5.7.** Calculate the output voltage for the circuit of Fig. 5.7.1 with inputs of  $V_1 = 40 \text{ mV rms}$  and  $V_2 = 20 \text{ mV rms}$ .

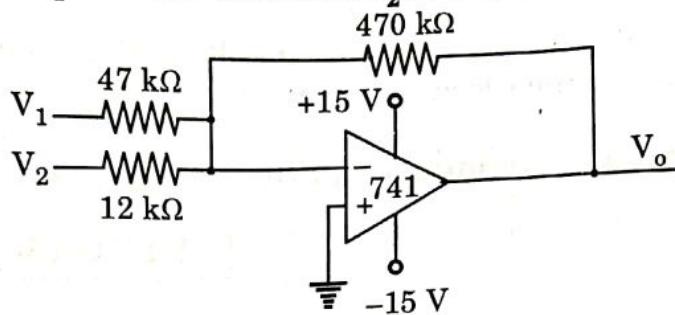


Fig. 5.7.1.

AKTU 2016-17, Marks 07

**Answer**

Given :  $V_1 = 40 \text{ mV rms}$ ,  $V_2 = 20 \text{ mV rms}$ ,  $R_1 = 47 \text{ k}\Omega$

$R_2 = 12 \text{ k}\Omega$ ,  $R_f = 470 \text{ k}\Omega$ .

To find :  $V_o$ .

$$\begin{aligned} V_o &= - \left[ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 \right] \\ &= - \left[ \frac{470}{47} \times 40 + \frac{470}{12} \times 20 \right] \\ &= - [400 + 783.3] = - 1183.33 \text{ mV rms} \\ &= - 1.18 \text{ V rms} \end{aligned}$$

- Que 5.8.** Determine the output voltage for the given Fig. 5.8.1.

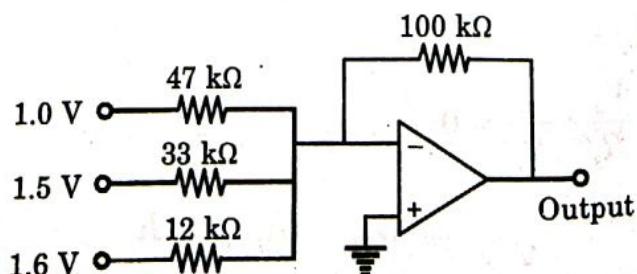


Fig. 5.8.1.

**Answer**

The output voltage of a summing amplifier is given by

$$\begin{aligned} V_o &= - \left[ \frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3 \right] \\ &= - \left[ \frac{100}{47} \times 1 + \frac{100}{33} \times 1.5 + \frac{100}{12} \times 1.6 \right] = -20 \text{ V} \end{aligned}$$

**PART-3**

*Precision Rectifier.*

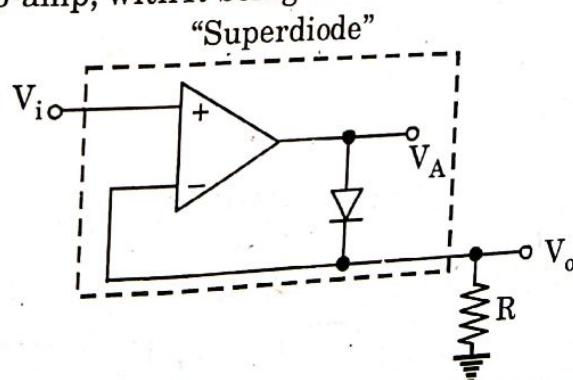
**Questions-Answers****Long Answer Type and Medium Answer Type Questions**

**Que 5.9.** What do you understand by precision rectifier? Explain the working of half wave precision rectifier.

**AKTU 2014-15, Marks 05**

**Answer**

- A. **Precision rectifier :** A circuit which can act as an ideal diode for rectifying voltages which are below the level of cut-in voltage of the diode are called precision rectifier circuit.
- B. **Half wave precision rectifier :** Fig. 5.9.1 shows a precision half-wave rectifier circuit consisting of a diode placed in the negative-feedback path of an op-amp, with  $R$  being the rectifier load resistance.



**Fig. 5.9.1. Precision half wave rectifier.**

**C. Operation :**

1. If  $V_i$  goes positive, the output voltage  $V_A$  of the op-amp will go positive and the diode will conduct, thus establishing a closed feedback path between the op-amp's output terminal and the negative input terminal.

2. The negative-feedback path will cause a virtual short circuit to appear between the two input terminals.
  3. Thus the voltage at the negative input terminal, which is also the output voltage  $V_o$ , will equal (to within a few millivolts) that at the positive input terminal, which is the input voltage  $V_i$ ,
- $$V_o = V_i, \text{ for } V_i \geq 0$$
4. Consider now the case when  $V_i$  goes negative. The op-amp's output voltage  $V_A$  will tend to follow and go negative.
  5. This will reverse-bias the diode, and no current will flow through resistance  $R$ , causing  $V_o$  to remain equal to 0 V. Thus, for  $V_i < 0$ ,

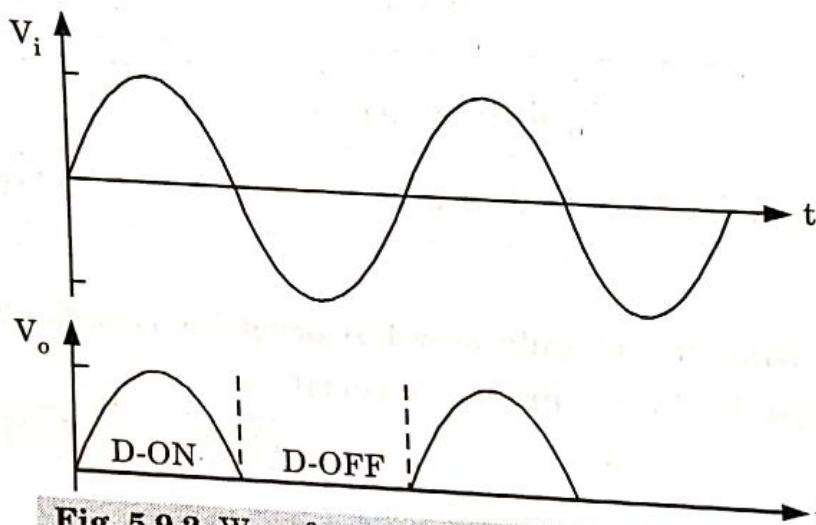


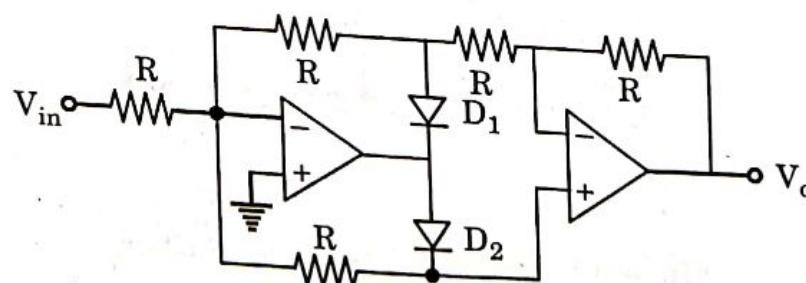
Fig. 5.9.2. Waveform of Half-wave precision rectifier.

**Que 5.10.** Draw the circuit diagram of full wave precision rectifier and find expression for output voltage for both positive and negative half cycle of input sinusoidal waveform.

**OR**  
Explain working of precision full wave rectifier with necessary waveform.

AKTU 2016-17, Marks 10

**Answer**



1. For positive half cycle of  $V_{in}$ , diode  $D_1$  will be ON and  $D_2$  will be OFF. Both the op-amps will act like inverter and thus,  $V_o$  will follow the input  $V_{in}$ .

Fig. 5.10.1.

From Fig. 5.10.2,

Hence,

$$V_{o1} = \frac{-R}{R} V_{in} = -V_{in}$$

and

$$V_o = \frac{-R}{R} (-V_{in}) = V_{in}$$

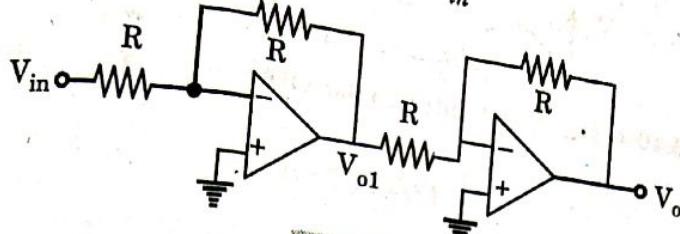


Fig. 5.10.2.

2. In negative half cycle of  $V_{in}$ , diode  $D_1$  will be OFF and  $D_2$  will be ON.

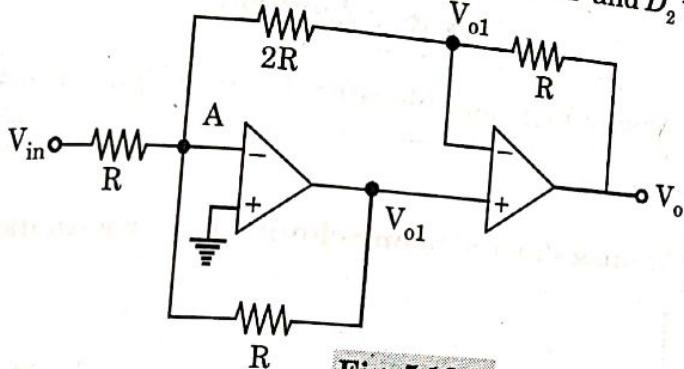


Fig. 5.10.3.

- i Applying KCL at node A,

$$\frac{V_A - V_{in}}{R} + \frac{V_A - V_{o1}}{R} + \frac{V_A - V_{o1}}{2R} = 0$$

- i Now,

[Virtual ground concept]

$$-\frac{V_{in}}{R} - \frac{V_{o1}}{R} - \frac{V_{o1}}{2R} = 0$$

$$V_{in} = -\frac{3}{2} V_{o1}$$

$$V_{o1} = -\frac{2}{3} V_{in}$$

Also,

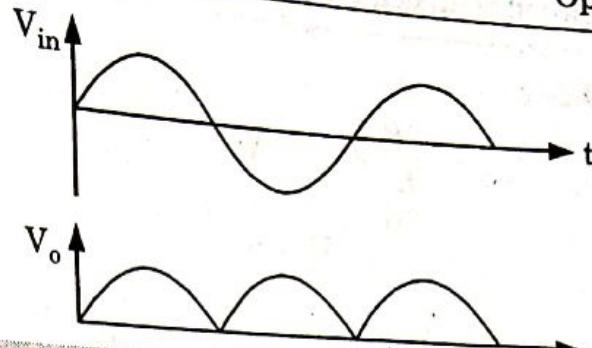
$$V_o = \left(1 + \frac{R}{2R}\right) V_{o1} = \left(1 + \frac{R}{2R}\right) \left(-\frac{2}{3} V_{in}\right)$$

Hence, for

$$V_o = -V_{in}$$

$$V_{in} < 0,$$

$$V_o = -V_{in}$$



**Fig. 5.10.4.** Input and output waveforms of full wave rectifier.

### PART-4

#### Schmitt Trigger and its Applications.

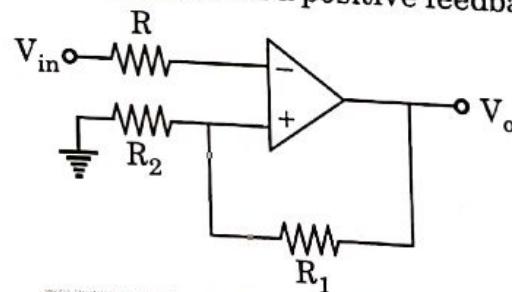
#### Questions-Answers

#### Long Answer Type and Medium Answer Type Questions

**Que 5.11.** Write a short note on Schmitt trigger with its waveform.

#### Answer

1. If positive feedback is added to the comparator circuit, gain can be increased greatly. This circuit is called Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback.



**Fig. 5.11.1.** Schmitt trigger.

2. Schmitt trigger also exhibits the phenomenon of hysteresis. The input voltage is applied to the (-ve) input terminal and feedback voltage to the (+ve) input terminal.
3. Input voltage  $V_{in}$  triggers output  $V_o$ , every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage ( $V_{UT}$ ) and lower threshold voltage ( $V_{LT}$ ).
4. Now, suppose the output  $V_o = +V_{sat}$ . The voltage at (+ve) input terminal will be

$$V_{UT} = \frac{R_2}{R_1 + R_2} (+V_{sat}) \quad \dots(5.11.1)$$

This voltage is upper threshold voltage. As long as  $V_{in}$  is less than  $V_{UT}$ , the output  $V_o$  remains constant at  $+V_{sat}$ .

5. When  $V_{in}$  is just greater than  $V_{UT}$ , the output then switches to  $-V_{sat}$  and remains at this level as long as  $V_{in} > V_{UT}$ .
6. For  $V_o = -V_{sat}$ , the voltage at (+ve) input terminal will be

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{sat}) \quad \dots(5.11.2)$$

This voltage is called lower threshold voltage.

7. The output voltage is  $-V_{sat}$  as long as  $V_{in}$  is above or positive with respect to  $V_{LT}$ . The output voltage  $V_o$  changes to  $+V_{sat}$  if  $V_{in}$  goes more negative than or below  $V_{LT}$ . Resistor  $R$  is shown as  $R_1 \parallel R_2$  compensate for input bias current.
8. Input and output voltage waveforms are shown in Fig. 5.11.2.

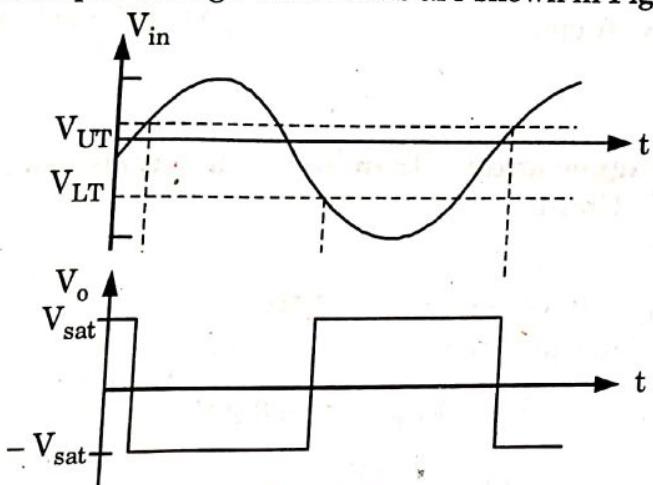


Fig. 5.11.2.

#### 9. Hysteresis curve (Transfer characteristics) :

- i. From eq. (5.11.1) and (5.11.2),

$$V_{UT} > V_{LT}$$

$$\therefore V_{UT} - V_{LT} = \frac{2R_2}{R_1 + R_2} V_{sat}$$

This difference is called Hysteresis width.

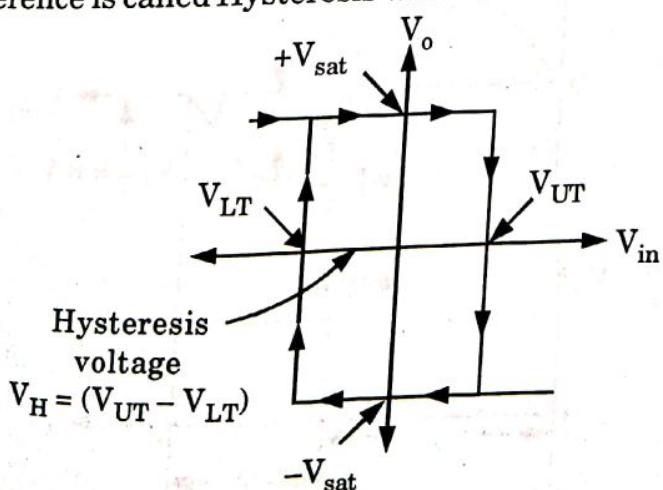


Fig. 5.11.3.

- ii.  $V_H$  is also called dead band because change in  $V_{in}$  do not change the output voltage. When the input exceeds  $V_{UT}$ , output switches from  $+V_{sat}$  to  $-V_{sat}$  and reverts back to its original state,  $+V_{sat}$ , when the input goes below  $V_{LT}$ .

- 10. Applications :** Schmitt trigger is used to convert any wave into a square wave.

**Que 5.12.** Describe the Schmitt trigger with the help of proper circuit diagram and transfer characteristics. A Schmitt trigger with the upper threshold level  $V_{UT} = 0 \text{ V}$  and hysteresis width is  $0.2 \text{ V}$  converts  $1 \text{ kHz}$  sine wave of amplitude  $4 \text{ V}_{PP}$  into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

AKTU 2015-16, Marks 15

**Answer**

Schmitt trigger and its transfer characteristics : Refer Q. 5.11, Page 5-12E, Unit-5.

**Numerical :**

Given :  $V_{UT} = 0 \text{ V}$ ,  $V_H = 0.2 \text{ V}$ ,  $f = 1 \text{ kHz}$

To Find : Time duration.

1.  $V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$

So,  $V_{LT} = -0.2 \text{ V}$

2. In Fig. 5.12.1 the angle  $\theta$  can be calculated as

$$\begin{aligned} -0.2 &= V_m \sin(\pi + \theta) = -V_m \sin \theta = -2 \sin \theta \\ \theta &= \arcsin 0.1 = 0.1 \text{ radian} \end{aligned}$$

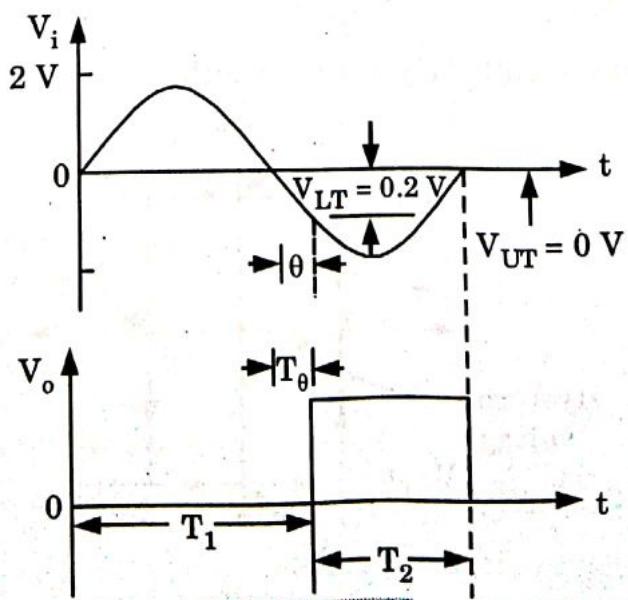


Fig. 5.12.1.

3. The period,

$$T = 1/f = 1/1000 = 1 \text{ ms}$$

$$\omega T_0 = 2\pi (1000) T_0 = 0.1$$

$$T_0 = (0.1/2\pi) \text{ ms} = 0.016 \text{ ms}$$

4. So,  
and

$$T_1 = T/2 + T_0 = 0.516 \text{ ms}$$

$$T_2 = T/2 - T_0 = 0.484 \text{ ms}$$

**Que 5.13.** Design and implement an inverting Schmitt trigger for the use as zero crossing detector with saturation voltages of  $\pm 15 \text{ V}$ , having hysteresis transition of  $\pm 25 \text{ mV}$ .

AKTU 2014-15, Marks 05

**Answer**

Given :  $V_{sat} = \pm 15 \text{ V}$ ,  $V_{UT} = 25 \text{ mV}$ ,  $V_{LT} = -25 \text{ mV}$

To Design : Inverting Schmitt trigger.

1.

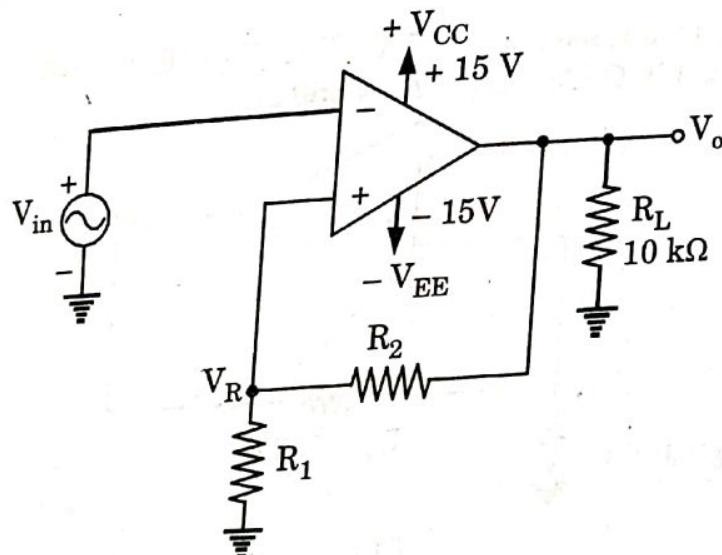


Fig. 5.13.1.

2. For this Schmitt trigger circuit,

$$V_{UT} = \frac{R_1}{R_1 + R_2} (+ V_{sat})$$

and

$$V_{LT} = \frac{R_1}{R_1 + R_2} (- V_{sat})$$

Putting given values,

$$25 \text{ mV} = \frac{R_1}{(R_1 + R_2)} (15)$$

and

$$-25 \text{ mV} = \frac{R_1}{R_1 + R_2} \times (-15)$$

$$\therefore \frac{25 \times 10^{-3}}{15} = \frac{R_1}{R_1 + R_2}$$

$$1.67 \times 10^{-3} = \frac{R_1}{R_1 + R_2}$$

$$1.67 (R_1 + R_2) = R_1 \times 10^3$$

Let

$$R_1 = 100 \Omega$$

$\therefore$

$$R_2 = 59.78 \text{ k}\Omega$$

**Que 5.14.** Explain how a Schmitt trigger circuit works with a neat diagram. Design a Schmitt trigger with  $V_{UT} = 2 \text{ V}$ ,  $V_{LT} = -2 \text{ V}$ . Assume  $\pm V_{sat} = \pm 13 \text{ V}$ .

**AKTU 2017-18, Marks 05**

### Answer

Schmitt trigger : Refer Q. 5.11, Page 5-12E, Unit-5.

Numerical :

Given :  $V_{UT} = 2 \text{ V}$ ,  $V_{LT} = -2 \text{ V}$ ,  $\pm V_{sat} = \pm 13 \text{ V}$

To Design : Schmitt trigger.

The procedure is same as Q. 5.13, Page 5-15E, Unit-5.

[Ans.  $R_2 = 100 \Omega$  (Assume),  $R_1 = 550 \Omega$ ]

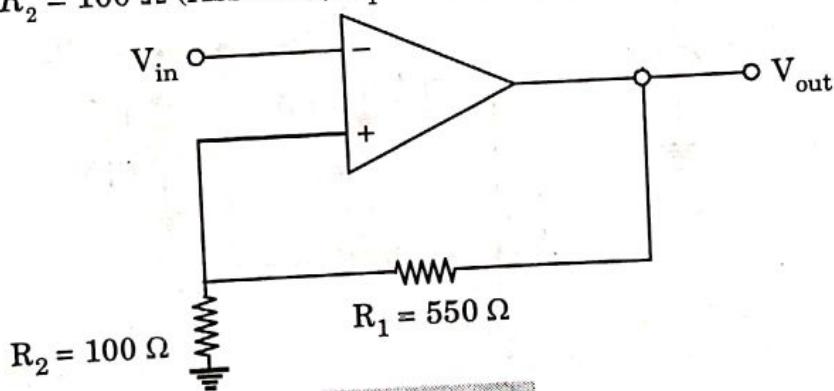


Fig. 5.14.1.

### PART-5

Active Filters : Low Pass, High Pass, Band Pass and Band Stop, Design Guidelines.

### Questions-Answers

Long Answer Type and Medium Answer Type Questions

**Que 5.15.** Classify Active filters and write its advantages with suitable examples.

**Answer**

1. Active filters employ transistors or op-amps in addition to resistors and capacitors.
2. The type of element used dictates the operating frequency range of the filter.

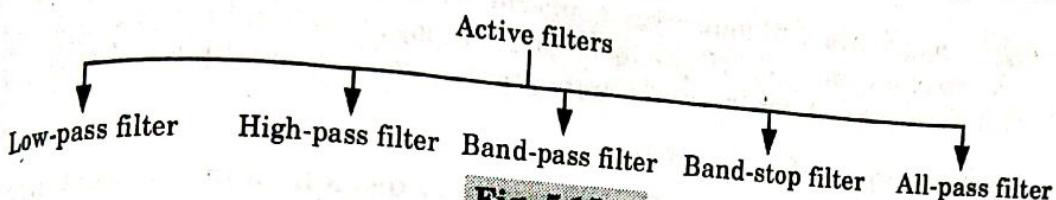
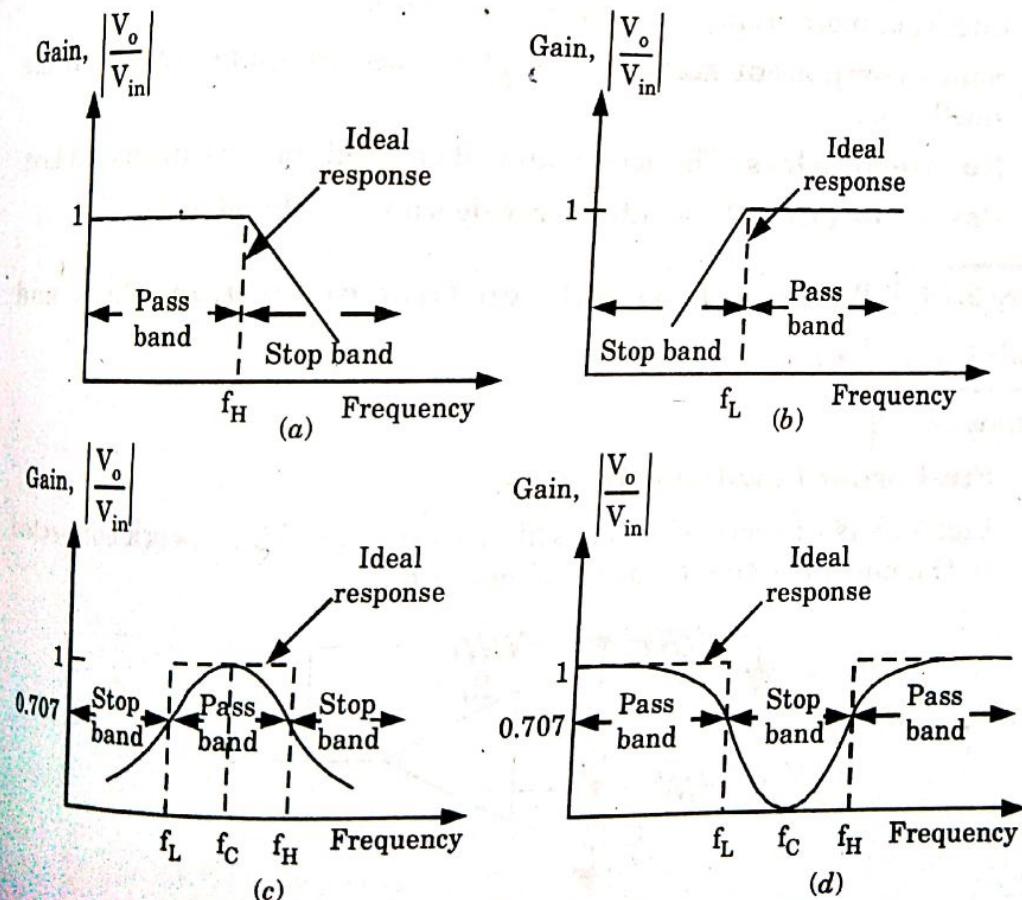
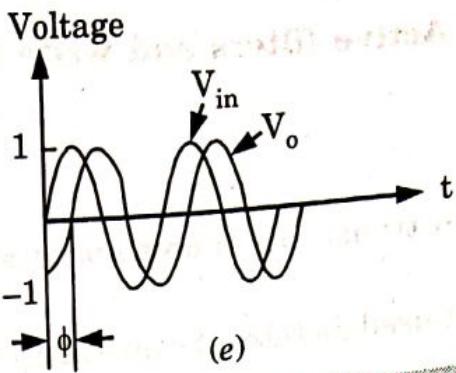


Fig. 5.15.1.

3. Each of these filters uses an op-amp as the active element and resistors and capacitors as the passive elements.
4. Fig. 5.15.2 shows frequency response characteristics of the five types of filters. The ideal response is shown by dashed curves, while the solid lines indicate the practical filter response.





**Fig. 5.15.2. Frequency response of the major active filters :**  
 (a) Low-pass ; (b) High-pass ; (c) Band-pass ; (d) Band-reject ;  
 (e) Phase shift between input and output voltage of an all-pass filter.

#### Advantages of active filters :

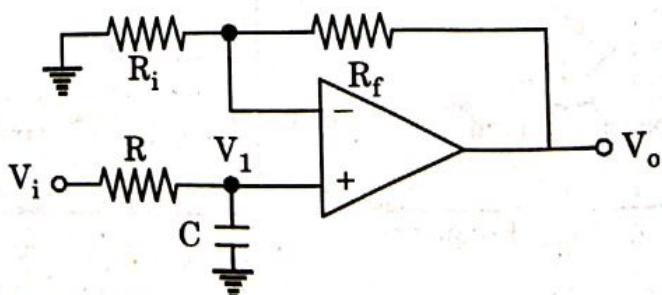
1. **No loading problem :** The op-amp provides a high input resistance and low output resistance. Therefore active filters using op-amp does not cause loading of the source or load.
2. **Flexibility in gain and frequency adjustment :** In active filters, the input signal is not attenuated while passing through filter and thus provides flexibility in gain. In addition, the active filter is easy to tune, therefore easy frequency adjustment is possible.
3. **Low cost :** Due to the absence of inductors in active filters, the active filters are more economical than passive filters.
4. **Small component size :** Active filters use components which are smaller in size.
5. **No insertion loss :** The active filters do not exhibit any insertion loss.
6. **Passband gain :** These filters provide some passband gain.

**Que 5.16.** Write a short note on first order Low-Pass and High-Pass filter.

#### Answer

##### A. First order Low-Pass filter :

1. Fig. 5.16.1 is an active low-pass filter with single  $RC$  network connected to the non-inverting terminal of op-amp.



**Fig. 5.16.1. First order low-pass filter with variable gain.**

2. The input resistor  $R_i$  and feedback resistor  $R_f$  are used to determine the gain of the filter in the passband.

3. Referring to Fig. 5.16.1, the voltage  $V_1$  across the capacitor is

$$V_1 = \frac{V_i}{1 + j2\pi f RC}$$

4. The output voltage  $V_o$  for non-inverting amplifier is

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_1 \quad \dots(5.16.1)$$

5. By substituting  $V_1$  in the eq. (5.16.1), the output voltage  $V_o$  becomes

$$V_o = \left(1 + \frac{R_f}{R_i}\right) \frac{V_i}{1 + j2\pi f RC}$$

$$\frac{V_o}{V_i} = \frac{A}{1 + j\left(\frac{f}{f_H}\right)}$$

or  
where  $V_o/V_i$  is the gain of the low-pass filter which is a function of frequency,  
 $A = 1 + (R_f/R_i)$  is the passband gain of the filter,

$f_H = 1/2\pi RC$  is the high cut-off frequency of the filter.

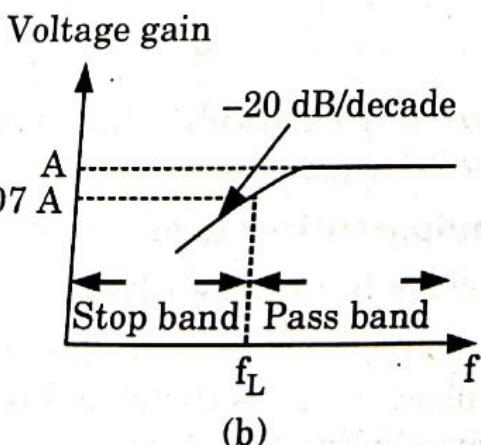
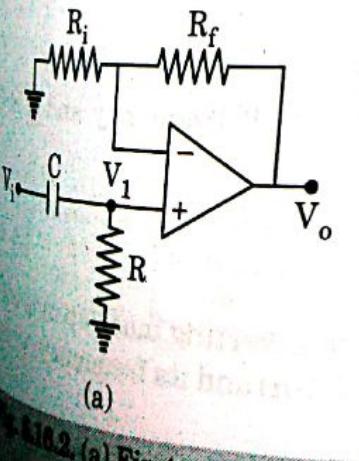
The frequency response of the filter can be determined by using the magnitude of the gain of the low-pass filter, which is expressed as

$$\left|\frac{V_o}{V_i}\right| = \frac{A}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}$$

#### First order High-Pass filter :

The active high-pass filter with a single  $RC$  network connected to non-inverting terminal of the Op-Amps shown in Fig. 5.16.2.

The input resistor  $R_i$  and feedback resistor  $R_f$  are used to determine the gain of the filter in the pass-band.



3. The output voltage  $V_o$  of the first order active high-filter is

$$V_o = \left(1 + \frac{R_f}{R_i}\right) \frac{j2\pi fRC}{1 + j2\pi fRC} V_i$$

4. Therefore, the gain of the filter becomes

$$\frac{V_o}{V_i} = A \left( \frac{j \left( \frac{f}{f_L} \right)}{1 + j \left( \frac{f}{f_L} \right)} \right)$$

where pass-band gain of the filter is  $A = 1 + (R_f/R_i)$ ,  $f$  is the frequency of the input signal and the lower cut-off frequency of the filter is

$$f_L = \frac{1}{2\pi RC}$$

5. The frequency response of the filter is obtained from the magnitude of the filter,

$$\text{That is, } |H(f)| = \left| \frac{V_o}{V_i} \right| = \frac{A \left( \frac{f}{f_L} \right)}{\sqrt{1 + \left( \frac{f}{f_L} \right)^2}} = \frac{A}{\sqrt{1 + \left( \frac{f_L}{f} \right)^2}}$$

**Que 5.17.** Explain Bandpass filters and its types.

**Answer**

1. A bandpass filter passes a particular band of frequencies and attenuates any input frequency outside this pass-band.
2. This filter has a maximum gain at the resonant frequency ( $f_r$ ), which is defined as

$$f_r = \sqrt{f_H f_L}$$

The figure of merit or quality factor  $Q$ , is given by

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{B}$$

where  $B$  is bandwidth,  $f_H$  is higher cut-off frequency and  $f_L$  is lower cut-off frequency.

**Bandpass filter is of two types :**

i. **Narrow bandpass filter :**

1. The narrow bandpass filter using one inverting mode op-amp with two feedback paths is shown in Fig. 5.17.1(a) and its frequency response is shown in Fig. 5.17.1(b).
2. The resonant frequency can be changed by adjusting  $R_f$  without changing the bandwidth or gain.

3. The bandwidth  $B$  is determined by resistor  $R$  and the two matched capacitors  $C$  as given by

$$B = \frac{0.1591}{RC}$$

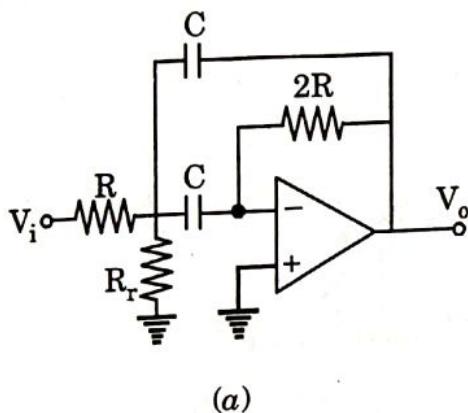
where  $B = f_r/Q$ .

4. The adjustable resistor  $R_r$  is determined by

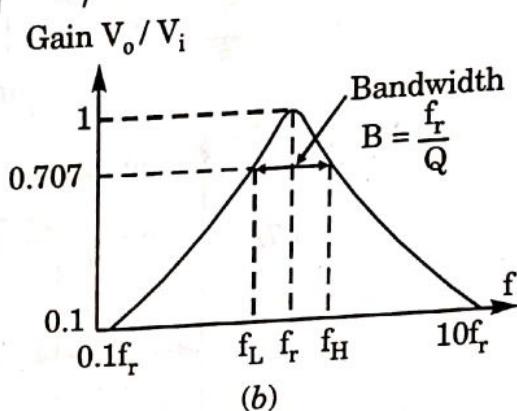
$$R_r = \frac{R}{2Q^2 - 1}$$

5. Its resonant frequency  $f_r$  is determined from

$$f_r = \frac{0.1125}{RC} \sqrt{1 + \frac{R}{R_r}}$$



(a)

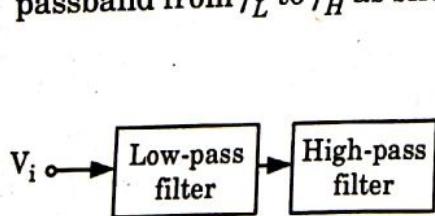


(b)

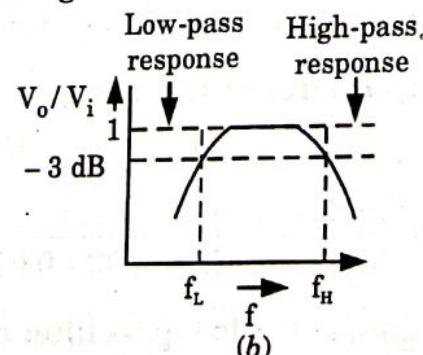
**Fig. 5.17.1.** (a) Narrow bandpass filter circuit and  
(b) Its frequency response.

## ii. Wide bandpass filter :

1. A bandpass filter can be constructed simply by connecting low-pass and high-pass filters in cascade as shown in Fig. 5.17.2(a).
2. Here the low-pass circuit will pass all frequencies up to its cut-off frequency  $f_H$ , while the high-pass circuit will block all frequencies below its cut-off frequency  $f_L$  provided  $f_H > f_L$  i.e.,  $f_H$  must be at least 10 times  $f_L$ .
3. The cut-off frequencies of the low and high-pass sections must have the equal passband gain. Hence, the combination gives a filter with passband from  $f_L$  to  $f_H$  as shown in Fig. 5.17.2(b).



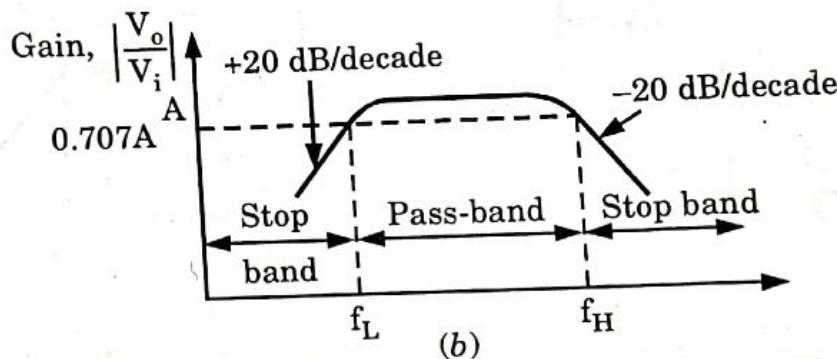
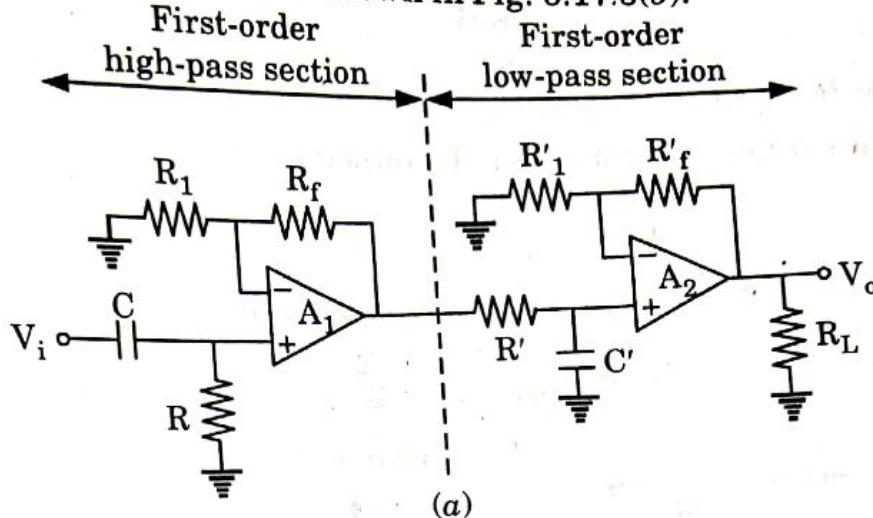
(a)



(b)

**Fig. 5.17.2.** (a) Cascaded low-pass and high-pass filters acting as bandpass filter (b) Frequency response of the bandpass filter.

4. For realizing a  $\pm 20$  dB/decade bandpass filter, first order high-pass and first order low-pass sections are cascaded as shown in Fig. 5.17.3(a). Its frequency response is shown in Fig. 5.17.3(b).



**Fig. 5.17.3. (a) Wide bandpass filter and  
(b) its frequency response.**

**Que 5.18.** Design a Wide Bandpass filter with lower cut-off frequency  $f_L = 200$  Hz, higher cut-off frequency  $f_H = 1$  kHz and a Pass-band gain = 4.

**AKTU 2016-17, Marks 10**

**Answer**

Given :  $f_L = 200$  Hz;  $f_H = 1$  kHz;  $A = 4$

To Design : Wide bandpass filter.

**A. Components of the low-pass filter :**

1. Let  $C_L' = 0.01 \mu\text{F}$

2.  $R_L' = \frac{1}{2\pi f_H C_L'} = \frac{1}{2\pi \times 1000 \times 0.01 \times 10^{-6}} = 15.91 \text{ k}\Omega$

3. The gain of the low-pass filter can be considered half of the pass-band gain,

$$A_{LF} = 2$$

$$2 = 1 + \frac{R_{FL}}{R_L}$$

$$R_{FL} = R_L = 10 \text{ k}\Omega \text{ (assume)}$$

**B. Components of the high-pass filter :**

1. Let

$$C_H' = 0.05 \mu\text{F}$$

$$2. R_H' = \frac{1}{2\pi f_L C_H'} = \frac{1}{2\pi \times 200 \times 0.05 \times 10^{-6}}$$

$$R_H' = 15.91 \text{ k}\Omega$$

3. The gain = 2

$$1 + \frac{R_{FH}}{R_H} = 2$$

$$R_{FH} = R_H = 10 \text{ k}\Omega \text{ (assume)}$$

$$4. \text{ Quality factor, } Q = \frac{f_c}{f_H - f_L} = \frac{\sqrt{f_H f_L}}{f_H - f_L}$$

$$= \frac{\sqrt{200 \times 1000}}{800} = 0.56$$

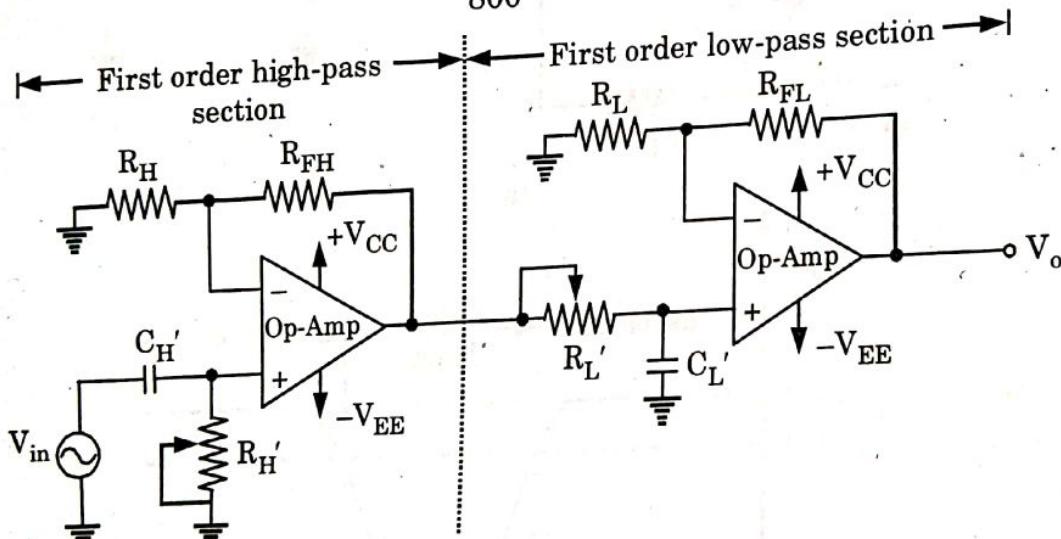


Fig. 2.16.1

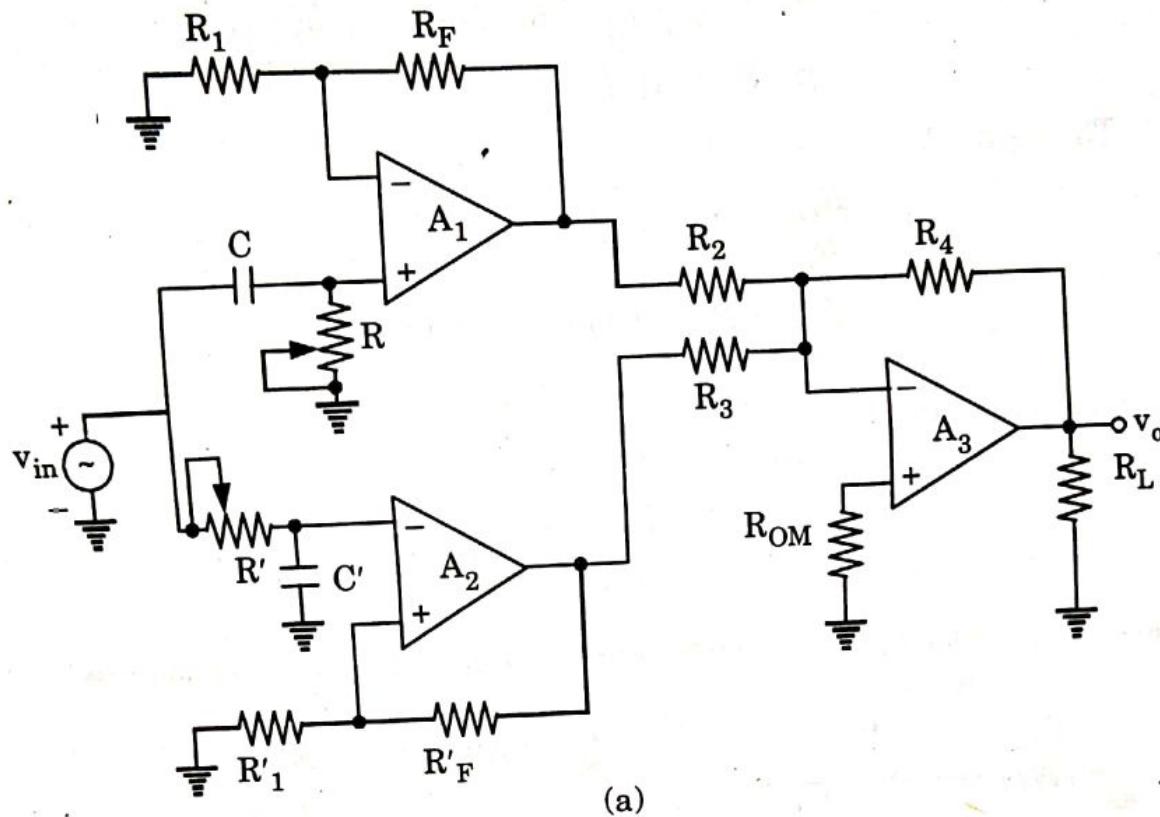
**Que 5.19.** Discuss band reject filter and its types.

**Answer**

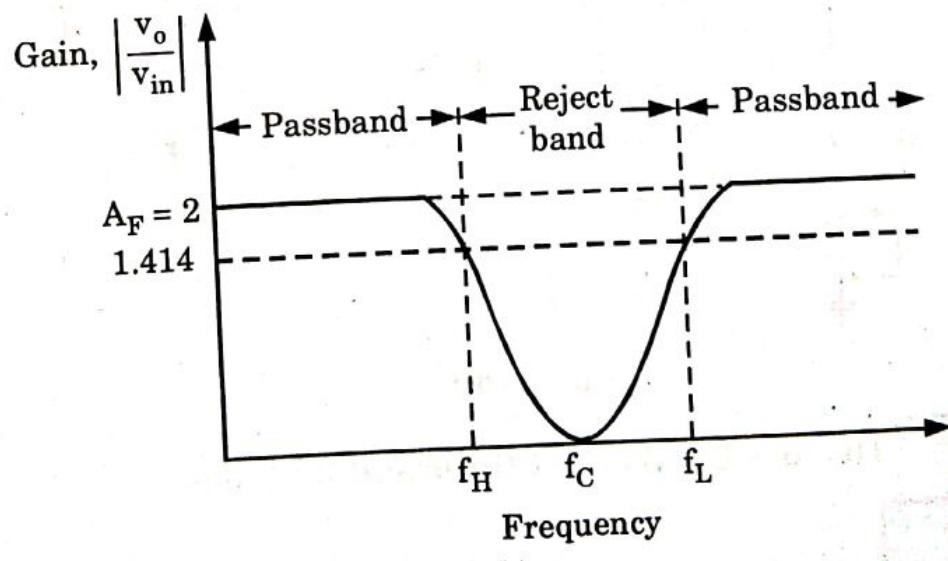
1. The band-reject filter is also called a band-stop or band-elimination filter.
2. In this filter, frequencies are attenuated in the stopband while they are passed outside this band.
3. Band reject filters are of two types.

i. **Wide band-reject filter :**

- Fig. 5.19.1(a) shows a wide band-reject filter using a low-pass filter, high-pass filter, and a summing amplifier.
- To realize a band-reject response, the low cut-off frequency  $f_L$  of the high-pass filter must be larger than the high cut-off frequency  $f_H$  of the low-pass filter.



(a)



(b)

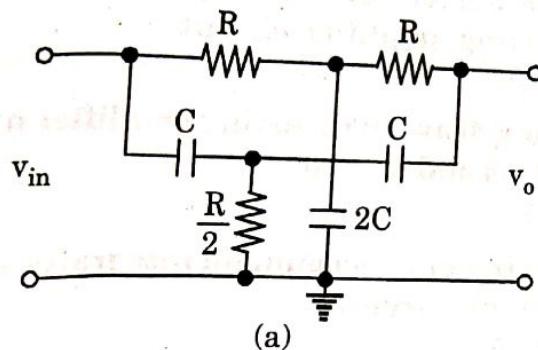
**Fig. 5.19.1. Wide band-reject filter.**

ii. **Narrow band-reject filter :**

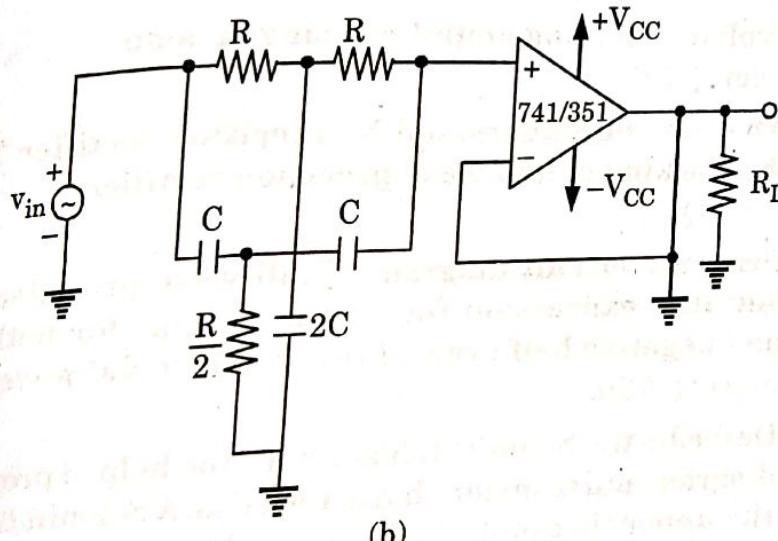
- The narrow band-reject filter, often called the notch filter, is commonly used for the rejection of a single frequency such as 60-Hz.

2. The most commonly used notch filter is the twin-T network is shown in Fig. 5.19.2(a).
3. One T network is made up of two resistors and a capacitor, while the other uses two capacitors and a resistor.
4. The notch-out frequency is the frequency at which maximum attenuation occurs; it is given by

$$f_N = \frac{1}{2\pi RC}$$



(a)



(b)

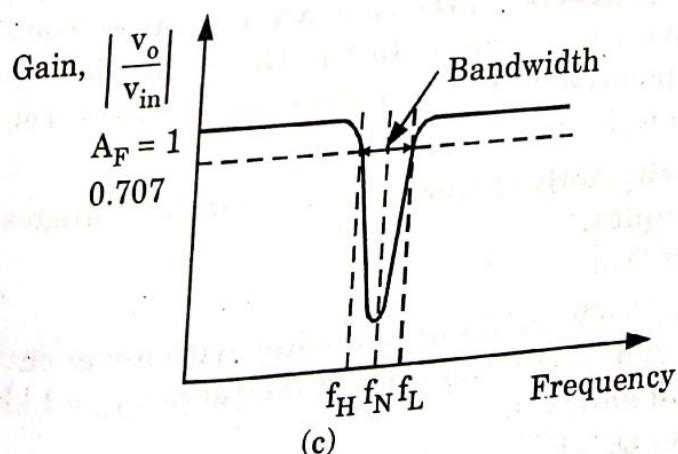


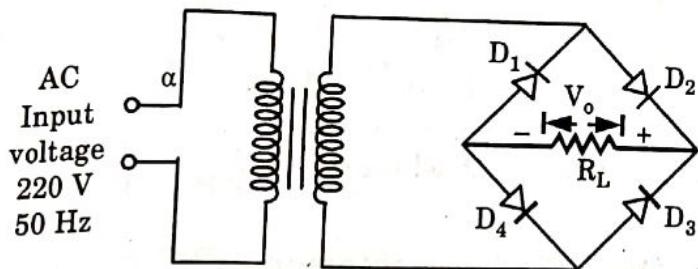
Fig. 5.19.2.



## Diode Circuits and Amplifier Models (2 Marks Questions)

- 1.1.** Draw a neat diagram of a full wave rectifier bridge circuit using diode.

**Ans:**

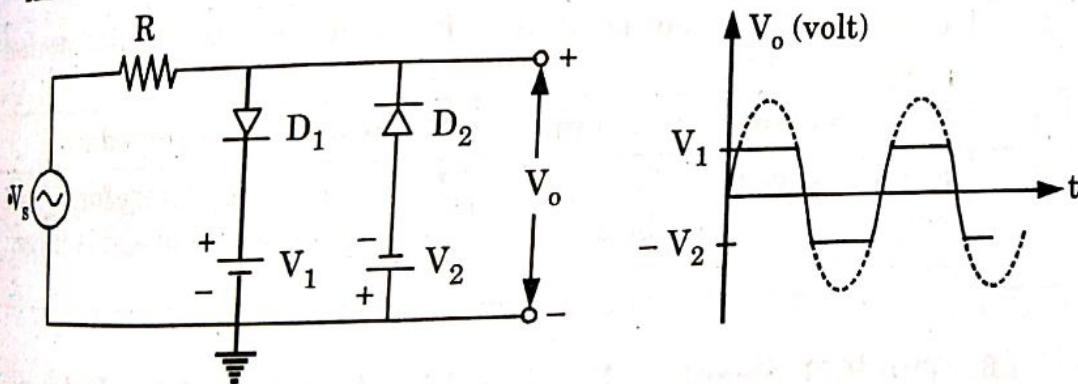


**Fig. 1.**

- 1.2.** Draw the double ended diode clipper circuit.

**AKTU 2015-16, Marks 02**

**Ans:**



**Fig. 2.**

- 1.3.** Write gain parameter and ideal characteristics of transconductance amplifier. Also draw the transconductance model.

**Ans:** Gain parameter :  
Short circuit transconductance,

$$G_m = \left. \frac{i_o}{v_i} \right|_{v_o=0} \quad (\text{A/V})$$

## Ideal characteristics :

$$R_i = \infty, R_o = \infty$$

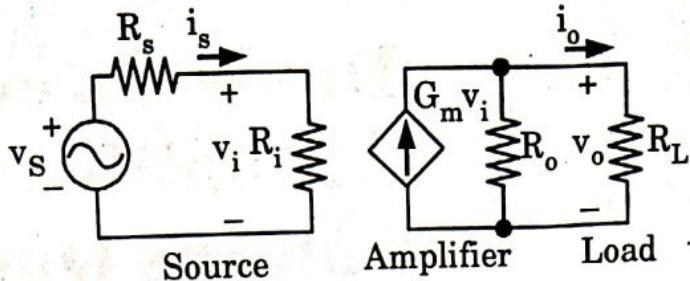


Fig. 3. Transconductance model.

**1.4. Establish the relationship between  $I_{CEO}$  and  $I_{CBO}$  of a BJT.**

**Ans:** The collector current can be expressed as

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO}$$

The collector current when  $I_B = 0$ ,  $I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$

**1.5. Enlist the difference between JFET and BJT.**

**Ans:**

S.No.	JFET	BJT
1.	Its operation depends only on majority carriers, so it is a unipolar device.	Its operation depends on both majority and minority carriers, so it is a bipolar device.
2.	It is a voltage controlled device.	It is a current controlled device.
3.	It has high input impedance.	It has low input impedance.
4.	Small in size, therefore space requirement on board is small.	Large in size, therefore space requirement on board is large.

**1.6. The BJT circuitry has  $I_C = 10 \text{ mA}$  and  $\alpha = 0.98$ . Determine the value of  $I_E$ .**

**Ans:**

Given :  $\alpha = 0.98$ ,  $I_C = 10 \text{ mA}$

To Find :  $I_E$

We know that,  $\alpha = I_C/I_E$

$$\therefore I_E = \frac{10 \times 10^{-3}}{0.98} = 10.2 \text{ mA}$$

**1.7. Derive the relation between  $\alpha$  and  $\beta$  for BJT.**

AKTU 2017-18, Marks 02

AKTU 2016-17, Marks 02

...(1.7.1)

**Ans:** We know that,  $I_E = I_C + I_B$ Dividing eq. (1.7.1) both sides by  $I_C$ , we get

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

But we know that  $\beta = I_C/I_B$  and  $\alpha = I_C/I_E$ 

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta} = \frac{\beta + 1}{\beta}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

**1.8. If  $\alpha$  of a transistor changes from 0.981 to 0.987, find the percentage change in  $\beta$ .**

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**Ans:** Here,

$$\beta_1 = \frac{\alpha_1}{1 - \alpha_1} = \frac{0.981}{1 - 0.981} = 51.632$$

$$\beta_2 = \frac{\alpha_2}{1 - \alpha_2} = \frac{0.987}{1 - 0.987} = 75.92$$

$$\% \text{ change in } \beta = \frac{\beta_2 - \beta_1}{\beta_1} = \frac{75.92 - 51.632}{51.632} = 47.04 \%$$

**1.9. Explain with proper reason the use of Emitter Follower.**

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**Ans:** The Emitter Follower is used as a voltage buffer for connecting a high resistance source to a low resistance load.**1.10. What is transconductance in FET? What is the relationship between  $g_m$  and  $g_{mo}$ ?**

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**Ans:** The control that the gate voltage has over drain current is measured by transconductance  $g_m$ . It is simply the slope of transfer characteristics.

$$g_m = \left( \frac{\Delta I_D}{\Delta V_{GS}} \right), \text{ when } V_{DS} \text{ held constant}$$

The unit of  $g_m$  is siemens (mho).

1.11. Draw the small signal  $\pi$ -model of BJT.

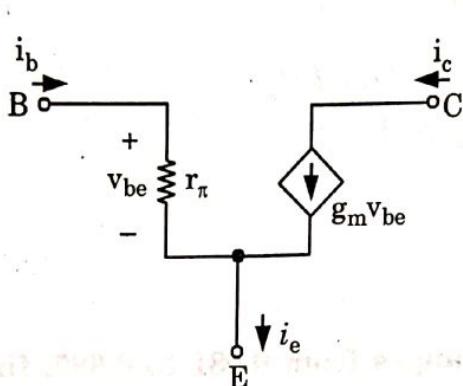
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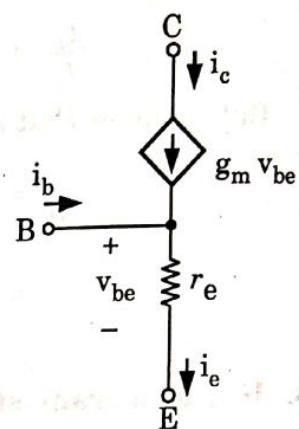
Draw hybrid -  $\pi$  model and  $T$ -model equivalent of  $npn$  transistor.

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Ans:



(a) Hybrid- $\pi$  model



(b)  $T$ -model

Fig. 4.

1.12. A  $CE$  amplifier is having  $I_C = 1 \text{ mA}$ ,  $\beta_o = 100$ ,  $V_A = 100 \text{ V}$ . Calculate  $g_m$ ,  $r_\pi$ ,  $r_o$ .

Ans:

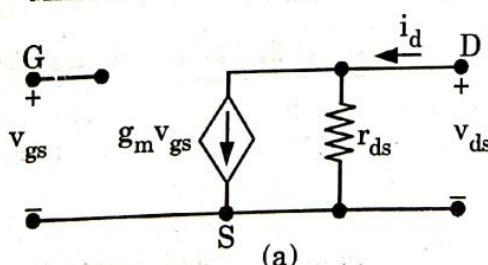
$$g_m = \frac{I_C}{V_T} = \frac{1 \times 10^{-3}}{25 \times 10^{-3}} = 40 \text{ mA/V}$$

$$r_\pi = \frac{\beta_o}{g_m} = \frac{100}{40 \times 10^{-3}} = 2.5 \text{ k}\Omega$$

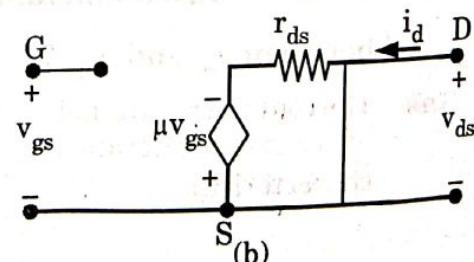
$$r_o = \frac{V_A}{I_C} = \frac{100}{1 \times 10^{-3}} = 100 \text{ k}\Omega$$

1.13. Draw small signal model of FET.

Ans:



(a)



(b)

Fig. 5. Small-signal model for the CS FET.





## Multistage Amplifiers and Feedback Topologies (2 Marks Questions)

**2.1. Define frequency response.**

**Ans.** The curve drawn between voltage gain and frequency of an amplifier is known as frequency response.

**2.2. Draw the frequency response of RC coupled amplifier.**

**Ans.**

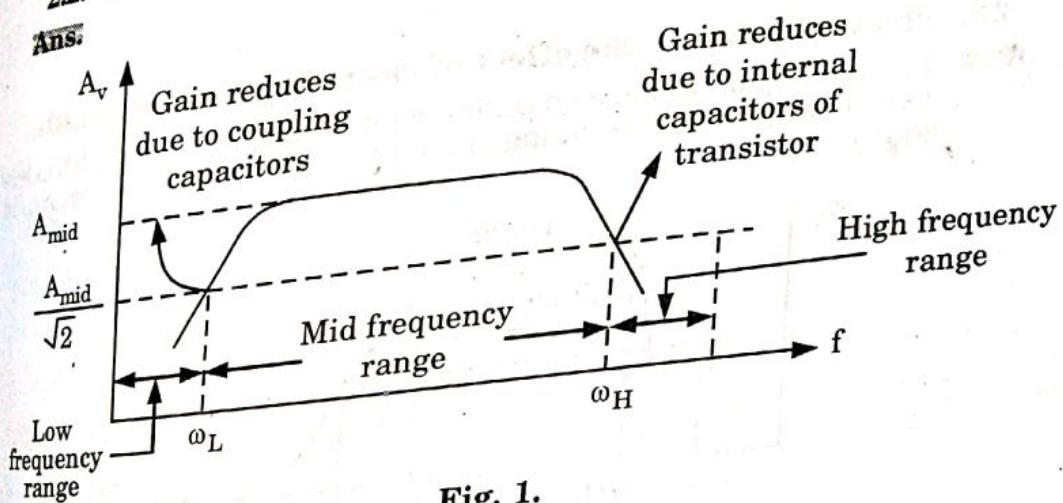


Fig. 1.

**2.3. What is the necessity of frequency response analysis ?**

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**Ans.** Frequency response directly led to the idea of filtering of signals using LTI systems. One important application involves the idea of frequency selective filtering.

**2.4. What are the requirements of a multistage amplifier ?**

**Ans.**

1. Gain should be sufficiently large.
2. Input impedance should match with source impedance.
3. Output impedance should match with load impedance.
4. Bandwidth should be adequately large.

**2.5. What is RC coupled amplifier ?**

**Ans:** In *RC* coupling, a resistor and a capacitor are used as coupling device. The capacitor connects the output of one stage to the input of next stage to pass AC signal and to block the DC bias voltages. The amplifier using *RC* coupling is called the *RC* coupled amplifier.

#### 2.6. What are the advantages of *RC* coupled amplifier ?

**Ans:**

1. Wide frequency response (large bandwidth).
2. It is the most convenient coupling.
3. Due to the coupling capacitor  $C_c$ ,  $Q$  point is unchanged.
4. The distortion in the output is low.

#### 2.7. What are the disadvantages of *RC* coupled amplifier ?

**Ans:**

1. Gain reduces at low frequencies due to coupling capacitors.
2. Ageing can make these amplifiers noisy.
3. No impedance matching.
4. Overall voltage gain is less.

#### 2.8. Show with figure the effect of cascading on bandwidth.

**Ans:** In cascading multistage amplifier, gain is high and bandwidth is less as compare to non-cascading or single stage amplifier, as shown in Fig. 2.

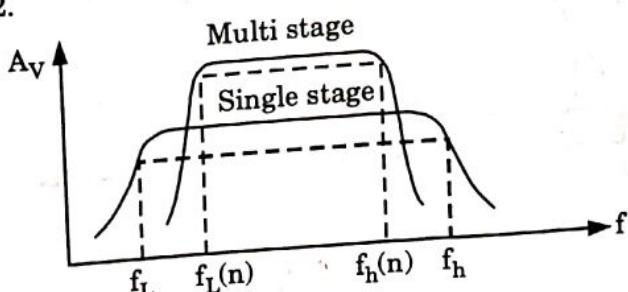


Fig. 2.

#### 2.9. What is cascode amplifier ?

**Ans:** A common gate (common-base) amplifier stage in cascade with a common-source (common-emitter) amplifier stage is known as the cascode configuration.

#### 2.10. Compare different amplifier classes.

S.No.	Class	Class-A	Class-B	Class-C	Class-AB
1.	Operating cycle	360°	180°	Less than 180°	180° to 360°
2.	Position of Q	Centre	on x-axis	Below x-axis	Above x-axis
3.	Efficiency	25% or 50%	78.5%	High (almost 100%)	50% to 78.5%
4.	Distortion	Absent	Present more than Class-A	Highest	Present less than Class-B

- Ans:** Name the four basic feedback topologies used in amplifiers ?
- The four basic feedback topologies are as follows :
1. Series-shunt feedback (voltage amplifier)
  2. Shunt-series feedback (current amplifier)
  3. Series-series feedback (transconductance amplifier)
  4. Shunt-shunt feedback (transresistance amplifier)

- Ans:** Compare different types of feedback network based on input and output resistance.

S.No.	Characteristics	Types of feedback network			
		voltage series	voltage shunt	current series	current shunt
1.	Input resistance	increases by a factor of $(1 + A\beta)$	decreases by a factor of $(1 + A\beta)$	increases by a factor of $(1 + A\beta)$	decreases by a factor of $(1 + A\beta)$
2.	Output resistance	decreases by a factor of $(1 + A\beta)$	decreases by a factor of $(1 + A\beta)$	increases by a factor of $(1 + A\beta)$	increases by a factor of $(1 + A\beta)$

- Ans:** Mention few properties of series-shunt and shunt-series feedback amplifiers.

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**Ans:** Properties of series-shunt feedback amplifier :

1. Increase the input resistance with feedback.
2. Decrease the output resistance with feedback.

**Properties of shunt-series feedback amplifier :**

1. Decrease the input resistance with feedback.
2. Increase the output resistance with feedback.

- 2.14. An amplifier has a midband gain of 125 and a bandwidth of 250 kHz. If 4% negative feedback is introduced, find the new bandwidth.

**Ans:**

$$BW_f = (1 + A\beta) BW$$

$$= (1 + 125 \times 0.04) \times 250 \times 10^3 \text{ Hz} = 262.5 \text{ kHz}$$

- 2.15. An amplifier with voltage gain of 60 dB uses  $\frac{1}{20}$  of its output in negative feedback. Calculate the gain with feedback in dB.

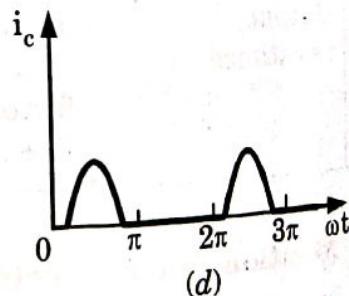
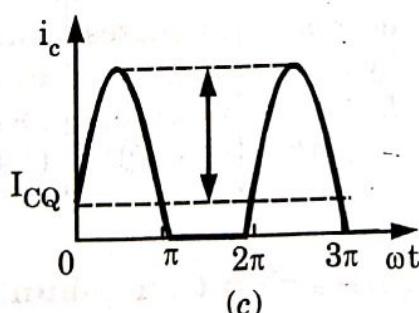
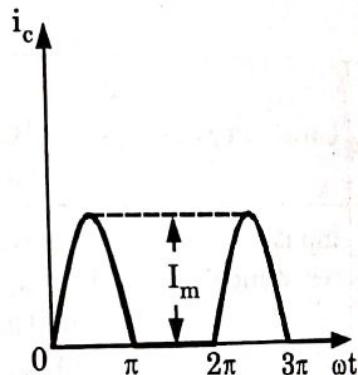
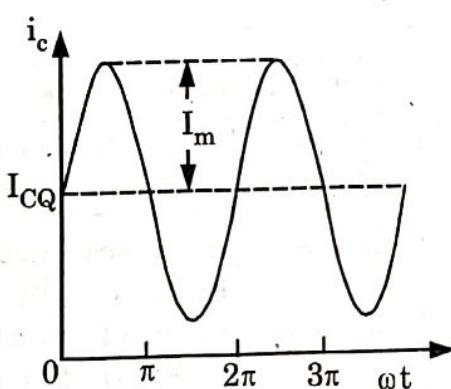
**Ans.** Given,

$$A_{\text{dB}} = 60 \text{ dB} \Rightarrow A = 1000$$

$$A_f = \frac{A}{1 + A\beta} = \frac{1000}{1 + \frac{1}{20} \times 1000} = \frac{60}{4} = 19.6$$

$$|A_f|_{\text{dB}} = 20 \log 19.6 = 25.84 \text{ dB}$$

- 2.16. Draw the waveforms for class A, B, AB and C amplifier.

**Ans.**

**Fig. 3.** Collector current waveforms for transistors operating in (a) Class A (b) Class B, (c) Class AB, and (d) Class C amplifier stages.



# 3

UNIT

## Oscillators (2 Marks Questions)

**3.1. What is an oscillator ?**

**Ans.** An oscillator is a device which generates an alternating voltage. It generates an AC output signal without requiring any externally applied input signal. The oscillator converts DC energy into AC energy. Feedback used in oscillator is positive feedback.

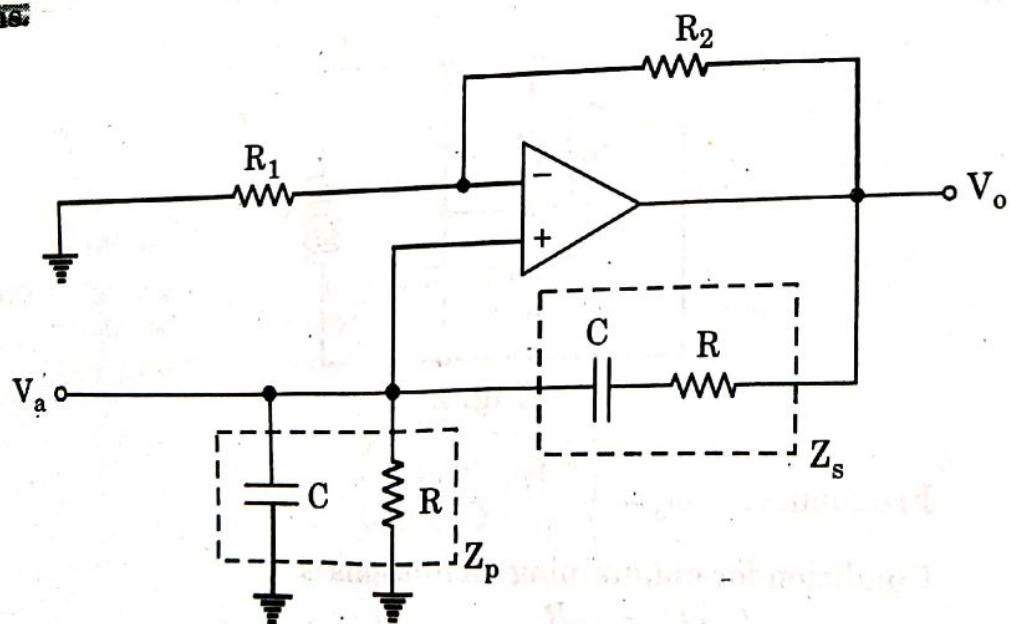
**3.2. Explain Barkhausen criterion. [AKTU 2016-17, Marks 02]**

**Ans.** Barkhausen criterion defines two basic requirements for oscillations :

1. Total phase shift in the closed loop is  $0^\circ$  or  $360^\circ$ .
2. The magnitude of loop gain i.e.,  $|A\beta| = 1$ .

**3.3. Draw the circuit of a Wien bridge oscillator and give condition for sustained oscillations.**

**Ans.**



**Fig. 1. Wien bridge oscillator.**

To obtain sustained oscillation at  $\omega_o = 1/RC$ , we should set the magnitude of the loop gain to unity. This can be achieved by selecting,

$$R_2/R_1 = 2$$

**3.4. List some advantages and disadvantages of Wien bridge oscillator.**

**Ans:** Advantages :

1. Good frequency stability.
2. Frequency of oscillations can be changed.
3. A very good quality of sine wave can be obtained at the oscillator output.

**Disadvantages :**

Oscillation frequency is dependent only on the values of  $R$  and  $C$  components.

**3.5. Write the advantages and disadvantages of phase-shift oscillator.**

**Ans:** Advantages :

1. It does not require transformers or inductors.
2. It can be used to produce very low frequencies.
3. The circuit provides good frequency stability.

**Disadvantages :**

1. It is difficult for the circuit to start oscillations as feedback is generally small.
2. The circuit gives small output.

**3.6. Draw the circuit of Colpitts oscillators and also write its frequency and condition of maintaining oscillations.**

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**Ans:**

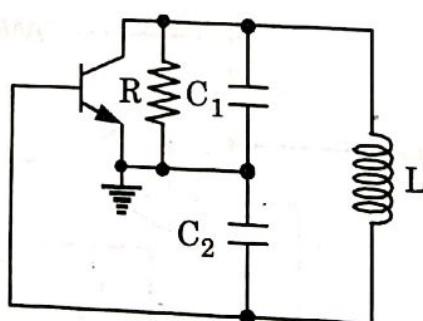


Fig. 2.

$$\text{Frequency, } \omega_o = 1/\sqrt{L \left( \frac{C_1 C_2}{C_1 + C_2} \right)}$$

Condition for maintaining oscillations is

$$C_2/C_1 = g_m R$$

**3.7. What is the drawback of Colpitts oscillator ? Name the oscillator to remove this drawback.**

**Ques.** The drawback of Colpitts oscillator is that its frequency stability is very poor.  
**Ans.** Clapp oscillator is used to removes this drawback.

**Ques.** What do you mean by self-limiting oscillators ?

**Ans.** LC tuned oscillators utilize the non-linear  $i_C - v_{BE}$  characteristics of the BJT for amplitude control. Thus, these LC tuned oscillators are known as self-limiting oscillators.

**Ques.** Which oscillator is well suited for the generation of wide range audio frequency sine waves ?

**Ans.** Wien bridge oscillator is well suited for the generation of wide range audio frequency sine waves.

**Ques.** How monostable multivibrator is used ?

**Ans.** Monostable multivibrator has one stable state and the other is quasi-stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal.

**Ques.** Draw the circuit diagram of triangular waveform generator.

**Ans.**

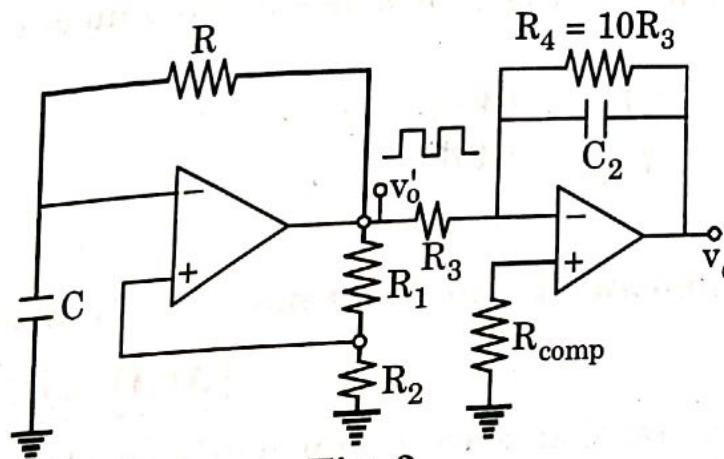


Fig. 3.

**Ques.** Why the monostable multivibrator also called as gating circuit ?

**Ans.** The monostable multivibrator is called as gating circuit as it generates a rectangular waveform at definite time and thus could be used to gate parts of a system.





## Current Mirror and Op-Amp Design (2 Marks Questions)

### 4.1. What is current steering ?

**Ans:** On a IC chip with a number of amplifier stages, a constant DC current (called a reference current) is generated at one location and then replicated at various other locations for biasing the various amplifier stages through a process known as current steering.

### 4.2. What is current transfer ratio ?

**Ans:** The relationship between the  $I_o$  and  $I_{REF}$  by the ratio of the aspect ratio of transistor is known as current gain or current transfer ratio.

$$\frac{I_o}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

### 4.3. What is meant by the term matched transistors ?

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**Ans:** If the two transistors are designed to be equal i.e., same size, same orientation, same surrounding and have identical values of saturation current, current gain and early voltage, then this pair of transistor is referred as matched transistors.

### 4.4. What is the advantage of Widlar current source over Wilson current source ?

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**Ans:**

1. It requires less chip area.
2. The output resistance  $R_o$  is higher than basic current source, this is due to the emitter resistance  $R_E$ .

### 4.5. What are the requirements of good current source ?

**Ans:**

1. The output current  $I_o$  should not depend upon  $\beta$ .
2. The output resistance of the current source should be high.

#### 4.6. What is the minimum output voltage for proper operation of MOSFET current mirror?

The current source will operate properly with an output voltage  $V_o$  greater than  $V_{OV}$ , which is a few tenths of a volt.

$$V_o \geq V_{GS} - V_t$$

$$V_o \geq V_{OV}$$

#### 4.7. Draw the output characteristics of MOS current source.

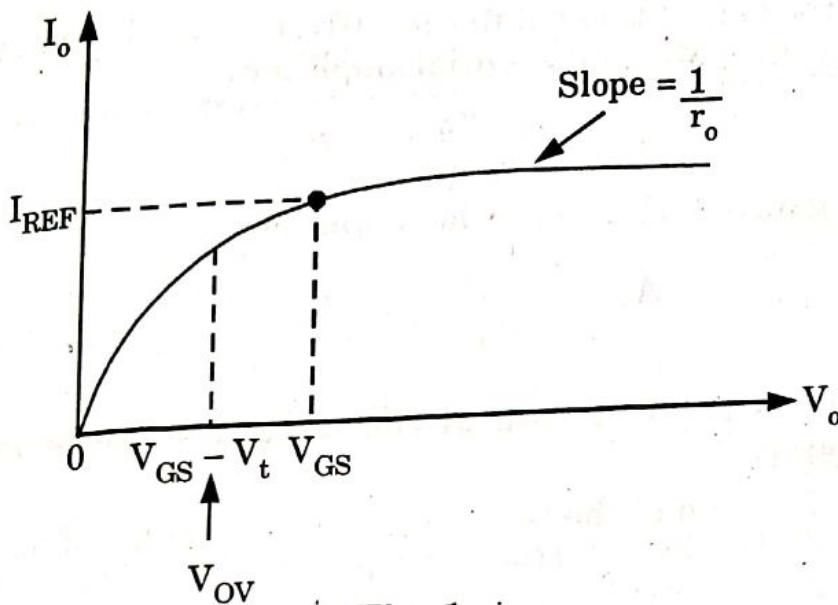


Fig. 1.

#### 4.8. Define ICMR (input common-mode range). What is the value of $v_{CM \max}$ and $v_{CM \min}$ of MOS amplifier?

Ans: ICMR is the range of  $v_{CM}$  over which the differential pair operates properly.

The maximum value of  $v_{CM}$  is,

$$v_{CM \max} = V_t + V_{DD} - \frac{I}{2} R_{DD}$$

The minimum value of  $v_{CM}$  is,

$$v_{CM \min} = -V_{SS} + V_{CS} + V_t + V_{OV}$$

#### 4.9. What is meant by common-mode rejection ratio (CMRR)?

Ans: The ability of a differential amplifier to reject a common mode signal is expressed by its common mode rejection ratio CMRR. CMRR is defined as the ratio of the differential voltage gain  $A_d$  to the common mode voltage gain  $A_{cm}$  i.e.,

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right|$$

#### 4.10. What is the ICMR range of BJT differential amplifier?

**Ans.** 1. The maximum value of  $v_{CM \max}$  is,

$$v_{CM \max} = V_C + 0.4 = V_{CC} - \frac{\alpha I}{2} R_C + 0.4$$

2. The minimum value of  $v_{CM \min}$  is,

$$v_{CM \min} = -V_{EE} + V_{CS} + V_{BE}$$

**4.11. Write the differential voltage gain of MOS and BJT differential amplifier.**

**Ans.** For the output taken differentially, the gain becomes,

1. The gain of MOS differential amplifier is,

$$A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

2. The gain of BJT differential amplifier

$$A_d = \frac{v_{c2} - v_{c1}}{v_{id}} = g_m R_C$$

**4.12. What is the function of the output stage or last stage of op-amp ?**

**Ans.** The function of the last stage or output stage of an op-amp is to supply the load current and provide low output impedance. It should also provide a large output voltage saving ideally the total supply voltage i.e.,  $V_{CC} + V_{EE}$ .

**4.13. What is the role of coupling capacitor ( $C_c$ ) in IC-741 internal circuit ?**

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**Ans.** The role of coupling capacitor ( $C_c$ ) in IC- 741 internal circuit is to compensate frequency using the Miller compensation techniques. Coupling capacitor ( $C_c$ ) is connected at the stage-II feedback path.

**4.14. How the effect of input bias current in non-inverting amplifier is compensated ?**

**Ans.** The effect of input bias current in a non-inverting amplifier is compensated by placing a compensating resistor  $R_{comp}$  in series with the input signal  $V_i$ .

**4.15. Why the bias circuit is used ?**

**Ans.** The bias circuit is used to provide proportional current in the collector of transistor.



# Op-amp Applications (2 Marks Questions)

**5.1. Define operational amplifier.**

**ANS:** An operational amplifier or op-amp is a high gain, direct coupled amplifier. It is designed to perform mathematical operations (addition, subtraction, integration, differentiation etc.).

**5.2. List of ideal characteristics of op-amp.**

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**OR**

**Write the characteristics of an ideal op-amp.**

**AKTU 2016-17, Marks 02**

- ANS:**
1. Input impedance is infinite.
  2. Output impedance is zero.
  3. Infinite CMRR.
  4. Bandwidth is infinite.
  5. Open loop gain is infinite.

**5.3. Sketch the circuit of op-amp as an integrator and differentiator.**

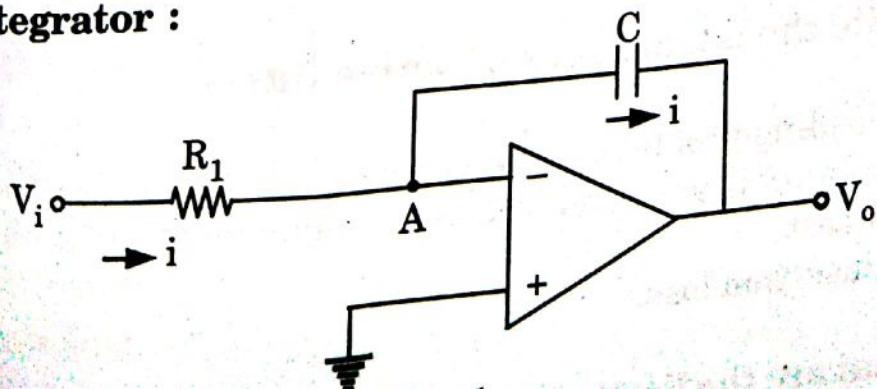
**AKTU 2017-18, Marks 02**

**OR**

**Derive the circuit of integrator using an ideal op-amp.**

**AKTU 2016-17, Marks 02**

**ANS: Integrator :**



**Fig. 1.**

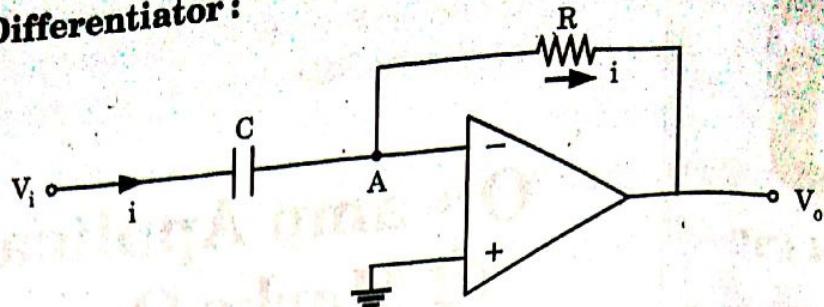
**Differentiator:**

Fig. 2.

**5.4. Why is integrator preferred over differentiator ?**

**Ans.** Integrator is preferred over differentiator for analog computers as the gain of integrator decreases with increase in frequency and hence signal to noise ratio of integrator is higher than that of differentiator.

**5.5. A non-inverting amplifier circuit is capable of providing a voltage gain of 15. Assuming ideal op-amp and  $R_1$  as  $1.3\text{ k}\Omega$ , calculate the feedback resistance.****Ans.**

$$\text{Given : } A_V = 15, R_1 = 1.3\text{ k}\Omega$$

**To Find :**  $R_f$ .

$$A_V = \left( 1 + \frac{R_f}{R_1} \right)$$

$$15 = 1 + \frac{R_f}{1.3 \times 10^3}$$

$$\frac{R_f}{1.3 \times 10^3} = 14$$

$$R_f = 14 \times 1.3 \times 10^3 = 18.2\text{ k}\Omega$$

**5.6. What are the applications of precision diode ?****Ans.**

- i. Half-wave rectifier
- ii. Full-wave rectifier
- iii. Peak value detector
- iv. Clipper
- v. Clamper

**5.7. Write the advantages of active filters.****Ans.**

- i. No loading problem.
- ii. Flexibility in gain and frequency adjustment.
- iii. Low cost.
- iv. No insertion loss.

**5.8. What are the limitations of active filters over passive filters ?**

1. The design of active filter becomes costly for high frequencies.
2. Active filters require dual polarity DC power supply whereas passive filters do not.

**5.9. Design a multiple feedback narrow bandpass filter with  $f_c = 1 \text{ kHz}$ ,  $Q = 3$  and  $A = 10$ .**

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**Ans:**

Given :  $f_c = 1 \text{ kHz}$ ,  $Q = 3$  and  $A = 10$

To Design : Multiple feedback narrow bandpass filter.

Let

$$C_1 = C_2 = C = 0.01 \mu\text{F}$$

$$R_1 = \frac{Q}{2\pi f_c C A} = \frac{3}{(2\pi)(10^3)(10^{-8})(10)} = 4.77 \text{ k}\Omega$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A)} = \frac{3}{(2\pi)(10^3)(10^{-8})[2(3)^2 - 10]} = 5.97 \text{ k}\Omega$$

$$R_3 = \frac{Q}{\pi f_c C} = \frac{3}{(\pi)(10^3)(10^{-8})} = 95.5 \text{ k}\Omega$$

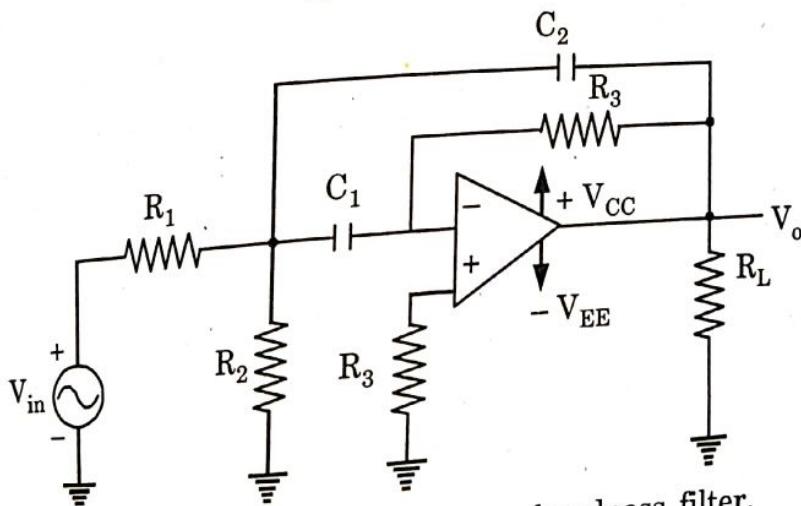


Fig. 3. Multiple feedback narrow bandpass filter.

**5.10. For a first order Butterworth high pass filter, evaluate the value of  $R$  if  $C = 0.0047 \mu\text{F}$  and  $f_c = 10 \text{ kHz}$ .**

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**Ans:**

Given :  $C = 0.0047 \mu\text{F}$ ,  $f_c = 10 \text{ kHz}$

To Find :  $R$ .

$$\text{We know that, } f_c = \frac{1}{2\pi RC}$$

Therefore,  $R = \frac{1}{2\pi f_c C} = \frac{1}{2\pi(10 \times 10^3) \times 47 \times 10^{-10}} = 3.39 \text{ k}\Omega$

- 5.11. Show the relationship between  $K$ ,  $Q$  and bandwidth in the twin-T notch filter.

**Ans.**  $Q = \frac{f_o}{\text{BW}} = \frac{1}{4(1 - K)}$

As  $K$  approaches unity,  $Q$ -Factor becomes very large and BW approaches 0.

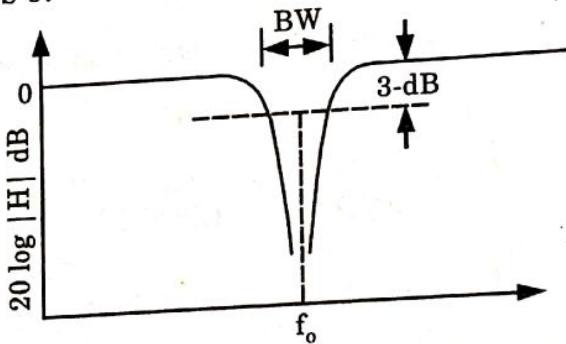


Fig. 4. Frequency response of notch filter.

