CA INNOVATIVE ASSIGNMENT

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Project Title:

Implementation of Storage Device (RAM)

Project Details:

- **Introduction:** (Random access memory) or read/write memory is a type of memory that provides direct access to any byte on the chip. This "byte addressing" means that the contents of any byte can be read or written without regard to the bytes before or after it. In addition, read and write speeds are symmetrical. It takes no longer to write a byte than it does to read one. RAM (also referred to as read-write memory, RWM) is considered volatile storage because its contents are lost when the power is removed.

- **RAM consists of the following connections:**
  - Address lines define the memory location to be selected for reading or writing.

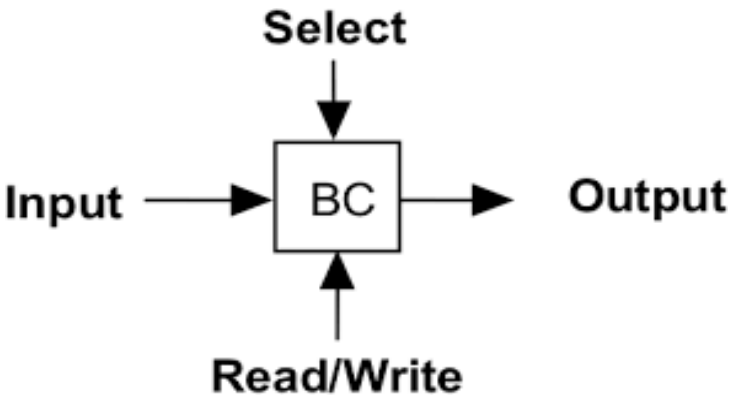
- Input/output data lines define the data to write to or read from memory.
- Write enable (WE) is a control input that selects between the memory read and write operations (usually active low).
- Output enable (OE) is a control input that enables the output buffer for reading data from the memory (usually active low).
- Power supply provides the necessary power to operate the circuit.

- **The Decoder:** A binary code of n bit is capable of representing up to 2^n distinct elements of the coded information. A decoder is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2^n unique output. The decoders in this case are called n-to-m line decoders, where m <= 2^n. their purpose is to generate the 2^n binary combination of the n input variables. A decoder has n inputs and m outputs and is referred to as an n*m decoder.

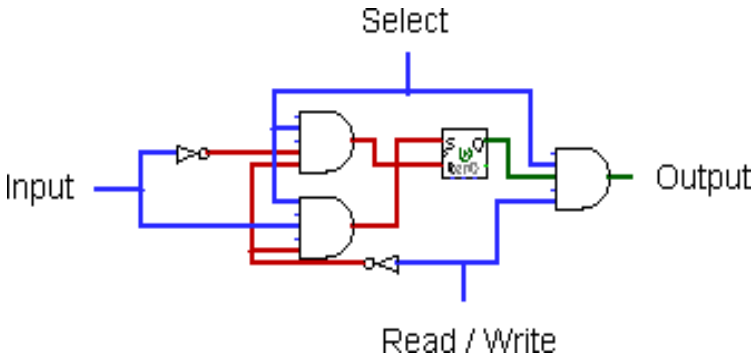
- **Binary Cell:** The memory cell is the fundamental building block of computer memory. The memory cell is an electronic circuit that stores one bit of binary information, and it must be set to store a logic 1 (high voltage level) and reset to store a logic 0 (low voltage level). Its value is maintained/stored until it is

changed by the set/reset process. The value in the memory cell can be accessed by reading it.

- Binary Cell Block Diagram:



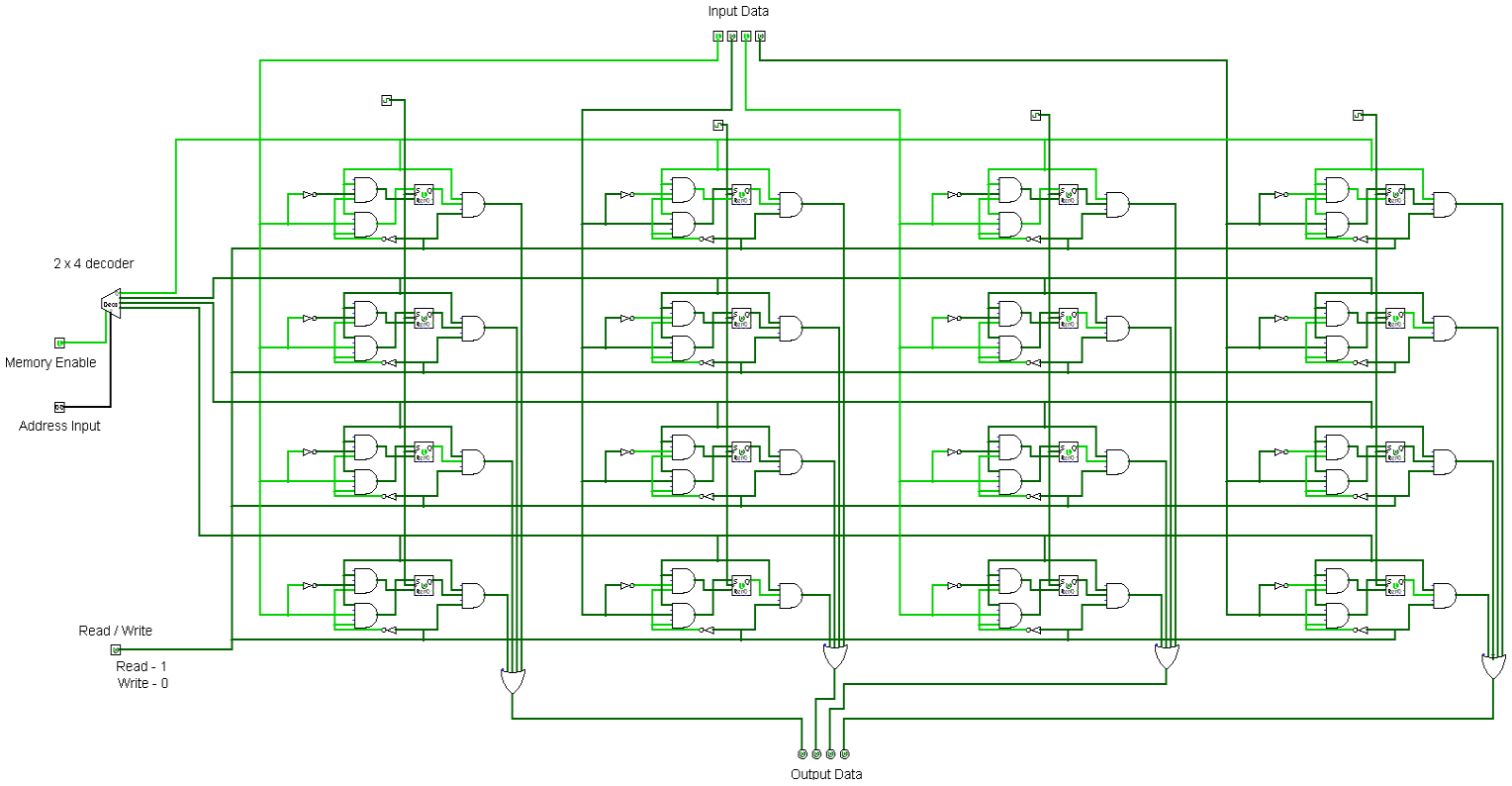
- **Binary Cell Logic Diagram:**



- **4 * 4 - bit RAM:** Design of 4*4bit Ram consist of (16) binary cells that arranged as an array and 2*4 decoder which give two address lines at its input to select one word from four words. The decoder is enabled by the memory enable input at which when memory enable is logic (0), all output of the decoder is logic (0) and none of the memory words are selected. when memory select at (1), one of from four words

is selected, dictated by the value in two address lines, once a word has been selected and the read/write input determine the operation. When read/write equal to one, we will read word from memory and four bits of the selected word go through four OR gates to the output terminal. When read/write equal to zero will write in the memory and the data available in the input lines are transferred into four binary cells of the selected word. The binary cells that are not selected are disabled and their previous binary values remain unchanged. When the memory select input that goes into the decoder is equal to (0), none of the words are selected and the contents of all cells remain unchanged regardless of the read/write input.

Circuit Diagram:


Input Data
2 x 4 decoder
Memory Enable
Address Input
Read / Write
Read - 1
Write - 0
Output Data