Design and Analysis of a RISC-V core with an External Instruction Memory SRAM Using Opensource Tools

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Abstract*—An instruction memory (imem) is where program instructions are stored. The paper constitutes the design and analysis of a RISC-V System on Chip (SoC) with its instruction memory in an external 4kB Static Random-Access Memory (SRAM). The SRAM is a memory array of 1024*32bits. An instruction word is 10 bits long and is byte-addressable. The main problem to be addressed in the project is integrating the SoC with an instruction memory located in an external SRAM. We achieved an access time of less than 2.5 ns using only open-source tools.

Keywords— CMOS, EDA, RISC-V, SoC, SPICE, SRAM

I. Introduction

In modern-day computer systems, memory has a vital role in storing data values and program instructions. This paper will describe a 6-Transistor SRAM used as an external instruction memory (imem) to a RISC-V SoC. SRAM is used here due to its high performance and low power consumption compared to the DRAM (Dynamic Random-Access Memory). It uses bistable latching circuitry to store each bit and exhibits data remembrance but is still volatile [1]. RISC-V is a load-store open standard instruction set architecture (ISA) based on established reduced instruction set computer (RISC) principles.

II. SRAM AND RISC-V ARCHITECTURE

A. SRAM Architecture

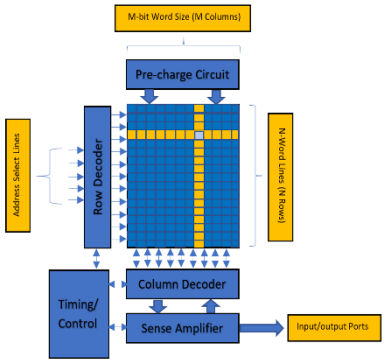

FIGURE 1: SRAM Architecture

Basic SRAM memory array consists of N-words, i.e., N number of rows in the memory array, and each word is M-bits wide, i.e., M number of columns in the memory array [2]. Row and column decoders are used for selecting a particular word and bit. A sense amplifier is present below the column decoder, which gives the I/O ports the amplified output of a particular bit line. Multiplexers can also be present to route the data through the latches before getting to the appropriate I/O ports. Finally, a pre-charge circuitry is present for each pair of bit lines, which pre-charges the bit lines equivalently. All these are shown in Fig. 1 above.

B. RISC-V

RISC-V is a standardized Instruction Set Architecture (ISA) that is an open-source specification for computer processor architectures, not a particular chip or implementation. It is little-endian, has floating-point instructions and a compressed instruction set. Concurrency, atomic instructions, privilege modes, and virtual memory are also part of the design [4].

C. RISC-V External Integration With An SRAM

We integrate a RISC-V core with SRAM because SRAM is fast, very mature, has little static power dissipation compared to DRAM. Integrating the core and memory requires buses such as the address line, control and data. We put the SRAM outside the core because the design is easier to modify when the SRAM is outside the core and each component can be interchanged without redesigning the whole system. It is also easier to implement techniques solely for the core or SRAM independently. These may include power-gating, Dynamic Voltage and Frequency Scaling (DVFS) and Error-Correcting Codes (ECC). Enhancements such as redundancy, branch prediction, speculation, consistency may be easier to implement as there would more chip area to implement them. Testing would be easier too when they are separated because each can be tested exhaustively.

Some drawbacks of the SRAM being external to the core may be a larger area, higher cost, more wire routing and complexity, longer delay and less ease of use with emerging applications such as in-memory computing or neuromorphic computing that may require tighter integration of core and memory.

III. Conclusion And Future Scope

The next step in this project is we aim to integrate with the 4kB SRAM. Components to be designed include SRAM bit cell, sense amplifier, write driver, tri-state buffer, and D flip-flop. Some tools employed in the process to achieve this are OpenRAM, Ngspice, and Magic.

IV. References

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