Mugilvanan Vinayagam

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OBJECTIVE:

Seeking Full-time opportunities in the field of RTL Design, Verification & Validation.

EDUCATION:

M.S., Electrical and Computer Engineering (RTL Design, Verification and Validation), expected - June'20.
Portland State University, Portland, OR, USA. **GPA:3.89/4.0**
Courses: Microprocessor System Design, SystemVerilog, Pre-Silicon validation, Computer Architecture, SoC with FPGA, Deep Learning, Verilog, Advanced Computer Architecture, High Performance Digital Systems.

Bachelor of Engineering in Electronics & Communication Engineering, May'16
Anna University, Chennai, India. **CGPA:3.4/4.0**

TECHNICAL SKILLS:

- **Programming language:** Verilog, SystemVerilog, VHDL, C, C++, Python, Shell, GNU Octave, MATLAB.
- **Tools:** QuestaSim, Xilinx ISE, Xilinx Vivado & SDK, ModelSim, Synopsys VCS & Verdi, Intel Altera Quartus.

PROFESSIONAL EXPERIENCE:

Hardware Engineer Intern, Waymo LLC, Mountain View. **(June'19 – Sep'19)**

[C++, SystemVerilog, Verdi] DRAM Memory Tester
- Developed memory tester using C++ that runs on Multi-core Embedded SoC to check the reliability of the DRAM.
- Replicated the memory tests given in the standard memtester86 and included tests to replicate the row hammering.

[Synopsys Z01X, Python, SystemVerilog] Fault Simulation
- Fault Simulation to achieve optimum fault coverage with a set of test vectors and ensure Functional Safety of the silicon design.
- Developed Python script to read the coverage report from the regression simulation run to collect the seed sequences.

FPGA - RTL designer, ZOHO Corporation, Chennai, INDIA. **(Dec'15 – Aug'18)**

[VHDL, Verilog, C, Xilinx ZC706(28 nm), OpenSSL] Hardware Acceleration of SSL Algorithms:
- Designed DES, Triple-DES, SHA, AES(ECB, CBC, GCM) using VHDL and implemented in Xilinx ZC706 FPGA(28 nm) for offloading SSL algorithms from Server to FPGA.
- Designed MD5 and RC4 algorithms using VHDL and implemented in the FPGA running at 250MHz.
- Timing issues faced were solved using Static Timing Analysis report provided by the Xilinx Vivado Tool.

[Verilog, ImageNets] Research on Convolutional Neural Networks and ImageNets:
- Designed Image convolution module in Verilog which will take an Image & filter and performs convolution.
- Research on different Convolutional Neural Networks from the ImageNet database using Tensorflow.

ACADEMIC PROJECTS:

[Systemverilog, VHDL, C, DPI-C] Verification of AES_GCM encryption/decryption(Individual Project)
- Verified VHDL design of AES GCM using SystemVerilog environment with generator, driver, scoreboard, BFM.
- The C implementation of AES GCM is called using DPI-C interface to act as a reference model.

[SystemVerilog] Design and verification of AXI4-Lite Master-slave protocol
- Designed a AXI4-lite Master controller and slave block RAM with the assumption of always ready.
- Verified the design using assertions, driver, scoreboard and checker components.

[SystemVerilog] L1 cache simulator for a 32-bit processor
- Designed a L-1 split cache with MESI protocol to ensure cache coherency and Least-Recently-Used replacement policy.
- The design will process the input command file and keeps track of cache hits, misses, reads and writes.

[Python, MIPS] Timing Simulator for MIPS Architecture(Individual Project)
- Implemented the MIPS ISA pipeline with and without Forwarding, assuming always taken branch prediction using Python.
- A timing simulator has been designed to keep track of the different hazards, types of instructions & stalls.
- The code also computes post execution statistics like dynamic Instructions Count, clock cycles, stall cycles and average CPI.

[C, SimpleScalar simulator] Cache Replacement algorithms
- Implemented alternative Cache Replacement algorithms using C language and integrated the same in the Simplescalar simulator to observe the changes in the performance.
- PC aware cache replacement policies are used to predict the future chances of a cache line getting accessed.
- Avoids polluting the cache with addresses that are not going to be accessed in future.

[Verilog, Nexys DDR4] Real Time Convolution of Video stream
- Achieved seamless convolution of RGB video stream(30 fps at 25MHz) - convolution running at 225 MHz.
- Frame-by-frame convolution is done with the filters chosen using the switches and displayed in the VGA display.

[Python, Deep Learning] HashedNets
- Research on Hashednets DNN which will group the weights in the network randomly to reduce the parameters storage size.
- The number of weights and biases are reduced by the factor chosen without affecting the accuracy of the network.