**Final Synthesis**

You have to [synthesize](https://forums.xilinx.com/t5/Vivado-TCL-Community/synthesize-one-file-only/td-p/673902) Full system and generate the gate level netlist and reports (timing, area, power)

**Steps: -**

1- Create your hierarchy under this path /home/IC/Projects

2- Add All the RTL files under /home/IC/Projects/System/RTL

3- Modify your CLK\_GATE file and move it under

/home/IC/Projects/System/RTL/Premapped

>> Modification: -

Instantiate the clock gating cell “TLATNCAX2M” from the library

4- Open design Compiler tool in GUI Mode by run design\_vision command in the terminal.

5- Do the following through GUI

1) Read the libraries

2) Read Design files

3) Run Link Command

Once succeeded and no problem reported regarding resolving the designs, close the GUI and run the script through dc\_shell

dc\_shell –f ./syn\_script.tcl

6- Add the following constrains

1) Create a clock on system clock port with frequency 20 MHz

2) Create a clock uncertainty with 0.2 ns for setup

3) Create a clock uncertainty with 0.1 ns for hold

4) Create a clock transition with 0.05 ns

5) Input delays on all input ports except (CLK & RST) with 20 clock period

6) output delays on all output ports with 20% clock period

7) Add Buffer driving cell for all input ports

8) Add load of 75 pf on all output ports