Mohamed Sayed Mohamed Tawfik

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EDUCATION

Fresh graduate student at faculty of engineering, Cairo University, Electronics and electrical communications department.

- Cumulative Grade: **Excellent with Honor (87%)** Cumulative Rank: **10th**
- Graduation year: **2022**

GRADUATION PROJECT

- **Project Title:** Hardware design and implementation of machine learning acceleration CNN network (Squeeze-Next Architecture).
- **Sponsored By:** Siemens EDA (Mentor Graphics).
- **Supervised By:** DR. Hassan Mostafa
- **Grade :** Excellent
- **Our Target:** Design and implement the CNN architecture on FPGA with high throughput, high accuracy and low energy, that's achieved by making many optimizations in timing, area, accuracy and power.
- **My Role:**
  - Finding the optimum building blocks for the network.
  - Modifying the network for better hardware design.
  - Controller design for all the architecture layers.
  - RTL coding and integration between layers using Verilog.
  - Performing many optimizations in area, power, timing, throughput and accuracy to achieve our target.
  - Completing the FPGA design flow (Target FPGA: Virtex-7 on VC-709 Board).

TECHNICAL PROJECTS

- **Digital-based projects:**
  - **16-bit Harvard-based Microprocessor** using Xilinx Spartan 6 FPGA implemented on PCB using VHDL.
  - **UART Transmitter and Receiver Implementation:**
    - Using Verilog HDL for describing the hardware of UART.
    - Using Xilinx ISE Design to simulate, debug and verify code by Testbenches, ILA and VIO.
    - Using FPGA Spartan 6 for implementing UART.
  - **The Advanced Encryption standard (AES)**: based on (RIJNDAEL) encryption algorithm 128-bit 10 rounds using Verilog (simulated and synthesized using Quartus) implemented on DE0-CV FPGA.
  - **Design of pipelined 16-bit Harvard-based Microprocessor (MIPS16 pipeline)** and solving hazards problems using Verilog (simulated and synthesized using Vivado).
  - **Design and implementation of General binary multiplier / divider array**:
    - Using Verilog HDL for describing the hardware and verifying the functionality.
    - Using L-EDIT tool to make the layout.
    - Using PSPICE circuit simulator to make the Post-Layout simulation.
  - **Design and implementation of a matrix multiplier circuit in three different styles:** (FSMD using Verilog, NIOS II, and ARM Cortex MO) for a final project at *Siemens EDA*. Conducted functional, timing simulations and synthesis using Quartus Prime and Modelsim, implemented on DE0-Nano FPGA.

- ❖ **Design and Synthesize a Full Digital System**: It is responsible for doing some processing using ALU block on Register File stored data to generate byte data then send it using Serial Communication Protocol UART.
- ❖ **Design of 32-Point Radix-2 FFT architecture based on Cooley and Tukey algorithm** using Verilog (simulated and synthesized using Vivado)**.**
- ❖ **RTL Design, Validation, and Implementation of an Elevator Controller:** for a final project at *PyramidTech* using VHDL, Validation of the design using self-checking testbenches and simulation using Questasim, The hardware implementation and validation of the controller using the Terasic DE0-CV development board.

- **Analog and Embedded-systems based projects:**
  - ❖ Design and Simulation for Active Filters based on Opamp-Rc and Gm-Cells.
  - ❖ Design and Simulation for Folded-Cascode Operational Amplifier.
  - ❖ Wireless Voting Machine using Atmel AVR microcontroller and RF modules implemented on PCB.
  - ❖ Smart Water cooling system using Atmel AVR microcontroller implemented on PCB.

EXPERIENCE

- Junior FPGA Engineer at *PyramidTech LLC* as a part time position. [September 2022 – January 2023]
- Teaching Assistant at The American University in Cairo (AUC). [September 2022 – December 2022]
- FPGA Design Using VHDL internship at *PyramidTech LLC Company*. [July 2022 – September 2022]
- Digital design and FPGA certified course at *SIEMENS ACADEMY*: Covering design and verification of combinational/sequential circuits, FPGA Implementation flow, timing closure,FSM design modeling, FSM with Datapath modeling and Platform Designer: Building and programming a processor on FPGA. [October 2021]
- Digital IC Design certified Diploma, program modules: Verilog HDL, TCL Scripting language,Power aware design, Logic Synthesis using Design Compiler. [August 2021 – October 2021]
- Hardware Description Languages for FPGA Design Course, One Lab. [March 2021]
- Participate in the 5th undergraduate engineering mathematics forum held at faculty of engineering, Cairo University (got full mark). [January 2020]

TECHNICAL SKILLS

- ❖ Hardware modeling and digital IC design
- ❖ Verification Methodology and UVM
- ❖ Layout design
- ❖ Deep Learning Fundamentals
- ❖ PCB design
- ❖ TCL Scripting language
- ❖ Hardware description languages :-VHDL - Verilog - System Verilog
- ❖ Programming languages : -C/C++ -Python -Matlab - Assembly
- ❖ EDA Tools:

-Cadence Virtuoso	-Multisim	-Modelsim	-ISE design Suite
-Proteus	-Altium designer	-Vivado	-L-EDIT (Layout Tool)
-PSPICE circuit simulator	-COMSOL Simulator	-Questasim	-Quartus Prime

- ❖ Language skills:
  - ❖ Arabic (native).
  - ❖ English (Proficient).
  - ❖ Germany (elementary proficiency).

PERSONAL INFORMATION

- Date of birth : 6/11/1998
- Military status: Currently serving (Completing on 1/3/2024).
- Address: Haram, Giza, Egypt.