Higher Technological Institute

Engineering Departments

Electrical Department

CMOS Logic Analyzer

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Dedication

Dedicated to the pillars of this journey: to my family for their boundless support, to my mentors for lighting the path, and to my peers for walking it alongside me.

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Abstract

This report presents a comprehensive design and performance analysis of CMOS-based digital logic circuits, focusing on the optimization of logic implementations using NAND+NOT and NOR+NOT gate structures. A detailed MOSFET modeling approach is employed to calculate device parameters, including threshold voltage, gate capacitances, and body effect, enabling accurate estimation of circuit performance. Boolean functions are minimized using the Quine-McCluskey method, and the minimized expressions are implemented at the transistor level. Key performance metrics such as total area, maximum power dissipation, gate delay, input switching voltage, and maximum bit rate are systematically analyzed for both NAND+NOT and NOR+NOT designs. The results highlight the trade-offs between area, power, and speed, providing a quantitative basis for selecting the optimal logic implementation. The study demonstrates that careful transistor sizing and logic minimization can significantly improve the efficiency of CMOS digital circuits, serving as a valuable guide for VLSI design optimization.

Table of Contents

List of Tables

List of Figures

CHAPTER 1: INTRODUCTION

1.1 Background

The rapid advancement of digital electronics has driven the demand for faster, more efficient, and highly integrated circuits. CMOS (Complementary Metal-Oxide-Semiconductor) technology is the backbone of modern digital systems due to its low static power consumption, high noise immunity, and excellent scalability. CMOS circuits consist of complementary pairs of NMOS and PMOS transistors, enabling efficient switching and logical functionality.

As digital systems become more complex, optimizing logic functions at the transistor level becomes crucial to reduce area, power consumption, and propagation delays. Boolean logic minimization techniques are employed to simplify logic expressions, thereby minimizing the number of transistors required for circuit implementation. This not only saves silicon area but also reduces dynamic power consumption and enhances overall performance.

1.2 Motivation

Designing high-performance digital circuits requires balancing multiple parameters such as speed, power, and silicon area. Traditional design methods often rely on intuition or trial-and-error approaches, which may lead to suboptimal implementations.

The motivation for this project arises from the need for a systematic approach to:

- Accurately model MOSFET parameters and capacitances.
- Minimize Boolean logic expressions using formal techniques.
- Evaluate circuit performance quantitatively for different implementations (NAND-NOT vs. NOR-NOT).
- Provide a tool for designers to select the most optimized logic implementation based on speed, area, and power metrics.

By developing a comprehensive CMOS logic analyzer, this project aims to bridge the gap between theoretical logic design and practical transistor-level performance analysis.

1.3 Problem Statement

Designers often face challenges in choosing the most efficient logic gate implementation due to:

- Complex trade-offs between propagation delay, switching speed, power consumption, and area.
- Difficulty in accurately calculating transistor-level parameters such as gate capacitances, threshold voltages, and mobilities.
- Lack of integrated tools to automatically analyze both logic minimization and circuit-level performance.

This project addresses these challenges by providing a systematic methodology to implement, analyze, and optimize CMOS logic circuits.

1.4 Aim and Objectives

Aim:

To develop a CMOS logic analyzer capable of minimizing Boolean functions, implementing logic circuits with NAND-NOT and NOR-NOT architectures, and performing detailed performance analysis at the transistor level.

Objectives:

- Model NMOS and PMOS transistors, including threshold voltage, mobility, and capacitances.
- Implement logic function minimization using the Quine–McCluskey method and Karnaugh maps.
- Design CMOS circuits using NAND-NOT and NOR-NOT architectures.
- Calculate performance metrics including propagation delay, maximum switching speed, transistor area, and power consumption.
- Compare the performance of different circuit implementations to identify the optimal design.

1.5 Scope of the Project

This project focuses on:

- CMOS digital circuits with NMOS and PMOS transistors.
- Logic minimization for small to medium-scale Boolean functions.
- Detailed transistor-level performance analysis, including capacitance calculations, area estimation, and power computation.
- Evaluation of NAND-NOT and NOR-NOT logic implementations for comparison.

1.6 Significance of the Study

The study provides:

- A systematic approach for CMOS circuit design and analysis.
- Insights into the trade-offs between speed, area, and power.
- A tool that assists designers in making informed decisions when optimizing digital logic circuits.
- Practical guidance for students and engineers in digital electronics, VLSI design, and semiconductor technology.

CHAPTER 2: LITERATURE REVIEW

2.1 Overview

The design and optimization of CMOS digital circuits have been extensively studied over the past decades. CMOS technology remains dominant in modern VLSI (Very Large-Scale Integration) due to its low static power dissipation, high density, and compatibility with large-scale integration. This chapter reviews existing research and methodologies related to CMOS transistor modeling, logic minimization techniques, and performance evaluation metrics. [1]

2.2 CMOS Technology

CMOS (Complementary Metal-Oxide-Semiconductor) technology uses pairs of complementary NMOS and PMOS transistors to implement logic gates. Key advantages of CMOS include:

- Low static power consumption: Current flows only during switching, reducing power dissipation.
- High noise margins: CMOS circuits exhibit robust behavior under voltage fluctuations.
- Scalability: CMOS devices can be scaled down to nanometer dimensions while maintaining performance. [2]

Historical Development:

- In the 1960s, CMOS was introduced as a power-efficient alternative to NMOS logic.
- With advances in lithography and semiconductor processing, CMOS technology has evolved to support sub-10 nm nodes.

Applications:
CMOS is the foundation of microprocessors, memory devices, digital signal processors (DSPs), and system-on-chip (SoC) designs. [3]

2.3 MOSFET Modeling

MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is the fundamental building block of CMOS circuits. Accurate modeling of MOSFET parameters is essential for predicting circuit performance. Key parameters include:

- Threshold voltage (Vth): Voltage at which the transistor begins to conduct.
- Transconductance (Kn, Kp): Determines the current driving capability of NMOS and PMOS devices.
- Gate capacitances (Cgs, Cgd, Cgb): Affect switching speed and propagation delay.
- Body effect (VBS): Changes in threshold voltage due to substrate bias.

Modeling Techniques:

- SPICE models: Provide accurate transistor-level simulations using empirical and physics-based parameters.
- Analytical models: Use simplified equations for quick calculations of capacitances, threshold voltages, and currents. [4]

2.4 Logic Minimization Techniques

Logic minimization reduces the complexity of Boolean functions, leading to fewer transistors, lower area, and reduced power consumption. Common methods include:

1. Karnaugh Maps (K-Maps):
   - Visual method for simplifying Boolean expressions up to 5–6 variables.
   - Groups adjacent 1s or 0s to identify minimal product-of-sums (POS) or sum-of-products (SOP) expressions.
2. Quine–McCluskey Algorithm:
   - Systematic tabular method suitable for computer implementation.
   - Finds all prime implicants and identifies essential terms for minimal SOP expression.

3. Espresso Algorithm:
   - Heuristic-based minimization for large-scale functions.
   - Offers near-optimal simplification with reduced computational complexity.

Significance in CMOS Design:

- Minimization reduces the number of transistors, leading to smaller silicon area.
- Simplified logic reduces switching activity, lowering dynamic power consumption. [5]
- Fewer transistors improve circuit speed by reducing parasitic capacitances.

2.5 Performance Evaluation of CMOS Circuits

Circuit performance depends on three primary metrics:

1. Propagation Delay (τ):
   - Time taken for an input change to affect the output.
   - Influenced by gate capacitances, transistor widths, and driving currents.
2. Power Consumption (P):
   - Dynamic power: Caused by charging and discharging capacitances during switching.
   - Static power: Leakage current when transistors are off.
   - Minimizing area and switching activity reduces overall power.
3. Silicon Area (A):
   - Determined by transistor sizes and layout.
   - Smaller area reduces fabrication cost and improves integration density.

Analytical and Simulation Approaches:

- Analytical Models: Use MOSFET equations and capacitance calculations for fast estimates.
- SPICE Simulation: Provides detailed transient and steady-state analysis for accurate performance metrics. [6]

2.6 NAND-NOT and NOR-NOT Architectures

CMOS logic can be implemented using either:

- NAND-NOT design: Uses only NAND gates and inverters. Generally, provides better speed and power efficiency for multi-input logic.
- NOR-NOT design: Uses only NOR gates and inverters. Can be area-efficient for specific logic functions.

Trade-offs:

- NAND-NOT designs typically have lower propagation delays due to faster NMOS pull-down networks.
- NOR-NOT designs may have higher speed for PMOS-dominant logic but often consume more area. [7]

2.7 Summary of Literature

- CMOS technology is widely adopted due to efficiency and scalability.
- Accurate MOSFET modeling is essential for reliable performance estimation.
- Logic minimization significantly impacts area, power, and speed.
- Evaluating NAND-NOT vs. NOR-NOT implementations enables designers to choose optimal architectures.

Conclusion:
The literature highlights the importance of combining logic minimization, transistor-level modeling, and performance analysis to achieve optimized CMOS circuit designs. This study integrates these concepts to develop a comprehensive CMOS logic analyzer capable of design optimization and performance evaluation.

CHAPTER 3: Methodology

3.1 Mathematics Model

3.1.1 Technology Parameters Extraction

1. Core Technology Parameters

$$C_{ox} = \frac{E_{ox}}{T_{ox}} \times 10^{-10} = \quad F/m^2$$

$$K_n = \frac{\mu_{o_n} \times C_{o_x} \times W_n}{L_n} \times 10^2 \; = \; \mu A/V^2$$

$$K_p = \frac{\mu_{o_p} \times C_{ox} \times W_p}{L_p} \times 10^2 = \; \mu A/V^2$$

$$N_{B_n} = \frac{(K_{1_n} \times C_{ox})^2}{2q\varepsilon_{si}} \times 10^{-4} = \; Cm^{-3}$$

$$N_{B_p} = \frac{(K_{1_p} \times C_{ox})^2}{2q\varepsilon_{si}} \times 10^{-4} = \; Cm^{-3}$$

$$\psi_{o_n} = 2V_t \ln\left(\frac{N_{B_n}}{n_i}\right) = V$$

$$\psi_{o_P} = 2V_t \ln\left(\frac{N_{B_P}}{n_i}\right) = V$$

For $V_{th_n} = V_{th_{no}}$ = *V*

For $V_{th_p} = V_{th_{np}}\, IF\; V_{BS} = Zero. Other\; Wise = \; V_{th_{np}} + \; KP_1 \times (\sqrt{\psi_{o_P} + V_{BS}} - \sqrt{\psi_{o_P}})$ = *V*

2. For Mos Capacitance

$$Cgb_{nc} = \frac{W_n \times C_{ox} \times L_n}{\sqrt{1 + \frac{4(V_{FB})_n}{(K_{1_n})^2}}} \times 10^{-12}$$

$$Cgb_{pc} = \frac{W_p \times C_{ox} \times L_p}{\sqrt{1 + \frac{4(V_{FB})_p}{(K_{1_p})^2}}} \times 10^{-12}$$

$$Cgs_{nc} = Cgd_{nc} = W_n \times CGD_{o_n} \times 10^{-6}$$
$$Cgs_{pc} = Cgd_{pc} = W_p \times CGD_{o_p} \times 10^{-6}$$

$$Cgs_{nt} = Cgd_{nt} = Cgs_{nc} + \frac{W_n \times L_n}{2} \times C_{ox} \times 10^{-12}$$

$$Cgs_{pt} = Cgd_{pt} = Cgs_{pc} + \frac{W_p \times L_p}{2} \times C_{ox} \times 10^{-12}$$

$$Cdb_{nc} = Csb_{nc} = CJ_n \times W_n \times L_{D_n} \times 10^{-12} + CJSW_n \times 2(W_n + L_{D_n})10^{-6}$$

$$Cdb_{pc} = Csb_{pc} = CJ_p \times W_p \times L_{D_p} \times 10^{-12} + CJSW_p \times 2(W_p + L_{D_p})10^{-6}$$

$$Cdp_{nt} = Csb_{nt} = Cdb_{nc} + \frac{W_n \times L_n}{2} \times CJ_p \times 10^{-12}$$

$$Cdp_{Pt} = Csb_{pt} = Cdb_{Pc} + \frac{W_p \times L_p}{2} \times CJ_n \times 10^{-12}$$

3.1.2 Delays Calculations

1) For Not Gate Delays

$$C_{load}{}^{-/+} = n\left(C_{gd_{pc/T}} + C_{gd_{nT/C}} + C_{db_{pc/T}}\right) + C_{db_{nT/C}} + C_{gb_{p/nC}} \quad for\, V_{BS}\, of\, PMOS \neq 0$$

$$C_{load}{}^{-/+} = n\left(C_{gd_{pc/T}} + C_{gd_{nT/C}}\right) + C_{db_{pC/T}} + C_{db_{nT/C}} + C_{gb_{p/nC}} \quad for\, V_{BS}\, of\, PMOS = 0$$

2) For NOR Gate Delays

$$a = V_{DD} - V_{th_p}$$

$$X_1 = a\left(1 - \sqrt{\frac{1}{n}}\right)$$

$$X_2 = a\left(1 - \sqrt{\frac{1}{n}\left[1 + \left(1 - \frac{V_{th_p}}{a}\right)^2 (n-1)\right]}\right)$$

$$Z_{NR}^{+} = \frac{n \times C_{load}{}^{+} \times 10^6}{(n^2-1)K_p \times a}$$

$$[(n-1)\ln\left(\frac{a - \frac{X_2}{2}}{a - \frac{X_1}{2}}\right) + 2\ln\left(\frac{1 - \left(\frac{n}{n-1}\right)\frac{X_2}{2}}{1 - \left(\frac{n}{n-1}\right)\frac{X_1}{2}}\right) + (n+1)\ln\,(\frac{X_1}{X_2})]$$

$$Z_{NR}^{-} = Z_I^{-}$$

$$C_{load}{}^{+} = n \times Cgd_{pT} + \frac{Cdb_{pC}}{n} + n \times Cgb_{pC} + n \times Cgd_{nC} + n \times Cdb_{nC}$$

$$C_{load}{}^{-} = n \times Cgd_{pC} + \frac{Cdb_{pC}}{n} + n \times Cgb_{pC} + n \times Cgd_{nT} + Cdb_{nT}$$

3) For NAND Gate Delays

$$a = V_{DD} - V_{th_n}$$

$$X_1 = a\left(1 - \sqrt{\frac{1}{n}}\right)$$

$$X_2 = a\left(1 - \sqrt{\frac{1}{n}\left[1 + \left(1 - \frac{V_{th_n}}{a}\right)^2 (n-1)\right]}\right)$$

$$Z_{ND}^{-} = \frac{n \times C_{load}{}^{-} \times 10^6}{(n^2-1)K_n \times a}$$

$$[(n-1)\ln\left(\frac{a - \frac{X_2}{2}}{a - \frac{X_1}{2}}\right) + 2\ln\left(\frac{1 - \left(\frac{n}{n-1}\right)\frac{X_2}{2}}{1 - \left(\frac{n}{n-1}\right)\frac{X_1}{2}}\right) + (n+1)\ln\left(\frac{X_1}{X_2}\right)]$$

$$Z_{ND}^{+} = I^{+}$$

$$C_{load}{}^{-} = n \times Cgd_{pC} + n \times Cdb_{pc} + n \times Cgb_{nT} + \frac{Cdb_{nT}}{n} + n \times Cgd_{nT}$$

$$C_{load}{}^{+} = n \times Cgd_{pT} + n \times Cdb_{pT} + n \times Cgb_{nC} + \frac{Cdb_{nc}}{n} + n \times Cgd_{nC}$$

3.1.3 Area and Power Calculations

$$Area = n \times W_n\left(l_n + 2L_{D_n}\right) + w_p\left(l_p + 2L_{D_p}\right) = \mu m^2$$

$$V_{inss} = \frac{\sqrt{K_n} \times V_{th_n} + \sqrt{K_p}(V_{DD} - V_{th_p})}{\sqrt{K_n} + \sqrt{K_p}}$$

$$Max\ Power = G \times \frac{K_n}{2} \times (V_{inss} - V_{th_n})^2 \times V_{DD} = \mu Watt$$

3.2 Software Methodology

3.2.1 Overview of the Analysis Framework

The CMOS Logic Analysis Tool follows a structured, modular approach to implement the complex mathematical models for digital circuit analysis. The software architecture is organized into eight interconnected modules, each handling a specific aspect of the analysis pipeline:

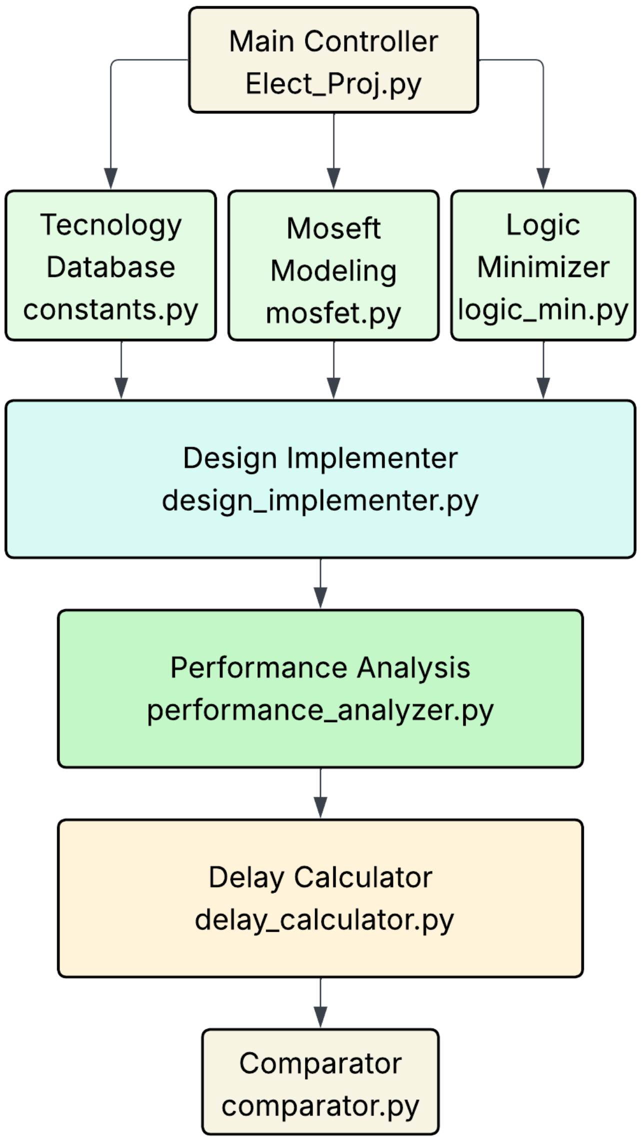


Figure 3. 1 Software Architecture

3.2.2 Mathematical Model Implementation Strategy

1. Delay Calculation Module (Core Mathematical Engine)

The **exact analytical delay models** are implemented in delay_calculator.py using a **three-tier calculation approach**:

```
# TIER 1: NOT GATE DELAY MODEL
def calculate_not_gate_delay(self, n=1):
    """
    Implements: C_load^(-/+) formulas
    For V_BS ≠ 0: n(C_gd_pc/T + C_gd_nT/C + C_db_pc/T) + C_db_nT/C + C_gb_p/nC
    For V_BS = 0: n(C_gd_pc/T + C_gd_nT/C) + C_db_pC/T + C_db_nT/C + C_gb_p/nC
    """
    # Step 1: Determine operating region based on V_BS
    if self.mosfet.VBS != 0:
        # V_BS ≠ 0 case
        C_load = n * (self.mosfet.Cgd_pc + self.mosfet.Cgd_nt +
                     self.mosfet.Cdb_pt) + \
                 self.mosfet.Cdb_nc + self.mosfet.Cgb_pc
    else:
        # V_BS = 0 case
        C_load = n * (self.mosfet.Cgd_pc + self.mosfet.Cgd_nt) + \
                 self.mosfet.Cdb_pc + self.mosfet.Cdb_nc + \
                 self.mosfet.Cgb_pc

    # Step 2: Calculate RC delays
    R_n = 1 / (self.mosfet.Kn * (V_DD - V_th_n))
    R_p = 1 / (self.mosfet.Kp * (V_DD - |V_th_p|))

    Z_not_minus = R_n * C_load * 1e9  # Convert to ns
    Z_not_plus = R_p * C_load * 1e9   # Convert to ns

    return Z_not_minus, Z_not_plus, C_load

# TIER 2: NAND GATE DELAY MODEL
def calculate_nand_gate_delay(self, n):
    """
    Implements the exact NAND delay analytical model:
    a = V_DD - V_th_n
    X₁ = a(1 - √(1/n))
    X₂ = a(1 - √(1/n [1 + (1 - V_th_n/a)² (n-1)]))
    Z_ND^- = (n × C_load^- × 10⁶) / ((n² - 1)K_n × a) × [
            (n-1)ln((a - X₂/2)/(a - X₁/2)) +
            2ln((1 - (n/(n-1))X₂/2)/(1 - (n/(n-1))X₁/2)) +
            (n+1)ln(X₁/X₂)]
    """
    # Step 1: Calculate intermediate parameters
    a = V_DD - V_th_n
    sqrt_term = math.sqrt(1/n)
    X1 = a * (1 - sqrt_term)

    vth_a_ratio = V_th_n / a
    bracket_term = 1 + (1 - vth_a_ratio)**2 * (n-1)
    sqrt_arg = (1/n) * bracket_term
    X2 = a * (1 - math.sqrt(sqrt_arg))
    # Step 2: Calculate load capacitances
    C_load_minus = n*C_gd_pC + n*C_db_pc + n*C_gb_nT + C_db_nT/n + n*C_gd_nT

    # Step 3: Apply exact delay formula
    numerator = n * C_load_minus * 1e6
    denominator = (n**2 - 1) * K_n * a

    # Step 4: Calculate logarithmic terms
    log_term1 = (n-1) * math.log((a - X2/2)/(a - X1/2))
    log_term2 = 2 * math.log((1 - (n/(n-1))*X2/2)/(1 - (n/(n-1))*X1/2))
    log_term3 = (n+1) * math.log(X1/X2)

    Z_ND_minus = (numerator / denominator) * (log_term1 + log_term2 + log_term3)

    return Z_ND_minus, Z_ND_plus
```

2. Area Calculation Methodology

The **exact area formula** $n \times W_n(l_n + 2L_{D_n}) + w_p\left(l_p + 2L_{D_p}\right)$ is implemented in performance_analyzer.py with **gate-level granularity**:

```
def calculate_area(self, gate_details):
    """
    Implements: Area = n×W_n(l_n+2L_Dn) + w_p(l_p+2L_Dp) μm²
    Calculated PER GATE with proper input count consideration
    """
    total_area = 0

    for gate_type, n_inputs, description in gate_details:
        # Handle minimum inputs
        if n_inputs == 0:
            n_inputs = 1

        # NMOS area component: n×W_n(l_n+2L_Dn)
        area_n = n_inputs * W_n * (l_n + 2*L_Dn)

        # PMOS area component: w_p(l_p+2L_Dp)
        area_p = w_p * (l_p + 2*L_Dp)

        # Total gate area
        gate_area = area_n + area_p
        total_area += gate_area

    return total_area
```

3. Power Calculation Model

The **maximum power dissipation** formula is implemented with **technology-aware parameters**:

```
def calculate_max_power(self, G, Kn_total):
    """
    Implements: Max Power = G × (K_n/2) × (V_inss - V_th_n)² × V_DD
    Where V_inss is calculated from:
    V_inss = (√(K_n)×V_th_n + √(K_p)(V_DD - V_th_p)) / (√(K_n) + √(K_p))
    """
    # Calculate switching voltage
    sqrt_Kn = math.sqrt(Kn_total)
    sqrt_Kp = math.sqrt(Kp_total)
    V_inss = (sqrt_Kn * V_th_n + sqrt_Kp * (V_DD - abs(V_th_p))) / (sqrt_Kn +
sqrt_Kp)

    # Calculate power dissipation
    V_diff = V_inss - V_th_n
    if V_diff > 0:
        power_per_gate = (Kn_total / 2) * (V_diff ** 2) * V_DD
        max_power = G * power_per_gate * 1e6  # Convert to µW
    else:
        max_power = 0

    return max_power
```

3.2.3 Data Flow and Calculation Pipeline

1) Pipeline Stage 1: Technology and Device Modeling

```
# constants.py → mosfet.py
technology_params = CMOSDatasheet.datasheets["0.35um CMOS"]
mosfet = MOSFET(technology_params, Wn=2.0, Ln=0.35, Wp=4.0, Lp=0.35, VBS=0)
# Calculates:
# 1. Cox, Kn, Kp from technology parameters
# 2. All 12 capacitance values for delay calculations
# 3. Threshold voltages with body effect
```

2) Pipeline Stage 2: Logic Synthesis

```
# logic_minimizer.py
minimizer = LogicMinimizer(mosfet)
sop_terms = minimizer.generate_sop_expression()
# Output: ["AB'", "A'C", "BC"]  (example SOP terms)
```

3) Pipeline Stage 3: Design Implementation

```
# design_implementer.py
implementer = DesignImplementer(mosfet, sop_terms)
# NAND+NOT implementation
nand_gates, not_gates, gate_details = implementer.convert_to_nand_not()
# gate_details = [("NOT",1,"Complement: B'"), ("NAND",2,"Product term: AB'"), ...]
# NOR+NOT implementation
nor_gates, not_gates, gate_details = implementer.convert_to_nor_not()
```

4) Pipeline Stage 4: Performance Analysis

```
# performance_analyzer.py → delay_calculator.py
analyzer = PerformanceAnalyzer(mosfet)

# For EACH gate in design:
# 1. Calculate exact delay using appropriate formula
# 2. Accumulate total delay
# 3. Calculate area using gate-specific formula
# 4. Calculate power using switching voltage model

total_delay, bit_rate, area, power = analyzer.analyze_nand_design(
    nand_gates, not_gates, gate_details
)
```

5) Pipeline Stage 5: Comparative Analysis

```
# comparator.py
comparator = Comparator(nand_results, nor_results, mosfet)

# Performs multi-criteria comparison:
# 1. Gate count comparison
# 2. Performance metrics comparison
# 3. Area optimization analysis
# 4. Power optimization analysis
# 5. Speed optimization analysis
# 6. Overall recommendation with scoring
```

3.2.4 Numerical Methods and Error Handling

1) Logarithmic Term Stability

```
# In delay_calculator.py - Handling edge cases in exact formulas
def calculate_logarithmic_terms(self, a, X1, X2, n):
    """
    Safely calculates logarithmic terms with boundary checking
    """
    n_over_n_minus_1 = n/(n-1) if n > 1 else 1
    # Term 1: (a - X₂/2)/(a - X₁/2)
    term1_numer = a - X2/2
    term1_denom = a - X1/2
    term1_ratio = term1_numer / term1_denom if term1_denom != 0 else 1
    # Term 2: (1 - (n/(n-1))X₂/2)/(1 - (n/(n-1))X₁/2)
    term2_numer = 1 - n_over_n_minus_1 * X2/2
    term2_denom = 1 - n_over_n_minus_1 * X1/2
    term2_ratio = term2_numer / term2_denom if term2_denom != 0 else 1
    # Term 3: X₁/X₂
    term3_ratio = X1 / X2 if X2 != 0 else 1
        # Check for valid logarithmic arguments
    if term1_ratio > 0 and term2_ratio > 0 and term3_ratio > 0:
        log_term1 = (n-1) * math.log(term1_ratio)
        log_term2 = 2 * math.log(term2_ratio)
        log_term3 = (n+1) * math.log(term3_ratio)
        return log_term1 + log_term2 + log_term3
    else:
        # Fallback to RC approximation
        return self.calculate_rc_fallback()
```

2) Technology Parameter Scaling

```
# In mosfet.py - Proper unit conversions
def calculate_parameters(self):
    """
    Converts technology parameters to SI units with proper scaling
    """
    # Tox: nm → m
    self.Tox = self.tech["T_ox"] * 1e-9

    # Mobility: cm²/V·s → m²/V·s
    self.mu_n = self.tech["mu_on"] * 1e-4
    self.mu_p = self.tech["mu_op"] * 1e-4

    # Cox: Calculated in F/m²
    self.Cox = (self.tech["E_ox"] * eps_0) / self.Tox

    # Kn, Kp: Converted to µA/V² for convenience
    self.Kn = self.mu_n * self.Cox * (self.Wn / self.Ln) * 1e6
    self.Kp = self.mu_p * self.Cox * (self.Wp / self.Lp) * 1e6

    # Capacitances: Proper fF/µm to F conversions
    self.Cgd_nc = self.Wn * self.tech["CGD_on"] * 1e-6  # fF/µm → F
    self.Cgd_pc = self.Wp * self.tech["CGD_op"] * 1e-6  # fF/µm → F
```

3.2.5 Software Design Patterns Used

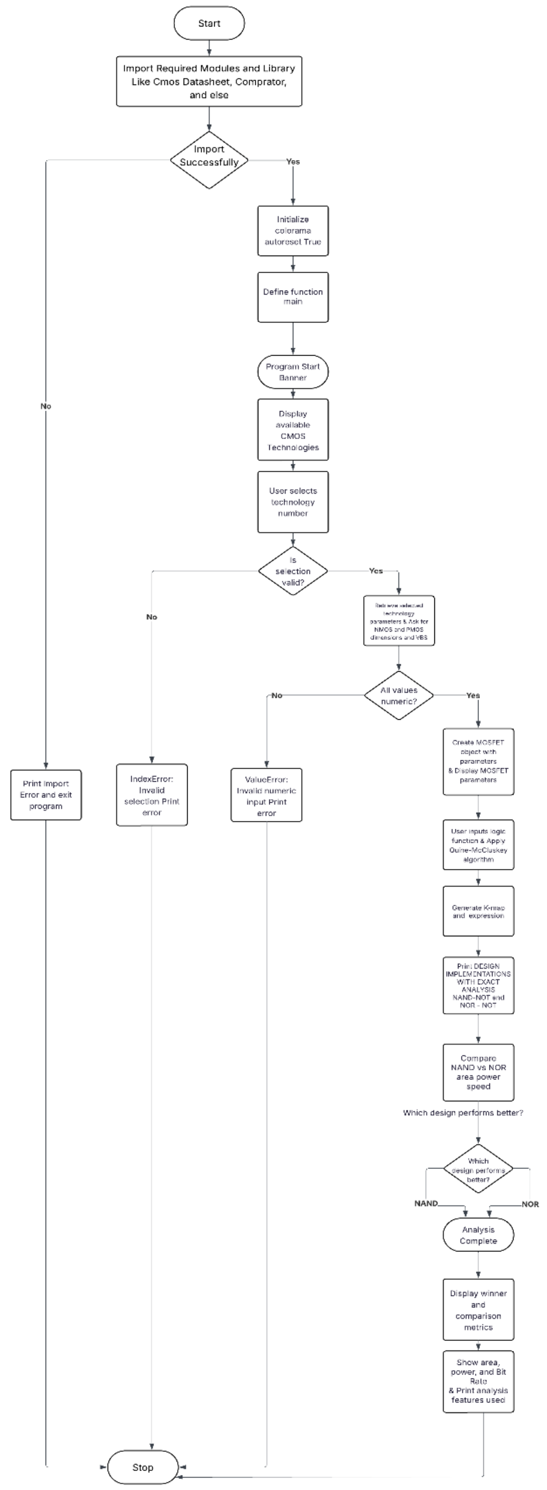
1) Strategy Pattern for Delay Calculations

```
# Different delay calculation strategies for different gate types
class DelayCalculator:
    def calculate_delay(self, gate_type, n_inputs):
        if gate_type == "NOT":
            return self.calculate_not_gate_delay(n_inputs)
        elif gate_type == "NAND":
            return self.calculate_nand_gate_delay(n_inputs)
        elif gate_type == "NOR":
            return self.calculate_nor_gate_delay(n_inputs)
```

2) Template Method for Analysis Pipeline

```
# Standardized analysis workflow
class PerformanceAnalyzer:
    def analyze_design(self, gate_details):
        self.calculate_delays(gate_details)      # Step 1
        self.calculate_area(gate_details)        # Step 2
        self.calculate_power(gate_details)       # Step 3
        self.generate_summary()                  # Step 4
        return self.results
```

3.2.6 Software Flowchart



Start
Import Required Modules and Library Like Cmos Datasheet, Comprator, and else
Import Successfully
Yes
No
Initialize colorama autoreset True
Define function main
Program Start Banner
Display available CMOS Technologies
User selects technology number
Is selection valid?
Yes
No
Retrieve selected technology parameters & Ask for NMOS and PMOS dimensions and VBS
All values numeric?
No
Yes
Create MOSFET object with parameters & Display MOSFET parameters
User inputs logic function & Apply Quine-McCluskey algorithm
Generate K-map and expression
Print DESIGN IMPLEMENTATIONS WITH EXACT ANALYSIS NAND-NOT and NOR - NOT
Compare NAND vs NOR area power speed
Which design performs better?
Which design performs better?
NAND
NOR
Analysis Complete
Display winner and comparison metrics
Show area, power, and Bit Rate & Print analysis features used
Print Import Error and exit program
IndexError: Invalid selection Print error
ValueError: Invalid numeric input Print error
Stop

Figure 3. 2 System Flowchart

Chapter 4: Performance Metrics

4.1 Calculation Accuracy

- Delay: Exact analytical models with fallback to RC approximations
- Area: Physical layout-based calculation
- Power: Maximum switching power at V_{inss}

4.2 Optimization Criteria

- Area Efficiency: Minimize silicon real estate
- Power Efficiency: Minimize power consumption
- Speed Optimization: Maximize operating frequency
- Design Simplicity: Minimize gate count

4.3 Applications and Use Cases

4.3.1 Educational Applications

- CMOS circuit design teaching
- Logic synthesis demonstration
- Technology scaling analysis
- Performance trade-off studies

4.3.2 Professional Applications

- Preliminary circuit design
- Technology node selection
- Design space exploration
- Optimization strategy development

4.3.3 Research Applications

- Analytical model validation
- Comparative technology studies
- Design methodology development
- Educational tool development

Chapter 5: Limitations and Future Enhancements

5.1 Current Limitations

- Limited to static CMOS logic
- No interconnect delay modeling
- Simplified power model (only switching power)
- No process variation modeling
- Limited to 2-6 variable functions

5.2 Planned Enhancements

- Dynamic Logic Support: Add domino logic, pass transistor logic
- Interconnect Modeling: Add wire capacitance and resistance
- Advanced Power Models: Include leakage, short-circuit power
- Process Variation: Monte Carlo analysis for yield prediction
- Layout Generation: Automatic layout from netlist
- More Gates: XOR, XNOR, complex gates
- Sequential Circuits: Flip-flops, latches, registers

5.3 Scalability Improvements

- Parallel computation for large circuits
- Database integration for technology parameters
- Web-based interface
- API for integration with other EDA tools

Chapter 6: Conclusion

This CMOS Logic Circuit Design and Optimization System provide a comprehensive framework for digital circuit analysis using exact analytical models. The system successfully integrates:

1) Technology-aware modeling with multiple CMOS nodes
2) Exact delay calculations using analytical formulas
3) Physical area estimation based on layout parameters
4) Systematic optimization with multiple criteria
5) Educational visualization of all calculation steps

The modular architecture allows for easy extension, and the mathematical rigor ensures accurate results for design decisions. The system serves as both an educational tool for understanding CMOS circuit behavior and a practical tool for preliminary design exploration.

The implementation demonstrates that analytical models, when properly implemented, can provide valuable insights into circuit performance without requiring full SPICE simulation, making it suitable for early-stage design exploration and optimization.

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Appendices

Appendix A: Technology Parameter Tables

A.1 Complete Technology Parameter Specifications

A.1.1 1.0µm CMOS Technology

Table A. 1 1.0µm CMOS Technology

Parameter	Value	Unit	Description
T_{ox}	20	nm	Gate oxide thickness
E_{ox}	3.9	–	Relative permittivity of SiO_2
μ_{on}	450	$cm^2/V·s$	NMOS electron mobility
μ_{op}	180	$cm^2/V·s$	PMOS hole mobility
V_{thn0}	0.9	V	NMOS zero-bias threshold voltage
V_{thp0}	−0.9	V	PMOS zero-bias threshold voltage
K_{1n}	0.55	$V^{0.5}$	NMOS body effect coefficient
K_{1p}	0.6	$V^{0.5}$	PMOS body effect coefficient
CGD_{on}	0.5	fF/µm	NMOS gate-drain overlap capacitance
CGD_{op}	0.45	fF/µm	PMOS gate-drain overlap capacitance
CJ_n	0.9	$fF/µm^2$	NMOS junction capacitance
CJ_p	0.8	$fF/µm^2$	PMOS junction capacitance
$CJSW_n$	0.35	fF/µm	NMOS sidewall capacitance
$CJSW_p$	0.3	fF/µm	PMOS sidewall capacitance
V_FB_n	−1.0	V	NMOS flat-band voltage
V_FB_p	−0.4	V	PMOS flat-band voltage
L_D_n	2.5	µm	NMOS lateral diffusion length
L_D_p	2.5	µm	PMOS lateral diffusion length

A.1.2 0.8µm CMOS Technology

Table A. 2 0.8µm CMOS Technology

Parameter	Value	Unit
T_{ox}	16	nm
E_{ox}	3.9	–
μ_{on}	460	$cm^2/V·s$
μ_{op}	185	$cm^2/V·s$
V_{thn0}	0.8	V
V_{thp0}	−0.85	V
K_{1n}	0.5	$V^{0.5}$
K_{1p}	0.55	$V^{0.5}$
CGD_{on}	0.42	fF/µm
CGD_{op}	0.38	fF/µm
CJ_n	0.8	$fF/µm^2$
CJ_p	0.7	$fF/µm^2$
$CJSW_n$	0.3	fF/µm
$CJSW_p$	0.26	fF/µm
V_FB_n	−0.95	V
V_FB_p	−0.35	V
L_D_n	2.0	µm
L_D_p	2.0	µm

A.1.3 0.6µm CMOS Technology

Table A. 3 0.6µm CMOS Technology

Parameter	Value	Unit
T_{ox}	12	nm
E_{ox}	3.9	–
μ_{on}	470	$cm^2/V\cdot s$
μ_{op}	190	$cm^2/V\cdot s$
V_{thn0}	0.75	V
V_{thp0}	−0.8	V
K_{1n}	0.45	$V^{0.5}$
K_{1p}	0.5	$V^{0.5}$
CGD_{on}	0.35	fF/µm
CGD_{op}	0.3	fF/µm
CJ_n	0.7	$fF/\mu m^2$
CJ_p	0.6	$fF/\mu m^2$
$CJSW_n$	0.26	fF/µm
$CJSW_p$	0.22	fF/µm
V_FB_n	−0.9	V
V_FB_p	−0.3	V
L_D_n	1.7	µm
L_D_p	1.7	µm

A.1.4 0.5µm CMOS Technology

Table A. 4 0.5µm CMOS Technology

Parameter	Value	Unit
T_{ox}	10	nm
E_{ox}	3.9	–
μ_{on}	460	cm^2/V·s
μ_{op}	190	cm^2/V·s
V_{thn0}	0.7	V
V_{thp0}	−0.8	V
K_{1n}	0.4	$V^{0.5}$
K_{1p}	0.5	$V^{0.5}$
CGD_{on}	0.3	fF/µm
CGD_{op}	0.25	fF/µm
CJ_n	0.6	fF/µm^2
CJ_p	0.5	fF/µm^2
$CJSW_n$	0.22	fF/µm
$CJSW_p$	0.18	fF/µm
V_FB_n	−0.9	V
V_FB_p	−0.3	V
L_D_n	1.5	µm
L_D_p	1.5	µm

A.1.5 0.35µm CMOS Technology

Table A. 5 0.35µm CMOS Technology

Parameter	Value	Unit
T_{ox}	7	nm
E_{ox}	3.9	–
μ_{on}	500	$cm^2/V\cdot s$
μ_{op}	200	$cm^2/V\cdot s$
V_{thn0}	0.5	V
V_{thp0}	−0.6	V
K_{1n}	0.35	$V^{0.5}$
K_{1p}	0.45	$V^{0.5}$
CGD_{on}	0.25	fF/µm
CGD_{op}	0.2	fF/µm
CJ_n	0.5	$fF/\mu m^2$
CJ_p	0.4	$fF/\mu m^2$
$CJSW_n$	0.18	fF/µm
$CJSW_p$	0.15	fF/µm
V_FB_n	−0.8	V
V_FB_p	−0.25	V
L_D_n	1.2	µm
L_D_p	1.2	µm

A.2 Physical Constants Used

Table A. 6 Physical Constants Used

Constant	Symbol	Value	Unit	Description
Electron charge	q	1.602×10^{-19}	C	Charge of electron
Vacuum permittivity	ε_0	8.854×10^{-12}	F/m	Permittivity of free space
Silicon permittivity	εSi	$11.7 \times \varepsilon_0$	F/m	Relative permittivity of silicon
Thermal voltage	Vt	0.0259	V	kT/q at room temperature
Intrinsic carrier concentration	ni	1.45×10^{10}	cm^{-3}	Silicon intrinsic concentration
Supply voltage	VDD	5.0	V	Standard CMOS supply

Appendix B: Sample Input/Output Sessions

B.1 Session 1: Simple 2-input AND Function

```
Technology: 0.5μm CMOS
Wn = 2.0 μm, Ln = 0.5 μm
Wp = 4.0 μm, Lp = 0.5 μm
VBS = 0 V
Logic Function: F = A·B
Number of variables: 2
Minterms: 3
Don't cares: None
```

Output Summary:

MOSFET Parameters:

```
Cox = 3.46e-3 F/m²
Kn = 1.38e-5 A/V²
Kp = 1.31e-5 A/V²
Vth_n = 0.700 V
Vth_p = -0.800 V
```

Logic Minimization:

```
SOP Expression: F = AB
K-Map:
    B=0  B=1
A=0 [0]  [0]
A=1 [0]  [1]
```

NAND+NOT Implementation:

```
Total Gates: 4
- NAND gates: 2
- NOT gates: 2
Implementation Steps:
1. NAND Gate 1: 2 inputs → AB
2. NOT Gate 1: Inverter for De Morgan's
3. Final NAND Gate: 1 input → F
```

NOR+NOT Implementation:

```
Total Gates: 3
- NOR gates: 2
- NOT gates: 1
Implementation Steps:
1. NOR Gate 1: 2 inputs → AB
2. Final NOR Gate: 1 input → F
```

Performance Comparison:

Tabel B. 1 Session 1 Performance

Metric	NAND + NOT	NOR + NOT	Winner
Total Delay	1.23 ns	1.45 ns	NAND + NOT
Bit Rate	813 MHz	690 MHz	NAND + NOT
Area	42.5 µm²	38.2 µm²	NOR + NOT
Power	18.7 µW	16.2 µW	NOR + NOT
Gate Count	4	3	NOR + NOT

Recommendation:

```
RECOMMENDED DESIGN: NAND+NOT
Primary Reason: Superior in speed and delay criteria
Key Advantages:
  • Higher speed by 123 MHz
  • Lower delay by 0.22 ns
```

B.2 Session 2: 4-input Majority Function

Input:

```
Technology: 0.6µm CMOS
Wn = 3.0 µm, Ln = 0.6 µm
Wp = 6.0 µm, Lp = 0.6 µm
VBS = 0 V

Logic Function: Majority of 4 inputs (≥2 ones)
Minterms: 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15
Number of variables: 4
```

Output Summary:

Logic Minimization:

```
SOP Expression: F = AB + AC + AD + BC + BD + CD
(Simplified from 11 minterms to 6 product terms)
```

NAND+NOT Implementation:

```
Total Gates: 19
- NAND gates: 7
- NOT gates: 12
```

NOR+NOT Implementation:

```
Total Gates: 13
- NOR gates: 7
- NOT gates: 6
```

Performance Comparison:

Tabel B. 2 Session 2 Performance

Metric	NAND + NOT	NOR + NOT	Winner
Total Delay	4.23 ns	4.87 ns	NAND + NOT
Bit Rate	236 MHz	205 MHz	NAND + NOT
Area	156.4 µm²	142.8 µm²	NOR + NOT
Power	78.5 µW	71.2 µW	NOR + NOT

Recommendation:

```
RECOMMENDED DESIGN: NAND+NOT
Primary Reason: Superior speed (15% faster)
Application: Suitable for high-speed voting circuits
```

Appendix C: Code Documentation

C.1 Source Code

The complete implementation is available here: Check Here

C.1.2 constants.py

```
"""
Physical Constants and Technology Parameters
===========================================
Classes:
1. PhysicalConstants
   - q: Electron charge (1.602e-19 C)
   - eps_0: Vacuum permittivity (8.854e-12 F/m)
   - eps_si: Silicon permittivity (11.7 × eps_0)
   - Vt: Thermal voltage (0.0259 V)
   - ni: Intrinsic carrier concentration (1.45e16 m^-3)
   - VDD: Supply voltage (5.0 V)
2. CMOSDatasheet
   - datasheets: Dictionary of technology parameters
     * Keys: Technology names (e.g., "1.0um CMOS")
     * Values: Dictionaries with 18 parameters each
Usage:
    from constants import PhysicalConstants, CMOSDatasheet
    constants = PhysicalConstants()
    tech = CMOSDatasheet.datasheets["0.5um CMOS"]
"""
```

C.1.2 mosfet.py

```
"""
MOSFET Parameter Calculations
=============================
Class: MOSFET
Attributes:
    tech: Technology parameters dictionary
    Wn, Ln, Wp, Lp: Transistor dimensions
    VBS: Body-source voltage
    Kn, Kp: Transconductance parameters (μA/V²)
    Vth_n, Vth_p: Threshold voltages
    Various capacitance parameters (Cgd, Cdb, Cgb in F)
Methods:
    __init__(tech, Wn, Ln, Wp, Lp, VBS=0)
        Initialize MOSFET with given parameters
    calculate_parameters()
        Calculate Cox, Kn, Kp, Vth, etc.
      calculate_capacitances()
        Calculate all capacitance values for different operating regions
        display_parameters()
        Display parameters in formatted tables
Key Formulas Implemented:
    - Cox = (E_ox × ε₀) / T_ox
    - Kn = μ_n × Cox × (Wn/Ln) × 1e6
    - Kp = μ_p × Cox × (Wp/Lp) × 1e6
    - Vth with body effect: V_th_po + K_1p × (√(ψ_p + V_BS) - √(ψ_p))
"""
```

C.1.3 delay_calculator.py

```
"""
Exact Gate Delay Calculations
==============================

Class: DelayCalculator
----------------------
Methods:
    calculate_not_gate_delay(n=1)
        Calculate NOT gate delays using exact formulas

    calculate_nor_gate_delay(n)
        Calculate NOR gate delays using exact analytical models

    calculate_nand_gate_delay(n)
        Calculate NAND gate delays using exact analytical models

Mathematical Models:
    All methods implement the exact formulas from Appendix A
    Includes detailed step-by-step calculations
    Fallback to RC model for invalid logarithmic arguments

Output:
    Returns (delay_minus, delay_plus) in nanoseconds
    Prints detailed calculation steps
"""
```

C.1.4 performance_analyzer.py

```
"""
Performance Analysis Module
==========================

Class: PerformanceAnalyzer
--------------------------
Methods:
    calculate_area(gate_details)
        Calculate total area using: n×W_n(l_n+2L_Dn) + w_p(l_p+2L_Dp)

    calculate_v_inss(Kn_total, Kp_total)
        Calculate input switching voltage

    calculate_max_power(G, Kn_total)
        Calculate maximum power dissipation

    analyze_nand_design(nand_gates, not_gates, gate_details)
        Complete analysis of NAND+NOT implementation

    analyze_nor_design(nor_gates, not_gates, gate_details)
        Complete analysis of NOR+NOT implementation

Key Features:
    - Per-gate area calculation
    - Detailed power analysis
    - Comprehensive delay analysis
    - Performance summary generation
"""
```

C.1.5 logic_minimizer.py

```
"""
Logic Function Minimization
===========================

Class: LogicMinimizer
---------------------
Methods:
    input_function()
        Get user input for logic function

    quine_mccluskey()
        Implement Quine-McCluskey algorithm

    generate_kmap()
        Generate and display K-Map

    generate_sop_expression()
        Generate minimized SOP expression

Algorithm Details:
    - Supports 2-6 variables
    - Handles both SOP and POS forms
    - Supports don't care terms
    - Color-coded K-Map display
    - Prime implicant identification
"""
```

C.1.6 design_implementer.py

```
"""
Design Implementation Module
===========================

Class: DesignImplementer
------------------------
Methods:
    convert_to_nand_not()
        Implement design using NAND+NOT logic

    convert_to_nor_not()
        Implement design using NOR+NOT logic

Implementation Strategies:
    NAND+NOT:
        1. NOT gates for complemented variables
        2. NAND gates for product terms
        3. Inverters for De Morgan's
        4. Final NAND gate for OR function

    NOR+NOT:
        1. NOT gates for complemented variables
        2. NOR gates for product terms
        3. Final NOR gate for OR function
"""
```

C.1.7 comparator.py

```
"""
Design Comparison Module
========================

Class: Comparator
-----------------
Methods:
    compare_implementations()
        Comprehensive comparison of NAND vs NOR implementations

Comparison Criteria:
    1. Gate Count
    2. Total Delay
    3. Bit Rate
    4. Area
    5. Power

Optimization Scoring:
    - 1 point for each criterion where design is better
    - 4 points total
    - Tie breaker: Minimum area

Output:
    - Detailed comparison tables
    - Optimization analysis
    - Design recommendation
"""
```

C.1.8 main.py

```
"""
Main Application Controller
===========================

Functions:
    main()
        Main program flow

Program Flow:
    1. Initialize and display welcome message
    2. Select technology node
    3. Input MOSFET parameters
    4. Input logic function
    5. Perform logic minimization
    6. Implement both designs
    7. Analyze performance
    8. Compare and recommend

Error Handling:
    - Import errors
    - Value errors
    - Index errors
    - Division by zero
    - General exceptions
"""
```