COMSATS University Islamabad, Lahore Campus

Block–B, Department of Electrical & Computer Engineering
1.5KMDefenceRoad, Off Raiwind Road, Lahore

COURSE DESCRIPTION FILE

1	**Course Title**	Computer Organization & Architecture
2	**Course Code**	CPE343
3	**Credit Hours**	4 (3,1)
4	**Prerequisites**	CPE241
5	**Semester**	Fall 2024
6	**Resource Person/Lab Engineer**	Dr. Muhammad Naeem Awais
7	**Contact Hours (Theory)**	3 hours per week
8	**Contact Hours (Lab)**	3 hours per week
9	**Office Hours**	10:00 AM to 4:00 PM (weekdays)
10	**Email**	naeem.awais@cuilahore.edu.pk
11	**Major Course Contents**	

Introduction to computer organization, MIPS ISA, Arithmetic operations in computers, Integer and floating-point operations, Measuring and improving the performance of a computer, ALU design, Data path implementation, Single cycle data path, Multi cycle data path implementation, Control path, Introduction and overview of pipelining, Pipeline hazards, Memory hierarchy, Direct mapped cache memory, Set associative mapped cache memory, Fully associative mapped cache memory, Virtual memory, TLB, Disk storage, I/O devices, Multiprocessor Organization, Clusters, Network Topologies, Difference between CISC and RICS machines.

12	**Textbook:**

Textbook:

1. Computer organization and design: The hardware/software interface by David A. Patterson & John L. Hennessy 5th edition

Reference Books:

1. Computer organization and architecture designing for performance by William Stallings 8th edition
2. Computer system organization and architecture by John D. Capinelli
3. Computer Architecture – A quantitative approach by Hennessy and Patterson

13	Course Learning Outcomes (CLOs)

Theory Part:

After successfully completing this course, the students will be able to:

1. **Apply** suitable arithmetic algorithms to solve basic computer arithmetic using hardware, and **produce** assembly code for a high-level language code using MIPS instruction set to lay the foundations of a simplified processor design. (PLO2-C3)
2. **Design** a datapath for single-cycle, multi-cycle and pipelined MIPS architecture using different hardware modules. (PLO3-C5)
3. **Compute** the performance of computer programs, modern processors, the cache systems using terms related to various hardware/software constituents to highlight tradeoffs between different design choices. (PLO3-C3)

Lab. Part:

4. **Follow** the procedure to assemble different parts of the MIPS 32-bit microprocessor in HDL and reproduce its response using a software tool and hardware platform. (PLO5-P3)

14	Tentative Lecture Plan						
Week	**Topic**	**CLO**	**Specific Outcome**	**Contact Hours**	**Students Learning Hours**	**Bloom Taxonomy**	**Assessment**
1	Introduction to Computer Organization & Architecture, Difference between computer architecture and computer organization, Brief history of computer evolution, Classes of computers, Basic Terminology, Functional Units of Computer, Bus Structure in CPU, Classification of Instructions, Instruction Set Architecture	CLO 1	To understand the difference between Computer Organization & Architecture, their related terminologies and relate these concepts to modern processor design.	3	4	PLO2-C3	

2, 3	Number Systems, Conversion among number systems, Signed number representation, Operations on integers: Addition and subtraction, Hardware for Addition and subtraction, Multiplication, Multiplication Algorithm, Hardware for Multiplication, Division, Division Algorithm, Hardware for Division, Signed Number Arithmetic: Multiplication and Division of Signed Numbers using Un-signed Number Arithmetic Methods, Floating Point Representation, Floating Point Arithmetic: Addition, Subtraction, Multiplication and Division	CLO 1	To understand arithmetic algorithms and apply these arithmetic algorithms to solve basic computer arithmetic using hardware to lay the foundations of a simplified processor design.	6	8	PLO2-C3	Q1, A1, Midterm

4, 5	MIPS R3000 ISA, Registers in MIPS Processor, Introduction to MIPS Programming, MIPS Programmer's Model, MIPS-Register File, Assembly Variables: Registers, Comments in Assembly, Assembly Instructions: MIPS Addition and Subtraction Instructions, Memory Addressing, Addressing Modes, Load from Memory Instruction, Store to Memory Instruction, Variable Array Index, Pointers vs Values, Control instructions: conditional branches, set on less than, Handling of If Then Else statements, Handling of While Loop, Procedures: Jump and link instruction, Stack, Storage management on call/return, Leaf Procedure Example, Nested Procedures, Dealing with characters, Assembly to Machine Conversion for R-type, I-type and J-type Instructions, Machine to Assembly Conversion	CLO 1	To understand assembly language and produce assembly code for a high-level language code using MIPS instruction set to lay the foundations of a simplified processor design.	6	8	PLO2-C3	Q2, A2, Midterm, Terminal

6, 7	Logic Design Basics, Clock Terminology, Instruction Execution, Datapath Overview, Register files: Implementing the read port and the write port, SRAM: Read and Write in SRAMs, Addressing in SRAMs, DRAM: Read and Write in DRAMS, DRAM chip organization, Addressing in DRAMs, MIPS Datapath Building: Building Datapath for R-Type instructions such as add, sub, AND, OR etc, Building Datapath for I-Type instructions such as lw, sw, addi etc, Building Datapath for beq and bne Instructions, Building Datapath for J-Type Instruction, Datapath Integration	CLO 2	To design a datapath for a single cycle MIPS architecture using different hardware modules.	6	8	PLO3-C5	Q3, A3, Midterm, Terminal
8	Controlling operations in Processor, Building Control Unit for ALU and Main Control Unit	CLO 2	To design a control unit for the datapath of a single cycle MIPS architecture .	3	4	PLO3-C5	
9	Single-cycle vs Multicycle, Multicycle MIPS Datapath, Different stages of multicycle, Design of Control Unit for Multicycle MIPS Datapath	CLO 2	To design a datapath for a multi-cycle MIPS architecture using different hardware modules.	3	4	PLO3-C5	
10	An overview of pipelining, MIPS pipelined datapath, MIPS pipelined control, Pipeline Hazards & their elimination: Structural hazard (Memory & Register File), Pipeline Hazards & their	CLO 2	To design a datapath for a pipelined MIPS architecture using different	3	4	PLO3-C5	

	elimination: Data Hazards (RAW, WAR, WAW), Control Hazard		hardware modules.				
11	Branch Prediction: Static Brach Prediction (Branch Taken, Branch Not-taken, Delayed Branch), Dynamic Branch Prediction (1-bit and 2-bit), Branch Prediction Buffer	CLO 3	Compute the performance of computer system in presence of difference branch predictors and to highlight tradeoffs between different design choices.	3	4	PLO3-C3	Q4, A4, Terminal
12	Multi-cycle Floating Point (FP) MIPS Pipeline, MIPS FP Pipeline supporting multiple FP Operations, Hazards in MIPS FP pipeline, Performance of CPU	CLO 3	Compute the performance of MIPS FP Pipeline supporting multiple FP in presence of difference hazards and to highlight tradeoffs between different design choices.	3	4	PLO3-C3	

13, 14	Cache Memory: Processor Memory Performance Gap, Relationship of Caches and Pipeline, Memory Hierarchy, CPU-Cache Interaction, General Organization of Cache, Addressing Cache, Addressing Cache, Types of Cache, Block Placement, Accessing Direct-Mapped Caches, Block Identification-Direct Mapped, Accessing Set Associative Caches, Block Identification-Set Associative, Block Identification-Fully Associative, Block Replacement, Write Strategy, Write allocation, Types of Cache Misses, Problems	CLO 3	Compute the performance of computer system in presence of difference Cache organizations and to highlight tradeoffs between different design choices.	6	8	PLO3-C3	
15	Virtual Memory, Virtual Address, Virtual Address Translation into Physical Address, Page Table, Translation Lookaside Buffer	CLO 3	Compute the performance of computer system in presence of Virtual Memory.	3	4	PLO3-C3	

15	Assessment Plan

Theory

Quizzes (minimum 4)	15%
Homework assignments (minimum 4)	10%
1 Midterm exam (in class, 90 minutes)	25%
Terminal exam (3 hours)	50%
Total (theory)	**100%**

Lab

Lab assessments	25%
1 Midterm exam (in class, 180 minutes)	25%
Lab Terminal exam (50% Lab performance + 50% Lab assessments)	50%
Total (lab)	**100%**

Final Marks	Theory marks * 0.75 + Lab marks * 0.25

16	Course Learning Outcomes (CLOs) and Assessment Plan																						
CLO / Activity	CLO 1	CLO2	CLO3	CLO4	CLO5	Cognitive Domain						Affective Domain					Psychomotor Domain						
						C1	C2	C3	C4	C5	C6	A1	A2	A3	A4	A5	P1	P2	P3	P4	P5	P6	P7
Quiz 1	X							X															
Assignment 1	X							X															
Quiz 2	X							X															
Assignment 2	X							X															
Lab Midterm					X														X				
Midterm	X	X						X		X													
Quiz 3		X								X													
Assignment 3		X								X													
Quiz 4			X					X															
Assignment 4			X					X															
Terminal	X	X	X					X		X													
Lab Terminal					X														X				

17	Mapping of CLOs to PLOs

PLO1	**Engineering Knowledge:** An ability to apply knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems. **(Cognitive)**
PLO2	**Problem Analysis:** An ability to identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principlesofmathematics,naturalsciencesandengineeringsciences.**(Cognitive)**
PLO3	**Design/Development of Solutions:** An ability to design solutions for complex engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations. **(Cognitive)**
PLO4	**Investigation:** An ability to investigate complex engineering problems in a methodical way including literature survey, design and conduct of experiments, analysis and interpretation of experimental data, and synthesis of information to derive valid conclusions. **(Cognitive, Psychomotor)**
PLO5	**Modern Tool Usage:** An ability to create, select and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities, with an understanding of the limitations. **(Psychomotor)**
PLO6	**The Engineer and Society:** An ability to apply reasoning informed by contextual knowledge to assess societal health, safety, legal and cultural issues and the consequent responsibilities relevant to professional engineering practice and solution to complex engineering problems. **(Cognitive)**
PLO7	**Environment and Sustainability:** An ability to understand the impact of professional engineering solutions in societal and environmental contexts and demonstrate knowledge of and need for sustainable development. **(Cognitive)**
PLO8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of engineering practice. **(Affective)**
PLO9	**Individual and Teamwork:** An ability to work effectively, as an individual or in a team, on multi-faceted and/or multidisciplinary settings. **(Affective)**
PLO10	**Communication:** An ability to communicate effectively, orally as well as in writing, on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions. **(Affective)**
PLO11	**Project Management:** An ability to demonstrate management skills and apply engineering principle to one's own work, as a member and/or leader in a team, to manage projects in a multidisciplinary environment. **(Affective)**
PLO12	**Lifelong Learning:** An ability to recognize importance of and pursue lifelong learning in the broader context of innovation and technological developments. **(Affective)**

PLO / CLOs	PLO1	PLO2	PLO3	PLO4	PLO5	PLO6	PLO7	PLO8	PLO9	PLO10	PLO11	PLO12	Cognitive Domain						Affective Domain					Psychomotor Domain						
													C1	C2	C3	C4	C5	C6	A1	A2	A3	A4	A5	P1	P2	P3	P4	P5	P6	P7
CLO1		X													X															
CLO2			X														X													
CLO3			X												X															
CLO4 (LAB)					X																					X				

18	PLOs Coverage Explanation

PLO 2 - Problem Analysis:

The students learn to apply various arithmetic algorithms to solve basic computer arithmetic using hardware, and produce assembly code for a high-level language code using MIPS instruction set to lay the foundations of a simplified processor design.

PLO 3 -Design/Development of Solutions:

The students learn to design a datapath for single-cycle, multi-cycle and pipelined MIPS architecture using different hardware modules and learn to evaluate different design solutions (relating to processors and memory systems) using various tradeoffs to come up with the best possible solution keeping in view the purpose of the design.

PLO 5 –Modern Tool Usage:

The students learn VHDL – a design tool to simulate integrated circuits – to design a processor using bottom-up approach. They have to implement this on FPGA to show its working and analyze its performance.

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Annexure - 1

List of Experiments

Lab #	Experiment Title
01	Explain VHDL and Altera Quartus tool with the design of combinational circuit
02	Display the output of combinational circuit using conditional signal assignments in VHDL programming
03	Display the output of combinational circuit using library building technique of VHDL programming
04	Display the output of the sequential circuit using VHDL programming techniques
05	Follow the steps to reproduce the sequential circuit using advanced VHDL programming techniques
06	Explain LCD programming using VHDL and implementation on FPGA
07	Follow the steps to reproduce digital circuits using procedures and packages in VHDL
08	Follow the steps to reproduce the Fetch module of MIPS 32-bit microprocessor using VHDL and implementation on FPGA
09	Follow the steps to reproduce the Decode module of MIPS 32-bit Microprocessor using VHDL and implementation on FPGA
10	Follow the procedure to reproduce the Control unit and Data Memory of MIPS 32-bit microprocessor using VHDL and implementation on FPGA
11	Follow the steps to reproduce the Execution unit of MIPS 32-bit Microprocessor using VHDL and implementation on FPGA
12	Follow the steps to reproduce the single cycle MIPS 32-bit microprocessor using VHDL
13	Show the results of single cycle MIPS 32-bit microprocessor on FPGA