Lab Task_01

Binary counter using D Flip-Flop

ENTITIES:

1: DLatch

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY myDLatch is port (
    clk   : in std_logic;
    D     : in std_logic;
    Q     : out std_logic;
    Q_not : out std_logic
);

end myDLatch;

architecture bhv of myDLatch is
begin
    process (clk)
        begin
            if clk = '1' then
                Q <= D;
                Q_not <= not D ;
            end if;
    end process;
end bhv;
```

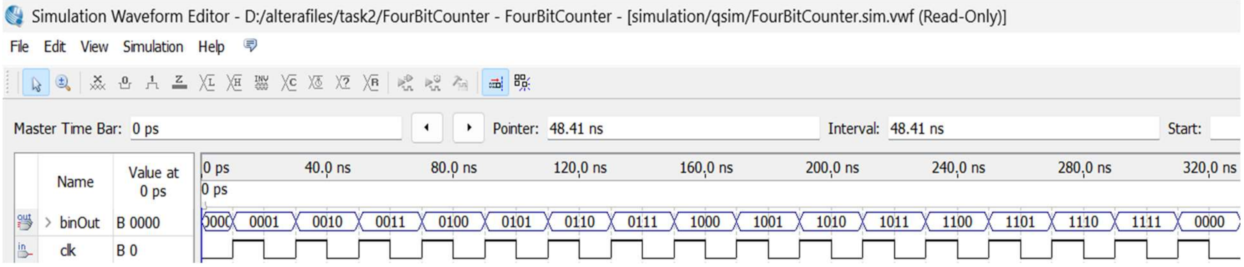
PACKAGE:

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

package My_Package is
    component myDLatch is
        port (
            clk   : in std_logic;
            D     : in std_logic;
            Q     : out std_logic;
            Q_not : out std_logic
        );
    end component;
end package My_Package;
```

TOP-ENTITY(Wrapper File)

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE WORK.My_Package.ALL;

ENTITY FourBitCounter IS
    PORT (
        o_output : OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
        clk     : IN  STD_LOGIC
    );
END FourBitCounter;

ARCHITECTURE bhv OF FourBitCounter IS
    SIGNAL q    : STD_LOGIC_VECTOR(3 DOWNTO 0);
    SIGNAL qnot : STD_LOGIC_VECTOR(3 DOWNTO 0);
    SIGNAL d    : STD_LOGIC_VECTOR(3 DOWNTO 0);
BEGIN
    U1 : myDLatch PORT MAP (clk, d(0), q(0), qnot(0));
    U2 : myDLatch PORT MAP (clk, d(1), q(1), qnot(1));
    U3 : myDLatch PORT MAP (clk, d(2), q(2), qnot(2));
    U4 : myDLatch PORT MAP (clk, d(3), q(3), qnot(3));

    d(0) <= NOT q(0);
    d(1) <= q(1) XOR q(0);
    d(2) <= q(2) XOR (q(1) AND q(0));
    d(3) <= q(3) XOR (q(2) AND q(1) AND q(0));

    o_output <= q;

END bhv;
```

Simulation:



Simulation Waveform Editor - D:/alterafiles/task2/FourBitCounter - FourBitCounter - [simulation/qsim/FourBitCounter.sim.vwf (Read-Only)]

Master Time Bar: 0 ps

Pointer: 48.41 ns

Interval: 48.41 ns

Start:

Name	Value at 0 ps
binOut	B 0000
clk	B 0

Simulation 1 :Four-Bit up Counter with Clock Positive Edge Sensitive

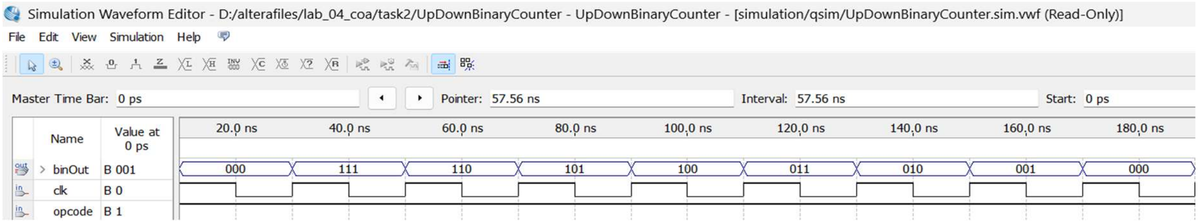
Lab Task_02

Up/Down Binary counter

TOP-ENTITY(Wrapper File)

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE WORK.My_Package.ALL;

ENTITY UpDownBinaryCounter IS
    PORT (
        binOut : OUT STD_LOGIC_VECTOR(2 DOWNTO 0);
        opcode : IN  STD_LOGIC;
        clk    : IN  STD_LOGIC
    );
END UpDownBinaryCounter;

ARCHITECTURE bhv OF UpDownBinaryCounter IS

    SIGNAL q : STD_LOGIC_VECTOR(2 DOWNTO 0);
    SIGNAL qnot : STD_LOGIC_VECTOR(2 DOWNTO 0);
    SIGNAL d : STD_LOGIC_VECTOR(2 DOWNTO 0);
BEGIN
    U1 : myDLatch PORT MAP ( clk, d(0), q(0), qnot(0));
    U2 : myDLatch PORT MAP ( clk, d(1), q(1), qnot(1));
    U3 : myDLatch PORT MAP ( clk, d(2), q(2), qnot(2));

    d(0) <= NOT q(0);
    d(1) <= (q(1) XOR q(0)) WHEN opcode = '0' ELSE (q(1) XOR qnot(0));
    d(2) <= (q(2) XOR (q(1) AND q(0))) WHEN opcode = '0' ELSE (q(2) XOR
(qnot(1) AND qnot(0)));
 binOut <= q;
END bhv;
```

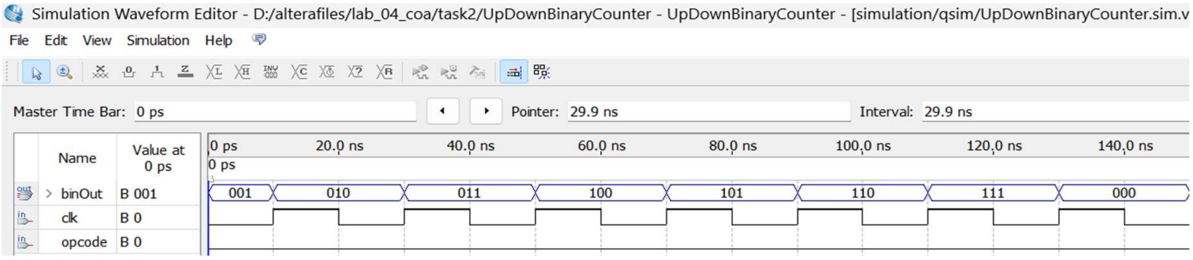
Simulation:



Simulation Waveform Editor - D:/alterafiles/lab_04_coa/task2/UpDownBinaryCounter - UpDownBinaryCounter - [simulation/qsim/UpDownBinaryCounter.sim.vwf (Read-Only)]

Master Time Bar: 0 ps   Pointer: 57.56 ns   Interval: 57.56 ns   Start: 0 ps

Name	Value at 0 ps
binOut	B 001
clk	B 0
opcode	B 1


Simulation Waveform Editor - D:/alterafiles/lab_04_coa/task2/UpDownBinaryCounter - UpDownBinaryCounter - [simulation/qsim/UpDownBinaryCounter.sim.v
File
Edit
View
Simulation
Help
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
140.0 ns
0 ps
001
010
011
100
101
110
111
000

Master Time Bar: 0 ps

Pointer: 29.9 ns

Interval: 29.9 ns

Name	Value at 0 ps
binOut	B 001
clk	B 0
opcode	B 0

Simulation 2: :Three-Bit up-down Counter with Clock Positive Edge Sensitive