**Lab Task 2:**

**Implement a 4-bit sequence detector(1011)**

**VHDL Code:**

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**std\_logic\_unsigned**.all;**

**entity** FSM\_sequence\_detactor **is**

**port** **(**

clk **:** **in** std\_logic**;**

letstart **:** **in** std\_logic**;**

y **:** **out** std\_logic

**);**

**end** FSM\_sequence\_detactor**;**

**architecture** bhv **of** FSM\_sequence\_detactor **is**

--define state using one hot coding

**constant** state0 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "00001"**;**

**constant** state1 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "00010"**;**

**constant** state2 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "00100"**;**

**constant** state3 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "01000"**;**

**constant** state4 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "10000"**;**

-- State Memory

**signal** mystate **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** state0**;** -- 00001

**begin**

**process** **(**clk**)**

**begin**

**if** **(**clk'**event** **and** clk **=** '1'**)** **then** -- positive edge sensitive

**case** mystate **is**

------

**when** state0 **=>**

y **<=** '0'**;**

**if** **(**letstart **=** '1'**)** **then**

mystate **<=** state1**;**

**else** -- 0

mystate **<=** state0**;**

**end** **if;**

------

**when** state1 **=>**

y **<=** '0'**;**

**if** **(**letstart **=** '0'**)** **then**

mystate **<=** state2**;**

**else** -- 1

mystate **<=** state1**;**

**end** **if;**

------

**when** state2 **=>**

y **<=** '0'**;**

**if** **(**letstart **=** '1'**)** **then**

mystate **<=** state3**;**

**else** --0

mystate **<=** state0**;**

**end** **if;**

------

**when** state3 **=>**

y **<=** '1'**;**

**if** **(**letstart **=** '1'**)** **then**

mystate **<=** state4**;**

**else** -- 0

mystate **<=** state2**;**

**end** **if;**

------

**when** state4 **=>**

y **<=** '1'**;**

**if** **(**letstart **=** '1'**)** **then**

mystate **<=** state0**;**

**else** -- 0

mystate **<=** state0**;**

**end** **if;**

------

**when** **others** **=>**

mystate **<=** state0**;**

------

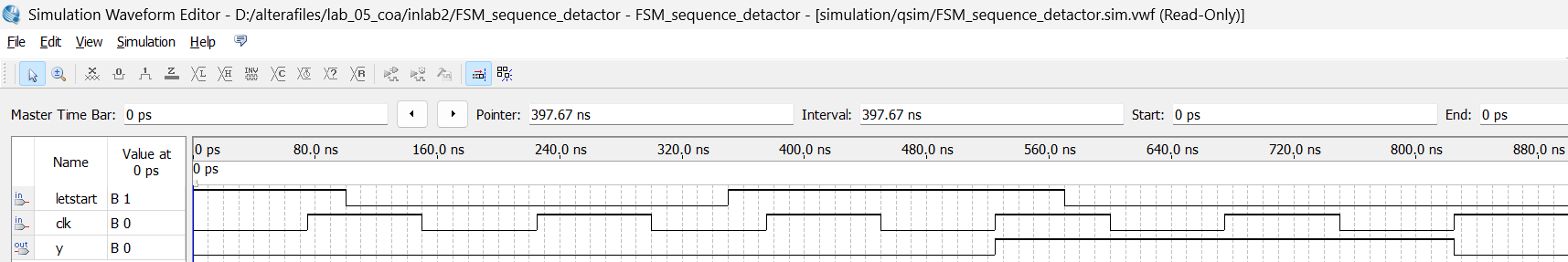
**end** **case;**

**end** **if;**

**end** **process;**

**end** bhv**;**

**Simulation:**



Simulation 1: detects the input(let start) pattern of 1011

**Lab Task 2:**

**Implement a 4-bit sequence detector(1011)**

**VHDL Code:**

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**use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**std\_logic\_unsigned**.all;**

**entity** FSM\_sequence\_detactor **is**

**port** **(**

clk **:** **in** std\_logic**;**

letstart **:** **in** std\_logic**;**

y **:** **out** std\_logic

**);**

**end** FSM\_sequence\_detactor**;**

**architecture** bhv **of** FSM\_sequence\_detactor **is**

--define state using one hot coding

**constant** state0 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "00001"**;**

**constant** state1 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "00010"**;**

**constant** state2 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "00100"**;**

**constant** state3 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "01000"**;**

**constant** state4 **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** "10000"**;**

-- State Memory

**signal** mystate **:** std\_logic\_vector**(**4 **downto** 0**)** **:=** state0**;** -- 00001

**begin**

**process** **(**clk**)**

**begin**

**if** **(**clk'**event** **and** clk **=** '1'**)** **then** -- positive edge sensitive

**case** mystate **is**

------

**when** state0 **=>**

y **<=** '0'**;**

**if** **(**letstart **=** '1'**)** **then**

mystate **<=** state1**;**

**else** -- 0

mystate **<=** state0**;**

**end** **if;**

------

**when** state1 **=>**

y **<=** '0'**;**

**if** **(**letstart **=** '0'**)** **then**

mystate **<=** state2**;**

**else** -- 1

mystate **<=** state1**;**

**end** **if;**

------

**when** state2 **=>**

y **<=** '0'**;**

**if** **(**letstart **=** '1'**)** **then**

mystate **<=** state3**;**

**else** --0

mystate **<=** state0**;**

**end** **if;**

------

**when** state3 **=>**

y **<=** '1'**;**

**if** **(**letstart **=** '1'**)** **then**

mystate **<=** state4**;**

**else** -- 0

mystate **<=** state2**;**

**end** **if;**

------

**when** state4 **=>**

y **<=** '1'**;**

**if** **(**letstart **=** '1'**)** **then**

mystate **<=** state0**;**

**else** -- 0

mystate **<=** state0**;**

**end** **if;**

------

**when** **others** **=>**

mystate **<=** state0**;**

------

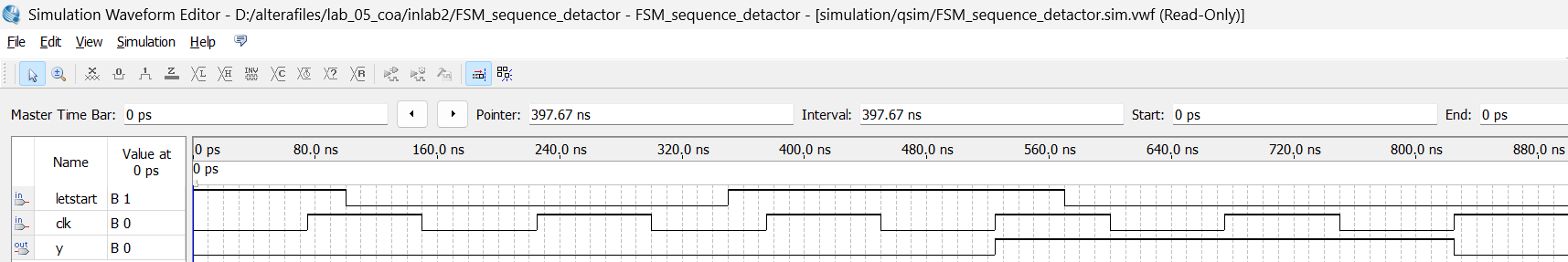
**end** **case;**

**end** **if;**

**end** **process;**

**end** bhv**;**

**Simulation:**



Simulation 1: detects the input(let start) pattern of 1011