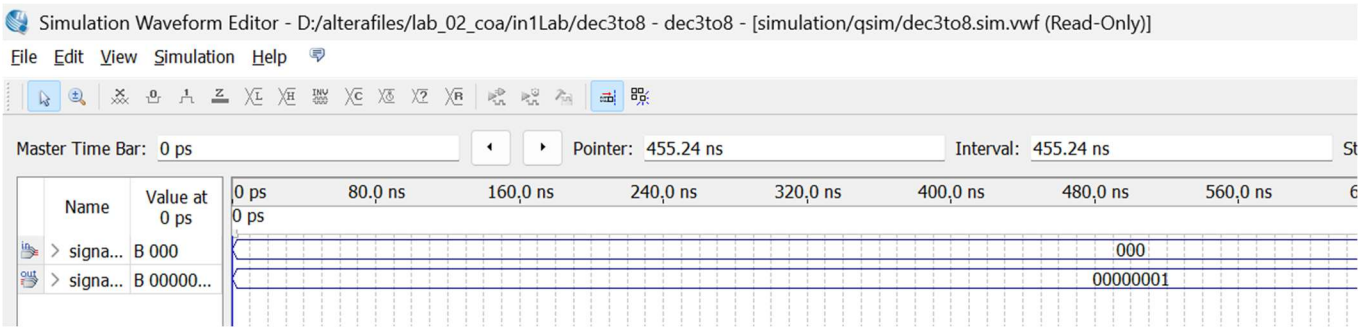
Lab Task_01

Implement the 3-to-8 decoder

VHDL Code:

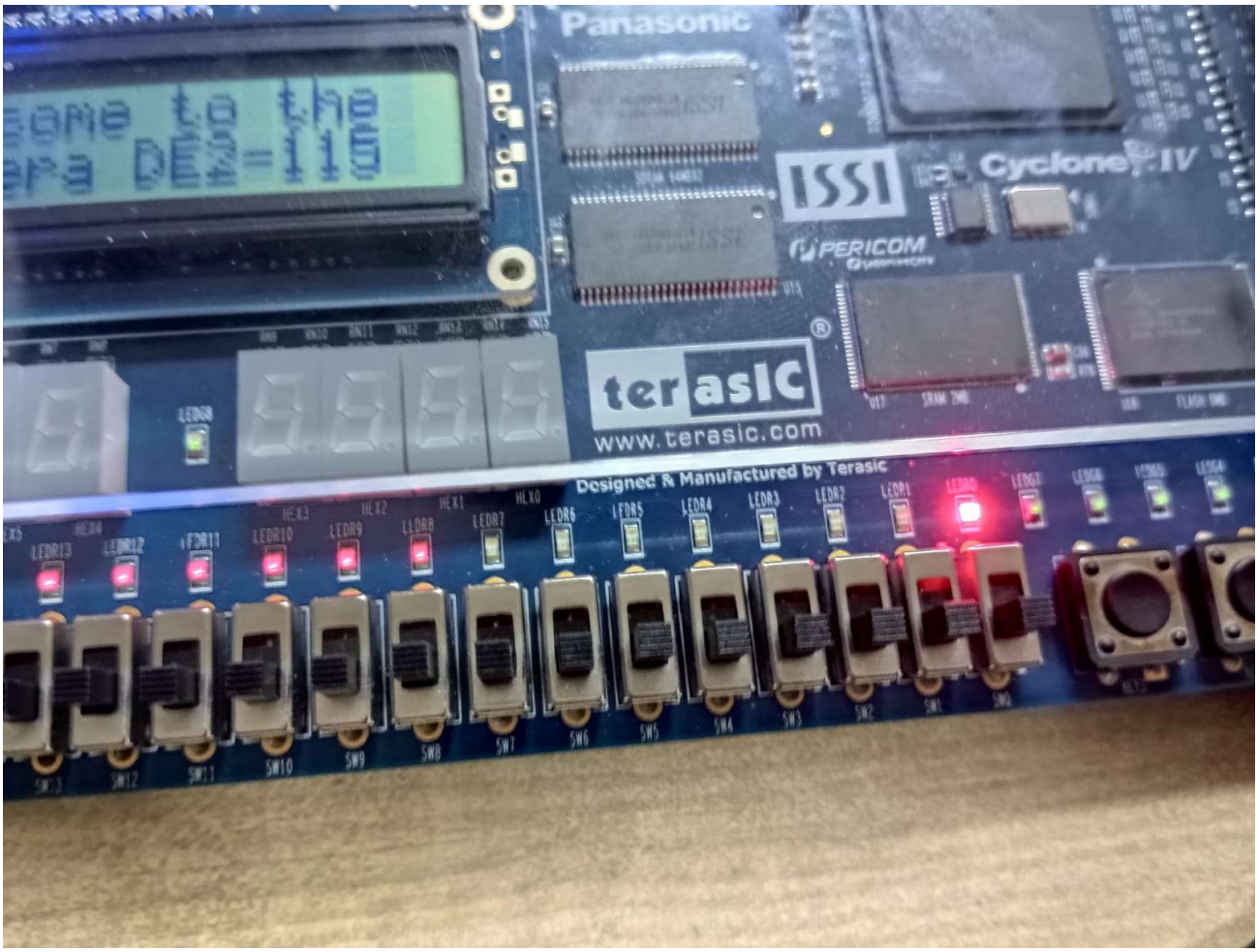
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity dec3to8 is
    port (
        input : in std_logic_vector(2 downto 0);
        output : out std_logic_vector(7 downto 0)
    );
end dec3to8;

architecture Behavioral of dec3to8 is
begin
output <= "00000001" when (input = "000") else
"00000010" when (input = "001") else
"00000100" when (input = "010") else
"00001000" when (input = "011") else
"00010000" when (input = "100") else
"00100000" when (input = "101") else
"01000000" when (input = "110") else
"10000000";
end Behavioral;
```

Simulation:



Simulation 1: *Input is 000, so the respective output is 00000001*

Implementation FPGA Board:



FPGA Hardware 1: *All the three inputs are off (0) so only the first output Led is on (1)*

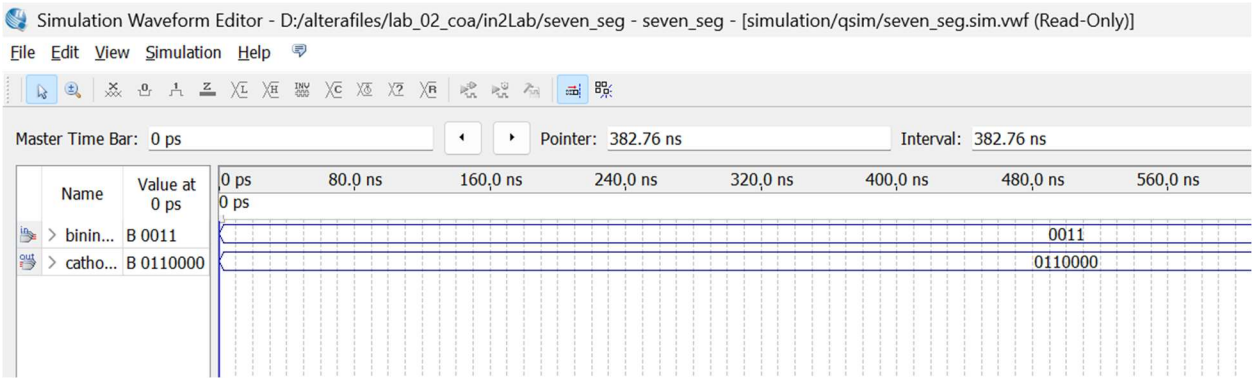
Lab Task_02

Seven Segment Display (SSD)

VHDL Code:

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY seven_seg IS
    PORT(
        bininput : IN std_logic_vector(3 DOWNTO 0);
        cathodes : OUT std_logic_vector(6 DOWNTO 0)
    );
END seven_seg;

architecture dataflow of seven_seg is
begin
    cathodes <= "1000000" when(bininput = "0000") else
                "1111001" when (bininput = "0001") else
                "0100100" when (bininput = "0010") else
                "0110000" when (bininput = "0011") else
                "0011001" when (bininput = "0100") else
                "0010010" when (bininput = "0101") else
                "0000010" when (bininput = "0110") else
                "1111000" when (bininput = "0111") else
                "0000000" when (bininput = "1000") else
                "0010000" when (bininput = "1001") else
                "0001000" when (bininput = "1010") else
                "0000011" when (bininput = "1011") else
                "1000110" when (bininput = "1100") else
                "0100001" when (bininput = "1101") else
                "0000110" when (bininput = "1110") else
                "0001110" when (bininput = "1111") else
                "1111111";
end dataflow;
```

Simulation:



Simulation 2: *Input is 0011, so the respective output is 0110000 which display 3 on seven segment*

Implementation FPGA Board:

FPGA Hardware 2:*First two input pins are on, so input is 0011, which corresponds to 3 at seven segment display*

FPGA Hardware 3: :*First four input pins are on, so input is 1111, which corresponds to F at seven segment display*