Pre Lab-Task

Nand Gate:

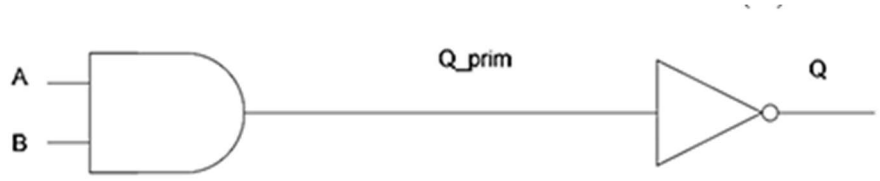


Figure 0 NAND gate using AND & NOT gate

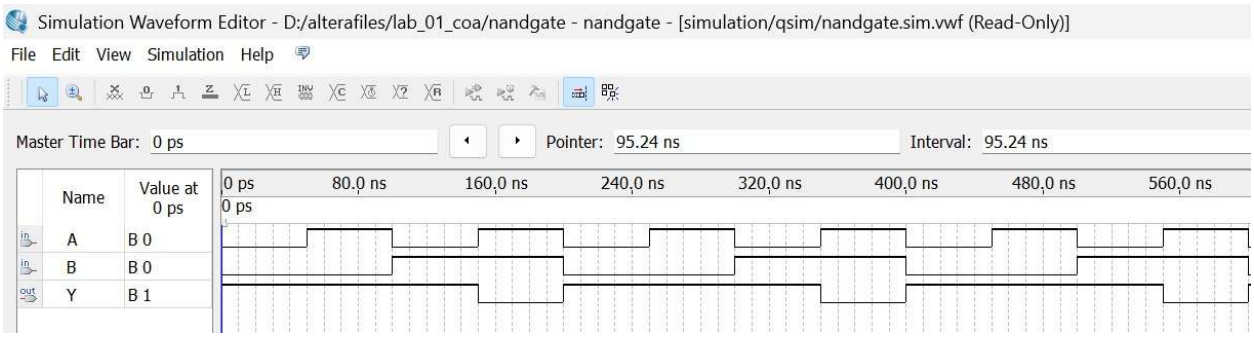
VHDL Code:

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY nandgate IS
    PORT (
        A : IN STD_LOGIC;
        B : IN STD_LOGIC;
        Y : OUT STD_LOGIC
    );
END nandgate;

ARCHITECTURE behavior OF nandgate IS
BEGIN
    Y <= NOT (A AND B);
END behavior;
```

Simulation:



Simulation 1

Lab Task_01

Circuit:

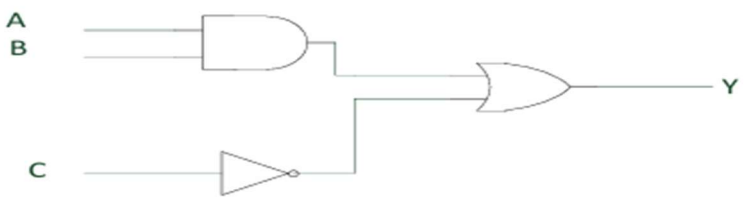


Figure 1 Circuit containing AND,OR&NAND gates

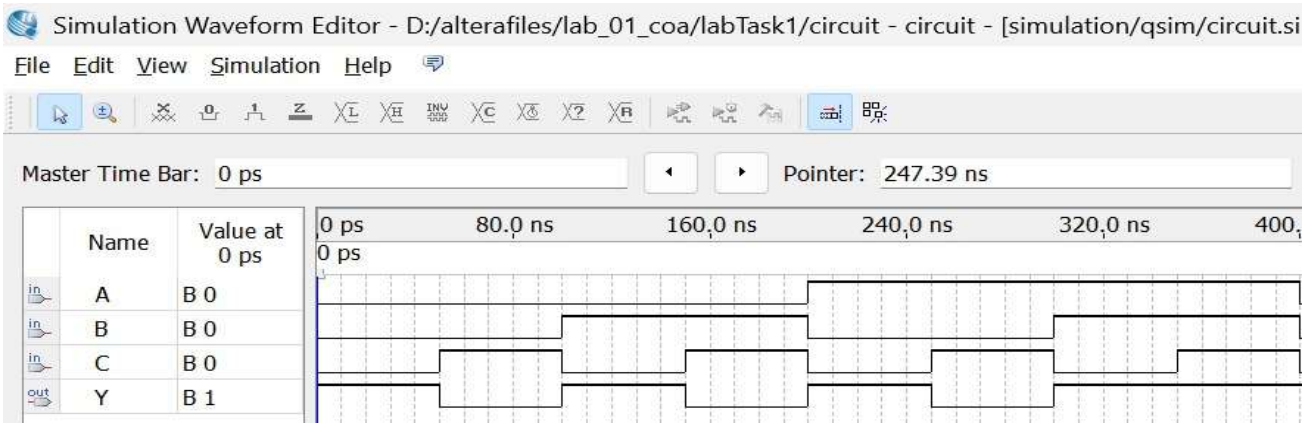
VHDL Code:

```
Library IEEE;
Use IEEE.STD_LOGIC_1164.all;

Entity circuit is
Port(
        A, B , C: IN bit;
        Y : OUT bit
     );
End circuit;

Architecture struct of circuit is
Begin
    Y<= (A AND B) OR (NOT C);
End struct;
```

Simulation:



Simulation 2