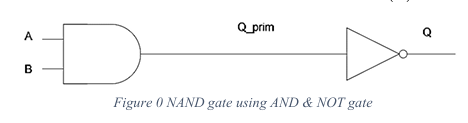
**Pre Lab-Task**

**Nand Gate:**

****

**VHDL Code:**

**LIBRARY** IEEE**;**

**USE** IEEE**.**STD\_LOGIC\_1164**.ALL;**

**ENTITY** nandgate **IS**

**PORT** **(**

A **:** **IN** STD\_LOGIC**;**

B **:** **IN** STD\_LOGIC**;**

Y **:** **OUT** STD\_LOGIC

**);**

**END** nandgate**;**

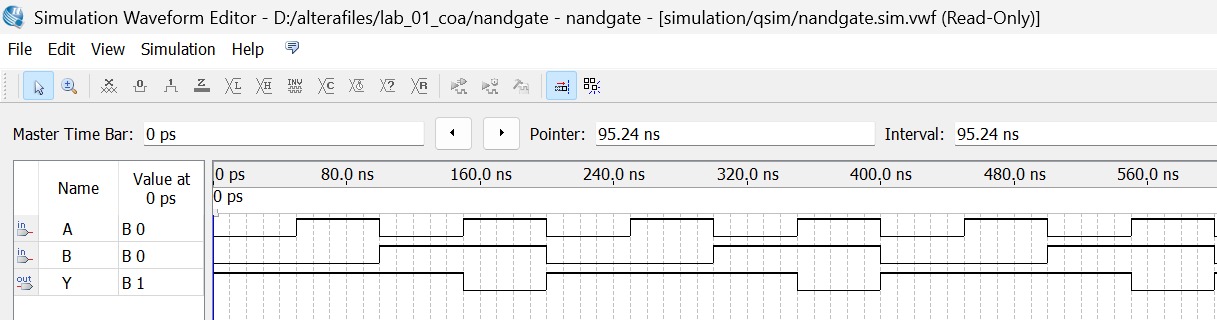
**ARCHITECTURE** behavior **OF** nandgate **IS**

**BEGIN**

Y **<=** **NOT** **(**A **AND** B**);**

**END** behavior**;**

**Simulation:**



Simulation 1

**Lab Task\_01**

**Circuit:**

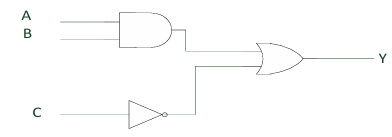
****

Figure 1 Circuit containing AND,OR&NAND gates

**VHDL Code:**

**Library** IEEE**;**

**Use** IEEE**.**STD\_LOGIC\_1164**.all;**

**Entity** circuit **is**

**Port(**

A**,** B **,** C**:** **IN** bit**;**

Y **:** **OUT** bit

**);**

**End** circuit**;**

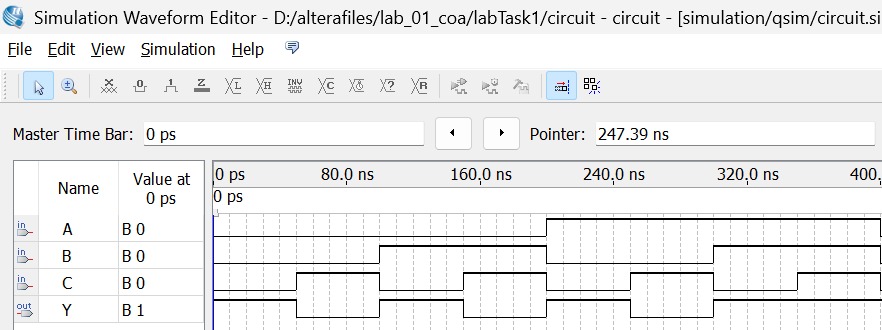
**Architecture** struct **of** circuit **is**

**Begin**

Y**<=** **(**A **AND** B**)** **OR** **(NOT** C**);**

**End** struct**;**

**Simulation:**



Simulation 2