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| Name: Muuhammad Ahmad | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-68 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual**

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| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

1. **TRUTH TABLE**

a,b,c are inputs

x,y are outputs

x = c’ ^ a|b

y = a|b & (a|b ^ (a&b)’)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **a** | **b** | **c** | **x** | **y** |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

1. **Error found in codes:**

**(I) Errors in rtl code:**

**(i.i)** There is a colon in line no 6 after carry which should not be there.

**(i.ii**) No assigning statement to the sum which is output in line no 9.

**(i.iii)** Missing of and operator between c and a XOR b in line no 10.

**(II) Errors in test bench code:**

(i.i) carry1 is not defined locally in full\_adder\_tb

(i.ii) In Line no 7 function name for assigning local inputs to the original input is not written.

(i.iii) In line no 18 there is a,b,c instead of a1,b1,c1 respectively

(i.iv)In line no 20 and 24 30 c , b , a instead of c1, b1 and a1 respectively.

(i.v) missing end statement before endmodule

1. **Corrected Codes**
2. **Rtl code:**

module full\_adder(

input logic a,

input logic b,

input logic c,

output logic sum,

output logic carry

);

assign sum = (a ^ b) ^ c;

assign carry = (a & b) | (c&(a ^ b));

endmodule

1. **Test bench:**

module full\_adder\_tb();

logic a1;

logic b1;

logic c1;

logic sum1;

logic carry1;

full\_adder UUT(

.a(a1),

.b(b1),

.c(c1),

.sum(sum1),

.carry(carry1)

);

initial

begin

// Provide different combinations of the inputs to check validity of code

a1 = 0; b1 = 0; c1 = 0;

#10;

a1 = 0; b1 = 0; c1 = 1;

#10;

a1 = 0; b1 = 1; c1 = 0;

#10;

a1 = 0; b1 = 1; c1 = 1;

#10;

a1 = 1; b1 = 0; c1 = 0;

#10;

a1 = 1; b1 = 0; c1 = 1;

#10;

a1 = 1; b1 = 1; c1 = 0;

#10

a1 = 1; b1 = 1; c1 = 1;

#10;

$stop;

end

endmodule