|  |  |
| --- | --- |
| Name: Muhammad Ahmad | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-68 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual**

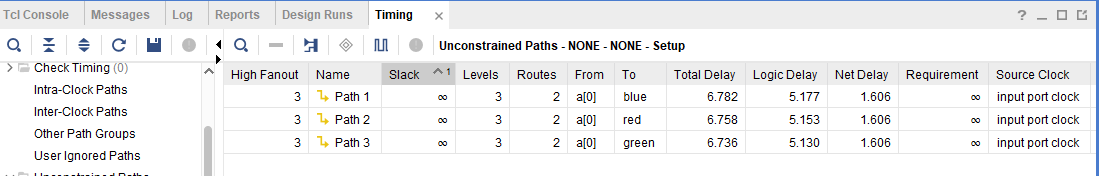
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

**Truth Table:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **a[1]** | **a[0]** | **b[1]** | **b[0]** | **red** | **green** | **blue** | **Result** |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | Y |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | C |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | C |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | C |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | P |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | Y |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | C |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | C |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | P |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | P |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | Y |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | C |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | P |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | P |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | P |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | Y |

**(e) Maximum combinational delay:**

My mamimum combinational delay is from a[0] to blue and that is 6.782



**(f) Sources in FPGA:**

+-------------------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-------------------------+------+-------+-----------+-------+

| Slice LUTs\* | 2 | 0 | 63400 | <0.01 |

| LUT as Logic | 2 | 0 | 63400 | <0.01 |

| LUT as Memory | 0 | 0 | 19000 | 0.00 |

| Slice Registers | 0 | 0 | 126800 | 0.00 |

| Register as Flip Flop | 0 | 0 | 126800 | 0.00 |

| Register as Latch | 0 | 0 | 126800 | 0.00 |

| F7 Muxes | 0 | 0 | 31700 | 0.00 |

| F8 Muxes | 0 | 0 | 15850 | 0.00 |

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| Ref Name | Used | Functional Category |

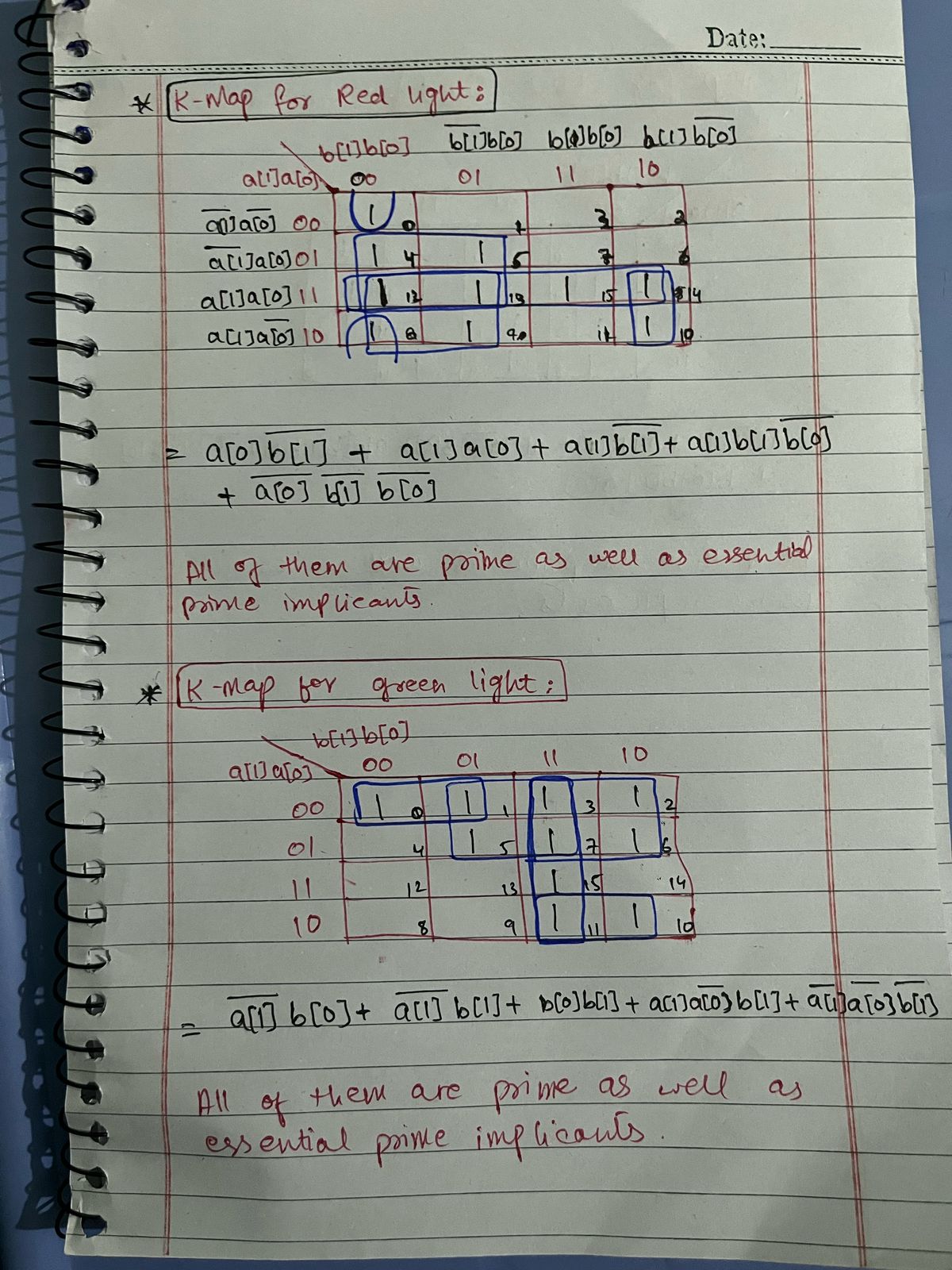
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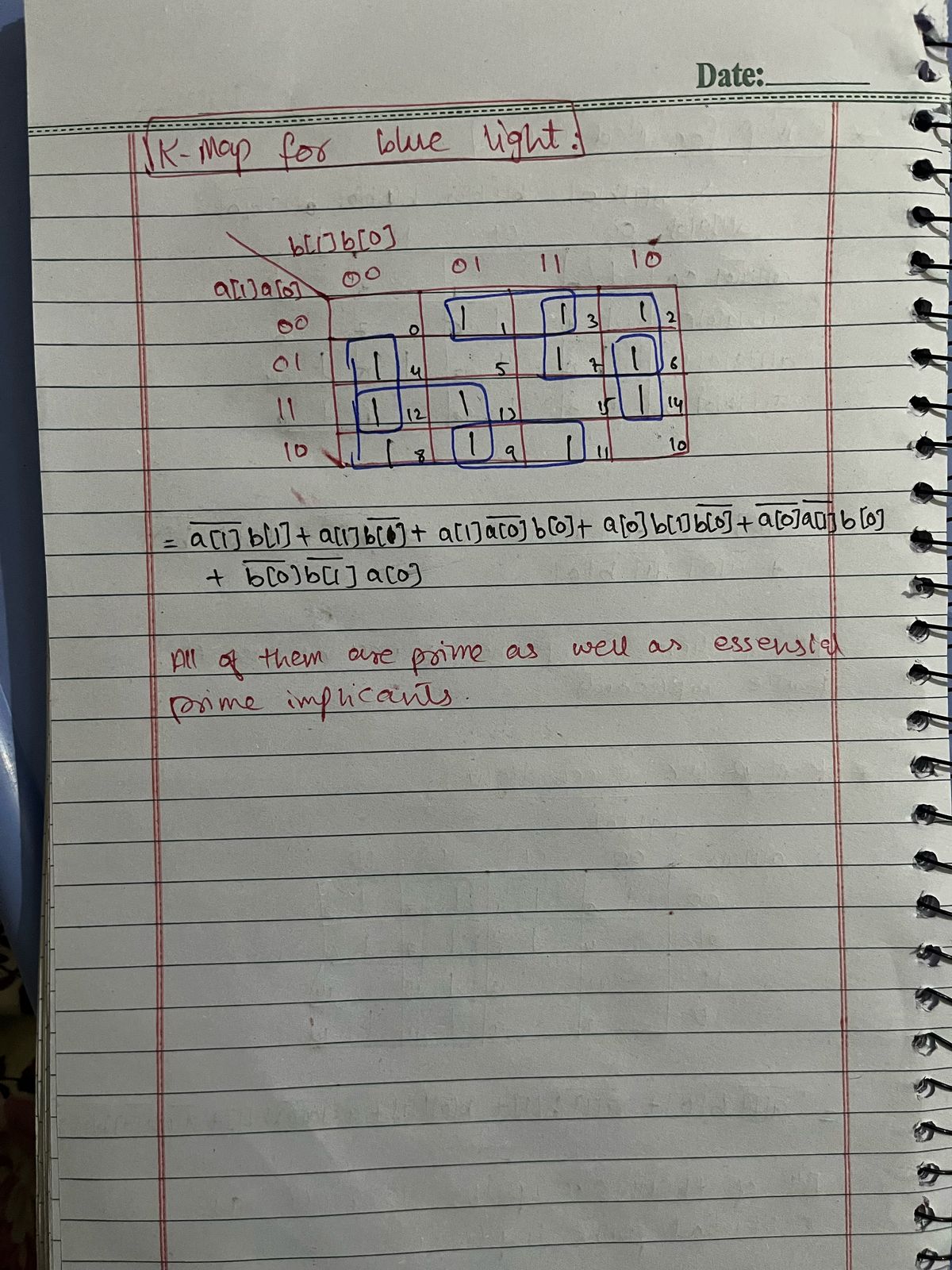
| IBUF | 4 | IO |

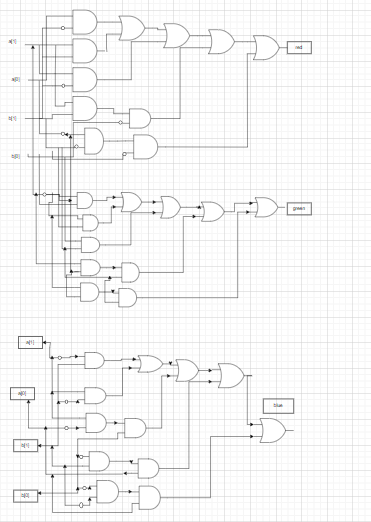
| OBUF | 3 | IO |

| LUT4 | 3 | LUT |

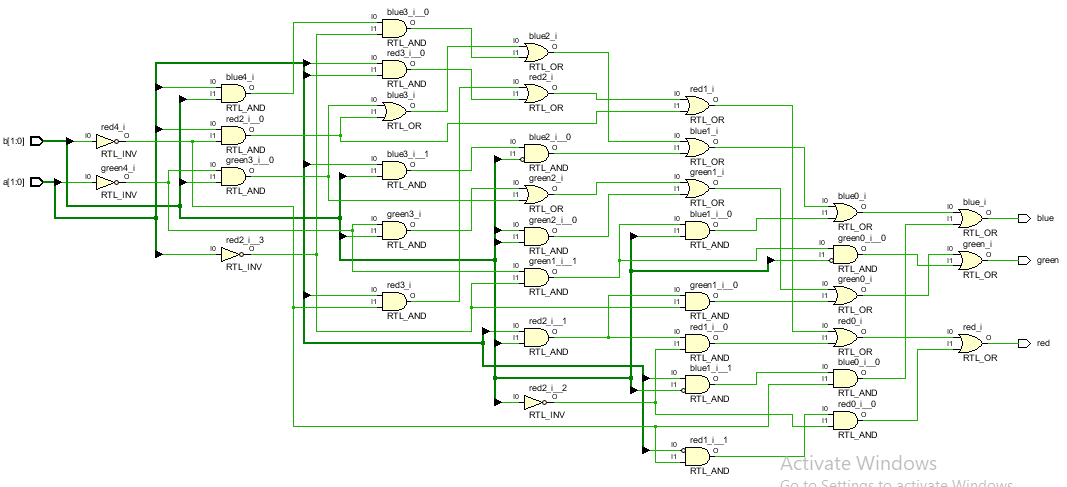
**(b) K-Maps used to minimized the logic:**



**(c) Circuit diagram on drawio:**

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**Circuit diagram by Vivado:**

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