|  |  |
| --- | --- |
| Name: Muuhammad Ahmad | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-68 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

1. **TRUTH TABLE**

a,b,c are inputs

x,y are outputs

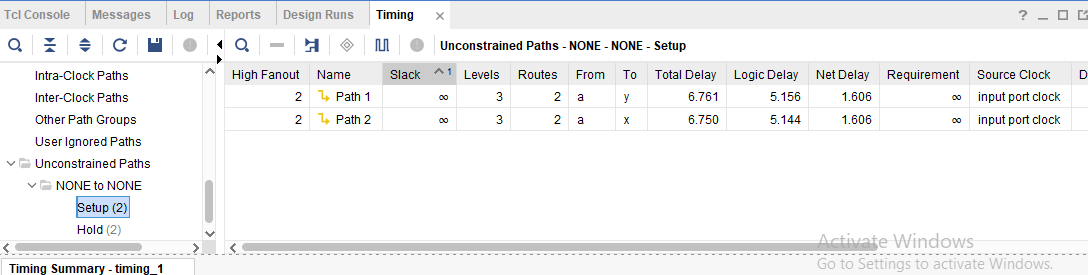
x = c’ ^ a|b

y = a|b & (a|b ^ (a&b)’)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **a** | **b** | **c** | **x** | **y** |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

1. **Maximum combinational delay:**

My maximum combinational delay is from path a to y which is 6.761



1. Resource utilization:

1. Slice Logic

--------------

+-------------------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-------------------------+------+-------+-----------+-------+

| Slice LUTs\* | 1 | 0 | 63400 | <0.01 |

| LUT as Logic | 1 | 0 | 63400 | <0.01 |

| LUT as Memory | 0 | 0 | 19000 | 0.00 |

| Slice Registers | 0 | 0 | 126800 | 0.00 |

| Register as Flip Flop | 0 | 0 | 126800 | 0.00 |

| Register as Latch | 0 | 0 | 126800 | 0.00 |

| F7 Muxes | 0 | 0 | 31700 | 0.00 |

| F8 Muxes | 0 | 0 | 15850 | 0.00 |

+-------------------------+------+-------+-----------+-------+

7. Primitives

-------------

+----------+------+---------------------+

| Ref Name | Used | Functional Category |

+----------+------+---------------------+

| IBUF | 3 | IO |

| OBUF | 2 | IO |

| LUT3 | 1 | LUT |

| LUT2 | 1 | LUT |

+----------+------+---------------------+

4. IO and GT Specific

---------------------

+-----------------------------+------+-------+-----------+-------+

| Site Type | Used | Fixed | Available | Util% |

+-----------------------------+------+-------+-----------+-------+

| Bonded IOB | 5 | 0 | 210 | 2.38 |

| Bonded IPADs | 0 | 0 | 2 | 0.00 |

| PHY\_CONTROL | 0 | 0 | 6 | 0.00 |

| PHASER\_REF | 0 | 0 | 6 | 0.00 |

| OUT\_FIFO | 0 | 0 | 24 | 0.00 |

| IN\_FIFO | 0 | 0 | 24 | 0.00 |

| IDELAYCTRL | 0 | 0 | 6 | 0.00 |

| IBUFDS | 0 | 0 | 202 | 0.00 |

| PHASER\_OUT/PHASER\_OUT\_PHY | 0 | 0 | 24 | 0.00 |

| PHASER\_IN/PHASER\_IN\_PHY | 0 | 0 | 24 | 0.00 |

| IDELAYE2/IDELAYE2\_FINEDELAY | 0 | 0 | 300 | 0.00 |

| ILOGIC | 0 | 0 | 210 | 0.00 |

| OLOGIC | 0 | 0 | 210 | 0.00 |