



## Digital Design Verification Lab # 42 Report

**Muhammad Asim** 

Date: 19 June 2025





## Task 1:

· Does the hierarchy match your expectations?

Yes, The hierarchy matches the expected results.

• Use the topology print to find the full hierarchical pathname from your test class to your UVC sequencer (e.g., tb.yapp.agent.sequencer) and write it below.

```
uvm_test_top.tb.yapp_uvc.agent.sequencer.run_phase.
```

• Use your topology to find the value of the is\_active property of the YAPP agent. What is the value of the is\_active variable when you printed the hierarchy?

The value of is\_active variable is UVM\_ACTIVE.

Run a simulation with base\_test and check which start\_of\_simulation\_phase() method
was called first. Which is called last? Why? You will need to set the right
+UVM VERBOSITY option to see the phase method messages.

As the simulation phases proceed according to bottom to top approach, the simulation phase method of driver was called first, and that of testbench was called the last.





## Task 2:

You should get a configuration usage report from check\_config\_usage(). Why do you get this?

The output of check\_config\_usage() is 0 in the report as there are no mismatches in the simulation.

https://github.com/Muhammad-Asim5/Uvm Labs.git

Lab # 42 Report

3