Name:	Muhammad Attiq
Reg. No:	FA23–BCE–060
Section:	BCE–5A
Subject:	Computer Organization & Architecture
Instructor:	Dr. Irfanullah
Lab Report:	5

Lab # 05 Introduction to Verilog HDL
Combinational Circuits 1

Objectives

- Gate Level Modeling

In-Lab

Tasks (Use Xilinx)

(Define input and output as vectors ; and not multiple variables)

- Write the Verilog gate-level description and testbench for a circuit with 3-bit input(X) and 1-bit output (Y). The output is 1 if the input number is a palindrome (reads the same backward and forward eg 101 or 010). The minterms of the output will be

```
module palindrome(input [2:0]x,output y);
```

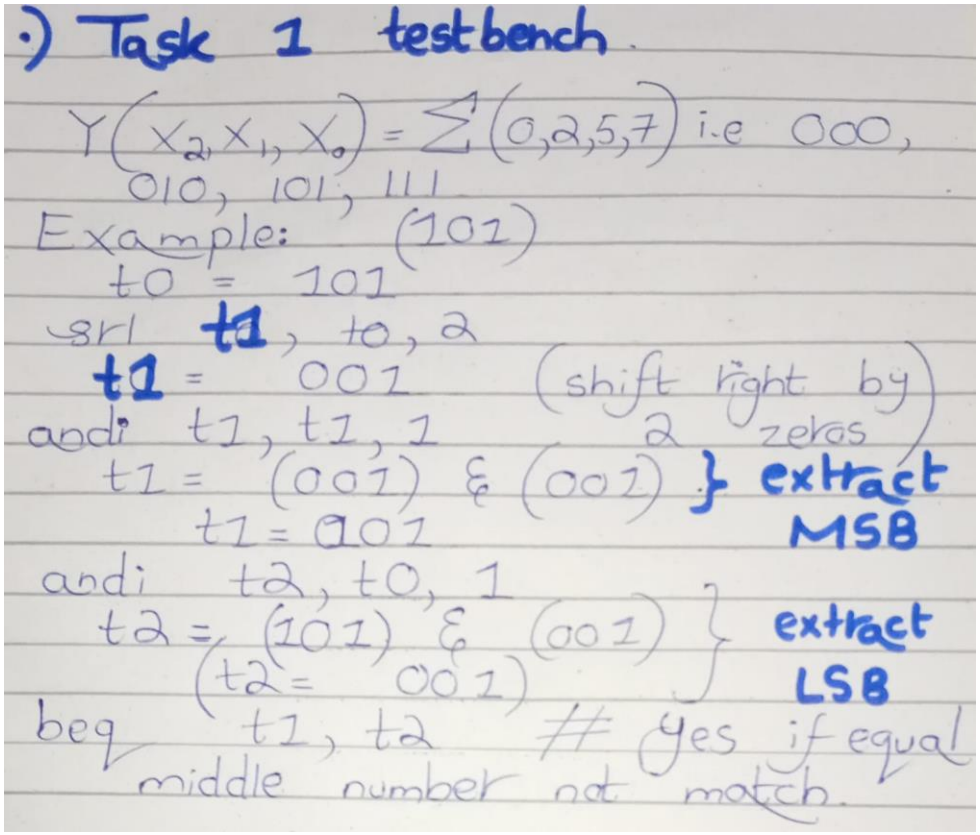
$$Y(X_2,X_1,X_0) = \sum(0,2,5,7) \text{ i.e. } 000,010,101 \text{ and } 111$$

```
.data
prompt:     .asciiz "Enter the 3 bit number: \n"
result:     .asciiz "The number is palindrome\n"
not_result: .asciiz "The number is not palindrome\n"
.text
main:
    li $v0, 4
    la $a0, prompt
    syscall
    li $v0, 5
    syscall
    move $t0, $v0
    srl $t1, $t0, 2
    andi $t1, $t1, 1
    andi $t2, $t0, 1
    beq $t1, $t2, yes
    j no
yes:
    li $v0, 4
    la $a0, result
    syscall
    j exit
no:
```

```
    li $v0, 4
    la $a0, not_result
    syscall
exit:
    li $v0, 10
    syscall
```

```
Enter the 3 bit number:
101
The number is palindrome
```

Output



Task 1 Testbench

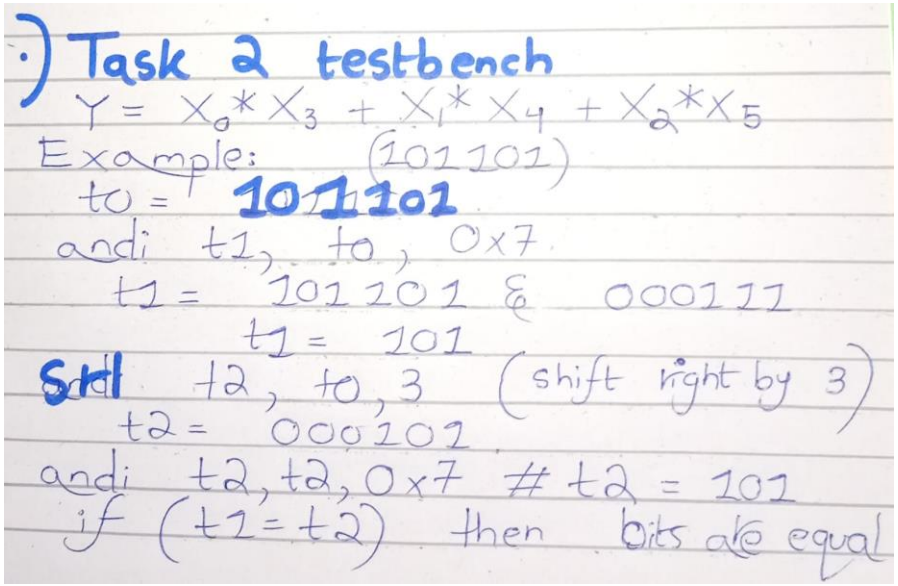
- Write the Verilog gate-level description and testbench for a circuit with 6-bit input(X) and 1-bit output (Y). It compares the first three bits of the inputs with the latter three and sets output equal to 1 when both are equal.

$$Y=X_0*X_3 + X_1*X_4 + X_2*X_5$$

```
.data
prompt:     .asciiz "Enter the 6-bit number: "
yes_result: .asciiz "The number is equal\n"
no_result:  .asciiz "The number is not equal\n"
.text
main:
    li $v0, 4
    la $a0, prompt
    syscall
    li $v0, 5
    syscall
    move $t0, $v0
    andi $t0, $t0, 0x3F
    andi $t1, $t0, 0x7
    srl  $t2, $t0, 3
    andi $t2, $t2, 0x7
    bne $t1, $t2, no
    j yes
yes:
    li $v0, 4
    la $a0, yes_result
    syscall
    j exit
no:
    li $v0, 4
    la $a0, no_result
    syscall
exit:
    li $v0, 10
    syscall
```

```
Enter the 6-bit number: 101101
The number is equal
```

Output



Task 2 Testbench

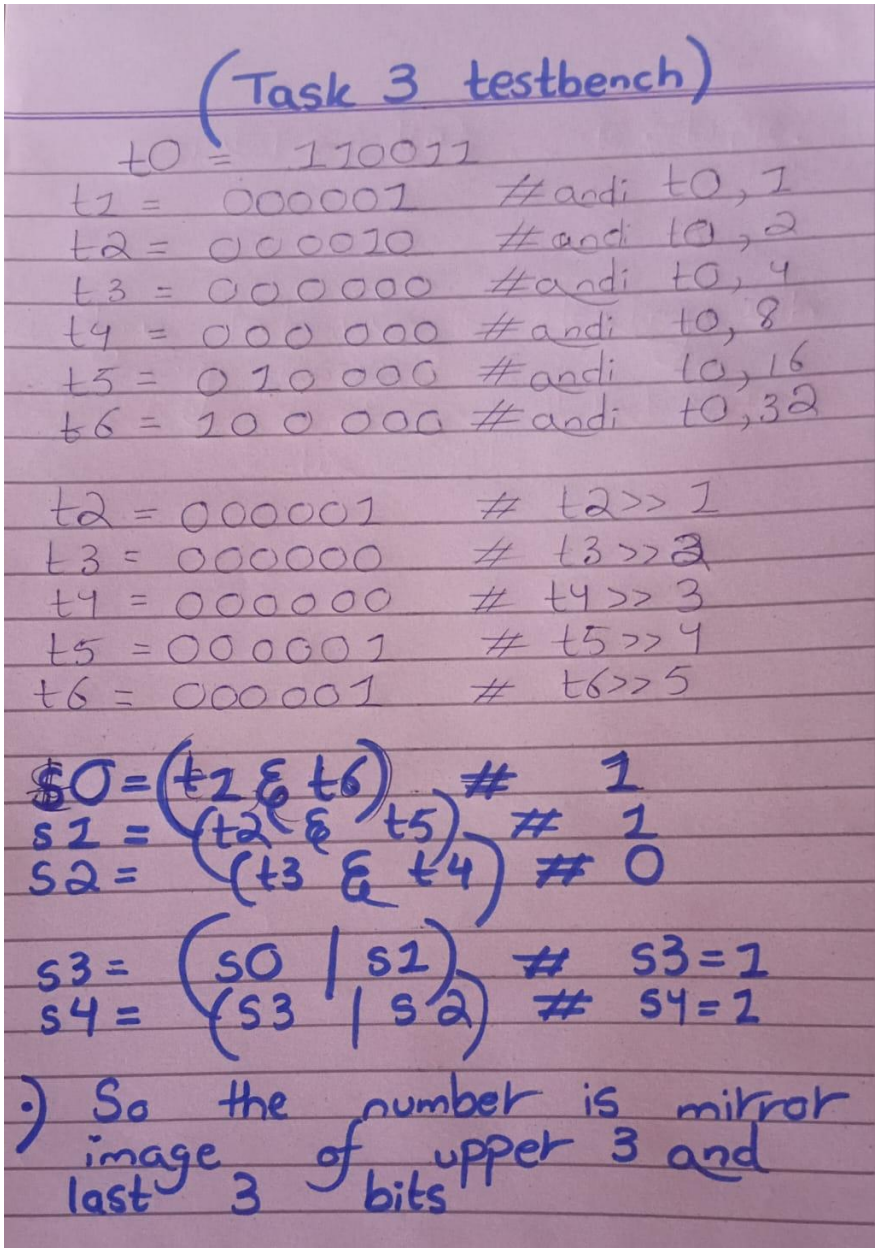
- Write the Verilog gate-level description and testbench for a circuit with 6-bit input(X) and 1-bit output (Y). It compares the first three bits of the inputs with the latter three and sets output equal to 1 when both are mirror image. For example 100 001 or 110 011

$$Y=X_0*X_5 + X_1*X_4 + X_2*X_3$$

```
.data
    prompt: .asciiz "Enter a 6-bit number (0-63): "
    result_true: .asciiz "Output Y = 1 (Mirror image)\n"
    result_false: .asciiz "Output Y = 0 (Not mirror image)\n"
.text
.globl main
main:
    li $v0, 4
    la $a0, prompt
    syscall
    li $v0, 5
    syscall
    move $t0, $v0
    andi $t1, $t0, 1
    andi $t2, $t0, 2
    andi $t3, $t0, 4
    andi $t4, $t0, 8
    andi $t5, $t0, 16
    andi $t6, $t0, 32
    srl $t2, $t2, 1
    srl $t3, $t3, 2
    srl $t4, $t4, 3
    srl $t5, $t5, 4
    srl $t6, $t6, 5
    and $s0, $t1, $t6
    and $s1, $t2, $t5
    and $s2, $t3, $t4
    or $s3, $s0, $s1
    or $s4, $s3, $s2
    beq $s4, $zero, print_false
print_true:
    li $v0, 4
    la $a0, result_true
    syscall
    j exit
print_false:
    li $v0, 4
    la $a0, result_false
    syscall
exit:
    li $v0, 10
    syscall
```

```
Enter a 6-bit number (0-63): 110011
Output Y = 1 (Mirror image)
```

Output



Task 3 Testbench

Critical Analysis / Conclusion

Doing these logic tasks in MIPS assembly is a great learning exercise. It forces you to understand how a processor works with simple ones and zeros. You learn to break down a problem into tiny, step-by-step instructions, which shows you how software commands are connected to the hardware's physical logic. This is a

fundamental skill for writing efficient, low-level code for systems that need to be fast or run on simple devices.

Lab Assessment		
Pre Lab	**/5**	**/25**
Performance	**/5**	
Results	**/5**	
Viva	**/5**	
Critical Analysis	**/5**	
Instructor Signature and Comments		