Assignment #01 20u-1898

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Q1 (-a)

(i) Control flags: It enables or disables certain operations of processor and it determine how instructions are carried out.

(ii) Status flags: It reflects the result of an instruction executed by the processor.

b) • In Real address mode programs can access any part of main memory, on the otherhand in virtual save mode memory is limited to assigned symants.

• Program running in real address mode can cause operating system to crash while in virtual mode if a program crashes it will not affect their programs running at same time.

• Only 1 MB can be addressed in real addres mode for one program. In virtual mode for one program. In virtual mode different/multiple programs runs each having 1 MB of memory.

(c) • In real addres mode, 16-bit segment register indicate base address of pre-assigned memory areas named segment.

• In protected mode, segment register hold pointers to segment discripton table.

(d) • The execution of single machine instruction can be divided into sequence of individual operations. Before executing a program is loaded into memory Thus the pointer holds the address of next instruction to execute.

• Conventional memory is outside the CPU and it responds more slowly to accss request; Registers are hard wired inside the CPU.

(e) The CPU go through a predefined sequence of steps to execute a machine instruction called the instruction execution cycle.

(f) The instruction pointer (IP) register holds the address of the instruction we want to execute.

Here are steps to execute it:

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(1) Fetch: CPU fetches the instruction from instruction queue; then increments the instruction.

(2) Decode: CPU then decodes the instructions from binary to executable.

(3) Fetch Operands: CPU fetches the operands from register & memory.

(4) Execute: CPU executes the instructions; stores the value and ~~outputs the~~ provides output.

(5) Machine Cycle: The time and cycle (fetch-Decode-Execute) that a CPU performs.
Instruction Cycle: The steps required by CPU to fetch and execute an instruction is called an instruction cycle.

(6) High Level Languages like C, C++ and Java has one to many relationship with Machine Language.

Q#2, (i) AL = 85
AL = 34
AL = BF
AL = AE

(ii) In instruction MOV EAX, VAR2 ; the value of VAR2 is stored/moved in EAX register.
In MOV EAX, OFFSET VAR2 the address of whereas is the distance in bytes from first or location/address is stored in EAX register.

(iii) (a) Illegal ; PUSH is for 64 bit while AL is of 8 bit.
(b) Illegal; only 2x is required.
(c) Illegal; WORD is of 16 bit; AL is of 8 bit.
(d) Illegal; BASE register not memory expression will be used.
(e) Illegal; INC or DEC are used with destination register.

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(a) (i) AX = 8F 7A SF = 0 CF = 0
OF = 0 ZF = 1

(b) AX = 0A72 OF = 0 ZF = 0
CF = 1 SF = 0

(c) AX = FA77 OF = 0 ZF = 1
CF = 0 SF = 0

(d) AX = FA78 OF = 0 ZF = 0
CF = 0 SF = 1

(v) 4424 bytes. = 200 + 200 + 20 + 20 + 2

Q3 Real Address = Segment x 10 + offset.

a) Real Address => B6168
b) Offset => 1852F
c) Segment => FA5B

Qtn 2 => 20 bit Address = 2ABEH + 2378H
= 2CF57H

Starts at 1200 & ends at 1400

Q5 (a) In fetch; instruction is loaded from memory to instruction; decoded & contents are moved to AX register.

(b) Memory location is specified, AX contents are located into memory. Then executes & waits for next location.