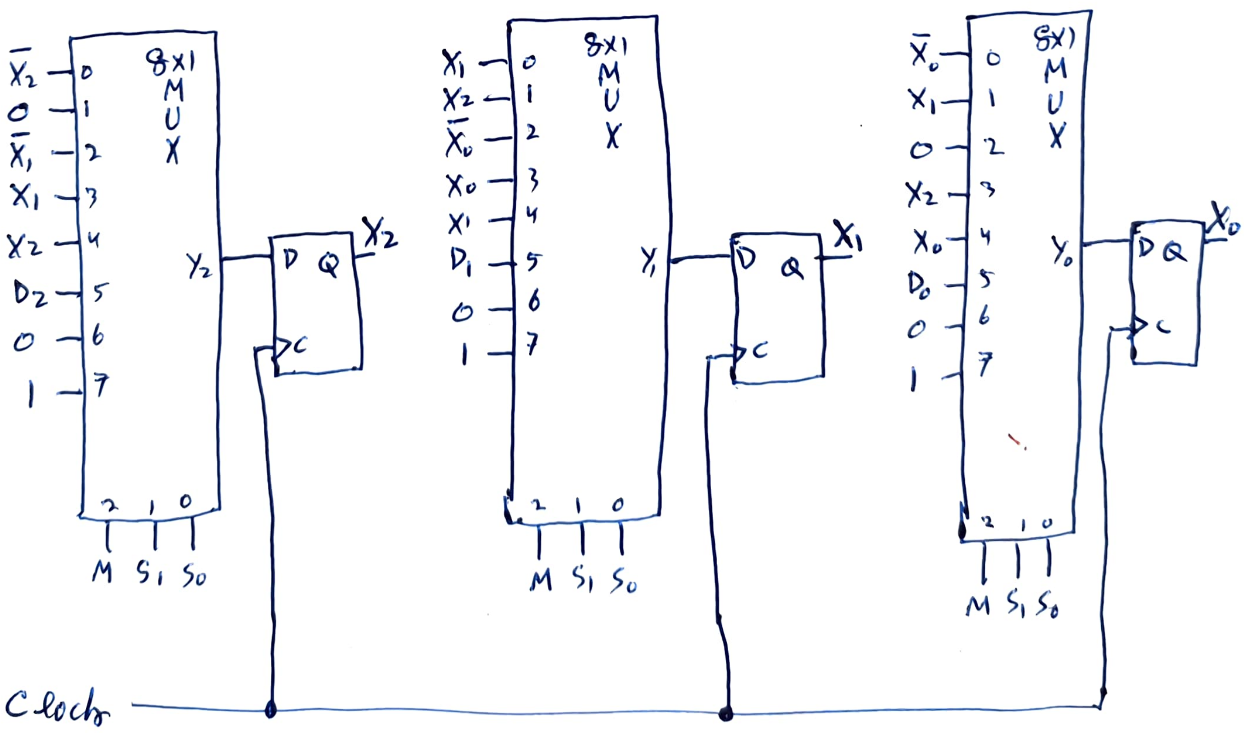
Q.1 Solution

Control Inputs M S_1 S_0	Microoperation	Next State $X_2(t+1)$	$X_1(t+1)$	$X_0(t+1)$
0 0 0	Flip X_2 and X_0 only	$\bar{X}_2$	X_1	$\bar{X}_0$
0 0 1	Shift right	0	X_2	X_1
0 1 0	Flip all bits and Shift left	$\bar{X}_1$	$\bar{X}_0$	0
0 1 1	Rotate left	X_1	X_0	X_2
1 0 0	No change (hold)	X_2	X_1	X_0
1 0 1	Load parallel data	D_2	D_1	D_0
1 1 0	Clear Register to 0	0	0	0
1 1 1	Set register to all 1	1	1	1

Design using 8x1 MUX and D flip-flops



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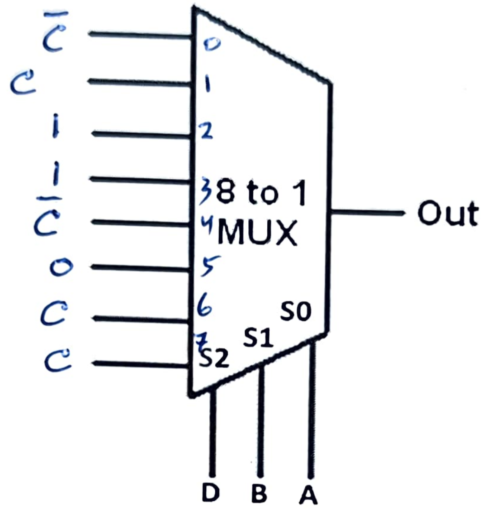
CLO # 2: Construct optimized combinational circuit design Solution

Q2: Implement the following function F(A, B, C, D) using an 8x1 MUX with D, B, and A connected to the select bits S2, S1 and S0 respectively. You can only use NOT gates other than the MUX.
F(A, B, C, D) = Σm(0,1,4,6,7,10,12,14,15) **[15 marks]**



A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Re arranging the table

	D	B	A	C	F	
I_0	0	0	0	0	1	$F = \bar{C}$
	0	0	0	1	0	
I_1	0	0	1	0	0	$F = C$
	0	0	1	1	1	
I_2	0	1	0	0	1	$F = 1$
	0	1	0	1	1	
I_3	0	1	1	0	1	$F = 1$
	0	1	1	1	1	
I_4	1	0	0	0	1	$F = \bar{C}$
	1	0	0	1	0	
I_5	1	0	1	0	0	$F = 0$
	1	0	1	1	0	
I_6	1	1	0	0	0	$F = C$
	1	1	0	1	1	
I_7	1	1	1	0	0	$F = C$
	1	1	1	1	1	
	S_2	S_1	S_0			

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CLO # 3: Analyze and Design Sequential Circuit

Q3. Consider a PR flip-flop implemented using a D flip-flop, as described by the given characteristic table.

[5+5+5 marks]

Characteristic Table

P	R	Q(t)
0	0	0
0	1	Q(t)
1	0	Q(t)'
1	1	Q(t) ⊕ R

Complete the expanded Characteristic Table

P	R	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

b. Derive the simplified logic equation for the input D..

Q(t+1) or D(t+1) **Equation of D** = $P\bar{Q} + \bar{P}RQ$

K-Map:

P \ RQ	00	01	11	10
0			1	
1	1			1

$D(t+1) = P\bar{Q} + \bar{P}RQ$
or $Q(t+1)$

c. Give the excitation table for PR flip-flop.

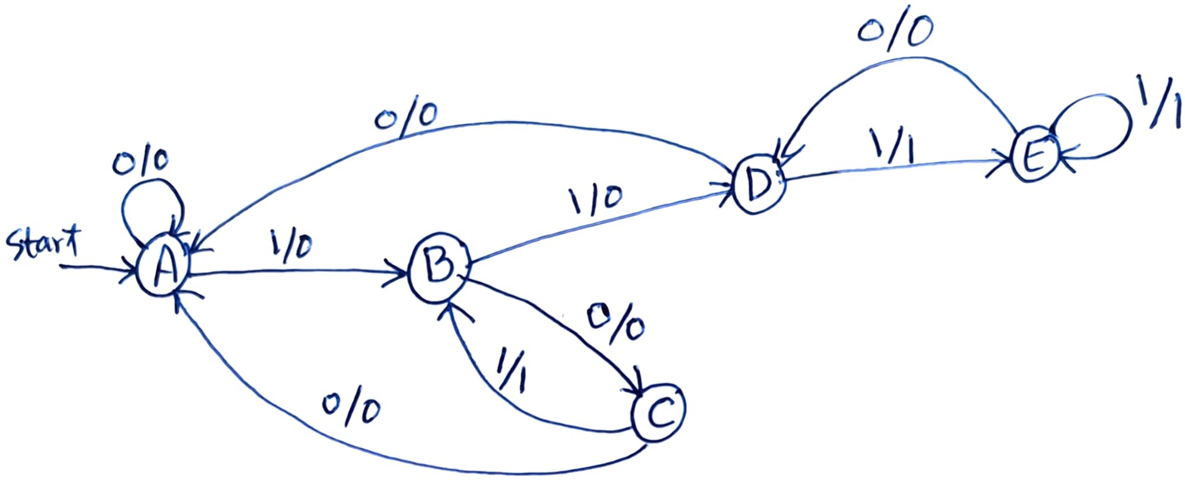
Excitation Table			
Q(t)	Q(t+1)	P	R
0	0	0	0
0	0	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	1	0
1	~~1~~ 0	1	1
1	1	0	1

Compact form of Excitation Table

Q(t)	Q(t+1)	P	R
0	0	0	X
0	1	1	X
1	0	X 1	0 1
1	1	0	1

or
00
1X

Q.4-a A Solution



Q.4-b Solution.

Inputs X Y	Present State A B	Next State A B	Output Z	D_A	J_B	K_B
0 0	0 0	0 0	0	0	0	X
0 0	0 1	0 1	1	0	X	0
0 0	1 0	0 0	0	0	0	X
0 0	1 1	0 1	1	0	X	0
0 1	0 0	1 0	0	1	0	X
0 1	0 1	1 1	1	1	X	0
0 1	1 0	1 0	0	1	0	X
0 1	1 1	1 1	1	1	X	0
1 0	0 0	0 0	0	0	0	X
1 0	0 1	0 0	1	0	X	1
1 0	1 0	1 1	0	1	1	X
1 0	1 1	1 1	1	1	X	0
1 1	0 0	0 0	0	0	0	X
1 1	0 1	0 0	1	0	X	1
1 1	1 0	1 1	0	1	1	X
1 1	1 1	1 1	1	1	X	0

(Flip flop Inputs: D_A, J_B, K_B)

K-Maps

D_A XY \ AB	00	01	11	10
00				
01	1	1	1	1
11			1	1
10			1	1

$D_A = \bar{X}Y + XA$

J_B XY \ AB	00	01	11	10
00		X	X	
01		X	X	
11		X	X	1
10		X	X	1

$J_B = XA$

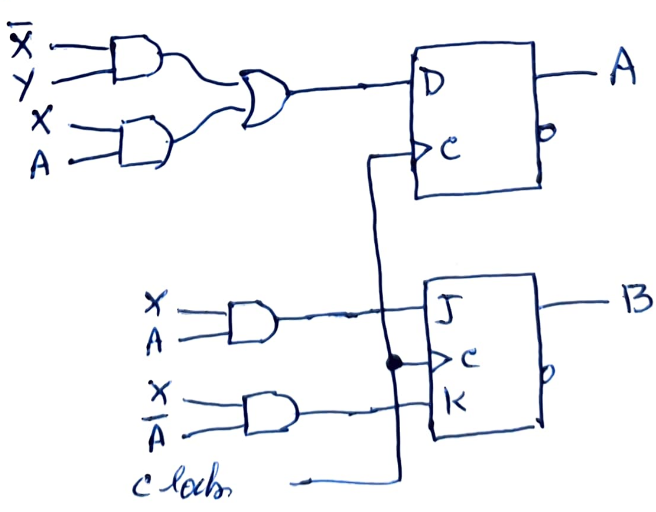
K_B XY \ AB	00	01	11	10
00	X			X
01	X			X
11	X	1		X
10	X	1		X

$K_B = X\bar{A}$

The values of D_A, J_B & K_B are obtained from their respective excitation tables

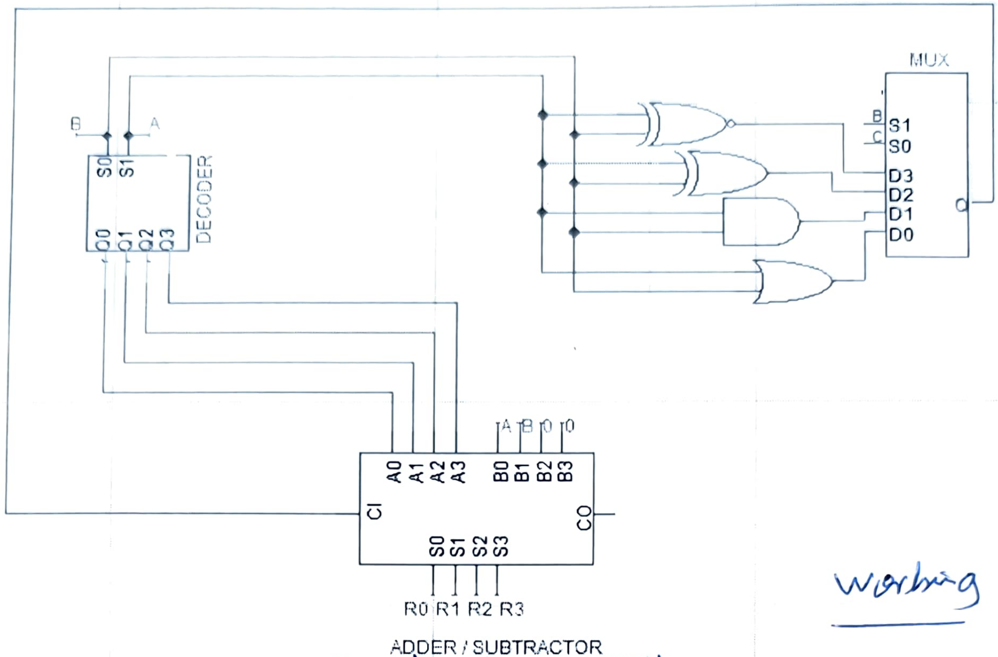
$Z = B$ from K-Map or looking at the table.

Circuit Diagram



CLO # 2: Construct optimized combinational circuit design

Q5. The adder/subtractor in the circuit given below performs the addition $(A_3A_2A_1A_0 + B_3B_2B_1B_0)$ if the control signal *CI* is 0 or the subtraction $(A_3A_2A_1A_0 - B_3B_2B_1B_0)$ if *CI* is 1. *CI* is coming from the output of the multiplexer. Fill in the given table for the result $R_3R_2R_1R_0$. **[15 marks]**



A	B	C	R_3	R_2	R_1	R_0	BC 00 A+B	BC 01 AB	BC 10 A⊕B	BC 11 A⊙B
0	0	0	0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0	0	0	1
0	1	0	0	0	0	0	1	0	1	0
0	1	1	0	1	0	0	1	0	1	0
1	0	0	0	0	1	1	1	0	1	0
1	0	1	0	1	0	1	1	0	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	1	1	1	0	1

Result

working

working

$A_3A_2A_1A_0$	0001	AB
$B_3B_2B_1B_0$	0000	00
	0010	AB
	0010	01
	0100	AB
	0001	10
	1000	AB
	0011	11