National University of Computer and Emerging Sciences 0400

Lahore Campus

Digital Logic Design (EE1005) Sessional-II Exam

Date: April 12, 2025

Total Time (Hrs): 1
Total Marks: 45
Total Questions: 3

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Roll No _____ Section _____ Student Signature _____

Semester: SP-2025

Campus: Lahore

Department: CS, DS, SE

Do not write below this line.

- Calculators are not allowed.
- **Solve Q. # 2 (a) and Q # 3 on Question Paper and attach it with your answer sheets.**
- Be precise; your answer to each question should be readable.
- Show full working for each question.

CLO#2: Construct optimized combinational circuit design

Question#1 [14 Marks]: Design a combinational circuit that takes a 3-bit input ($X_2X_1X_0$) pattern and outputs the binary position of the first '1', scanning from the ***least significant bit*** (LSB – position 0, rightmost) to the ***most significant bit*** (MSB – position 2, leftmost).
The circuit should generate two outputs:

1. An ***n-bit binary code*** indicating the position of the first '1'. Use the minimum number of bits to represent the binary code (*in other words, cleverly choose **n***).
2. A ***validity signal V*** that specifies whether the output is meaningful.
   a. If the input is '000', then **V = 0**, indicating no '1' is present and the position output is invalid.
   b. For all other input patterns, **V = 1**, and the binary output gives the correct position of the first '1'.

Design the required circuit using 3 x 8 decoder(s) and minimum additional logic [NOT gates, 2-input (AND, OR, NAND, NOR) gates only].

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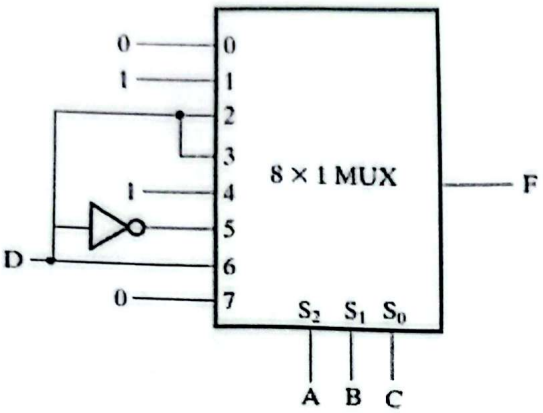
Question#2 [5+10=15 Marks]:

a) Write the Boolean function (in canonical form [Sum of product]) for the circuit shown in the figure below:



A	B	C	D	F	
0	0	0	0	0	I_0
0	0	0	1	0	
0	0	1	0	1	I_1
0	0	1	1	1	
0	1	0	0	0	I_2
0	1	0	1	1	
0	1	1	0	0	I_3
0	1	1	1	1	
1	0	0	0	1	I_4
1	0	0	1	1	
1	0	1	0	1	I_5
1	0	1	1	0	
1	1	0	0	0	I_6
1	1	0	1	1	
1	1	1	0	0	I_7
1	1	1	1	0	

Simplified :

F (A, B, C, D) = $\bar{B}(A \oplus C) + \bar{A}BD + A(\bar{B}C\bar{D} + B\bar{C}D)$

$\sum m(2,3,5,7,8,9,10,13)$

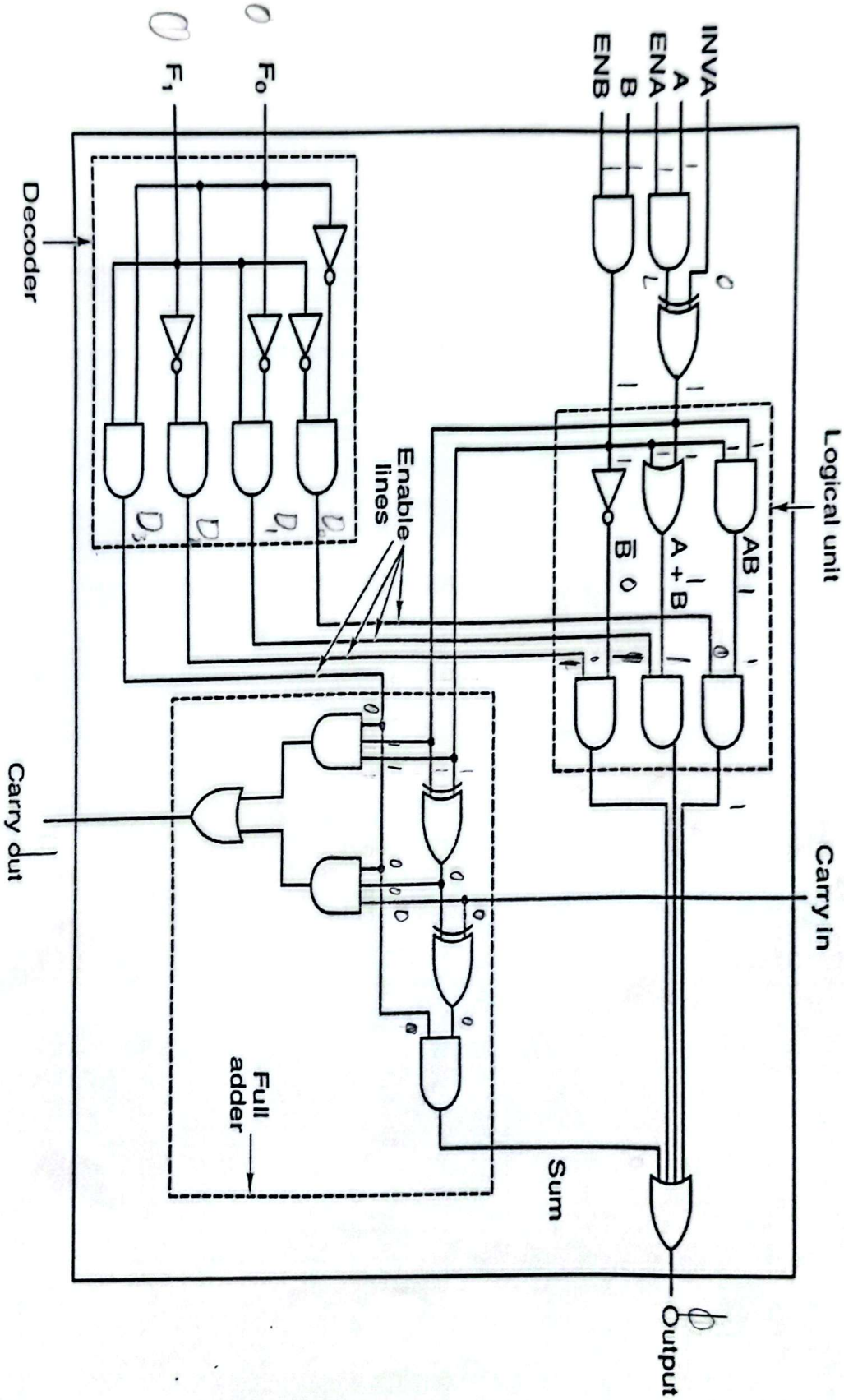
(5)

b) A Boolean Function G (A, B, C, D) = ∑ m (0,1,4,5,8,10,13,15) is required to be implemented by using a 4 x 1 Multiplexer with minimum additional logic. Show your design. Available resources are **NOT gates** and **2-input (AND, OR, NAND, NOR) gates**.

Question#3 [16 Marks]: Find the truth table for Output and Carry Out for the circuit shown in the figure **(where INVA=0, ENA=B=ENB=A=1, Carry In =0):**

F0	F1	Output	Carry Out
0	0	1	0
0	1	1	0
1	0	0	0
1	1	0	1

(16)


F1
F0
INVA
ENA
A
ENB
B
Decoder
Enable lines
Logical unit
Carry dut
Carry in
Full adder
Sum
Output