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Section: C
Repository: https://github.com/Muhammad-Furrukh/DSD_2022-EE-111.git

Reg. No.: 2022-EE-111 Marks Obtained: _____

Lab Manual

DSD Lab Manual Evaluation Rubrics

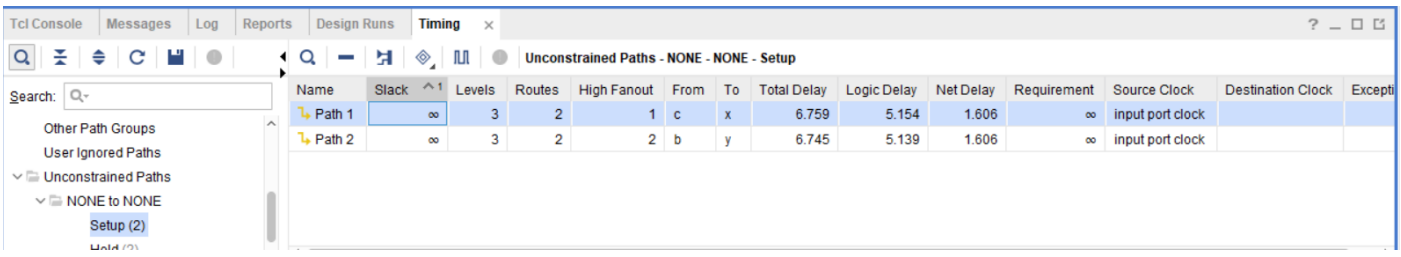
Assessment	Total Marks	Marks Obtained	0-30%	30-60%	70-100%
Code Organization	3		No Proper Indentation and descriptive naming, no code organization. Zero to Some understanding but not working	Proper Indentation or descriptive naming or code organization. Mild to Complete understanding but not working	Proper Indentation and descriptive naming, code organization. Complete understanding, and proper working
Simulation	5		Simulation not done or incorrect, without any understanding of waveforms	Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms	Working simulation without any errors, etc and complete understanding of waveforms
FPGA	2		Not implemented on FPGA and questions related to synthesis and implementation not answered.	Correctly Implemented on FPGA or questions related to synthesis and implementation answered.	Correctly Implemented on FPGA and questions related to synthesis and implementation answered.

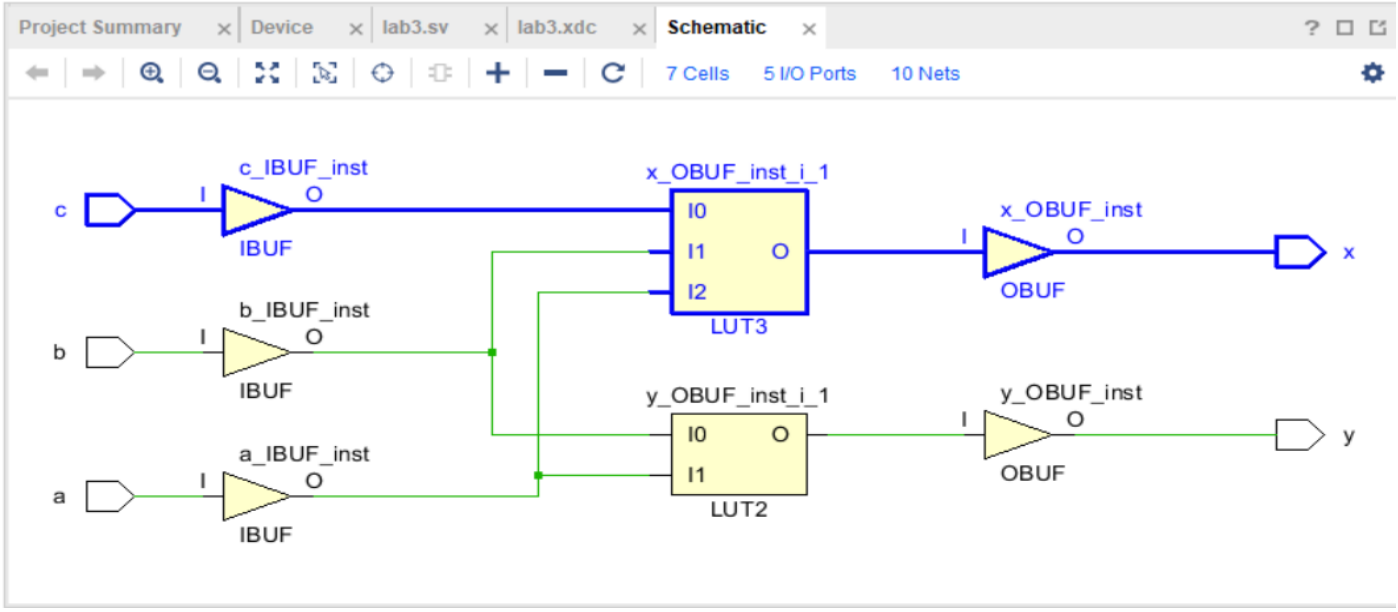
Report
LAB 3

1. Truth table of the implemented circuit:

a	b	c	x	y
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

2. Maximum Combinational Delay in Synthesis:





The maximum combinational delay is from c to x of 6.759 ns, as can be seen from the attached snap.

3. Resources Utilized in FPGA, in synthesis report:

Only 1 LUT as Logic out of 63 400 were used.

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1	0	63400	<0.01
LUT as Logic	1	0	63400	<0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

5 out of 210 input/output blocks on the FPGA were used.

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	5	0	210	2.38
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

From the primitives, 3 input buffers, 2 output buffers, 1 3-input LUT and 1 2-input LUT was used.

7. Primitives

Ref Name	Used	Functional Category
IBUF	3	IO
OBUF	2	IO
LUT3	1	LUT
LUT2	1	LUT