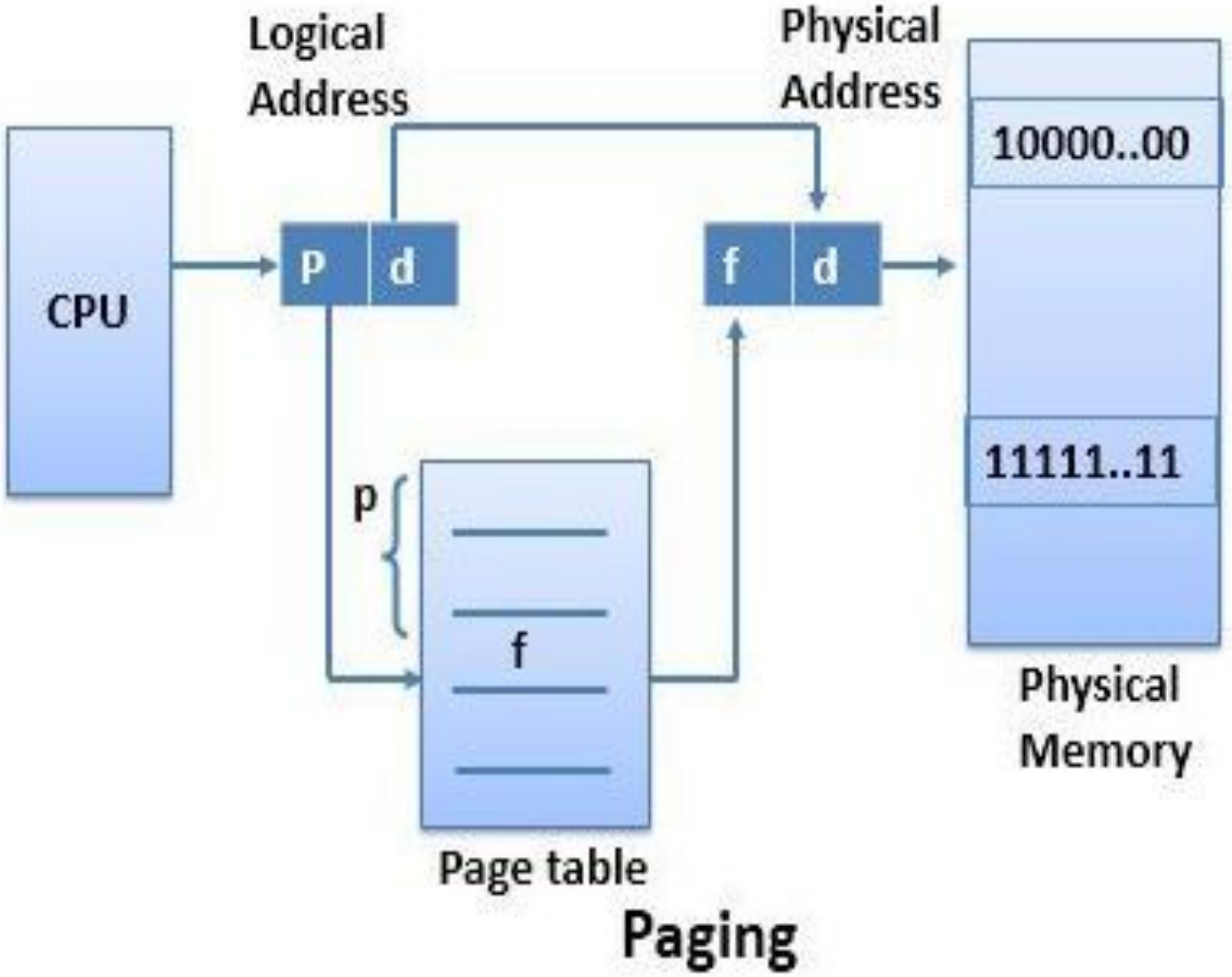
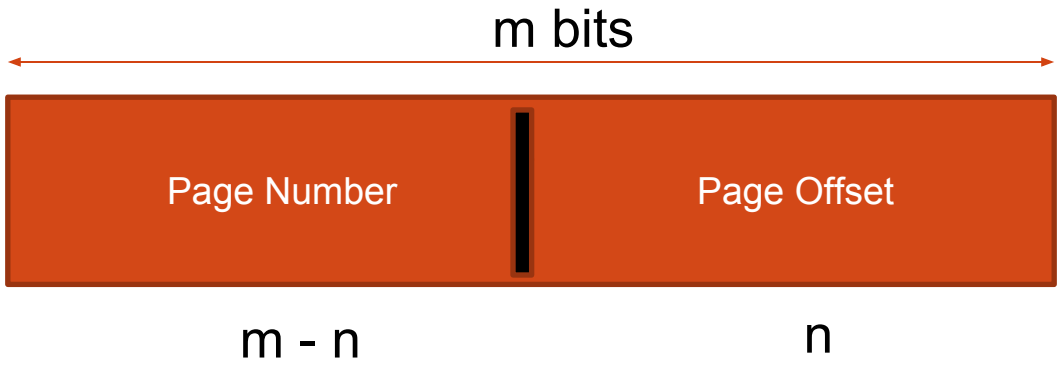

Logical
Address
Physical
Address
CPU
p
d
f
d
10000..00
11111..11
p
f
Page table
Physical
Memory
Paging

PAGING

Rules:

- If we have ***M*** bit processor, then logical address will also of ***M*** bits long.

- Let the size of logical address space is ***2^m*** and page size is ***2^n*** (bytes or words), then the high order (**m-n**) bits of logical address designate the page number (**p**) and lower order bits (**n**) designate the page of offset.



Logical Address

- **Example:**

- Consider the logical address space of **8** pages of **1024** words mapped onto physical memory of **32** frames

- **1. How many bits are there in logical address:**

Given page size = 1024 words = 1k

Page size = 2^10 ⇔ 2^n so, ***n = 10***

Logical Address space = 8 x 1K = 8K = 2^3 x 2^10 = 2^13 so, **m = 13**

p = 3 (m – n)

d = 10 (n)

There are **13 bits** in logical address space.

- **2. How many bits are there in physical address**

Physical address space = 32 x 1K = 32K = 2^5 x 2^10 = 2^15

There are **15 bits** in physical address.

- **Example:**
- Given **32-bit** processor, page size = 1024 bytes
- **Find:**
- **1. size of logical address :**

32 bits (as 32-bit processor)

- **2. No. of bits to represent page number and offset:**

As page size = 1024 bytes = 2^10 (2^n) so, **n = 10**

No. of bits used to represent page no. = m – n = 32 – 10 = **22 bits**

- **3. Max size of logical address space:**

2^32 bytes = 2^2 x 2^30 = 4GBytes

- **4. Max number of pages in logical address space:**

Space = 2^m-n = 2^22 = 2^2 x 2^20 = 4MBytes = 4 Million

- **5. Max length of page table of a process :**

4 M entries (max no. of pages in process)

- ***Note to remember:***
- *1K = 2^10 Bytes*
- *1MB = 1024KB*

= 2^10 x 2^10

= 2^20 Bytes

- *1 GB = 1024 MB*

= 2^30 Bytes

- **Example:** Assume a logical address space of 16 pages of 1024 words, each mapped into a physical memory of 32 frames.

  - No. of bits needed for p =ceiling[log16] 2^4=4bits
  - No. of bits needed for f = ceiling[log32] 2^5=5bits
  - No. of bits needed for d = 2048bytes =2^11
  - Logical address size = |p|+|d|=4+11=15bits
  - Physical address size =|f|+|d|=5+11=16bits

- **Page Table Size**—Page table size = NP * PTES, (assuming a byte size page table entry)

  - where NP is the number of pages in the process address space and PTES is the page table entry size (equal to |f|)

- 16-bit logical address
- 2^16
- 8K page size
- Maximum pages in a process address space =
- 2^16/8K=8pages
- |d| = log2 8K =13bits
- |p| = 16-13=3bits

- **Example**:
- Logical address = 32-bit
- Process address space = 2^{32} B = 4 GB
- Main memory = RAM = 512 MB
- Page size = 4K
- Maximum pages in a process address space = 2^32/4K=1M
- |d| =32-20=12bits
- |p| = ceiling[log1M]=20bits
- No. of frames = 512MB/4K =128K
- |f| = ceiling[log128K]=17bits
- Physical address = |f|+|d|=17+12=29bits