



PROGRESS REPORT

Week 1

Submitted By

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Batch: 2023

Department: Electrical Engr.

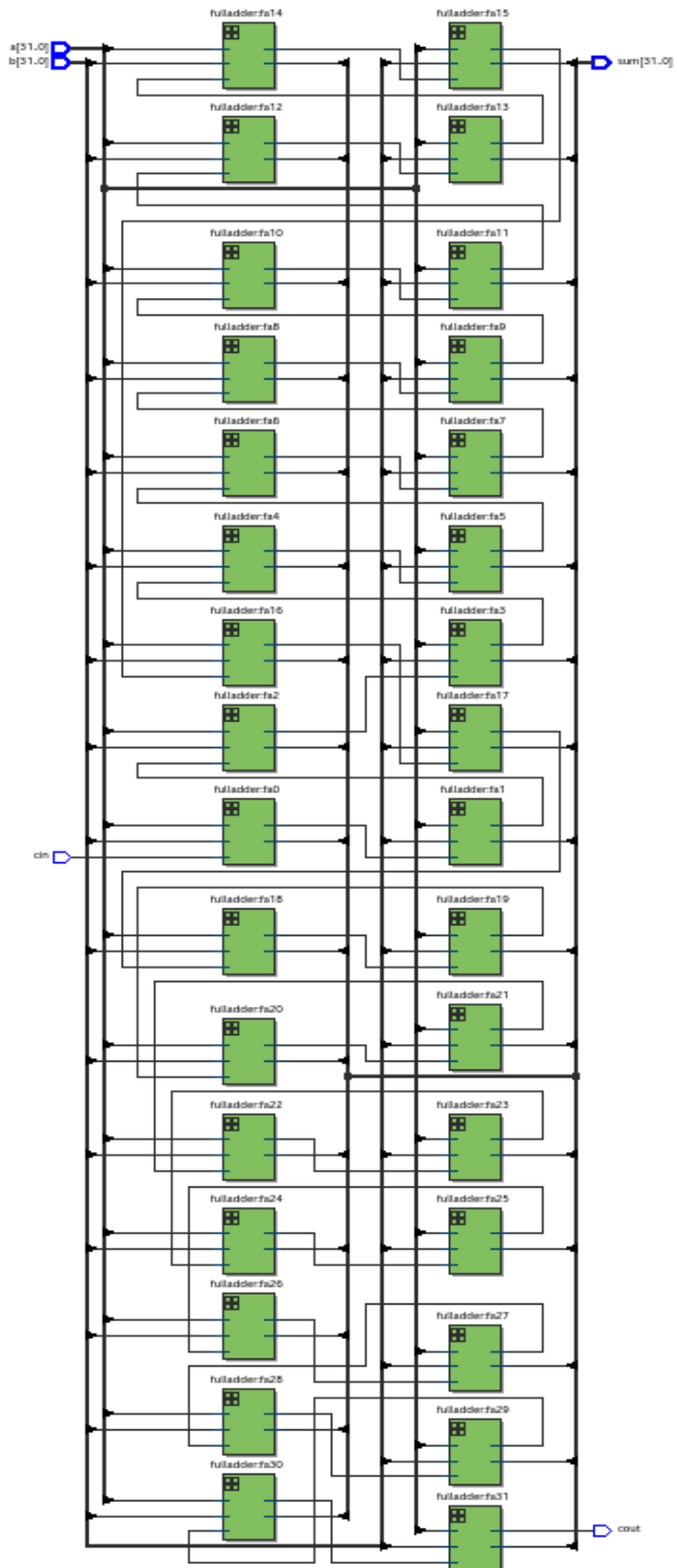
Submitted To

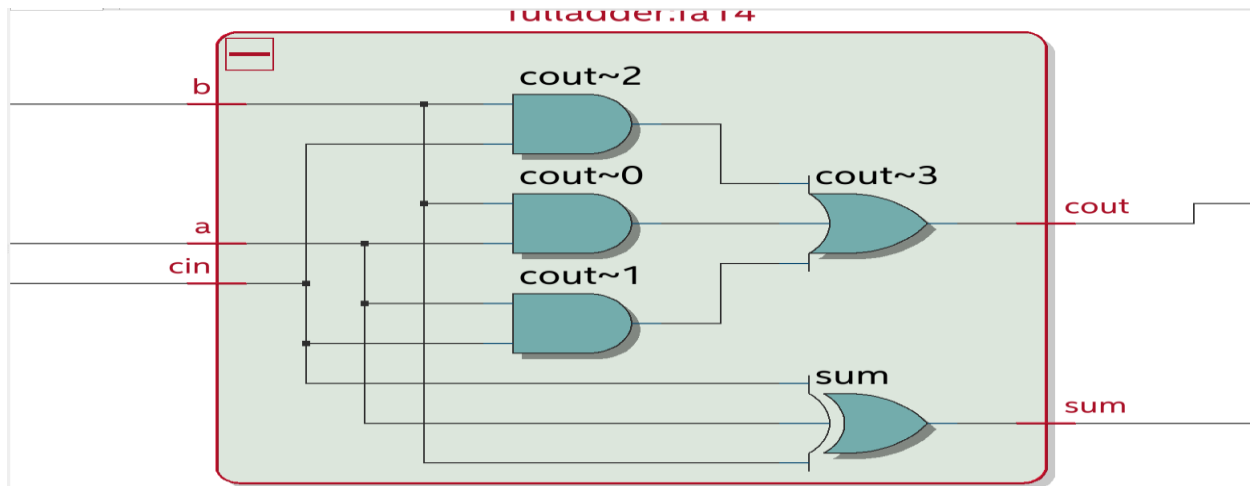
Miss Hafsa Amanullah

Dr. Fahim-Ul-Haq

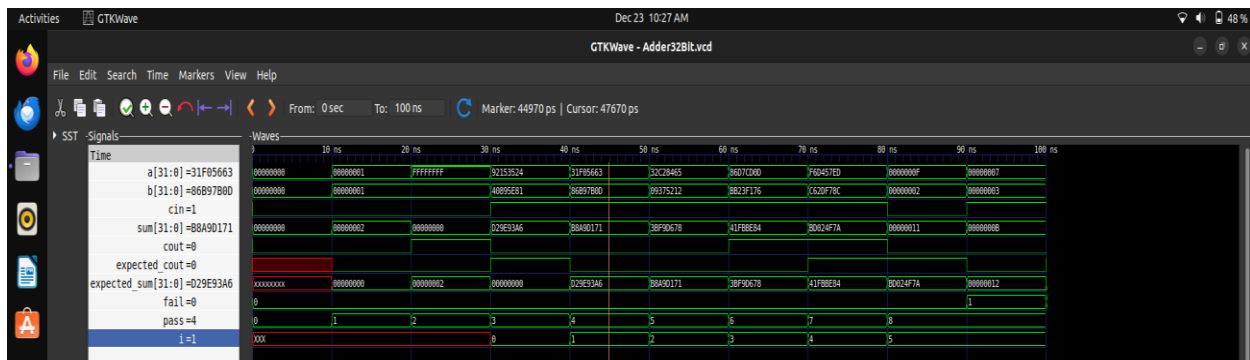
TASK 1: 32 BIT ADDER

RTL View:





Simulation View:



Command View With Test Summary:

```

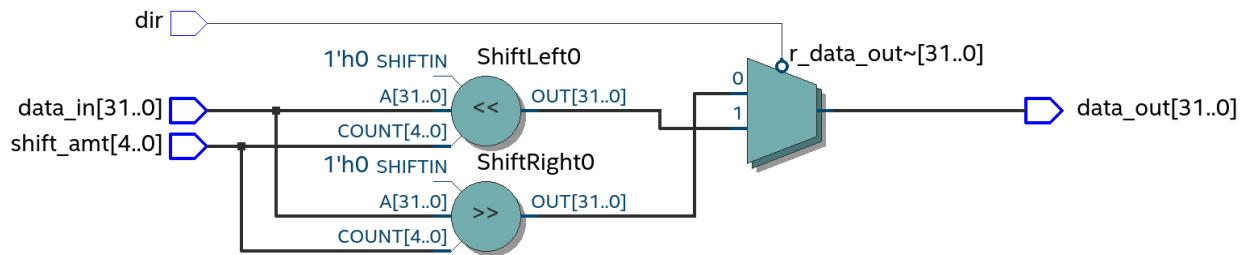
taha_aka_beast@ubuntu ~ → cd /home/taha_aka_beast/project_verilog/Adder32Bit
taha_aka_beast@ubuntu ~/project_verilog/Adder32Bit → ls
Adder32Bit.qpf      db                output_files
Adder32Bit.qsf      fulladder.sv     simulation
Adder32Bit.qws      fulladder.sv.bak tb_Adder32Bit.sv
Adder32Bit.sv       incremental_db   tb_Adder32Bit.sv.bak
Adder32Bit.sv.bak   Manchester_Encoder_Mealy.sv tmp_compile.qsf
cs_pin_model_dump.txt modelsin_project unsaved
taha_aka_beast@ubuntu ~/project_verilog/Adder32Bit → rm -f *.vcd adder_sim
taha_aka_beast@ubuntu ~/project_verilog/Adder32Bit → iverilog -g2012 fulladder.sv Adder32Bit.sv tb_Adder32Bit.sv -o adder_sim
taha_aka_beast@ubuntu ~/project_verilog/Adder32Bit → vvp adder_sim
VCD info: dumpfile Adder32Bit.vcd opened for output.
==== Adder32Bit Testbench Start ====
PASS: a=0 b=0 cin=0 => sum=0 cout=0
PASS: a=1 b=1 cin=0 => sum=2 cout=0
PASS: a=4294967295 b=1 cin=0 => sum=0 cout=1
PASS: a=2450863396 b=1082744449 cin=1 => sum=3533607846 cout=0
PASS: a=837834339 b=2260302605 cin=1 => sum=3098136945 cout=0
PASS: a=851608677 b=154620434 cin=1 => sum=1006229112 cout=0
PASS: a=2262289677 b=3139694966 cin=1 => sum=1107017348 cout=1
PASS: a=4141111277 b=3324901260 cin=1 => sum=3171045242 cout=1
FAIL: a=15 b=2 cin=0 => sum=17 cout=0 (expected sum=18 cout=0)
FAIL: a=7 b=3 cin=1 => sum=11 cout=0 (expected sum=0 cout=1)
-----
Total Passed: 8
Total Failed: 2
-----
taha_aka_beast@ubuntu ~/project_verilog/Adder32Bit → gtkwave Adder32Bit.vcd &
[1] 8028
taha_aka_beast@ubuntu ~/project_verilog/Adder32Bit →
GTKWave Analyzer v3.3.104 (w)1999-2020 BSI

[0] start time.
[100000] end time.
taha_aka_beast@ubuntu ~/project_verilog/Adder32Bit →

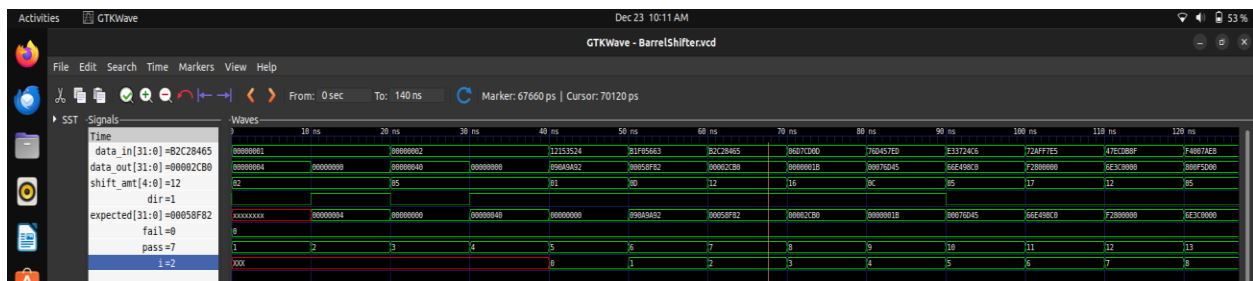
```

TASK 2: 32 BIT BARREL SHIFTER

RTL View:



Simulation View:



Command View With Test Summary:

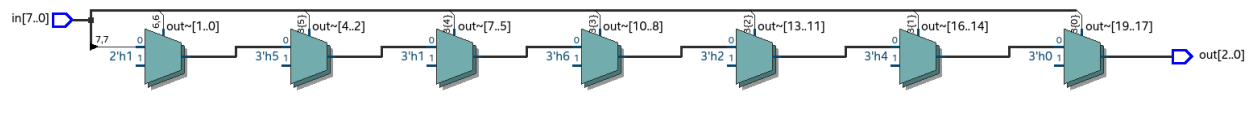
```
Activities Terminal Dec 23 10:08 AM

taha_aka_beast@ubuntu ~ → cd /home/taha_aka_beast/project_verilog/Barrel_Shifter_32Bit
ls
BarrelShifter.pqf  BarrelShifter.sv.bak  c5_pin_model_dump.txt  shifter_sim
BarrelShifter.qsf  BarrelShifter_tb.sv    db                      simulation
BarrelShifter.qws  BarrelShifter_tb.sv.bak incremental_db
BarrelShifter.sv   BarrelShifter.vcd      output_files
taha_aka_beast@ubuntu ~/project_verilog/Barrel_Shifter_32Bit → rm -f *.vcd shifter_sim
taha_aka_beast@ubuntu ~/project_verilog/Barrel_Shifter_32Bit → iverilog -g2012 BarrelShifter.sv BarrelShifter_tb.sv -o shifter_sim
taha_aka_beast@ubuntu ~/project_verilog/Barrel_Shifter_32Bit → vvp shifter_sim
VCD info: dumpfile BarrelShifter.vcd opened for output.
_____Test Start_____
PASS: data_in=1 shift=2 dir=0 out=4
PASS: data_in=1 shift=2 dir=1 out=0
PASS: data_in=2 shift=5 dir=0 out=64
PASS: data_in=2 shift=5 dir=1 out=0
PASS: data_in=303379748 shift=1 dir=1 out=151689874
PASS: data_in=2985317987 shift=13 dir=1 out=364418
PASS: data_in=2999092325 shift=18 dir=1 out=11440
PASS: data_in=114806029 shift=22 dir=1 out=27
PASS: data_in=1993627629 shift=12 dir=1 out=486725
PASS: data_in=3812041926 shift=5 dir=0 out=1726257344
PASS: data_in=1924134885 shift=23 dir=0 out=4068474880
PASS: data_in=1206705039 shift=18 dir=0 out=1849425920
PASS: data_in=4093672168 shift=5 dir=0 out=2148490496
PASS: data_in=3733858493 shift=13 dir=1 out=455793
-----SUMMARY-----
Total Passed: 15
Total Failed: 0
-----
taha_aka_beast@ubuntu ~/project_verilog/Barrel_Shifter_32Bit → gtkwave BarrelShifter.vcd &
[1] 7227
taha_aka_beast@ubuntu ~/project_verilog/Barrel_Shifter_32Bit →
GTKWave Analyzer v3.3.104 (w)1999-2020 BSI

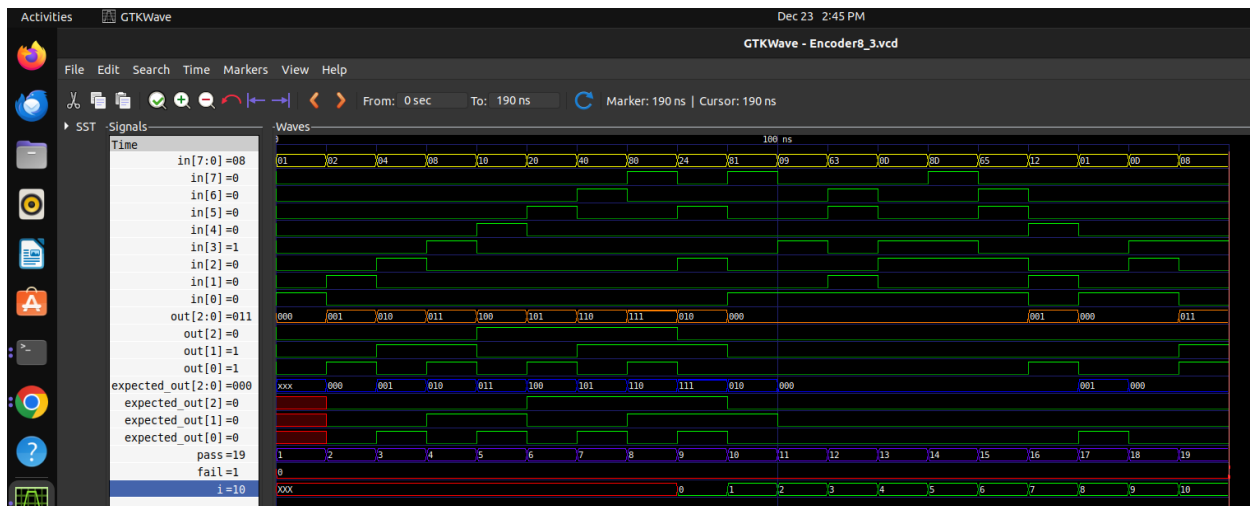
[0] start time.
[140000] end time.
taha_aka_beast@ubuntu ~/project_verilog/Barrel_Shifter_32Bit →
```

TASK 3: ENCODER (8 to 3)

RTL View:



Simulation View:



Command View With Test Summary:

```
Activities Terminal Dec 23 2:46 PM
taha_aka_beast@ubuntu ~ → cd /home/taha_aka_beast/project_verilog/Encoder
taha_aka_beast@ubuntu ~/project_verilog/Encoder → rm -f *.vcd encoder_sim
taha_aka_beast@ubuntu ~/project_verilog/Encoder → iverilog -g2012 Encoder8_3.sv tb_Encoder8_3.sv -o encoder_sim
Encoder8_3.sv:9: error: r_out is not a valid l-value in tb_Encoder8_3.dut.
Encoder8_3.sv:6:      : r_out is declared here as wire.
1 error(s) during elaboration.
taha_aka_beast@ubuntu ~/project_verilog/Encoder → iverilog -g2012 Encoder8_3.sv tb_Encoder8_3.sv -o encoder_sim
Encoder8_3.sv:8: error: Could not find variable `r_out' in `tb_Encoder8_3.dut'
1 error(s) during elaboration.
taha_aka_beast@ubuntu ~/project_verilog/Encoder → iverilog -g2012 Encoder8_3.sv tb_Encoder8_3.sv -o encoder_sim
Encoder8_3.sv:8: error: Could not find variable `r' in `tb_Encoder8_3.dut'
1 error(s) during elaboration.
taha_aka_beast@ubuntu ~/project_verilog/Encoder → iverilog -g2012 Encoder8_3.sv tb_Encoder8_3.sv -o encoder_sim
vvp encoder_sim
gtkwave Encoder8_3.vcd
VCD info: dumpfile Encoder8_3.vcd opened for output.
===== Encoder8_3 Testbench Start =====
PASS: in=00000001 => out=000
PASS: in=00000010 => out=001
PASS: in=00000100 => out=010
PASS: in=00001000 => out=011
PASS: in=00010000 => out=100
PASS: in=00100000 => out=101
PASS: in=01000000 => out=110
PASS: in=10000000 => out=111
PASS: in=001000100 => out=010
PASS: in=100000001 => out=000
PASS: in=000010001 => out=000
PASS: in=011000011 => out=000
PASS: in=00001101 => out=000
PASS: in=10001101 => out=000
PASS: in=01100101 => out=000
PASS: in=00010010 => out=001
PASS: in=00000001 => out=000
PASS: in=00001101 => out=000
FAIL: in=00001000 => out=011 (expected=000)
-----SUMMARY-----
Total Passed: 19
Total Failed: 1
-----
GTKWave Analyzer v3.3.104 (w)1999-2020 BSI
[0] start time.
[190000] end time.
GTKWAVE | Select one or more traces.
GTKWAVE | Select one or more traces.
GTKWAVE | Select one or more traces.
```

Note:

The codes for all three tasks have been included in this GitHub repository: [Xcelerium internship Repository](#).