



PROGRESS REPORT

Week 2

Submitted By

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Batch: 2023

Department: Electrical Engr.

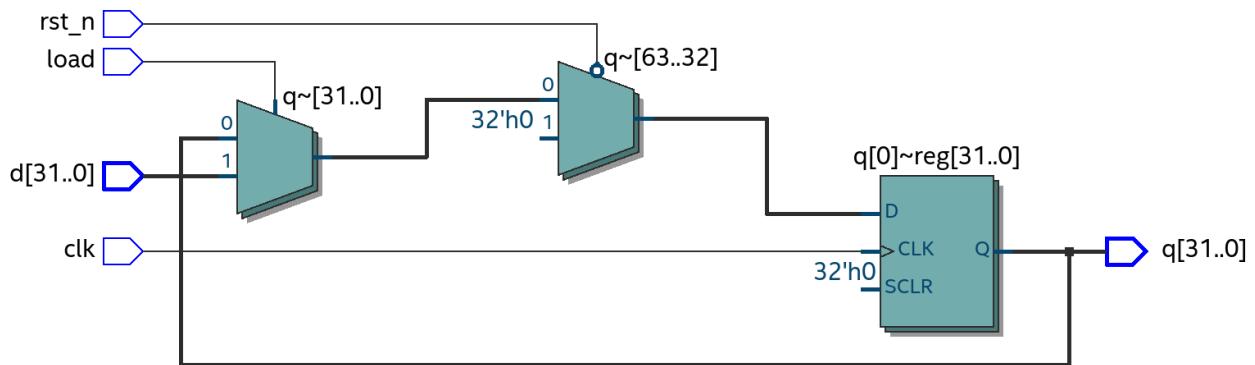
Submitted To

Miss Hafsa Amanullah

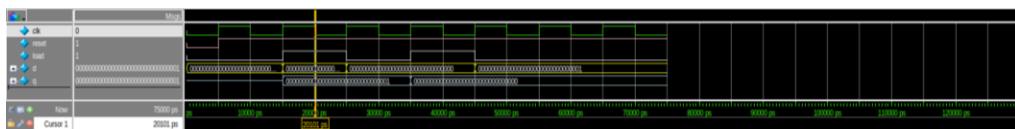
Dr. Fahim-Ul-Haq

TASK 1: 32 BIT REGISTER

RTL View:



Simulation View:

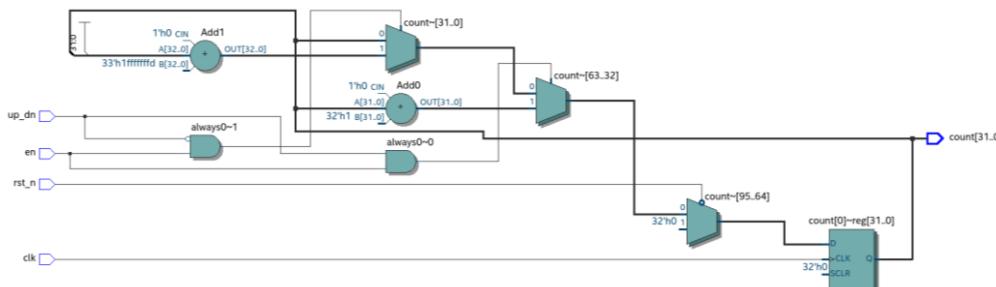


Note:

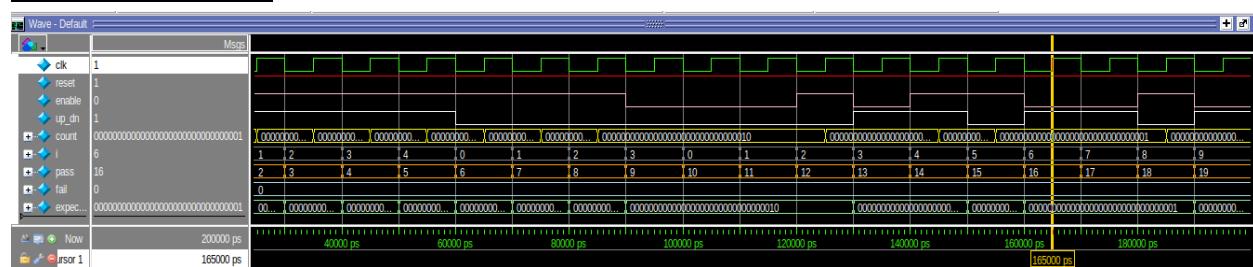
The codes of this module, along with their respective simulation file, have been included in the GitHub repository: [Xcelerium Internship Repository](#)

TASK 2: 32 BIT COUNTER

RTL View:



Simulation View:



Summary:

```

#> Transcript
ModelSim cd /home/taha_aka_beast/projects_verilog/Counter
ModelSim vdel -all
ModelSim vlog tb_counter.v
ModelSim vlog -sv tb_counter.sv
# Model Technology Modelsim - Intel FPGAs Edition vlog 2020.1 Compiler 2020.02 Feb 28 2020
start time: 03:27:02 on Dec 27, 2025
# VLOG-1000: "tb_counter.sv" loaded
# -- Compiling module counter
# -- Compiling module tb_counter
#
# Top level modules:
# tb_counter
# End compilation time: 03:27:02 on Dec 27, 2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim vsim work.tb_counter
# vsim work.tb_counter
# Start time: 03:27:02 on Dec 27, 2025
# Loading av_std.svh
# Loading work.tb_counter
# Loading work.tb_counter
# Loading work.tb_counter
VSM> add wave -r *
VSM> run -all
# ----- STARTING DIRECTED TEST -----
# ----- DIRECTED TEST -----
# ----- TEST COMPLETE -----
# PASSED = 20, FAILED = 0
# * Notes: $finish + tb_counter.sv(98)
# * Time: 200 ns Iteration: 0 Instances: /tb_counter
# 1
VSM>
VSM>
VSM>

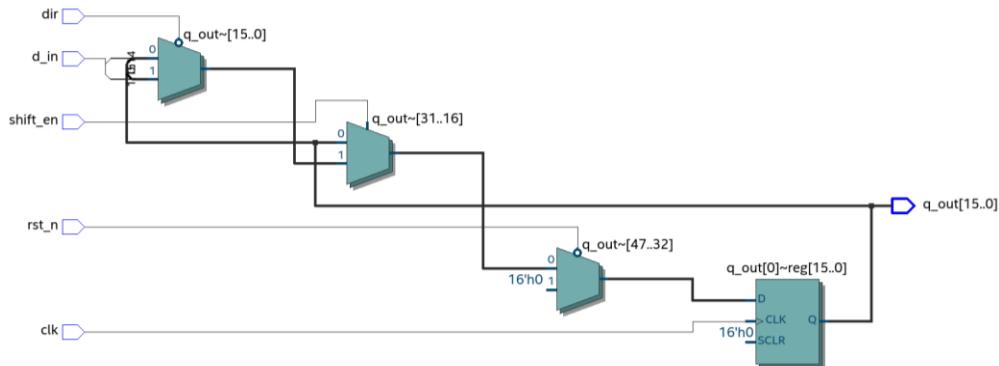
```

Note:

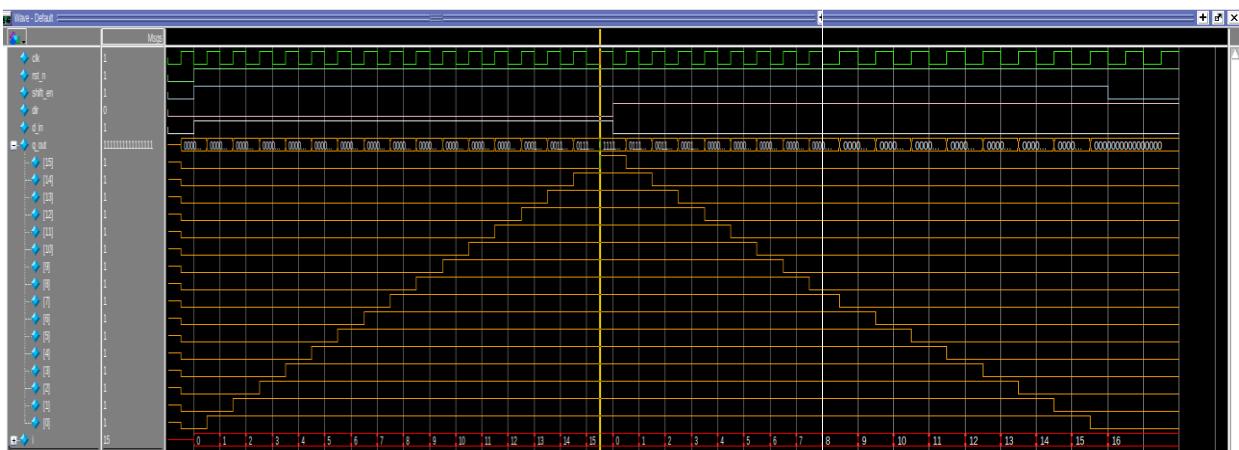
The codes of this module, along with their respective simulation file, have been included in the GitHub repository: [Xcelerium Internship Repository](#)

TASK 3: SHIFT REGISTER

RTL View:



Simulation View:



Summary:

```

Activities Dialog Dec 27 5:36 PM 11%
File Edit View Bookmarks Window Help
Transcript
ModelSim cd /home/sahab_aika_beans/projects_Verilog/shift_Reg
ModelSim vlib work
ModelSim vlog -sv shift_Reg.sv tb_shift_Reg.sv
ModelSim vlog -sv shift_Reg.sv tb_shift_Reg.sv
# Start time: 17:30:33 on Dec 27, 2020
# vlog -reportprogress 300 -arw shift_Reg.sv tb_shift_Reg.sv
# -- Compiling module tb_shift_Reg
# Top level modules:
#   tb_shift_Reg
# End synthesis time on Dec 27, 2020, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim vlib work+tb_shift_Reg
# Start time: 17:30:33 on Dec 27, 2020
# Loading ev_std.wlf
# Loading work.tb_shift_Reg
# Loading work.tb_shift_Reg
# Loading work.tb_shift_Reg
# VSM> run -all
# T=0 rsel=0 en=0 dir=0 din=0 q= 0
# T=100000 rsel=1 en=0 dir=0 din=0 q= 0
# T=105000 rsel=1 en=1 dir=0 din=1 q= 0
# T=150000 rsel=1 en=1 dir=0 din=1 q= 1
# T=200000 rsel=1 en=1 dir=0 din=1 q= 2
# T=250000 rsel=1 en=1 dir=0 din=1 q= 3
# T=300000 rsel=1 en=1 dir=0 din=1 q= 7
# T=350000 rsel=1 en=1 dir=0 din=1 q= 15
# T=400000 rsel=1 en=1 dir=0 din=1 q= 31
# T=450000 rsel=1 en=1 dir=0 din=1 q= 63
# T=500000 rsel=1 en=1 dir=0 din=1 q= 127
# T=550000 rsel=1 en=1 dir=0 din=1 q= 255
# T=600000 rsel=1 en=1 dir=0 din=1 q= 511
# T=650000 rsel=1 en=1 dir=0 din=1 q= 1023
# T=1100000 rsel=1 en=1 dir=1 din=1 q= 2047
# T=1150000 rsel=1 en=1 dir=1 din=1 q= 4095
# T=1200000 rsel=1 en=1 dir=1 din=1 q= 8191
# T=1450000 rsel=1 en=1 dir=1 din=1 q= 65535
# T=1650000 rsel=1 en=1 dir=1 din=1 q= 131073
# T=1750000 rsel=1 en=1 dir=1 din=1 q= 32767
# T=1850000 rsel=1 en=1 dir=1 din=1 q= 18383
# T=2050000 rsel=1 en=1 dir=1 din=1 q= 4095
# T=2250000 rsel=1 en=1 dir=1 din=1 q= 8191
# T=2250000 rsel=1 en=1 dir=1 din=1 q= 1023
# T=2350000 rsel=1 en=1 dir=1 din=1 q= 511
# T=2550000 rsel=1 en=1 dir=1 din=1 q= 255
# T=2550000 rsel=1 en=1 dir=1 din=1 q= 127
# T=2750000 rsel=1 en=1 dir=1 din=1 q= 63
# T=2850000 rsel=1 en=1 dir=1 din=1 q= 31
# T=2950000 rsel=1 en=1 dir=1 din=1 q= 15
# T=3050000 rsel=1 en=1 dir=1 din=1 q= 7
# T=3050000 rsel=1 en=1 dir=1 din=1 q= 3
# T=3250000 rsel=1 en=1 dir=1 din=1 q= 1
# T=3350000 rsel=1 en=1 dir=1 din=1 q= 0
# T=3350000 rsel=1 en=1 dir=1 din=1 q= 0
# -- None: $finish : vlog shift_Reg.sv@14

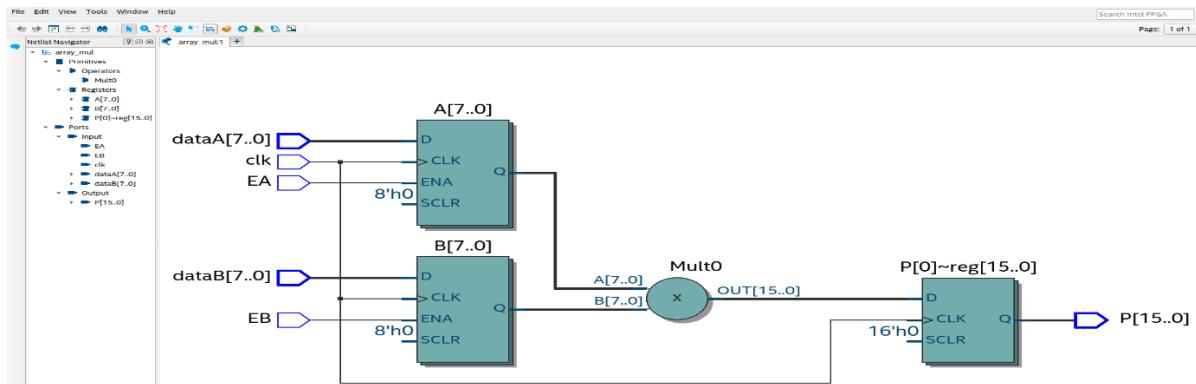
```

Note:

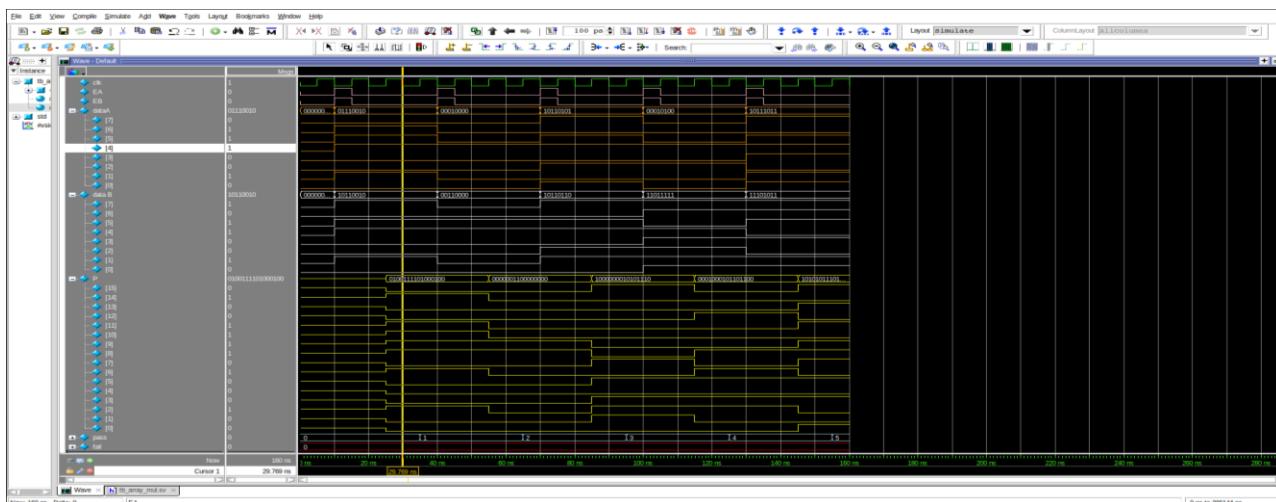
The codes of this module, along with their respective simulation file, have been included in the GitHub repository: [Xcelerium Internship Repository](#)

TASK 4: ARRAY MULTIPLIER

RTL View:



Simulation View:



Summary:

```

ModelSim cd "/home/ahaa_aka_beast/project_verilog/array Multiplier"
ModelSim -cd "/home/ahaa_aka_beast/project_verilog/array Multiplier" -sv
ModelSim -vlib work
ModelSim vlog -sv array_mult.sv tb_array_mult.sv
# Model Technology Modelsim - Intel FPGA Edition vlog 2020.1 Compiler 2020.02 Feb 28 2020
# File: /home/ahaa_aka_beast/project_verilog/array Multiplier/tb_array_mult.sv
# vlog -reportprogress 300 -sv array_mult.sv tb_array_mult.sv
# -- Compiling module array_mult
# -- Compiling module tb_array_mult
# -- End of compilation
# Top level modules:
#   tb_array_mult
# End time: 100 ns on Dec 10, 2025, Elapsed timer: 0:00:00
# Errors: 0, Warnings: 0
ModelSim vsim work.tb_array_mult
vsim tb_array_mult
# Start time: 02:01:00 on Dec 10, 2025
# Loading sv_std.sv
# Loading sv_tb_array_mult
# Loading tb_array_mult
# Using Verilog 2001 syntax
VSM> add wave -r *
VSM> run -all
# TEST 1 PASS : 114 * 178 = 202292
# TEST 2 PASS : 16 * 48 = 768
# TEST 3 PASS : 181 * 182 = 32942
# TEST 3 PASS : 20 * 223 = 4460
# TEST 4 PASS : 187 * 235 = 43945
#
# ----- SUMMARY -----
# Total Tests : 5
# Tests Passed : 5
# Tests Failed : 0
# Overall Status : ALL TESTS PASSED
# -- Note: $finish in tb_array_mult.sv(55)
# Time 100 ns Iteration 0 Instances: /tb_array_mult
# 1
# break in module tb_array_mult at tb_array_mult.sv line 55
VSM>

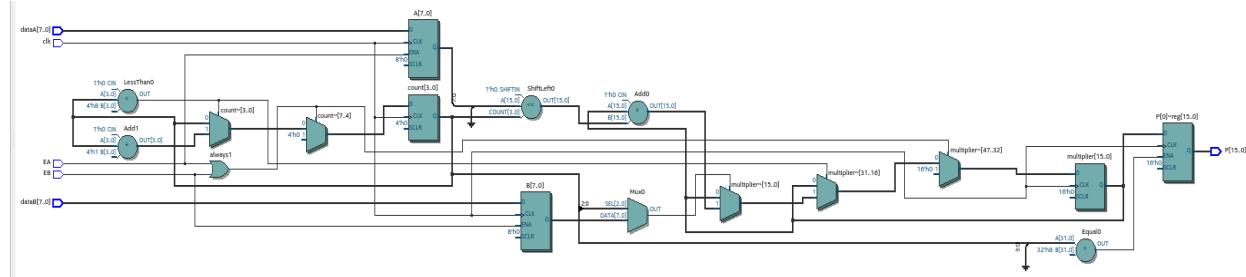
```

Note:

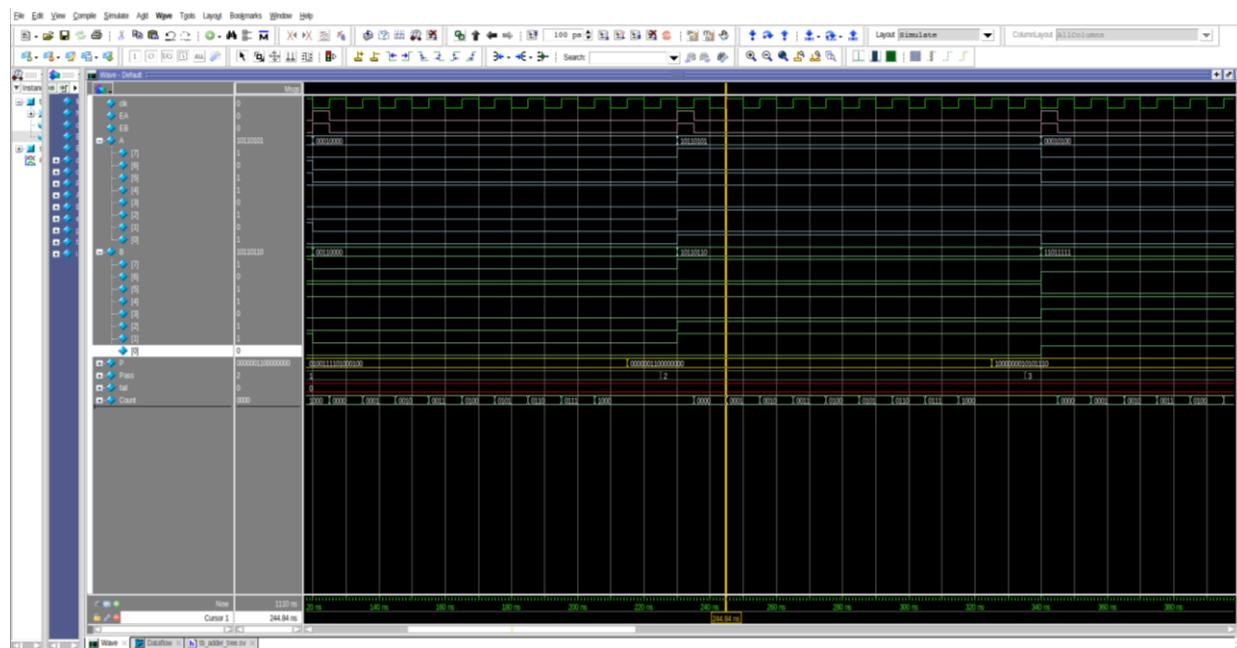
The codes of this module, along with their respective simulation file, have been included in the GitHub repository: [Xcelerium Internship Repository](#)

TASK 5: ADDER TREE

RTL View:



Simulation View:



Summary:

```
# Timer: 1000 ns Scope: tb_adder_tree File: tb_adder_tree.v Log: 14
# ===== SUMMARY =====
# Total Tests : 10
# Tests Passed : 10
# Tests Failed : 0
# OVERALL STATUS : SOME TESTS FAILED
# ===== TESTS =====
# * Notes: $finish + tb_adder_tree.v(7)
# Timer: 1000 ns Iteration: 0 Instances: /tb_adder_tree
# ===== TEST 1 =====
# Errors: 0, Warnings: 0
# Breaks in module tb_adder_tree at tb_adder_tree.v line 71
VSM40 vodel -all
VSM40
VSM40 vlog -sv adder_tree.v tb_adder_tree.v
# Model Technology Modelsim - Intel FPG Edition Vlog 2020.02 Feb 28 2020
# Compiler Version: 2020.02.02.000000
# vlog -reportprogress 300 -sv adder_tree.v tb_adder_tree.v
# -svc vlog.log -svc adder_tree.vc
# -Compiler module tb_adder_tree
# Top level modules:
#   tb_adder_tree
# End of compilation on Dec 31,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
VSM40 vsim work.tb_adder_tree
# Model Technology Modelsim - Intel FPG Edition Vsim 2020.02 Feb 28 2020
# Compiler Version: 2020.02.02.000000
# Start time: 09:37:17 on Dec 31,2025
# Loading svd.vhd
# Loading work.tb_adder_tree
# Loading work.adder_tree
# Loading work.tb_adder_tree
# Using -vopt+mc=1
VSM40 run -all
# TEST 0 PASS : 111 * 111 = 20392
# TEST 1 PASS : 111 * 111 = 20392
# TEST 2 PASS : 181 * 182 = 32942
# TEST 3 PASS : 181 * 182 = 32942
# TEST 4 PASS : 187 * 238 = 43945
# TEST 5 PASS : 187 * 238 = 43945
# TEST 6 PASS : 129 * 2 = 414
# TEST 7 PASS : 252 * 93 = 23436
# TEST 8 PASS : 252 * 93 = 23436
# TEST 9 PASS : 22 * 63 = 1386
# ===== SUMMARY =====
# Total Tests : 10
# Tests Passed : 10
# Tests Failed : 0
# Overall Status: ALL TESTS PASSED
# ===== TEST 10 =====
# Notes: $finish + tb_adder_tree.v(7)
# Timer: 1110 ns Iteration: 0 Instances: /tb_adder_tree
# ===== TEST 11 =====
# Errors: 0, Warnings: 0
# Breaks in module tb_adder_tree at tb_adder_tree.v line 71
VSM40
VSM40
```

Note:

The codes of this module, along with their respective simulation file, have been included in the GitHub repository: [Xcelerium Internship Repository](#)