PROGRESS REPORT

Week 2

Submitted By

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Batch: 2023

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Submitted To

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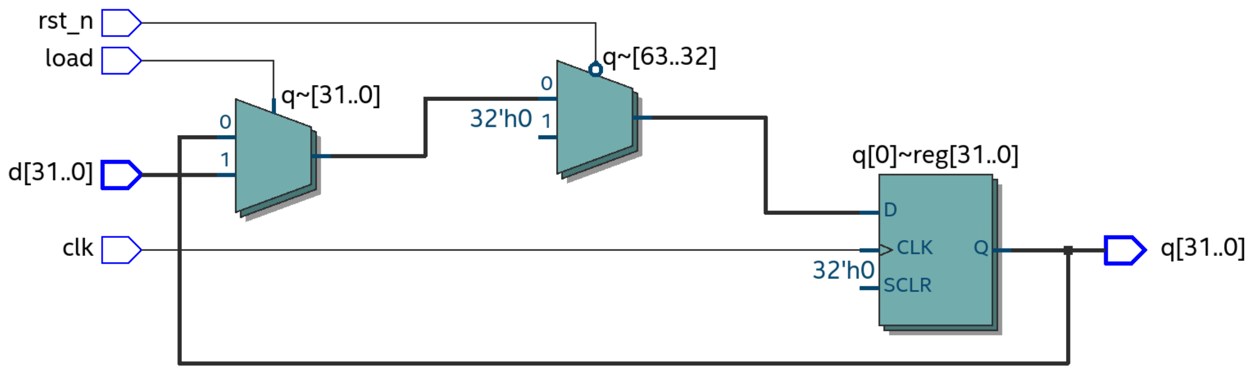
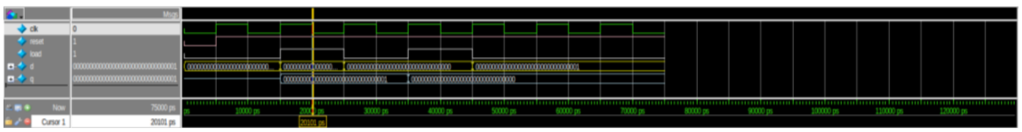
TASK 1: 32 BIT REGISTER

RTL View:



Simulation View:

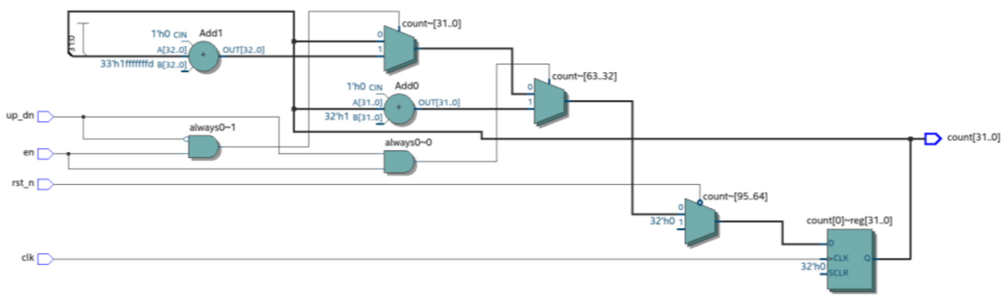


Note:

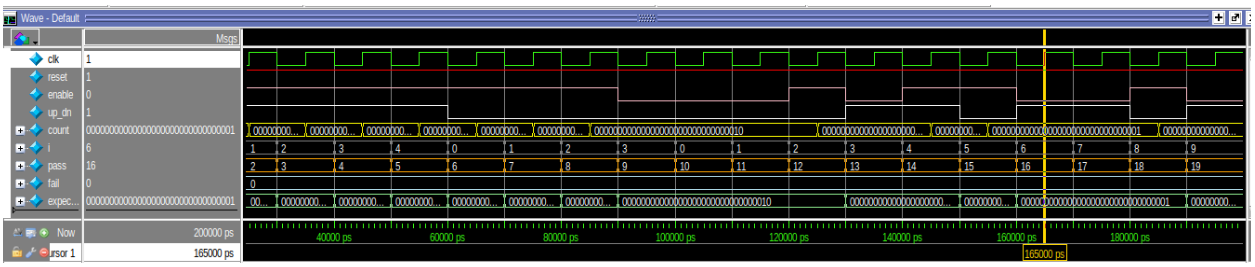
The codes of this module, along with their respective simulation file, have been included in the GitHub repository: **Xcelerium Internship Repository**

TASK 2: 32 BIT COUNTER

RTL View:



Simulation View:



Summary:

Note:

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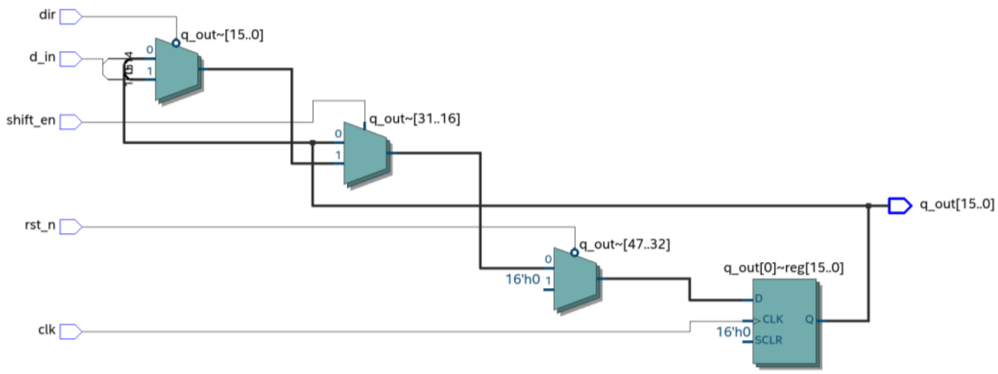
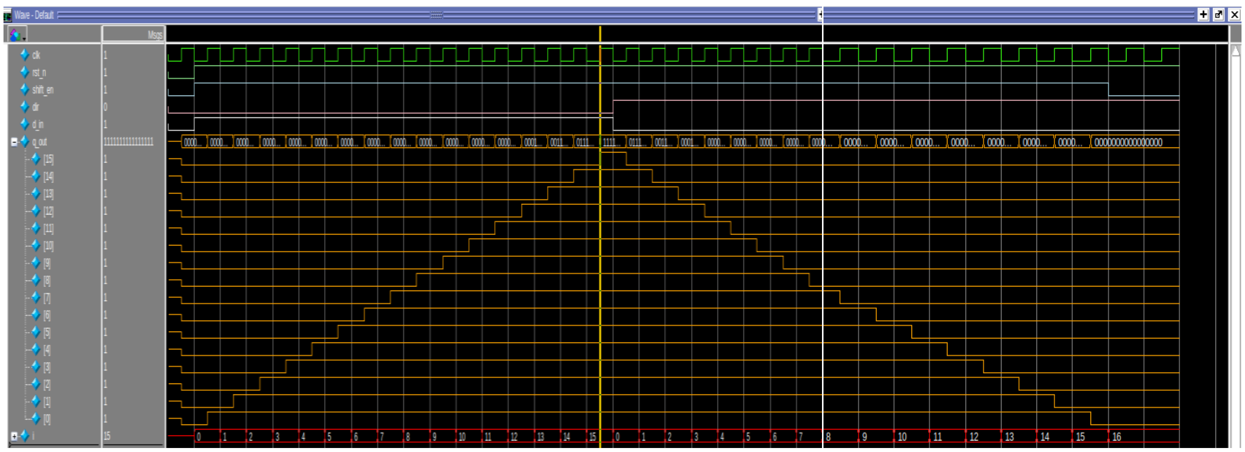
TASK 3: SHIFT REGISTER

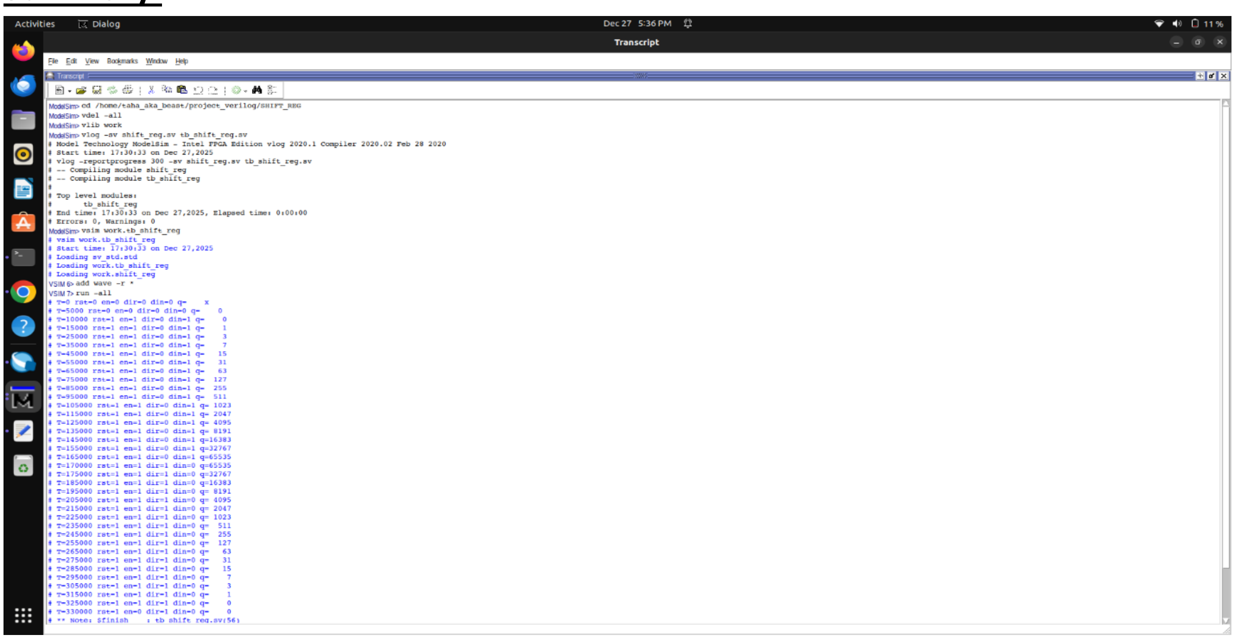
RTL View:



Simulation View:



Summary:



Note:

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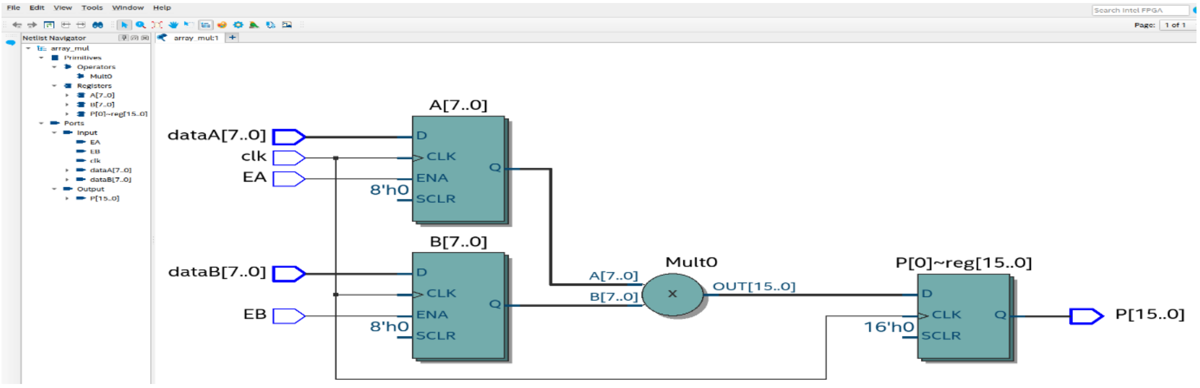
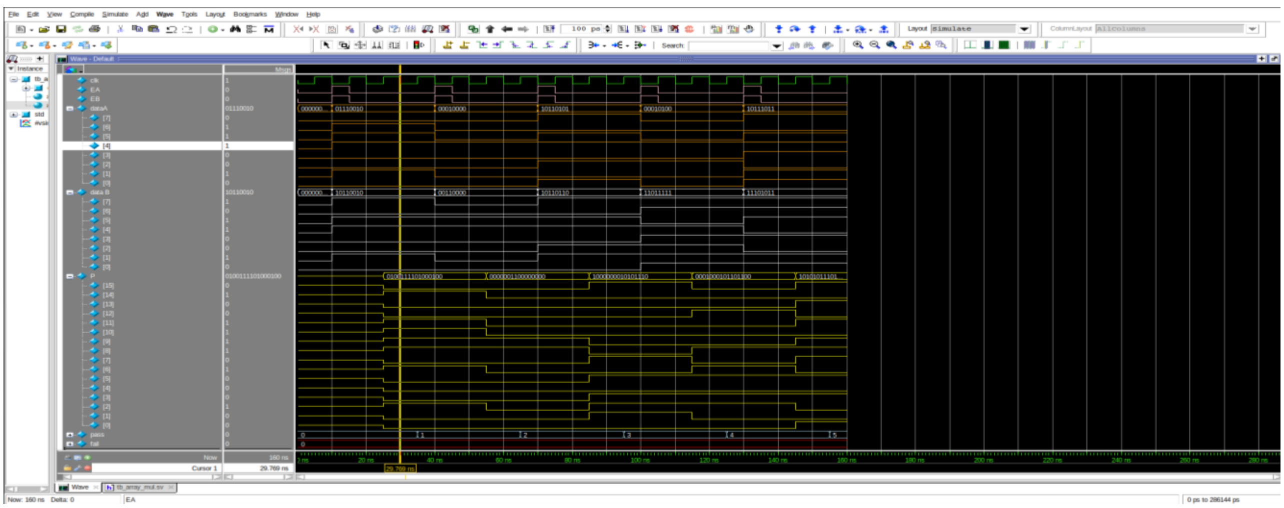
TASK 4: ARRAY MULTIPLIER

RTL View:



Simulation View:



Summary:

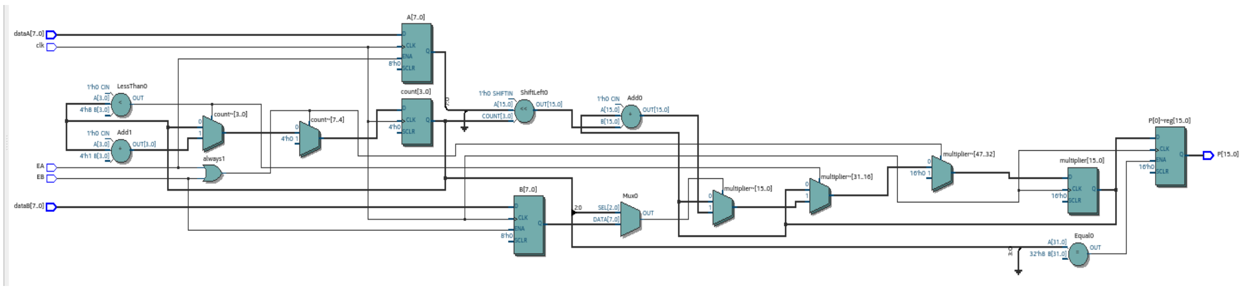
```
ModelSim> cd "/home/taha_aka_beast/project_verilog/Array Multiplier"
ModelSim> vdel -all
ModelSim> vlib work
ModelSim> vlog -sv array_mul.sv tb_array_mul.sv
# Model Technology ModelSim - Intel FPGA Edition vlog 2020.1 Compiler 2020.02 Feb 28 2020
# Start time: 02:01:50 on Dec 30,2025
# vlog -reportprogress 300 -sv array_mul.sv tb_array_mul.sv
# -- Compiling module array_mul
# -- Compiling module tb_array_mul
#
# Top level modules:
#       tb_array_mul
# End time: 02:01:50 on Dec 30,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim> vsim work.tb_array_mul
# vsim work.tb_array_mul
# Start time: 02:01:50 on Dec 30,2025
# Loading sv_std.std
# Loading work.tb_array_mul
# Loading work.array_mul
VSIM 6> add wave -r *
VSIM 7> run -all
# TEST 0 PASS : 114 * 178 = 20292
# TEST 1 PASS : 16 * 48 = 768
# TEST 2 PASS : 181 * 182 = 32942
# TEST 3 PASS : 20 * 223 = 4460
# TEST 4 PASS : 187 * 235 = 43945
#
# ----------------- SUMMARY -----------------
# Total Tests  : 5
# Tests Passed : 5
# Tests Failed : 0
# OVERALL STATUS : ALL TESTS PASSED
# -------------------------------------------
# ** Note: $finish    : tb_array_mul.sv(55)
#    Time: 160 ns  Iteration: 0  Instance: /tb_array_mul
# 1
# Break in Module tb_array_mul at tb_array_mul.sv line 55

VSIM 8>
```

Note:

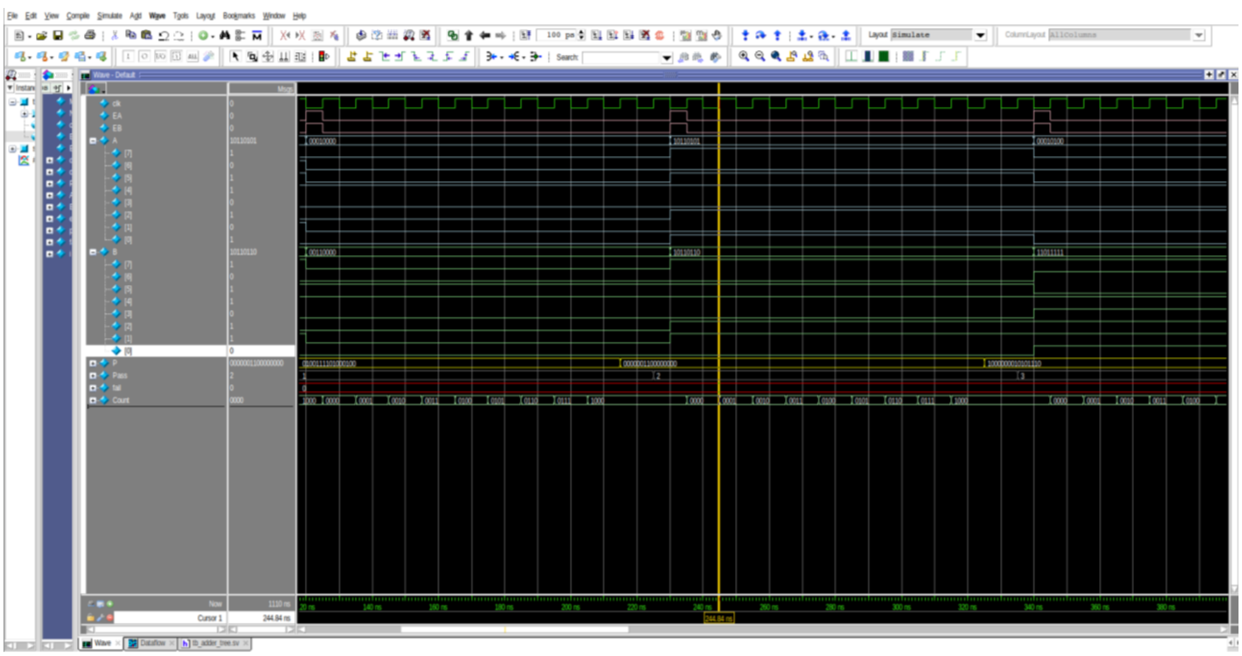
The codes of this module, along with their respective simulation file, have been included in the GitHub repository: **Xcelerium Internship Repository**

TASK 5: ADDER TREE

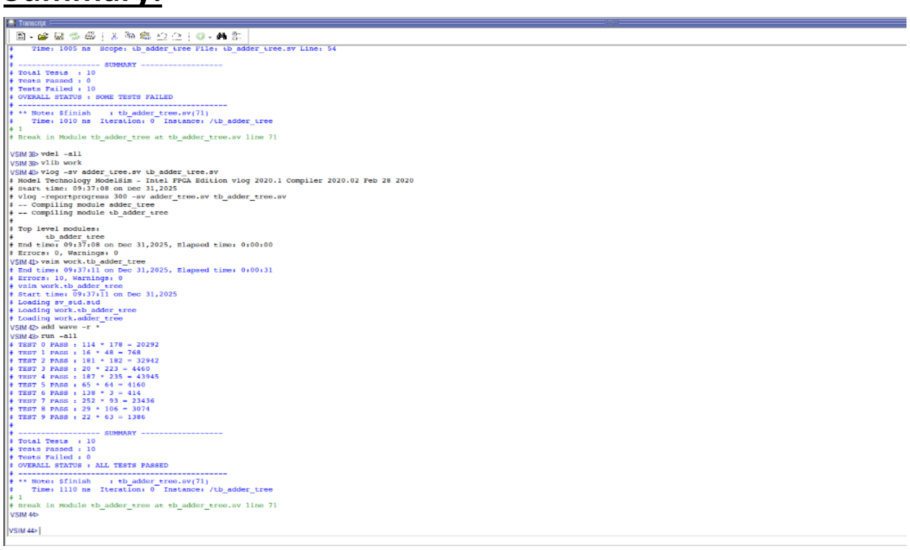
RTL View:



Simulation View:



Summary:



```
Transcript
#    Time: 1005 ns  Scope: tb_adder_tree File: tb_adder_tree.sv Line: 54
#
# ------------------ SUMMARY ------------------
# Total Tests  : 10
# Tests Passed : 0
# Tests Failed : 10
# OVERALL STATUS : SOME TESTS FAILED
# ----------------------------------------------
# ** Note: $finish    : tb_adder_tree.sv(71)
#    Time: 1010 ns  Iteration: 0  Instance: /tb_adder_tree
# 1
# Break in Module tb_adder_tree at tb_adder_tree.sv line 71

VSIM 38> vdel -all
VSIM 39> vlib work
VSIM 40> vlog -sv adder_tree.sv tb_adder_tree.sv
# Model Technology ModelSim - Intel FPGA Edition vlog 2020.1 Compiler 2020.02 Feb 28 2020
# Start time: 09:37:08 on Dec 31,2025
# vlog -reportprogress 300 -sv adder_tree.sv tb_adder_tree.sv
# -- Compiling module adder_tree
# -- Compiling module tb_adder_tree
#
# Top level modules:
#       tb_adder_tree
# End time: 09:37:08 on Dec 31,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
VSIM 41> vsim work.tb_adder_tree
# End time: 09:37:11 on Dec 31,2025, Elapsed time: 0:00:31
# Errors: 10, Warnings: 0
# vsim work.tb_adder_tree
# Start time: 09:37:11 on Dec 31,2025
# Loading sv_std.std
# Loading work.tb_adder_tree
# Loading work.adder_tree
VSIM 42> add wave -r *
VSIM 43> run -all
# TEST 0 PASS : 114 * 178 = 20292
# TEST 1 PASS : 16 * 48 = 768
# TEST 2 PASS : 181 * 182 = 32942
# TEST 3 PASS : 20 * 223 = 4460
# TEST 4 PASS : 187 * 235 = 43945
# TEST 5 PASS : 65 * 64 = 4160
# TEST 6 PASS : 138 * 3 = 414
# TEST 7 PASS : 252 * 93 = 23436
# TEST 8 PASS : 29 * 106 = 3074
# TEST 9 PASS : 22 * 63 = 1386
#
# ------------------ SUMMARY ------------------
# Total Tests  : 10
# Tests Passed : 10
# Tests Failed : 0
# OVERALL STATUS : ALL TESTS PASSED
# ----------------------------------------------
# ** Note: $finish    : tb_adder_tree.sv(71)
#    Time: 1110 ns  Iteration: 0  Instance: /tb_adder_tree
# 1
# Break in Module tb_adder_tree at tb_adder_tree.sv line 71
VSIM 44>

VSIM 44>
```

Note:

The codes of this module, along with their respective simulation file, have been included in the GitHub repository: **Xcelerium Internship Repository**