



# PROGRESS REPORT

## Week 2

### **Submitted By**

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Batch: 2023

Department: Electrical Engr.

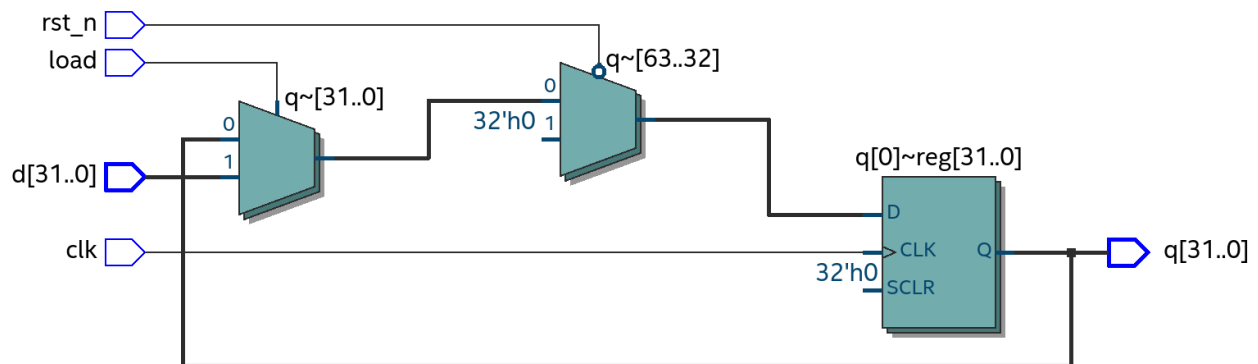
### **Submitted To**

Miss Hafsa Amanullah

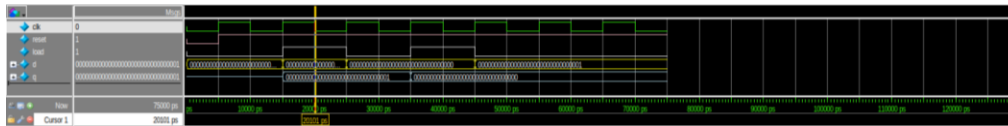
Dr. Fahim-Ul-Haq

## TASK 1: 32 BIT REGISTER

### RTL View:



### Simulation View:

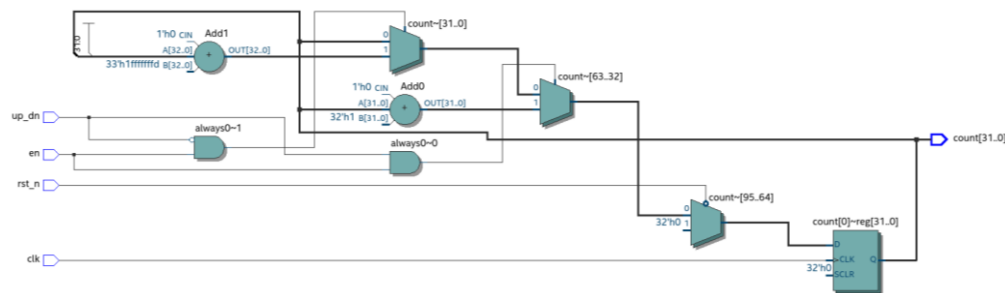


### Note:

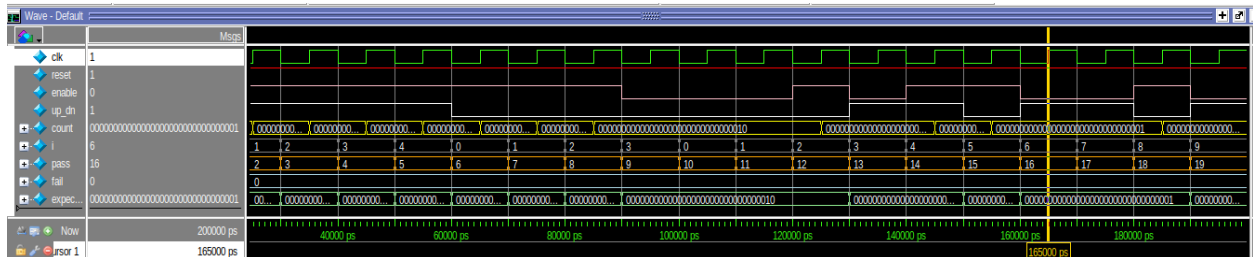
The codes of this module, along with their respective simulation file, have been included in the GitHub repository: [Xcelerium Internship Repository](#)

## TASK 2: 32 BIT COUNTER

### RTL View:



### Simulation View:



### Summary:

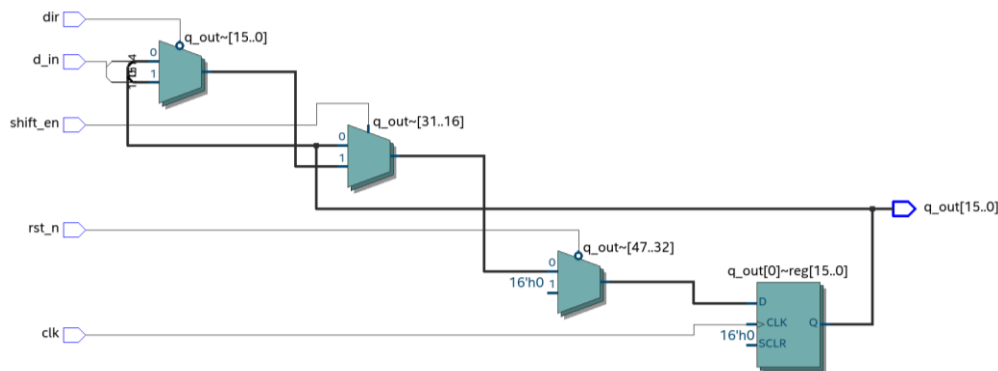
```
Transcript
ModelSim cd /home/taha_aka_beast/project_verilog/Counter
ModelSim vdel -all
ModelSim vlib work
ModelSim vlog -sv counter.sv tb_counter.sv
# Model Technology ModelSim - Intel FPGA Edition vlog 2020.12 Feb 28 2020
# Start time: 03:27:02 on Dec 27, 2025
# vlog -reportprogress 300 -sv counter.sv tb_counter.sv
# -- Compiling module counter
# -- Compiling module tb_counter
#
# Top level modules:
#   tb_counter
# End time: 03:27:02 on Dec 27, 2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim vaim work.tb_counter
# vaim work.tb_counter
# Start time: 03:27:02 on Dec 27, 2025
# Loading sv_std.sv
# Loading work.tb_counter
# Loading work.counter
VSIModel add wave -r *
VSIModel run -all
# ----- STARTING DIRECTED TEST -----
# ----- STARTING RANDOM TEST -----
# ----- TEST COMPLETE -----
# PASSED = 20, FAILED = 0
# -- Next: Finish -- : tb_counter.sv:98
# Time: 200 ns Iteration: 0 Instance: /tb_counter
# Break in Module tb_counter at tb_counter.sv line 98
VSIModel
VSIModel
```

### Note:

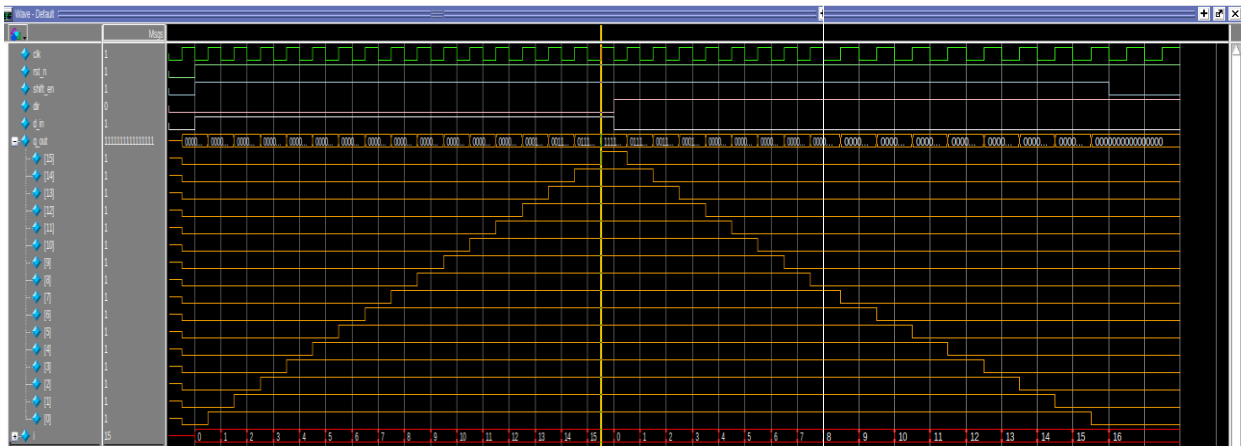
The codes of this module, along with their respective simulation file, have been included in the GitHub repository: [Xcelarium Internship Repository](#)

## TASK 3: SHIFT REGISTER

### RTL View:



### Simulation View:

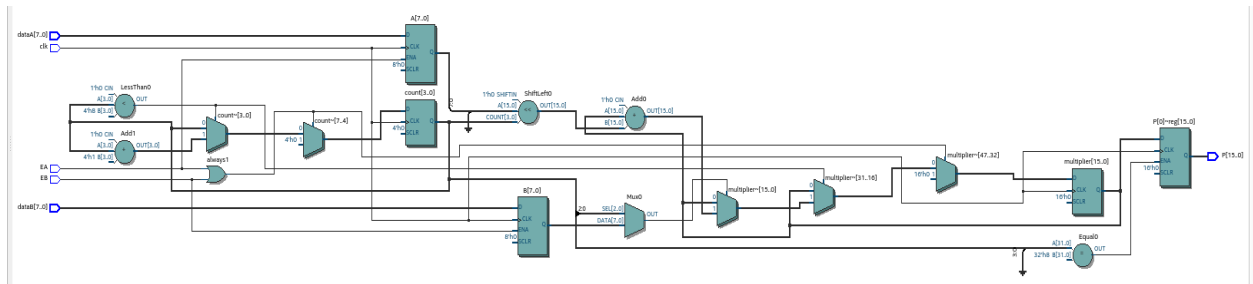


### Summary:

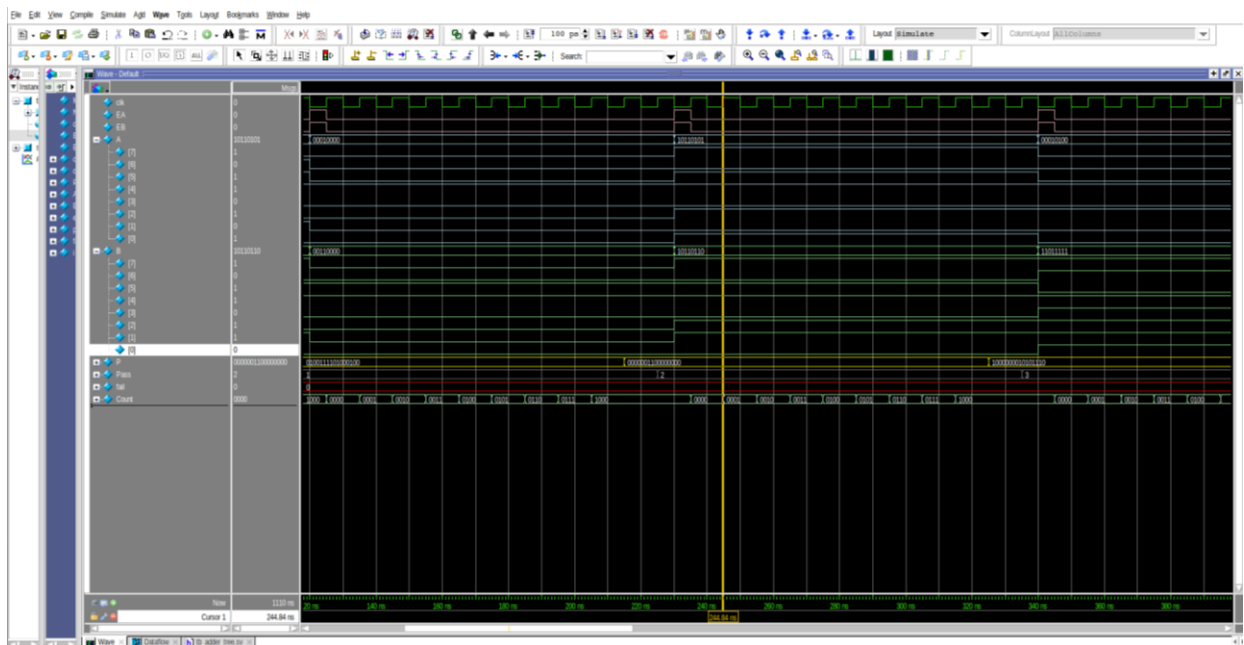
```
Activities [X] Dialog Dec 27 5:36 PM 11%
Transcript
ModelSim -vlog -sv shift_reg.v -tcl shift_reg.tcl
ModelSim vdel -all
ModelSim work
ModelSim vlog -sv shift_reg.v -tcl shift_reg.tcl
Model Technology ModelSim - Intel FPGA Edition vlog 2020.02 Feb 28 2020
# Start time: 17:30:33 on Dec 27, 2025
# vlog -reportprogress 300 -sv shift_reg.v -tcl shift_reg.tcl
# -- Compiling module shift_reg
# -- Compiling module tb_shift_reg
#
# Top level modules:
#   tb_shift_reg
# End time: 17:30:33 on Dec 27, 2025, elapsed time: 0:00:00
# Errors: 0, Warnings: 0
ModelSim vsim work.tb_shift_reg
# Start time: 17:30:33 on Dec 27, 2025
# Loading sv_sdl.acd
# Loading work.tb_shift_reg
# Loading work.tb_shift_reg
VSM>add wave -e
VSM>run -all
t=0 ns r=0 ns d=0 dir=0 q= 0
t=1000 ns r=0 ns d=0 dir=0 q= 0
t=1500 ns r=1 ns d=1 dir=0 q= 1
t=2000 ns r=1 ns d=1 dir=0 q= 3
t=3000 ns r=1 ns d=1 dir=0 q= 7
t=4000 ns r=1 ns d=1 dir=0 q= 15
t=5000 ns r=1 ns d=1 dir=0 q= 31
t=6000 ns r=1 ns d=1 dir=0 q= 63
t=7000 ns r=1 ns d=1 dir=0 q= 127
t=8000 ns r=1 ns d=1 dir=0 q= 255
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t=205000 ns r=1 ns d=1 dir=1 q= 5142201741628768881734278695491720266174115386003115999231
t=206000 ns r=1 ns d=1 dir=1 q= 10284403483257537763468557390983440532348230772006231998463
t=207000 ns r=1 ns d=1 dir=1 q= 20568806966515075526937114781966881064696461544012463996927
t=208000 ns r=1 ns d=1 dir=1 q= 41137613933030151053874229563933762129392923088024927993855
t=209000 ns r=1 ns d=1 dir=1 q= 82275227866060302107748459127867524258785846176049855987711
t=210000 ns r=1 ns d=1 dir=1 q= 164550455732120604215496918255735048517571692352099711975423
t=211000 ns
```

The codes of this module, along with their respective simulation file, have been included in the GitHub repository: **Xcelerium Internship Repository**

### RTL View:



### Simulation View:



### Summary:

```

#
Time: 1905 ns Scope: tb_adder_tree File: tb_adder_tree.v Line: 54
#
----- SUMMARY -----
#
Total Tests : 10
Tests Passed : 6
Tests Failed : 0
OVERALL STATUS : SOME TESTS FAILED
#
-----
#
-- Runaway: [finish] + tb_adder_tree.v[71]
#
Time: 1910 ns Iterations: 0 Instances: /tb_adder_tree
#
1
#
Break is module tb_adder_tree at tb_adder_tree.v line 71
#
VDM@vdm1> exit
VDM@vdm1> work
VDM@vdm1> vlog -sv adder_tree.v tb_adder_tree.v
Model Technology Report: Intel FPGA Edition vlog 2020.1 Compiler 2020.02 Feb 28 2020
Start time: 09:17:08 on Dec 31, 2025
Vlog reports progress 560 -sv adder_tree.v tb_adder_tree.v
-- Compiling module adder_tree
-- Compiling module tb_adder_tree
#
Top level modules:
tb_adder_tree
#
End time: 09:17:08 on Dec 31, 2025, Elapsed time: 0:00:00
#
Errors: 0, Warnings: 0
VDM@vdm1> work tb_adder_tree
#
End time: 09:17:11 on Dec 31, 2025, Elapsed time: 0:00:31
#
Errors: 0, Warnings: 0
Vdm@vdm1> work tb_adder_tree
#
Start time: 09:17:11 on Dec 31, 2025
Loading vj_ash.rpt
Loading work.tb_adder_tree
#
Loading work.tb_adder_tree
VDM@vdm1> add wave -r *
VDM@vdm1>
VDM@vdm1> run -all
#
TEST 0 PASS : 114 + 178 = 20292
TEST 1 PASS : 16 + 48 = 768
TEST 2 PASS : 181 + 182 = 32942
TEST 3 PASS : 20 + 223 = 4460
TEST 4 PASS : 187 + 235 = 43442
TEST 5 PASS : 65 + 64 = 4160
TEST 6 PASS : 138 + 2 = 424
TEST 7 PASS : 252 + 93 = 23436
TEST 8 PASS : 29 + 156 = 3074
TEST 9 PASS : 22 + 63 = 1386
#
----- SUMMARY -----
#
Total Tests : 10
Tests Passed : 10
Tests Failed : 0
OVERALL STATUS : ALL TESTS PASSED
#
-----
#
-- Runaway: [finish] + tb_adder_tree.v[71]
#
Time: 1110 ns Iterations: 0 Instances: /tb_adder_tree
#
1
#
Break is module tb_adder_tree at tb_adder_tree.v line 71
VDM@vdm1>

```

**Note:**

The codes of this module, along with their respective simulation file, have been included in the GitHub repository: **Xcelerium Internship Repository**