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Verification Plan

AMBA AHB-Lite Protocol

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Introduction to the Device-Under-Test (DUT)

AMBA AHB Lite is an interface between master and slaves. It has write data bus configurations of 64 to 1024 bits in powers of 2. The AHB block diagram is as follows:

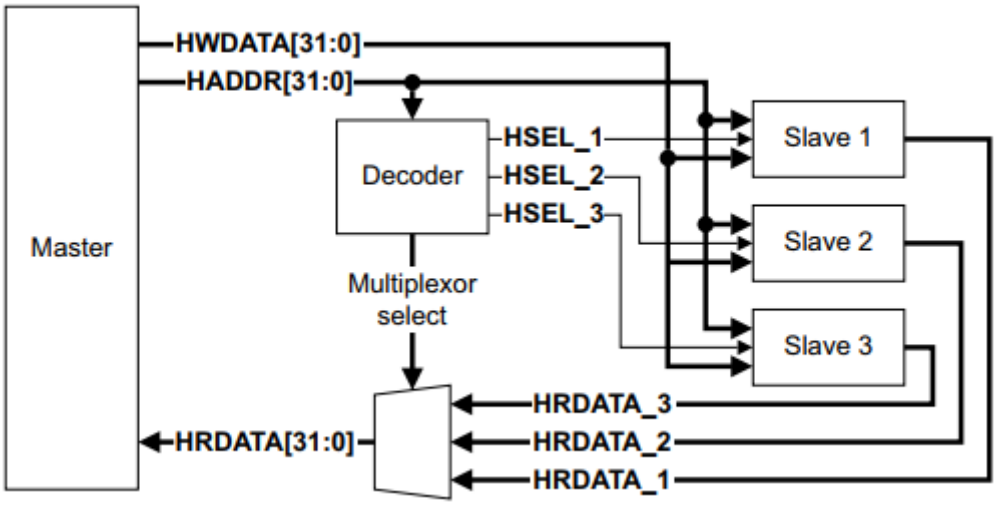

Figure 1: AHB block diagram

In the above figure, one master and three slaves are present. Moreover, decoder selects the slave from the information of the address from Master. Mux gives way back to that particular slave to Master. Master provides address and control information. Slave responds to the transfers initiated by the Master. Every transfer has an address and data cycle each.

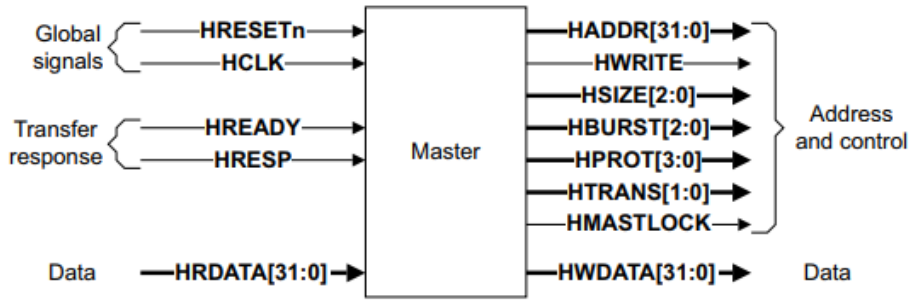

Figure 2: Master Interface

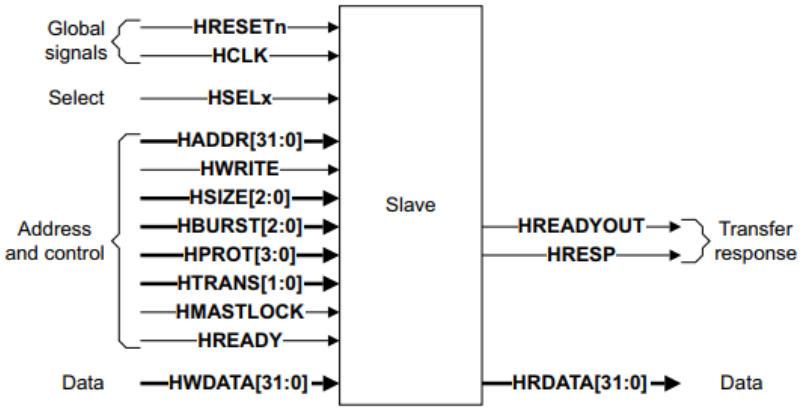

Figure 3: Slave Interface

The main components of the AHB-Lite system are as follows:

1) Master
2) Slave
3) Decoder
4) Multiplexor

An AHB-Lite master provides address and control information to initiate read and write operations. The slave responds to transfers initiated by masters in the system. The slave uses the select signal from the decoder to control when it responds to a bus transfer. The slave signals back to the master i.e., the success, failure, or waiting of the data transfer. This component decodes the address of each transfer and provides a select signal for the slave that is involved in the transfer. It also provides a control signal to the multiplexor. A slave-to-master multiplexor is required to multiplex the read data bus and response signals from the slaves to the master.

AMBA AHB-Lite Protocol:

Working of Protocol:

Global Signals:

Name	Source	Description
HCLK	Clock source	All signal timing diagrams are related to rising edge of HCLK
HRESTn	Reset Controller	The only active low signal here. It provides asynchronous primary reset for all bus elements.

Master Signals:

Name	Destination	Description
HADDR [31:0]	Slave & Decoder	Address bus of 32 bits
HBURST [2:0]	Slave	Indicates the type of burst signal including wrapping and incrementing bursts with number of beats
HSIZE [2:0]	Slave	Indicates the size of transfer from 8 bits to 1024 bits
HTRANS [1:0]	Slave	Indicates the transfer type: IDLE, BUSY, NON-SEQUENTIAL, SEQUENTIAL
HWDATA [31:0]	Slave	Transfers data from Master to Slave
HWRITE	Slave	Indicates transfer direction.

Slave Signals:

Name	Destination	Description
HRDATA [31:0]	Multiplexor	Read data bus to transfer the data from a Slave's location to the Master via multiplexor
HREADYOUT	Multiplexor	Indicates transfer has finished on the bus and is driven LOW to extend the data phase
HRESP	Multiplexor	Provides additional information that the transfer was successful or failed

Decoder Signals:

Name	Destination	Description
HSELx	Slave	Indicates current transfer is for intended for selected slave

Multiplexor Signals:

Name	Destination	Description
HRDATA [31:0]	Master	Read data bus to rout to Master
HREADY	Master and Slave	Indicates completion of previous transfer
HRESP	Master	Transfer response

Working Protocol:

The master starts a transfer by driving the address and control signals. These signals provide information about the address, direction, width of the transfer, and indicate if the transfer forms part of a burst. Transfers can be of different types for instance single, incrementing bursts that do not wrap at address boundaries, wrapping bursts that wrap at particular address boundaries, etc. The write data bus moves data from the master to a slave, and the read data bus moves data from a slave to the master.
Every transfer consists of two phases:

1) Address Phase: one address and control cycle
2) Data Phase: one or more cycles for the data.

A slave cannot request that the address phase is extended and therefore all slaves must be capable of sampling the address during this time. However, a slave can request that the master extends the data phase by using HREADY. This signal when LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to provide or sample data. The slave uses a response signal to indicate the success or failure of a transfer.

Verification Plan

No.	Feature	Test Description	Ref.	Type	Result	Comments
1	Write Transfer from Master to Slave	When **HWRITE** is HIGH then the Master will broadcast the data on the HWDATA [31:0] bus for individual burst types i.e., HBURST [2:0] including incrementing and wrapping types.	3.1	TR		Successful write. **HRESP** should be LOW **HREADY** should be HIGH
2	Read Transfer from Slave to Master	When **HWRITE** is LOW then the slave must generate the data on the HRDATA [31:0] bus for individual burst types i.e., HBURST [2:0] including incrementing and wrapping type.	3.1	TR		Successful read. **HRESP** should be LOW **HREADY** should be HIGH
3	Write-Read Transfer	Write transfer followed by Read transfer at a particular address A.	3.1	TR		**HRESP** is LOW, **HREADY** is HIGH The address location must have the updated value
4	Read-Write Transfer	Read transfer followed by Write transfer at a particular address A.	3.1	TR		**HRESP** is LOW, **HREADY** is HIGH The slave must return the previous Data (A).
5	Continuous writing to the same slave (same address)	When **HWRITE** is HIGH, the Master will broadcast the data packets on the HWDATA [31:0] bus.	3.1	TR		Successful write. **HRESP** should be LOW **HREADY** should be HIGH for the successive data packets
6	Continuous reading from the same slave and same address location	When HWRITE is low, the slave must generate the data packets on the HRDATA [31:0] bus.	3.1	TR		Successful read. **HRESP** should be low and **HREADY** should be high for the successive data packets
7	Random Write transfers	When HWRITE is high, the Master will broadcast the data packets on the HWDATA [31:0] bus.	3.1	TR		Successful write. **HRESP** should be low and **HREADY** should be high for the successive data packets

8	Random Read Transfers	When HWRITE is low, the slave must generate the data packets on the HRDATA [31:0] bus.	3.1	TR		Successful read. **HRESP** should be low and **HREADY** should be high for the successive data packets
9	Global Signal: **HCLK**	A clock signal is generated in the top module	7.1.1	A		All input signals must be sampled at the rising edge of the clock and changes in the output signals must occur after the rising edge.
10	Global Signal: **HRESTn**	Since this is an active LOW signal. When asserted then it must reset all bus elements. Note: Slaves must ensure that **HREADYOUT** is HIGH. **HTRANS** [1:0] must indicate **IDLE**.	7.1.2	TR		All previous binary information in the bust elements will be lost.
11	Master Signal: IDLE HTRANS [1:0] =b00	When **IDLE** transfer is inserted to an address.	3.2	TR		The **HREADY** must be LOW during the **IDLE** transfer. The transfer must be ignored by the slave. Slave must provide a **OKAY** response.
12	Transfer type changed during waited states: Scenario 1	Transfer type changes from **IDLE** to **NONSEQ** during waited states. The HTRANS signal must be kept constant after the transition until **HREADY** is HIGH	3.6.1	A		Successfully transfer type changed. Slave must give **OKAY** response.
13	Transfer type changed during waited states: Scenario 2	Transfer type changes from **BUSY** to **SEQ** during waited states for fixed length bursts. The **HTRANS** signal must be kept constant after the transition until **READY** is HIGH	3.6.1	A		Successfully transfer type changed. Slave must give an **OKAY** response.
14	Transfer type changed during waited states: Scenario 3	Transfer type changes from BUSY to any other type during waited states for undefined length burst. The burst continues if an **SEQ** transfer is performed but terminates if an **IDLE** or **NONSEQ** transfer is performed.	3.6.1	A		Successfully transfer type changed. Slave must give an **OKAY** response.
15	Transfer type changed during waited states: Scenario 4	Any scenario other than scenario 1 2 and 3 for example Transfer type changed from **IDLE** to **SEQ**.	3.6.1	A		Slave will give an **ERROR** response.
16	Slave response: Transfer done	Transfer is completed successfully.	5.1.1	A		Slave must give **HREADY** HIGH **HRESP** OKAY

17	Slave response: Transfer pending	Transfer is pending	5.1.2	A		Slave must give **HREADY** LOW **HRESP** OKAY
18	Slave response: transfer failed	Transfer is not completed successfully	5.1.3	A		**HRESP** must be HIGH. Two cycle response is required for an error condition.
19	HREADYOUT	When HIGH the transfer has finish on bus	2.3	A		When HIGH, the HREADYOUT signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
20	HREADY	When HIGH, the HREADY signal indicates to the master and all slaves, that the previous transfer is complete	2.5 6.1.1	A		If the transfer is extended than the master must hold the valid data until the transfer completes, as indicated by HREADY HIGH