GIK Institute of Engineering Sciences and Technology, Topi
Fall 2021 (FCSE) Final
17th January 2022, 09:00 am – 12:00 pm

| Course Code: CE221	Course Name: Logic Design
Instructor Name : Engr. Ahsan Shah	
Student Name:	Registration No:

- Read each question completely before answering it. There are **2 Sections and 12 pages only.**
- In case of any ambiguity, you may make assumption. But your assumption should not contradict any statement in the question paper.
- Write the answer in the space below each question.
- In **Section 2** attempt any 3 still question no 1 is mandatory.

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Time: 180 minutes.   **Max Marks**: 65 points

# Section 1 (Short Questions) [5 point each]

1. Complete the timing diagram of the circuit shown below:
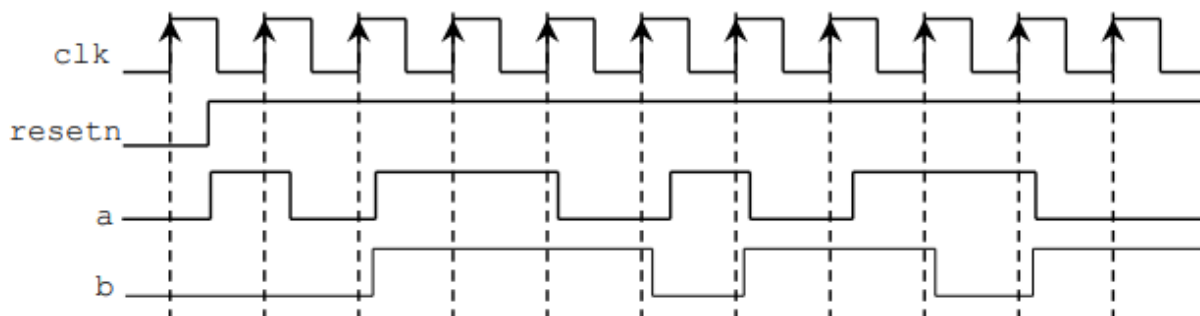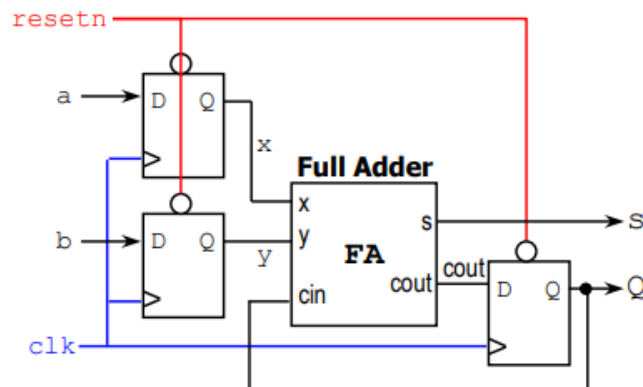
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2. A synchronous sequential circuit based on a shift register is used as a "Majority voter". The value of the input signal w that occurred most of the times in the past three clock pulses is displayed at the output y. The gate denoted by the "M" is a so-called majority gate, its output takes the same value as the majority of its inputs.
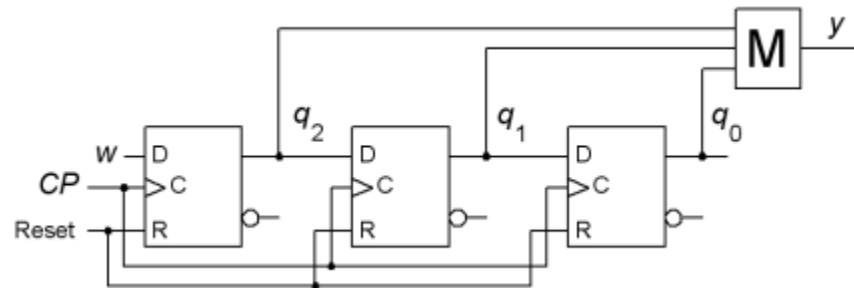
Analyze the shift register and draw state diagram and state table. (Please take the help of the initiated state diagram with eight states shown below, but draw your own figure to answer).
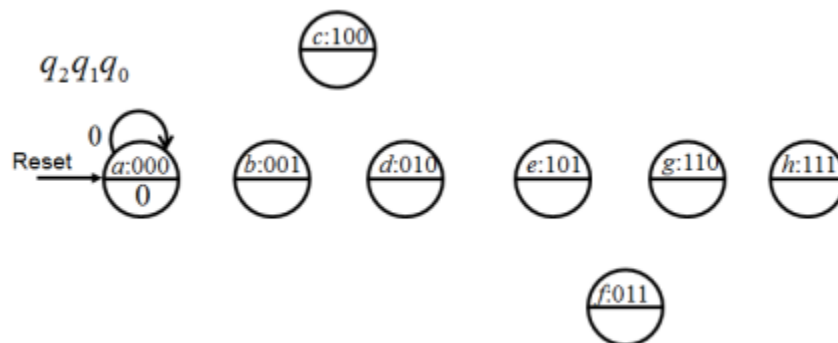
3. A sequential circuit with two D Flip-Flops, having Q_0 and Q_1; two inputs, x and y, is specified by the following next-state and output equations:

$$Q_0(t+1) = \bar{x}\,y + xQ_0$$

$$Q_1(t+1) = \bar{x}\,Q_1 + xQ_0$$

Draw circuit diagram for above given scenario.

4. A decade counter is a binary counter that is designed to count to 1001 (decimal 9). Design a counter that counts up the number of roll overs (9 to 0) in decade counter. Consider synchronous counter and JK flip flop for your design.

5. Given the 4-bit signed number $X = X_3 X_2 X_1 X_0$, write the simplest SOP expression for each of the following:

a) odd (should be 1 when X is odd and 0 otherwise): odd =_____

b) even (1 when X is even and 0 otherwise): even =_____

c) positive (1 when X is positive and 0 otherwise): positive =_____

d) negative (1 when X is negative and 0 otherwise): negative =_____

e) zero (1 when X is zero and 0 otherwise): zero =_____

f) maximum (1 when X has its largest possible value and 0 otherwise): maximum =_____

g) minimum (1 when X has its smallest possible value and 0 otherwise): minimum =_____

6. Determine the outputs functions A and B as sums of min-terms (canonical form) in circuit given below. You may use any process to determine the result, but show your work.
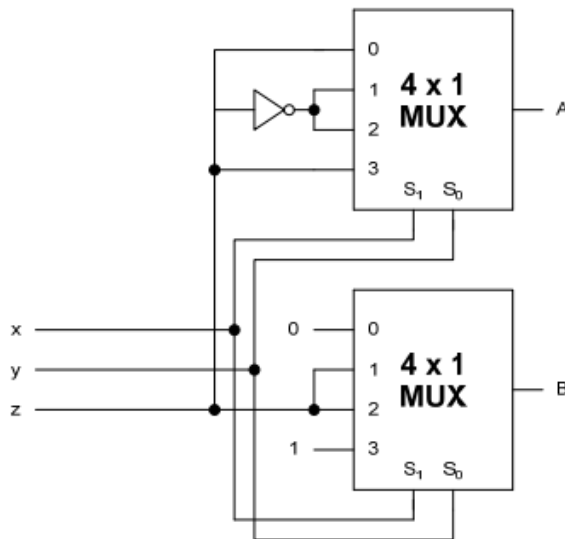
7. If the input to the digital circuit (in the figure) consisting of cascaded 19 XOR gates is X, then output Y is equal to:
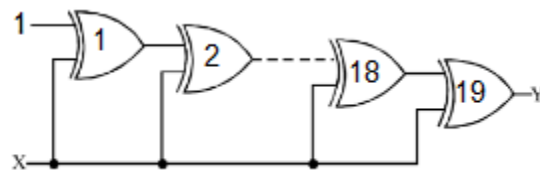
Section 2 (Long Questions) [10 point each]

1. A new Set-Reset-Toggle (SRT) flip-flop has just been announced by flipflops.com, a start-up company that specializes in internet delivery of storage elements to the electronics and computer industries. The device symbol and function table for this flip-flop are shown below:
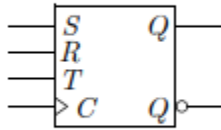
S	R	T	Function
X	X	1	Toggle (i.e., complement stored value)
1	0	0	Set
0	1	0	Reset
0	0	0	Hold
1	1	0	Hold

Derive characteristic equation for this new flip flop?

2. Design a magnitude comparator circuit for 2-bit binary numbers *A=A1A0* and *B=B1B0*. The outputs are F, G, and H, where F is 1 if A>B, G is 1 if A=B, and H is 1 if A. You can use only basic AND, OR and NOT Gates.

3. For function:
$$F(x, y, z) = \overline{x}\,\overline{y}z + \overline{x}yz + \overline{x}y\overline{z} + xy\overline{z} + x\overline{y}z$$

We want to design a circuit to implement function F(x,y,z) using three different methods.

First design is called **design MUX**. Function F(x,y,z) is implemented using Multiplexer. Second design is **design DEC**. F(x,y,z) is designed using Decoder. Then we want to optimize the function F(x, y, z), called **design OPT**, by logic optimization using K-map.

4. A Mealy Machine is an FSM whose output depends on the present state as well as the external input. Consider an external input x that is use to trigger the machine states from one to another. When the value of x is 0, it start counting up one by one (0 to 7). When the value is 1, it counts up two by two. Design a circuit using D flip flops.