BTS 7960

High Current PN Half Bridge NovalithIC™

43 A, 7 mΩ + 9 mΩ

Automotive Power

Infineon technologies

Never stop thinking.

High Current PN Half Bridge
NovalithIC™

BTS 7960B

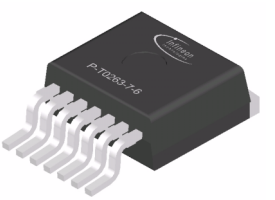
BTS 7960P

Product Summary

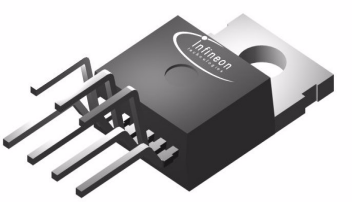
The **BTS 7960** is a fully integrated high current half bridge for motor drive applications. It is part of the **NovalithIC™** family containing one p-channel highside MOSFET and one n-channel lowside MOSFET with an integrated driver IC in one package. Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, overvoltage, undervoltage, overcurrent and short circuit.

The **BTS 7960** provides a cost optimized solution for protected high current PWM motor drives with very low board space consumption.

BTS 7960B
P-TO-263-7



BTS 7960P
P-TO-220-7



Basic Features

- Path resistance of typ. 16 mΩ @ 25 °C
- Low quiescent current of typ. 7 µA @ 25 °C
- PWM capability of up to 25 kHz combined with active freewheeling
- Switched mode current limitation for reduced power dissipation in overcurrent
- Current limitation level of 43 A typ.
- Status flag diagnosis with current sense capability
- Overtemperature shut down with latch behaviour
- Overvoltage lock out
- Undervoltage shut down
- Driver circuit with logic level inputs
- Adjustable slew rates for optimized EMI

Type	Ordering Code	Package
BTS 7960B	Q67060-S6160	P-TO-263-7
BTS 7960P	on request	P-TO-220-7

1 Overview

The **BTS 7960** is part of the **NovalithIC**™ family containing three separate chips in one package: One p-channel highside MOSFET and one n-channel lowside MOSFET together with a driver IC, forming a fully integrated high current half-bridge. All three chips are mounted on one common leadframe, using the chip on chip and chip by chip technology. The power switches utilize vertical MOS technologies to ensure optimum on state resistance. Due to the p-channel highside switch the need for a charge pump is eliminated thus minimizing EMI. Interfacing to a microcontroller is made easy by the integrated driver IC which features logic level inputs, diagnosis with current sense, slew rate adjustment, dead time generation and protection against overtemperature, overvoltage, undervoltage, overcurrent and short circuit. The BTS 7960 can be combined with other BTS 7960 to form H-bridge and 3-phase drive configurations.

1.1 Block Diagram

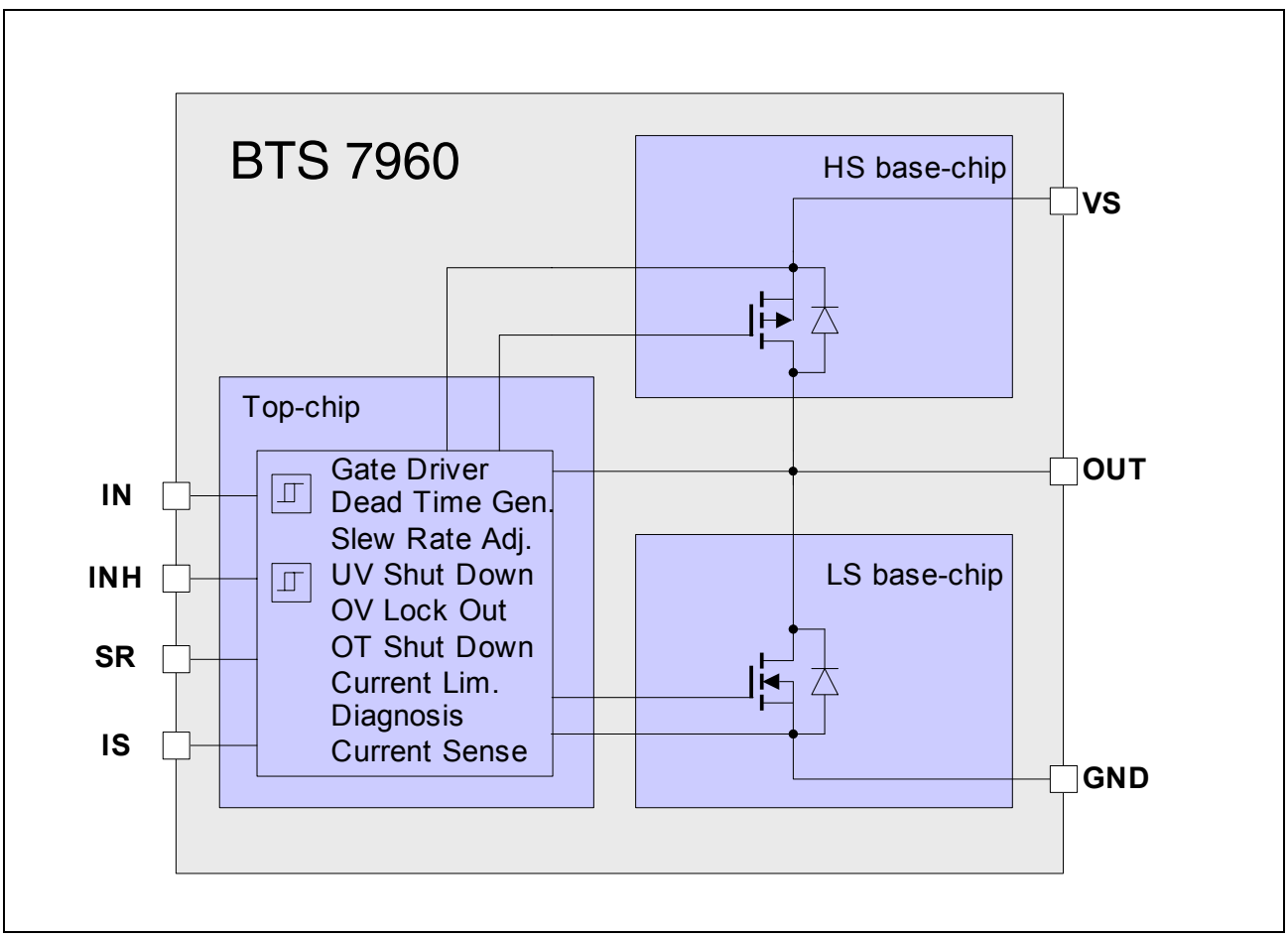


Figure 1 Block Diagram

1.2 Terms

Following figure shows the terms used in this data sheet.

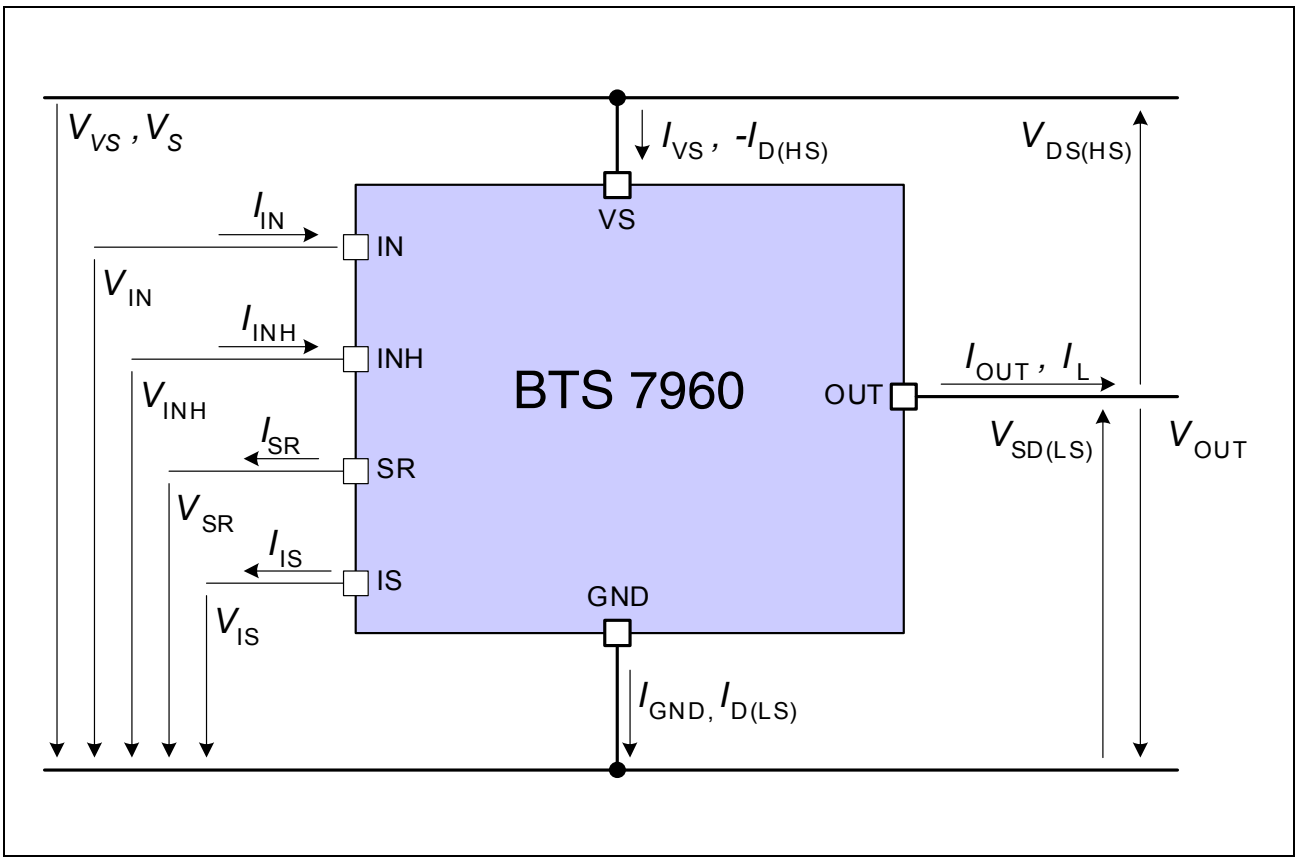


Figure 2 Terms

2 Pin Configuration

2.1 Pin Assignment

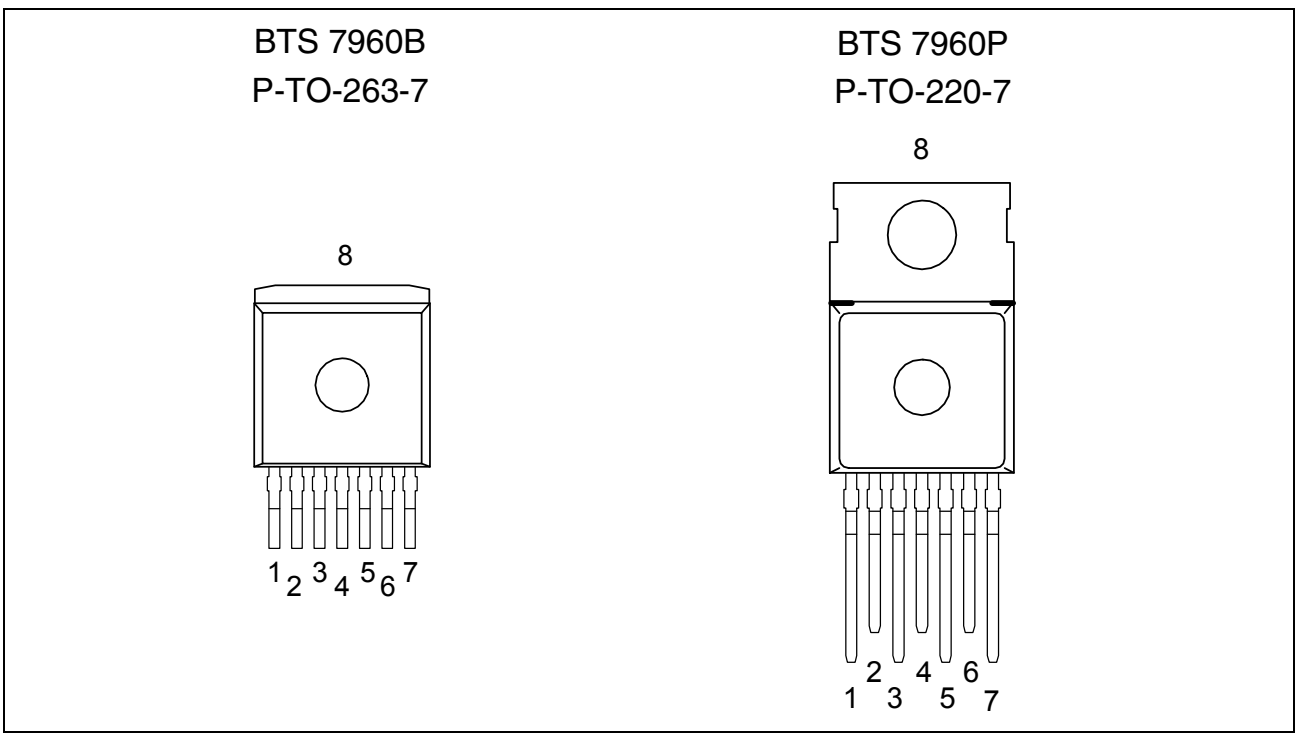


Figure 3 Pin Assignment BTS 7960B and BTS 7960P (top view)

2.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1	**GND**	**-**	**Ground**
2	IN	I	Input Defines whether high- or lowside switch is activated
3	INH	I	Inhibit When set to low device goes in sleep mode
4,8	**OUT**	**O**	**Power output of the bridge**
5	SR	I	Slew Rate The slew rate of the power switches can be adjusted by connecting a resistor between SR and GND
6	IS	O	Current Sense and Diagnosis
7	**VS**	**-**	**Supply**

Bold type: pin needs power wiring

3 Maximum Ratings

-40 °C < T_j < 150 °C (unless otherwise specified)

Pos	Parameter	Symbol	Limits		Unit	Test Condition
			min	max		
Electrical Maximum Ratings						
3.0.1	Supply voltage	V_{VS}	-0.3	45	V	
3.0.2	Logic Input Voltage	V_{IN} V_{INH}	-0.3	5.3	V	
3.0.3	HS/LS continuous drain current	$I_{D(HS)}$ $I_{D(LS)}$	-40	40[1)]	A	T_C < 85°C switch active
3.0.4	HS pulsed drain current	$I_{D(HS)}$	-60	60[1)]	A	T_C < 85°C t_{pulse} = 10ms
3.0.5	LS pulsed drain current	$I_{D(LS)}$	-60	60[1)]	A	
3.0.6	Voltage at SR pin	V_{SR}	-0.3	1.0	V	
3.0.7	Voltage between VS and IS pin	V_{VS} -V_{IS}	-0.3	45	V	
3.0.8	Voltage at IS pin	V_{IS}	-20	45	V	
Thermal Maximum Ratings						
3.0.9	Junction temperature	T_j	-40	150	°C	
3.0.10	Storage temperature	T_{stg}	-55	150	°C	
ESD Susceptibility						
3.0.11	ESD susceptibility HBM IN, INH, SR, IS OUT, GND, VS	V_{ESD}	 -2 -6	 2 6	kV	according to EIA/ JESD 22-A 114B

1) Maximum reachable current may be smaller depending on current limitation level

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the device. Exposure to maximum rating conditions for extended periods of time may affect device reliability

4 Block Description and Characteristics

4.1 Supply Characteristics

– 40 °C < T_j < 150 °C, 8 V < V_S < 18 V, I_L = 0A (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
General							
4.1.1	Operating Voltage	V_S	5.5	–	27.5	V	
4.1.2	Supply Current	$I_{VS(on)}$	–	2	3	mA	V_{INH} = 5 V V_{IN} = 0 V or 5 V R_{SR}=0 Ω DC-mode normal operation (no fault condition)
4.1.3	Quiescent Current	$I_{VS(off)}$	–	7	15	µA	V_{INH} = 0 V V_{IN} = 0 V or 5 V T_j <85 °C
			–	–	65	µA	V_{INH} = 0 V V_{IN} = 0 V or 5 V

4.2 Power Stages

The power stages of the BTS 7960 consist of a p-channel vertical DMOS transistor for the high side switch and a n-channel vertical DMOS transistor for the low side switch. All protection and diagnostic functions are located in a separate top chip. Both switches can be operated up to 25 kHz, allowing active freewheeling and thus minimizing power dissipation in the forward operation of the integrated diodes.

The on state resistance R_{ON} is dependent on the supply voltage V_S as well as on the junction temperature T_j . The typical on state resistance characteristics are shown in **Figure 4**.

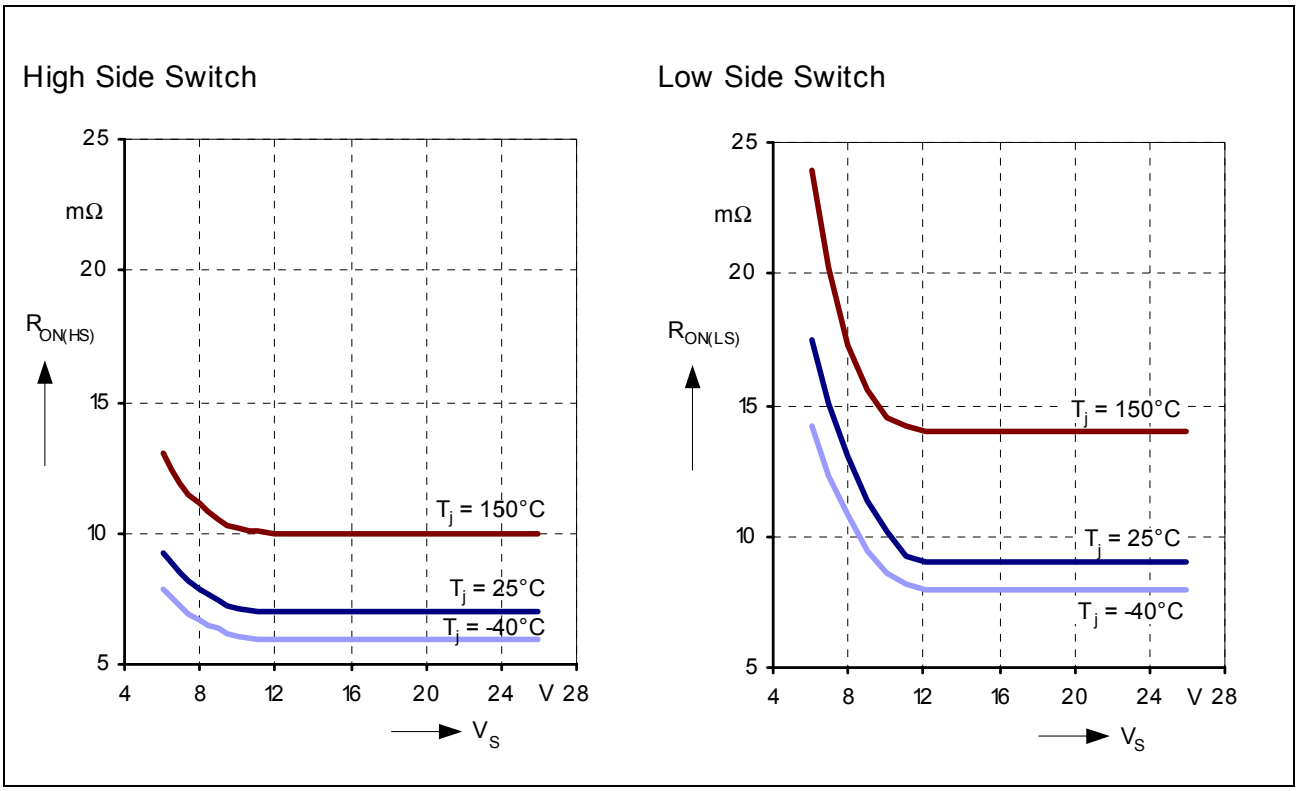


Figure 4 Typical On State Resistance vs. Supply Voltage

4.2.1 Power Stages - Static Characteristics

– 40 °C < T_j < 150 °C, 8 V < V_S < 18 V (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
High Side Switch - Static Characteristics							
4.2.1	On state high side resistance	$R_{ON(HS)}$				mΩ	I_{OUT} = 9 A V_S= 13.5 V
			–	7	9		T_j = 25 °C
			–	10	12.5		T_j = 150 °C
4.2.2	Leakage current high side	$I_{L(LKHS)}$	–	–	1	µA	V_{INH} = 0 V V_{OUT} = 0 V T_j < 85 °C
			–	–	50	µA	V_{INH} = 0 V V_{OUT} = 0 V T_j = 150 °C
4.2.3	Reverse diode forward-voltage high side [1]	$V_{DS(HS)}$				V	I_{OUT} = -9 A
			–	0.9	1.5		T_j = -40 °C
			–	0.8	1.1		T_j = 25 °C
			–	0.6	0.8		T_j = 150 °C
Low Side Switch - Static Characteristics							
4.2.4	On state low side resistance	$R_{ON(LS)}$				mΩ	I_{OUT} = -9 A V_S= 13.5V
			–	9	12		T_j = 25 °C
			–	14	18		T_j = 150 °C
4.2.5	Leakage current low side	$I_{L(LKLS)}$	–	–	1	µA	V_{INH} = 0 V V_{OUT} = V_S T_j < 85 °C
			–	–	15	µA	V_{INH} = 0 V V_{OUT} = V_S T_j = 150 °C
4.2.6	Reverse diode forward-voltage low side [1]	$V_{SD(LS)}$				V	I_{OUT} = 9 A
			–	0.9	1.5		T_j = -40 °C
			–	0.8	1.1		T_j = 25 °C
			–	0.6	0.8		T_j = 150 °C

[1] Due to active freewheeling, diode is conducting only for a few µs, depending on R_{SR}

4.2.2 Switching Times

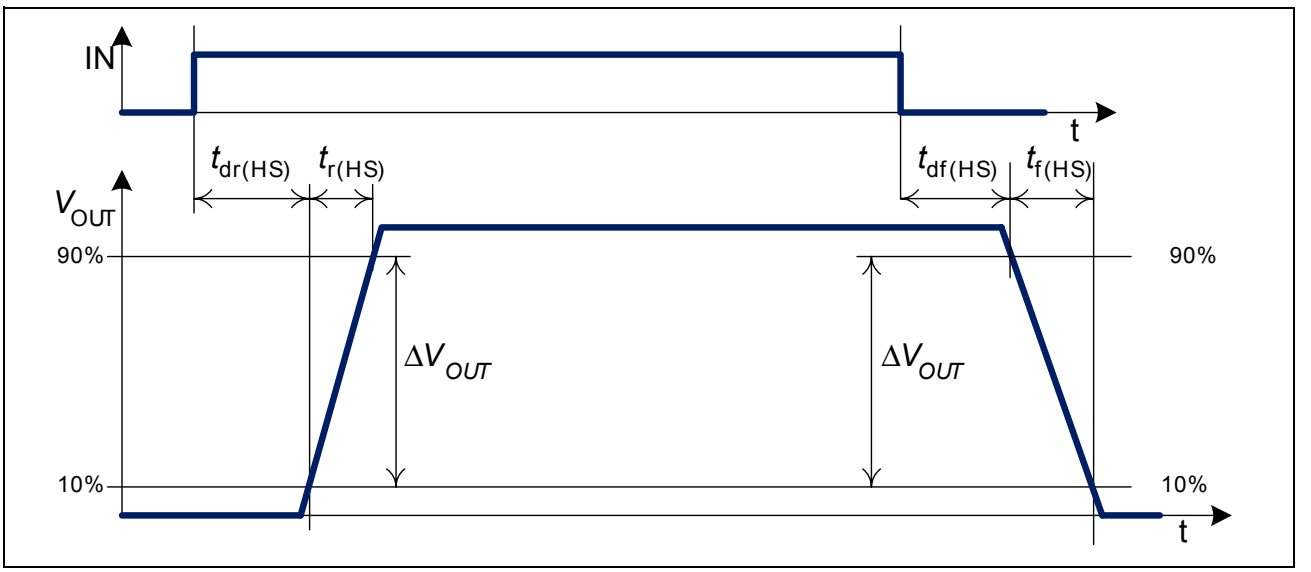


Figure 5 Definition of switching times high side (R_{load} to GND)

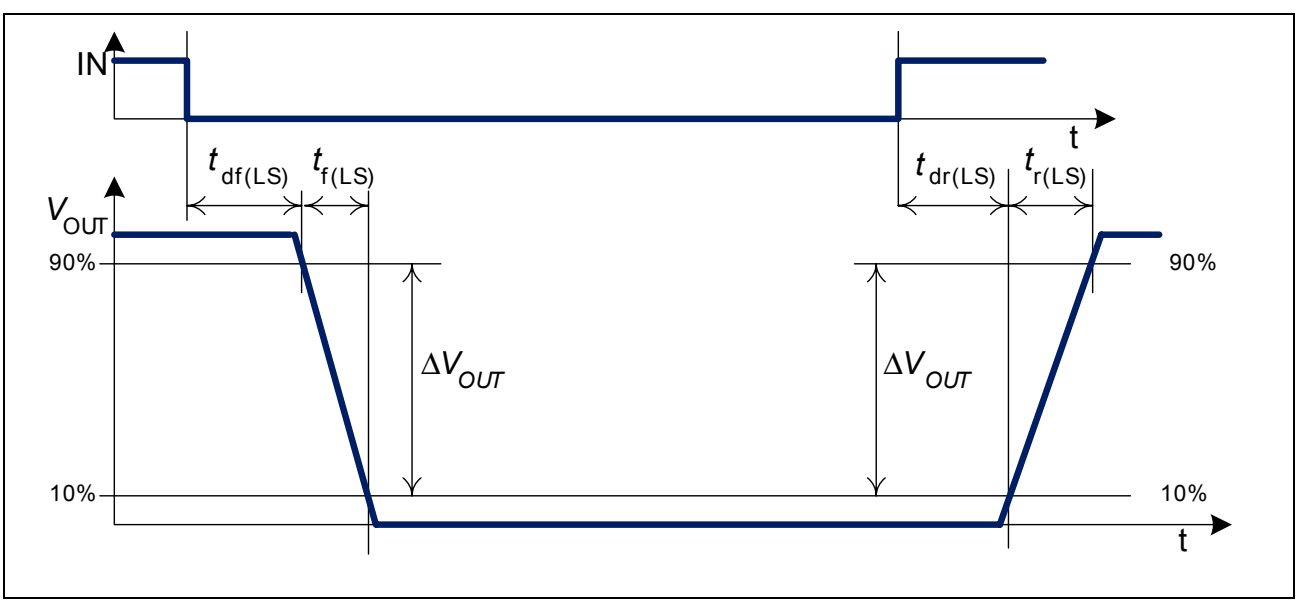


Figure 6 Definition of switching times low side (R_{load} to VS)

Due to the timing differences for the rising and the falling edge there will be a slight difference between the length of the input pulse and the length of the output pulse. It can be calculated using the following formulas:

- $\Delta t_{HS} = (t_{dr(HS)} + 0.5\ t_{r(HS)}) - (t_{df(HS)} + 0.5\ t_{f(HS)})$
- $\Delta t_{LS} = (t_{df(LS)} + 0.5\ t_{f(LS)}) - (t_{dr(LS)} + 0.5\ t_{r(LS)})$.

4.2.3 Power Stages - Dynamic Characteristics

-40 °C < T_j < 150 °C, V_S = 13.5 V, R_{load} = 2Ω (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
HIgh Side Switch Dynamic Characteristics							
4.2.7	Rise-time of HS	$t_{r(HS)}$	0.5 – 2.8	1 2 7	1.5 – 11	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.8	Slew rate HS on	$\Delta V_{OUT}/t_{r(HS)}$	– – –	11 6 1.6	– – –	V/µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.9	Switch on delay time HS	$t_{dr(HS)}$	1.7 – 5.6	3.1 4.4 14	4.5 – 22.4	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.10	Fall-time of HS	$t_{f(HS)}$	0.5 – 2.8	1 2 7	1.5 – 11	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.11	Slew rate HS off	$-\Delta V_{OUT}/t_{f(HS)}$	– – –	11 6 1.6	– – –	V/µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.12	Switch off delay time HS	$t_{df(HS)}$	1.2 – 4	2.4 3.4 10	3.6 – 16	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ

-40 °C < T_j < 150 °C, V_S = 13.5 V, R_{load} = 2Ω (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Low Side Switch Dynamic Characteristics							
4.2.13	Rise-time of LS	$t_{r(LS)}$	0.5 – 2.8	1 2 7	1.5 – 11	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.14	Slew rate LS switch off	$\Delta V_{OUT}/t_{r(LS)}$	– – –	11 6 1.6	– – –	V/µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.15	Switch off delay time LS	$t_{dr(LS)}$	0.7 – 2.8	1.3 2.2 7	1.9 – 11.2	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.16	Fall-time of LS	$t_{f(LS)}$	0.5 – 2.8	1 2 7	1.5 – 11	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.17	Slew rate LS switch on	$-\Delta V_{OUT}/t_{f(LS)}$	– – –	11 6 1.6	– – –	V/µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ
4.2.18	Switch on delay time LS	$t_{df(LS)}$	2.2 – 6.4	4 5.6 16	5.8 – 25.4	µs	R_{SR} = 0 Ω R_{SR} = 5.1 kΩ R_{SR} = 51 kΩ

4.3 Protection Functions

The device provides integrated protection functions. These are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not to be used for continuous or repetitive operation, with the exception of the current limitation (**Chapter 4.3.4**). In a fault condition the BTS 7960 will apply the highest slew rate possible independent of the connected slew rate resistor. Overvoltage, overtemperature and overcurrent are indicated by a fault current $I_{IS(LIM)}$ at the IS pin as described in the paragraph **“Status Flag Diagnosis With Current Sense Capability” on Page 17** and **Figure 10**.

In the following the protection functions are listed in order of their priority. Overvoltage lock out overrides all other error modes.

4.3.1 Overvoltage Lock Out

To assure a high immunity against overvoltages (e.g. load dump conditions) the device shuts the lowside MOSFET off and turns the highside MOSFET on, if the supply voltage is exceeding the over voltage protection level $V_{OV(OFF)}$. The IC operates in normal mode again with a hysteresis $V_{OV(HY)}$ if the supply voltage decreases below the switch-on voltage $V_{OV(ON)}$. In H-bridge configuration, this behavior of the BTS 7960 will lead to freewheeling in highside during over voltage.

4.3.2 Undervoltage Shut Down

To avoid uncontrolled motion of the driven motor at low voltages the device shuts off (output is tri-state), if the supply voltage drops below the switch-off voltage $V_{UV(OFF)}$. The IC becomes active again with a hysteresis $V_{UV(HY)}$ if the supply voltage rises above the switch-on voltage $V_{UV(ON)}$.

4.3.3 Overtemperature Protection

The BTS 7960 is protected against overtemperature by an integrated temperature sensor. Overtemperature leads to a shut down of both output stages. This state is latched until the device is reset by a low signal with a minimum length of t_{reset} at the INH pin, provided that its temperature has decreased at least the thermal hysteresis ΔT in the meantime.

Repetitive use of the overtemperature protection might reduce lifetime.

4.3.4 Current Limitation

The current in the bridge is measured in both switches. As soon as the current in forward direction in one switch (high side or low side) is reaching the limit I_{CLx}, this switch is deactivated and the other switch is activated for t_{CLS} . During that time all changes at the

IN pin are ignored. However, the INH pin can still be used to switch both MOSFETs off. After t_{CLS} the switches return to their initial setting. The error signal at the IS pin is reset after 2 * t_{CLS}. Unintentional triggering of the current limitation by short current spikes (e.g. inflicted by EMI coming from the motor) is suppressed by internal filter circuitry. Due to thresholds and reaction delay times of the filter circuitry the effective current limitation level I_{CLx} depends on the slew rate of the load current dI/dt as shown in **Figure 8**

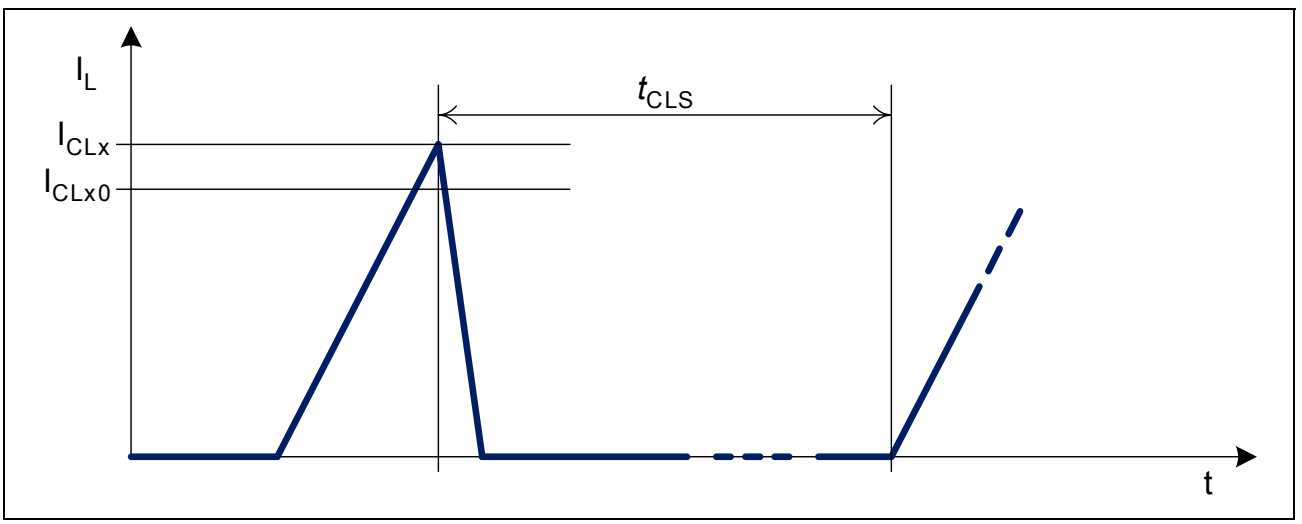


Figure 7 Timing Diagram Current Limitation

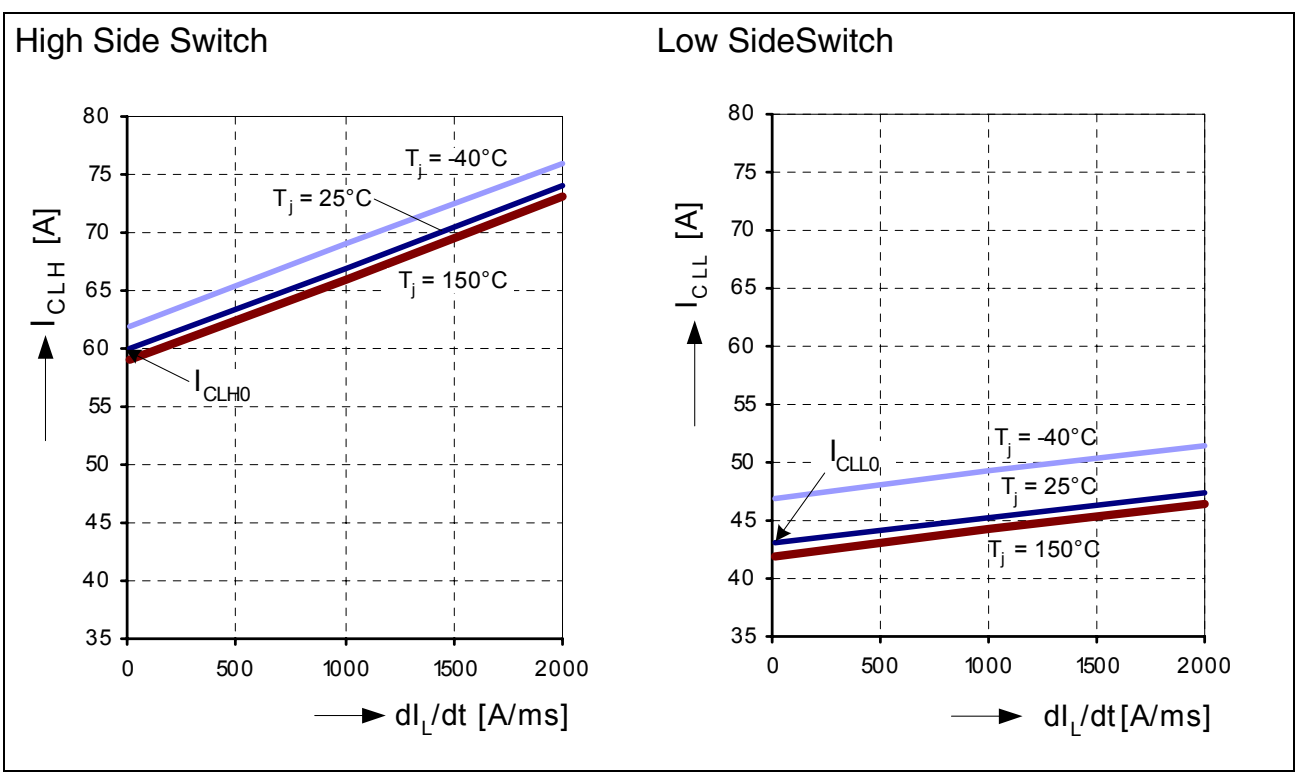


Figure 8 Current Limitation Level vs. Current Slew Rate dI/dt

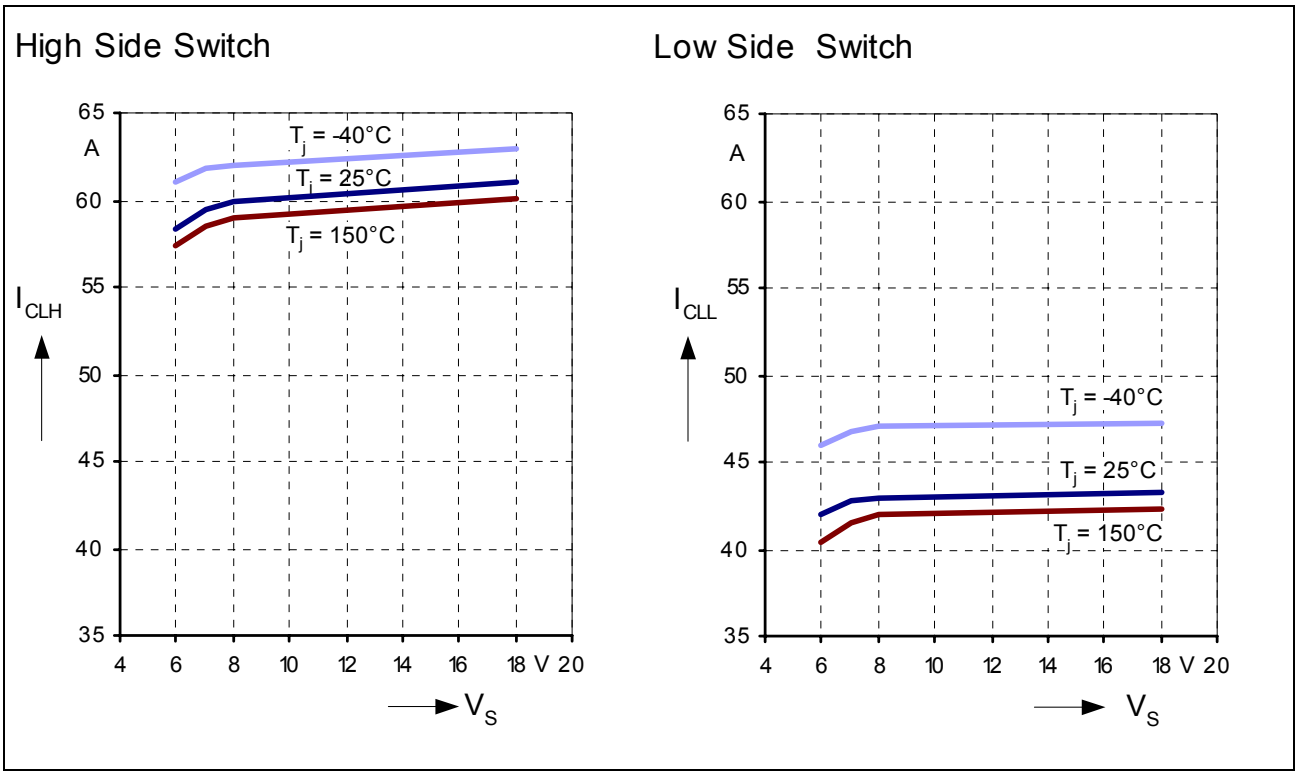


Figure 9 Typical Current Limitation Detection Levels vs. Supply Voltage

In combination with a typical inductive load, such as a motor, this results in a switched mode current limitation. That way of limiting the current has the advantage that the power dissipation in the BTS 7960 is much smaller than by driving the MOSFETs in linear mode. Therefore it is possible to use the current limitation for a short time without exceeding the maximum allowed junction temperature (e.g. for limiting the inrush current during motor start up). However, the regular use of the current limitation is allowed as long as the specified maximum junction temperature is not exceeded. Exceeding this temperature can reduce the lifetime of the device.

4.3.5 Short Circuit Protection

The device is short circuit protected against

- output short circuit to ground
- output short circuit to supply voltage
- short circuit of load

The short circuit protection is realized by the previously described current limitation in combination with the over-temperature shut down of the device

4.3.6 Electrical Characteristics - Protection Functions

– 40 °C < T_j < 150 °C; 8 V < V_S < 18 V (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Under Voltage Shut Down							
4.3.1	Switch-ON voltage	$V_{UV(ON)}$	–	–	5.5	V	V_S increasing
4.3.2	Switch-OFF voltage	$V_{UV(OFF)}$	4.0	–	5.4	V	V_S decreasing
4.3.3	ON/OFF hysteresis	$V_{UV(HY)}$	–	0.2	–	V	–
Over Voltage Lock Out							
4.3.4	Switch-ON voltage	$V_{OV(ON)}$	27.5	–	–	V	V_S decreasing
4.3.5	Switch-OFF voltage	$V_{OV(OFF)}$	27.6	–	30	V	V_S increasing
4.3.6	ON/OFF hysteresis	$V_{OV(HY)}$	–	0.2	–	V	–
Current Limitation							
4.3.7	Current limitation detection level high side	I_{CLH0}	47 44 43	62 60 59	84 80 79	A	V_S=13.5 V T_j = -40 °C T_j = 25 °C T_j = 150 °C
4.3.8	Current limitation detection level low side	I_{CLL0}	36 34 33	47 43 42	64 61 61	A	V_S=13.5V T_j = -40 °C T_j = 25 °C T_j = 150 °C
Current Limitation Timing							
4.3.9	Shut off time for HS and LS	t_{CLS}	70	115	210	µs	V_S=13.5V
Thermal Shut Down							
4.3.10	Thermal shut down junction temperature	T_{jSD}	152	175	200	°C	–
4.3.11	Thermal switch on junction temperature	T_{jSO}	150	–	190	°C	–
4.3.12	Thermal hysteresis	ΔT	–	7	–	K	–
4.3.13	Reset pulse at INH pin (INH low)	t_{reset}	3	–	–	µs	–

4.4 Control and Diagnostics

4.4.1 Input Circuit

The control inputs IN and INH consist of TTL/CMOS compatible schmitt triggers with hysteresis which control the integrated gate drivers for the MOSFETs. Setting the INH pin to high enables the device. In this condition one of the two power switches is switched on depending on the status of the IN pin. To deactivate both switches, the INH pin has to be set to low. No external driver is needed. The BTS 7960 can be interfaced directly to a microcontroller.

4.4.2 Dead Time Generation

In bridge applications it has to be assured that the highside and lowside MOSFET are not conducting at the same time, connecting directly the battery voltage to GND. This is assured by a circuit in the driver IC, generating a so called dead time between switching off one MOSFET and switching on the other. The dead time generated in the driver IC is automatically adjusted to the selected slew rate.

4.4.3 Adjustable Slew Rate

In order to optimize electromagnetic emission, the switching speed of the MOSFETs is adjustable by an external resistor. The slew rate pin SR allows the user to optimize the balance between emission and power dissipation within his own application by connecting an external resistor R_{SR} to GND.

4.4.4 Status Flag Diagnosis With Current Sense Capability

The status pin IS is used as a combined current sense and error flag output. In normal operation (current sense mode), a current source is connected to the status pin, which delivers a current proportional to the forward load current flowing through the active high side switch. If the high side switch is inactive or the current is flowing in the reverse direction no current will be driven except for a marginal leakage current $I_{IS(LK)}$. The external resistor R_{IS} determines the voltage per output current. E.g. with the nominal value of 8500 for the current sense ratio $k_{ILIS} = I_L / I_{IS}$, a resistor value of R_{IS} = 1kΩ leads to V_{IS} = (I_L / 8.5 A)V. In case of a fault condition the status output is connected to a current source which is independent of the load current and provides $I_{IS(lim)}$. The maximum voltage at the IS pin is determined by the choice of the external resistor and the supply voltage. In case of current limitation the $I_{IS(lim)}$ is activated for 2 * t_{CLS}.

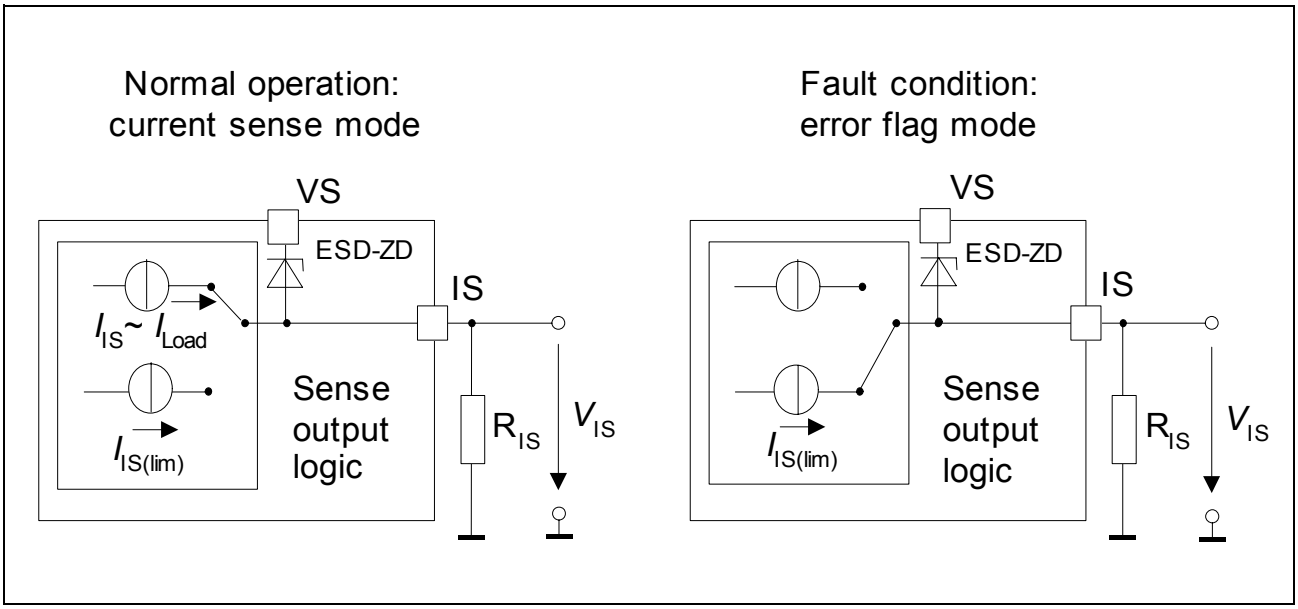


Figure 10 Sense current and fault current

4.4.5 Truth Table

Device State	Inputs		Outputs			Mode
	INH	IN	HSS	LSS	IS	
Normal operation	0	X	OFF	OFF	0	Stand-by mode
	1	0	OFF	ON	0	LSS active
	1	1	ON	OFF	CS	HSS active
Over-voltage (OV)	X	X	ON	OFF	1	Shut-down of LSS, HSS activated, error detected
Under-voltage (UV)	X	X	OFF	OFF	0	UV lockout
Overtemperature or short circuit of HSS or LSS	0	X	OFF	OFF	0	Stand-by mode, reset of latch
	1	X	OFF	OFF	1	Shut-down with latch, error detected
Current limitation mode	1	1	OFF	ON	1	Switched mode, error detected
	1	0	ON	OFF	1	Switched mode, error detected

Inputs:	Switches	Status Flag IS:
0 = Logic LOW	OFF = switched off	CS = Current sense mode
1 = Logic HIGH	ON = switched on	1 = Logic HIGH (error)
X = 0 or 1		

4.4.6 Electrical Characteristics - Control and Diagnostics

– 40 °C < T_j < 150 °C, 8 V < V_S < 18 V (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Control Inputs (IN and INH)							
4.4.1	High level voltage INH, IN	$V_{INH(H)}$ $V_{IN(H)}$	– 	1.75 1.6	2.15 2	V	–
4.4.2	Low level voltage INH, IN	$V_{INH(L)}$ $V_{IN(L)}$	1.1	1.4	–	V	–
4.4.3	Input voltage hysteresis	V_{INHHY} V_{INHY}	– –	350 200	– –	mV	–
4.4.4	Input current	$I_{INH(H)}$ $I_{IN(H)}$	–	30	150	µA	V_{IN} = V_{INH}= 5.3 V
4.4.5	Input current	$I_{INH(L)}$ $I_{IN(L)}$	–	25	125	µA	V_{IN} = V_{INH}=0.4 V
Current Sense							
4.4.6	Current sense ratio in static on-condition k_{ILIS} = I_L / I_{IS}	k_{ILIS}	 6 5 3	 8.5 8.5 8.5	 11 12 14	10^3	R_{IS} = 1 kΩ I_L = 30 A I_L = 15 A I_L = 5 A
4.4.7	Maximum analog sense current, sense current in fault condition	$I_{IS(lim)}$	4	4.5	7	mA	V_S = 13.5 V R_{IS} = 1kΩ
4.4.8	Isense leakage current	I_{ISL}	–	–	1	µA	V_{IN}= 0 V or V_{INH}= 0 V
4.4.9	Isense leakage current, active high side switch	I_{ISH}	–	1	200	µA	V_{IN} = V_{INH}= 5 V I_L= 0 A

5 Thermal Characteristics

Pos	Parameter	Symbol	Limits		Unit	Test Condition
			min	max		
5.0.1	Thermal Resistance Junction-Case, Low Side Switch $R_{thjc(LS)} = \Delta T_{j(LS)} / P_{v(LS)}$	$R_{thjc(LS)}$	–	1.8	K/W	
5.0.2	Thermal Resistance Junction-Case, High Side Switch $R_{thjc(HS)} = \Delta T_{j(HS)} / P_{v(HS)}$	$R_{thjc(HS)}$	–	0.9	K/W	
5.0.3	Thermal Resistance Junction-Case, both Switches $R_{thjc} = \max[\Delta T_{j(HS)}, \Delta T_{j(LS)}] / (P_{v(HS)} + P_{v(LS)})$	R_{thjc}	–	1.0	K/W	
5.0.4	Thermal Resistance Junction-Ambient	R_{thja}	–	35	K/W	6cm^2 cooling area

6 Application

6.1 Application Example

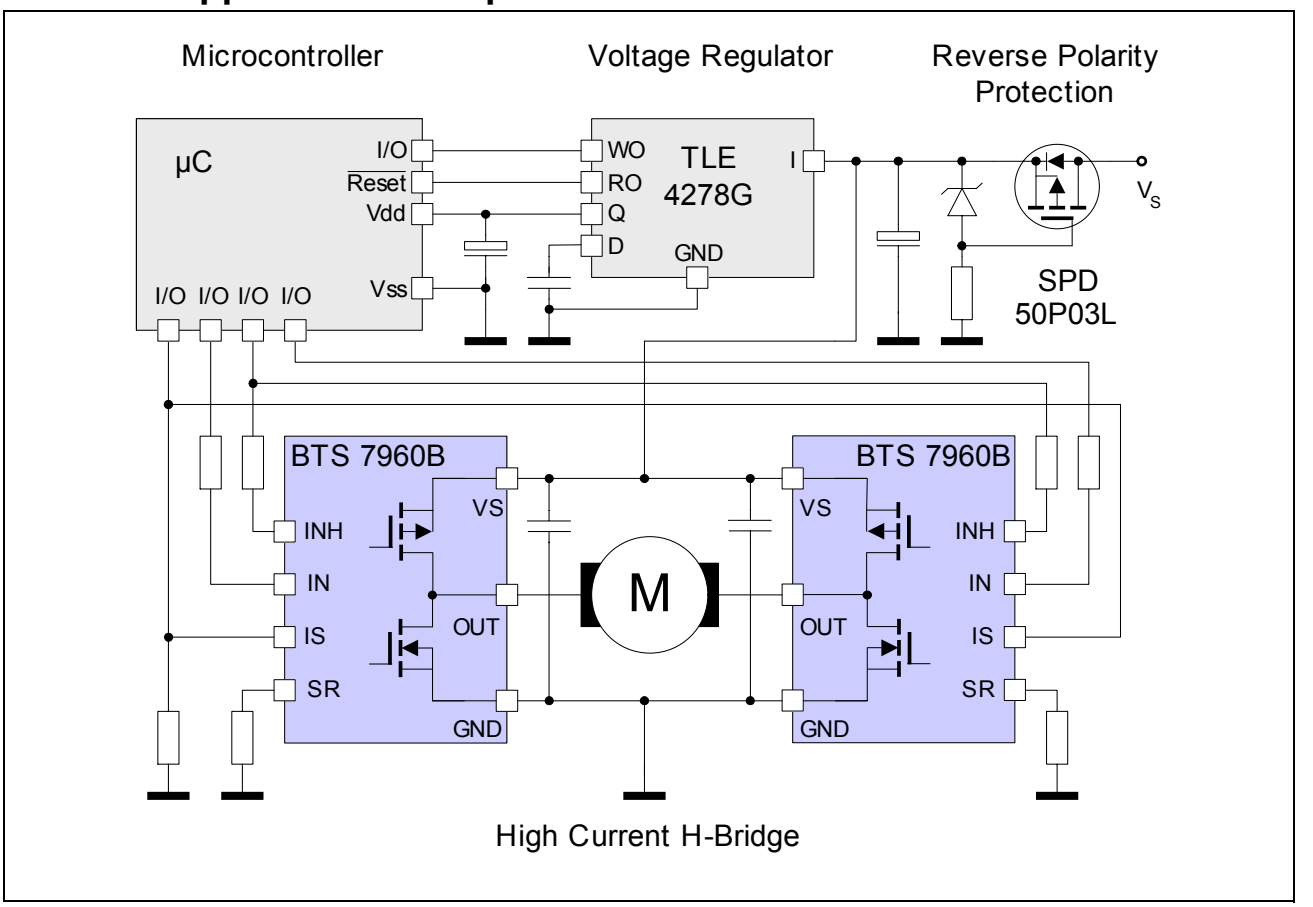


Figure 11 Application Example: H-Bridge with two BTS 7960B

6.2 Layout Considerations

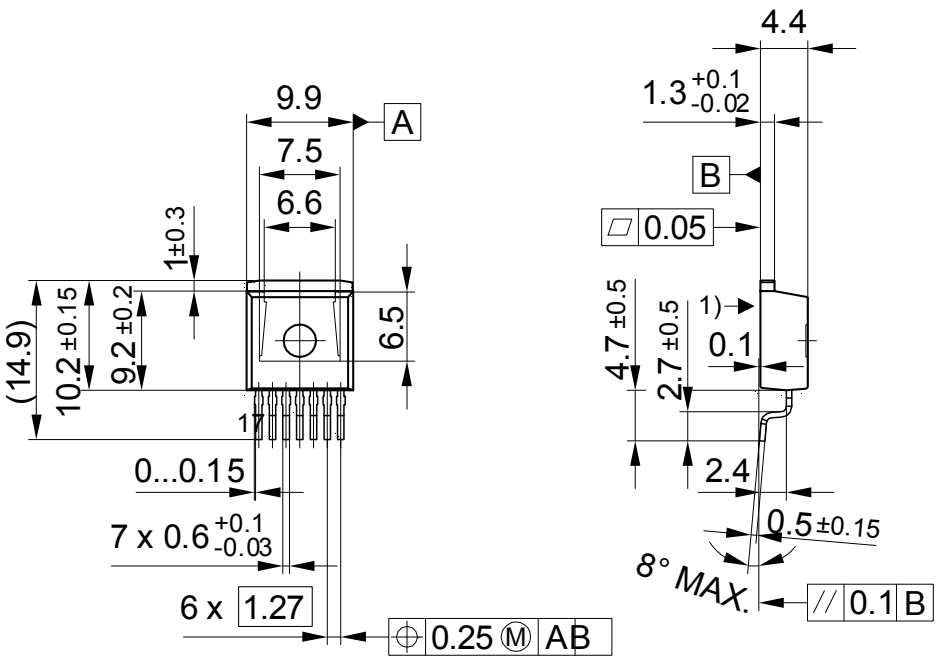
Due to the fast switching times for high currents, special care has to be taken to the PCB layout. Stray inductances have to be minimized in the power bridge design as it is necessary in all switched high power bridges. The BTS 7960 has no separate pin for power ground and logic ground. Therefore it is recommended to assure that the offset between the ground connection of the slew rate resistor, the current sense resistor and ground pin of the device (GND / pin 1) is minimized. If the BTS 7960 is used in a H-bridge or B6 bridge design, the voltage offset between the GND pins of the different devices should be small as well.

A ceramic capacitor from VS to GND close to each device is recommended to provide current for the switching phase via a low inductance path and therefore reducing noise and ground bounce. A reasonable value for this capacitor would be about 470 nF.

The digital inputs need to be protected from excess currents (e.g. caused by induced voltage spikes) by series resistors in the range of 10 kΩ.

7 Package Outlines P-TO-263-7

P-TO-263-7 (Plastic Transistor Single Outline Package)

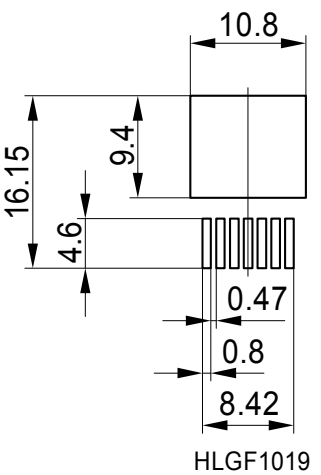


1) Shear and punch direction no burrs this surface

— Back side, heatsink contour

All metal sufaces tin plated, except area of cut .

Footprint



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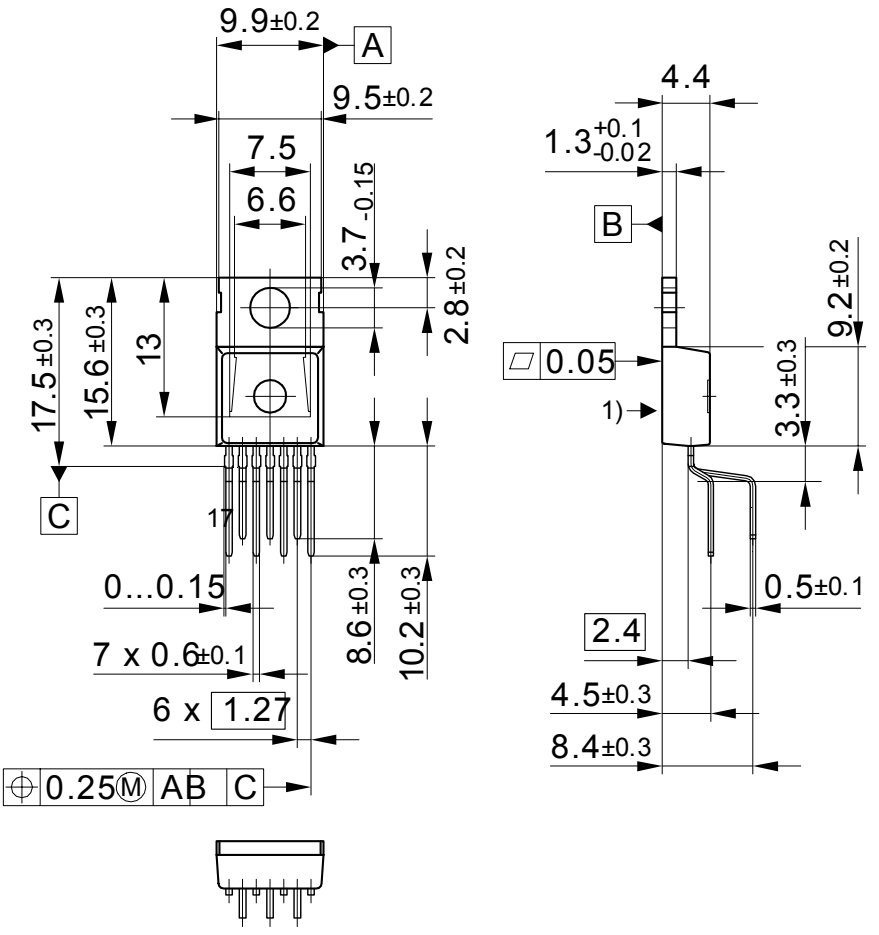
SMD = Surface Mounted Device

Dimensions in mm

8 Package Outlines P-TO-220-7

P-TO-220-7 (Plastic Transistor Single Outline Package)



1) Shear and punch direction no burrs this surface
Back side, heatsink contour
All metal surfaces tin plated, except area of cut.

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Dimensions in mm

9 Revision History

Revision	Date	Changes / Comments
n.a.	2004-03-18	Target Data Sheet
0.9	2004-10-10	Target Data Sheet converted to new layout
1.0	2004-11-30	Preliminary Data Sheet
1.1	2004-12-07	“Preliminary” removed; No other changes

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