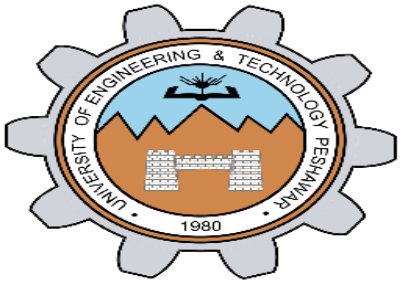
LAB REPORT NO 7



CSE-202L Digital logic design lab

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Class Section: A

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

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LAB 7

MULTIPLEXER AND DEMULTIPLEXER

OBJECTIVES

After completing this experiment, you will be able to:

- Design and construct Multiplexer and DeMultiplexer
- Verify their truth tables using basic logic gates

COMPONENTS REQUIRED

- Two 7411, 3 I/P AND gates
- 7432, 2 I/P OR gate
- 7404, hex inverter

THEORY

MULTIPLEXER:

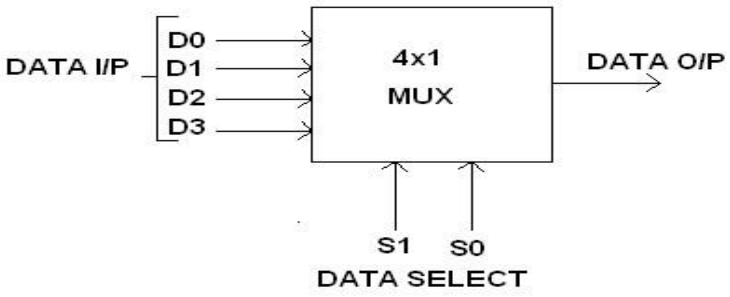
Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input line and n selection lines whose bit combination determine which input is selected.

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

In the 1x4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

BLOCK DIAGRAM FOR 4x1 MULTIPLEXER:

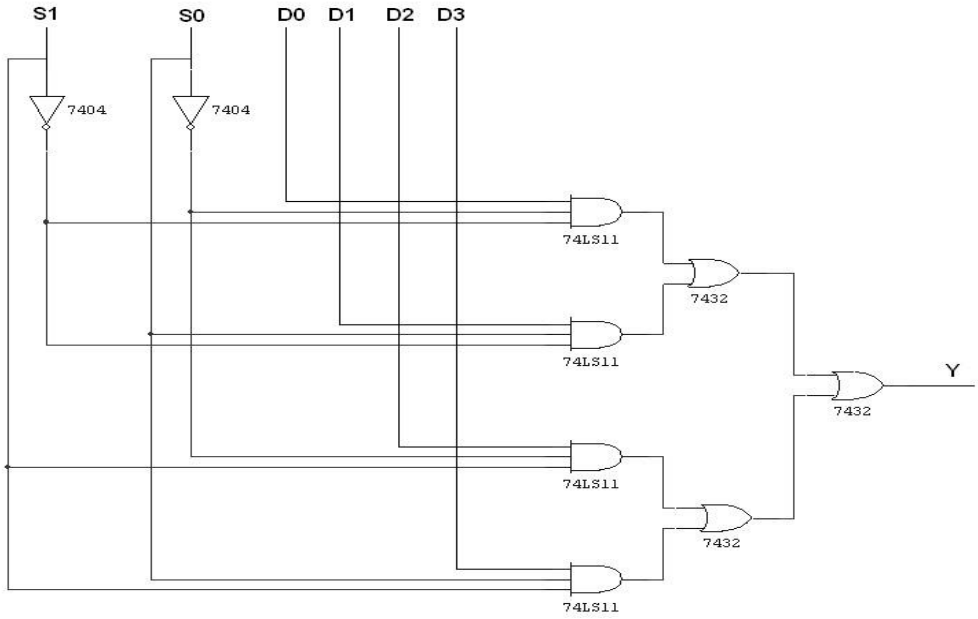


FUNCTION TABLE:

S1	S0	OUTPUT Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

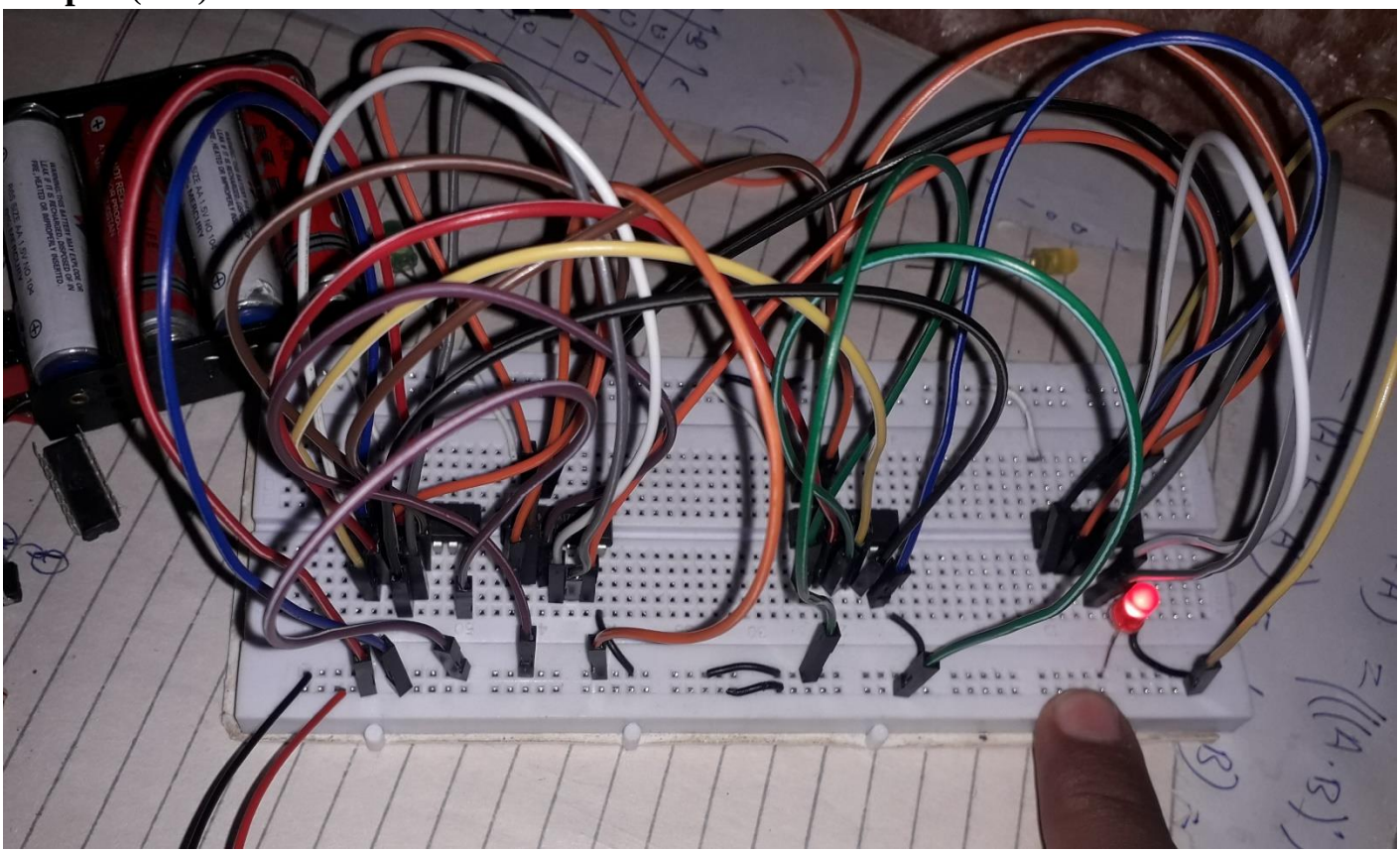
CIRCUIT DIAGRAM FOR 4x1 MULTIPLEXER:



Practical experimental circuit:-

Note: circuit is for input: (s_0=1, s_1=1 and D_3=1)

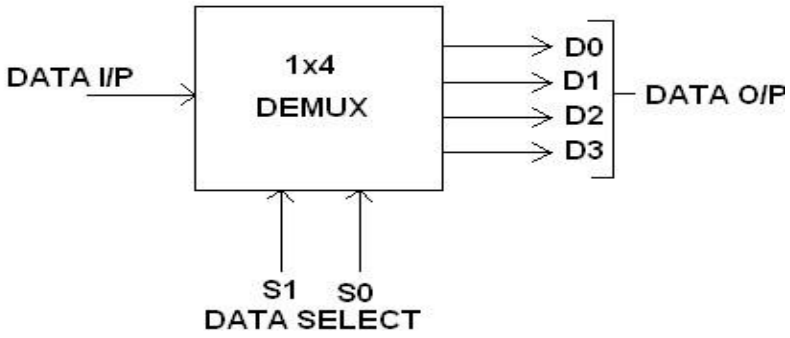
Output:(Y=1)



TRUTH TABLE:

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

BLOCK DIAGRAM FOR 1x4 DEMULTIPLEXER:

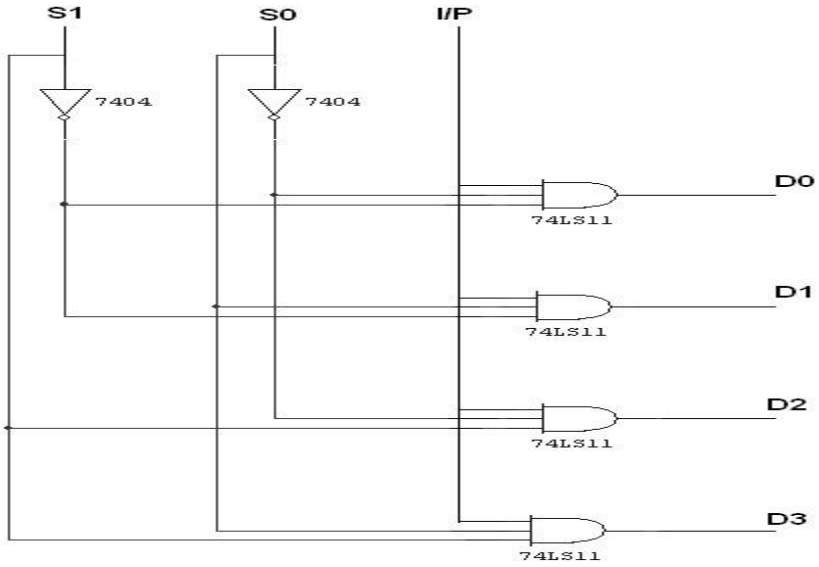


FUNCTION TABLE:

S1	S0	OUTPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0

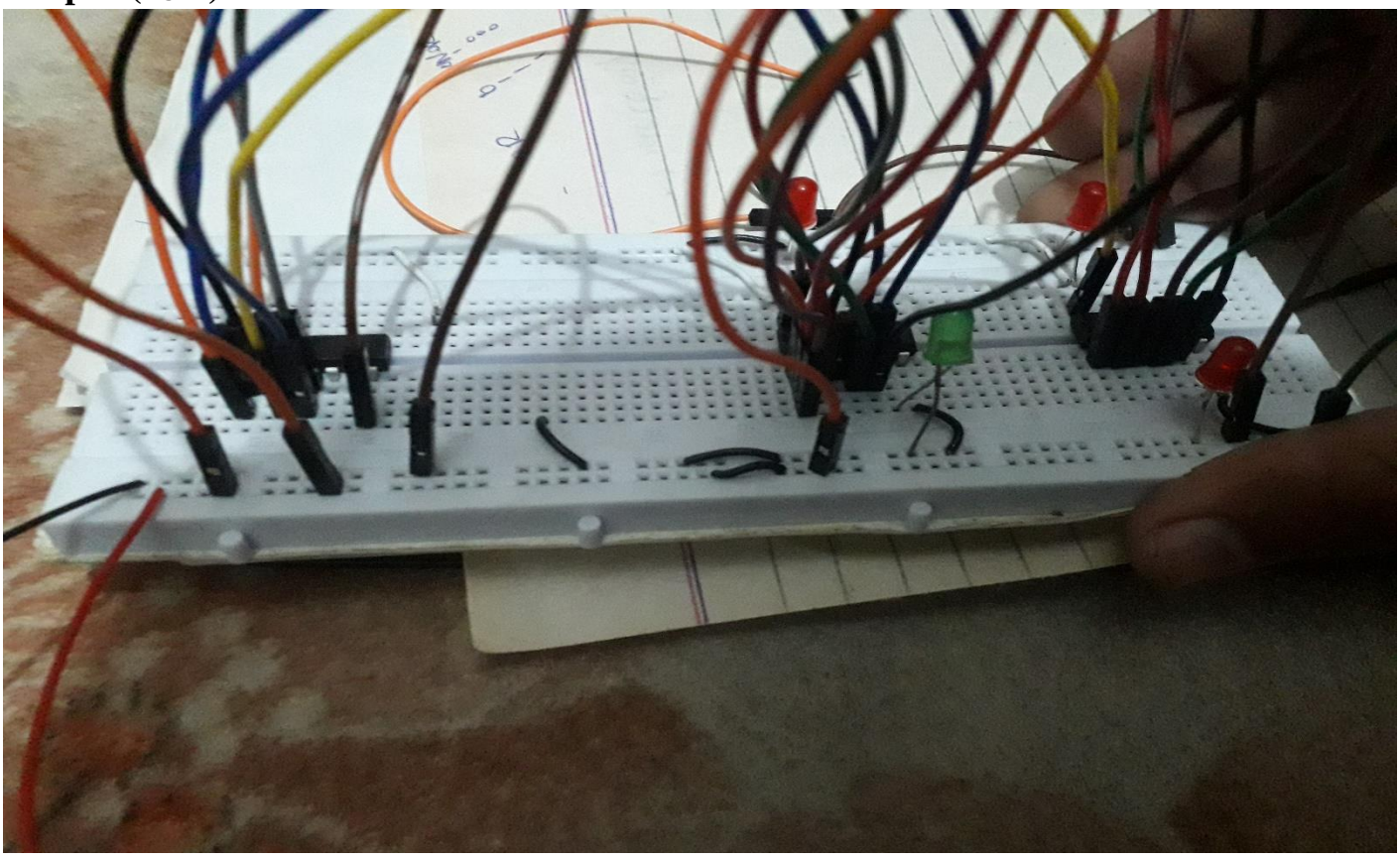
LOGIC DIAGRAM FOR DEMULTIPLEXER:



Practical experimental circuit:-

Note: circuit is for input: (s_0=1, s_1=1 and I/P=1)

Output:(D_3=1)



TRUTH TABLE:

INPUT			OUTPUT			
S1	**S0**	**I/P**	**D0**	**D1**	**D2**	**D3**
0	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**	**0**	**0**
0	**1**	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**1**	**0**
1	**1**	**0**	**0**	**0**	**0**	**0**
1	**1**	**1**	**0**	**0**	**0**	**1**

PROCEDURE

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

REVIEW QUESTIONS

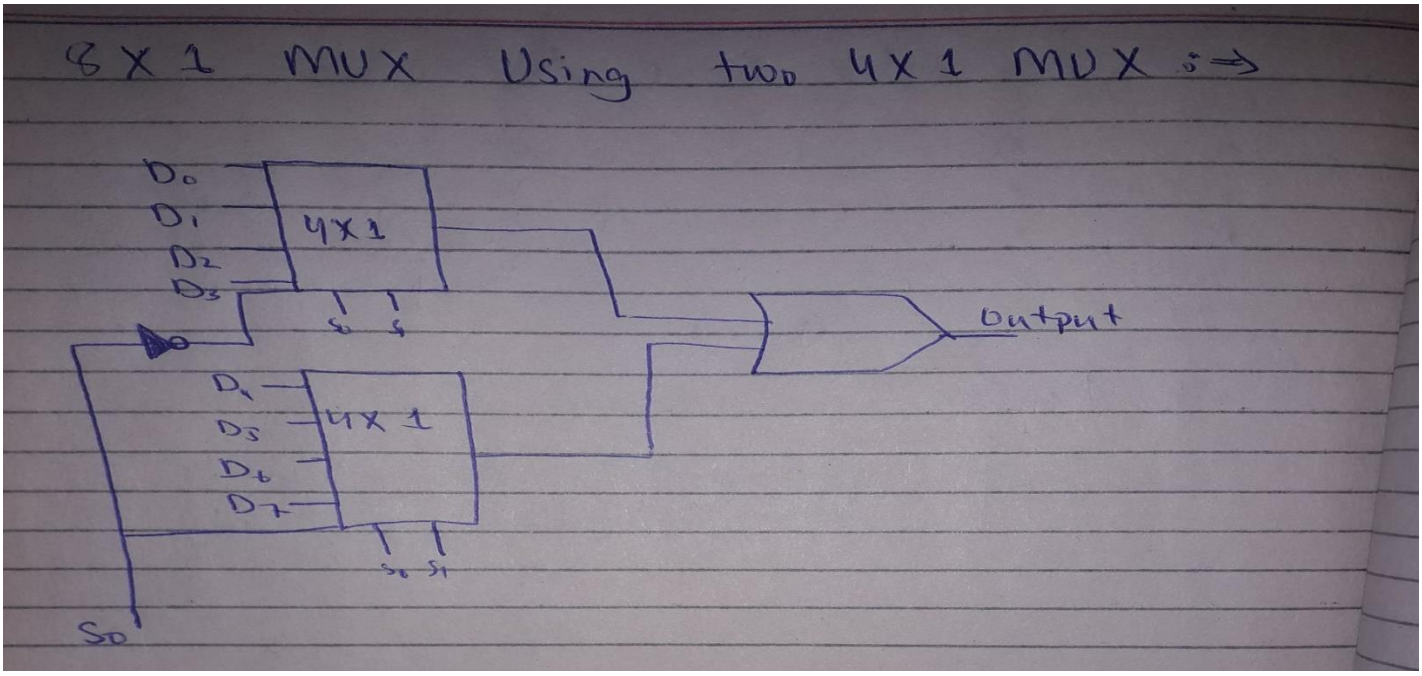
- **What is the difference between Multiplexer and De-Multiplexer?**

Answer:

- The major factor that differentiates multiplexer and demultiplexer is their ability to accept multiple input and single input respectively. The multiplexer also known as a MUX operates on several inputs but provide a single output. As against demultiplexer also known as DEMUX simply reverses the operation of MUX and operates on single input but transmits the data to multiple outputs.
- MUX perform parallel to series conversion while DEMUX perform series to parallel.
- MUX act as data selector while DEMUX act as data distributor.

- **Design a 8x1 MUX using two 4x1 MUXes (74153) and a 2x1 MUX (74157).**

Answer:- I)



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