University of Engineering & Technology Peshawar

Programme: B.Sc. Computer Systems Engineering
Semester: 3rd Semester
Paper: Digital Logic Design **Date: January 6, 2021**
Exam Type: Midterm

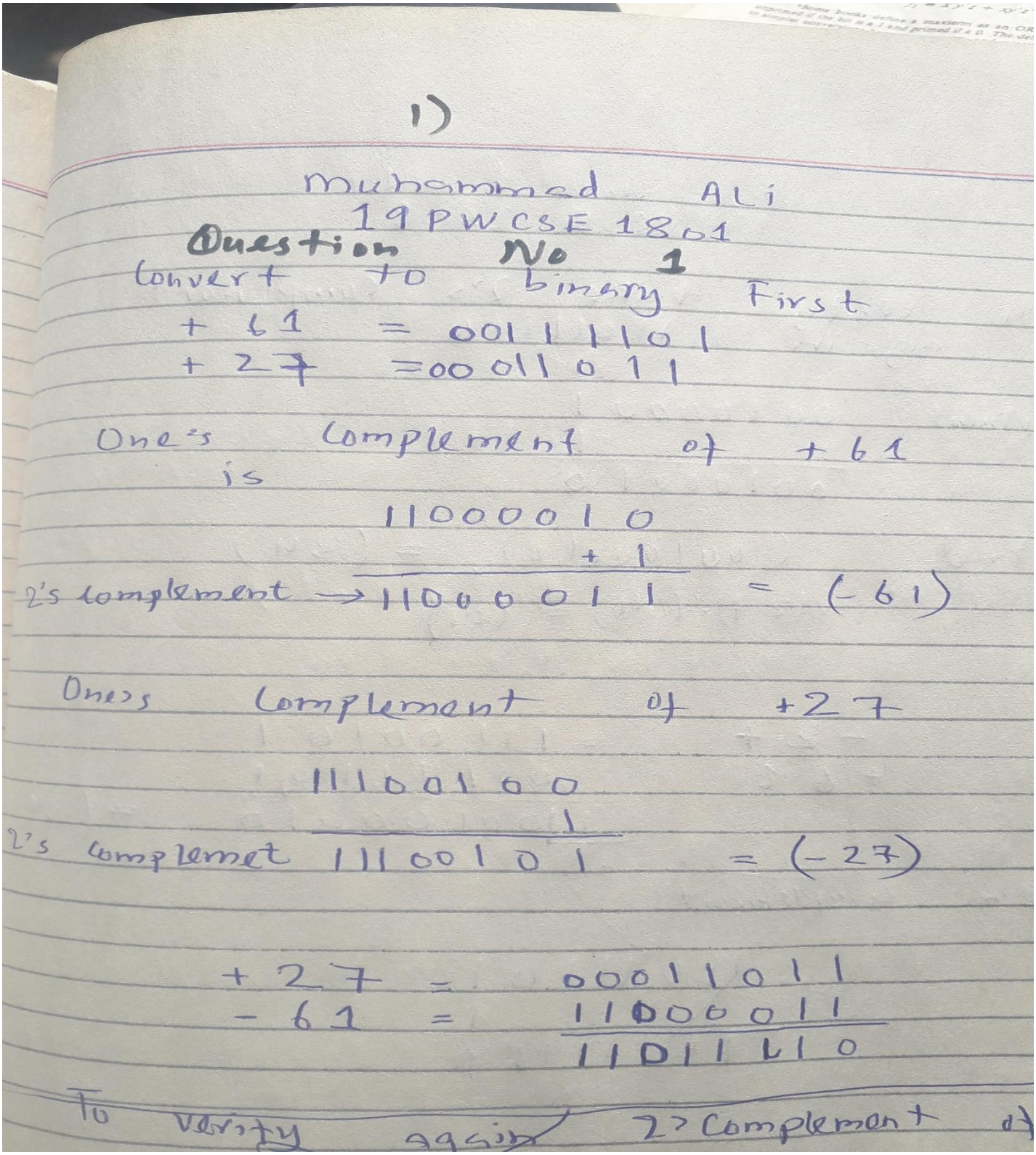
Allowed Time: 120 Minutes	**Max Marks: 30**
Student's Name:	**Student's Registration: pwcse1801**
Student's Signature:	

Instructions:

1- This exam is OPEN books/notes/Internet.
2- Sharing of books, notes and other materials during this exam is not permitted.
3- Answer ALL questions.
4- There are 9 questions in total. Some questions are harder than others. Answer the easy ones first to maximize your score.
5- Questions will not be interpreted during the exam.

Marks

Q. 1 Convert decimal +61 and +27 to binary using the signed-2's 6 complement representation and enough digits to accommodate the numbers. Then perform the binary equivalent of (+27) + (-61), (-27) + (+61) and (-27) + 61). Convert the answers back to decimal and verify that they are correct.



2)

Muhammad ALi
19PWCSE 1801

To verify take 2's complement
again 11011110

1's Complement 00100001
+ 1
00100010

Verified $(00100010)_2 = (34)$

In (27)-(64) = (34)

And

-27 = 11100101
+61 = 00111101
1|00100010 = (34)

3)

And

$-27 = 11100101$

$-61 = 11000011$

$\overline{1\,|\,10101000}$

Again 2's Complement to verify

01010111

$+\quad\quad 1$

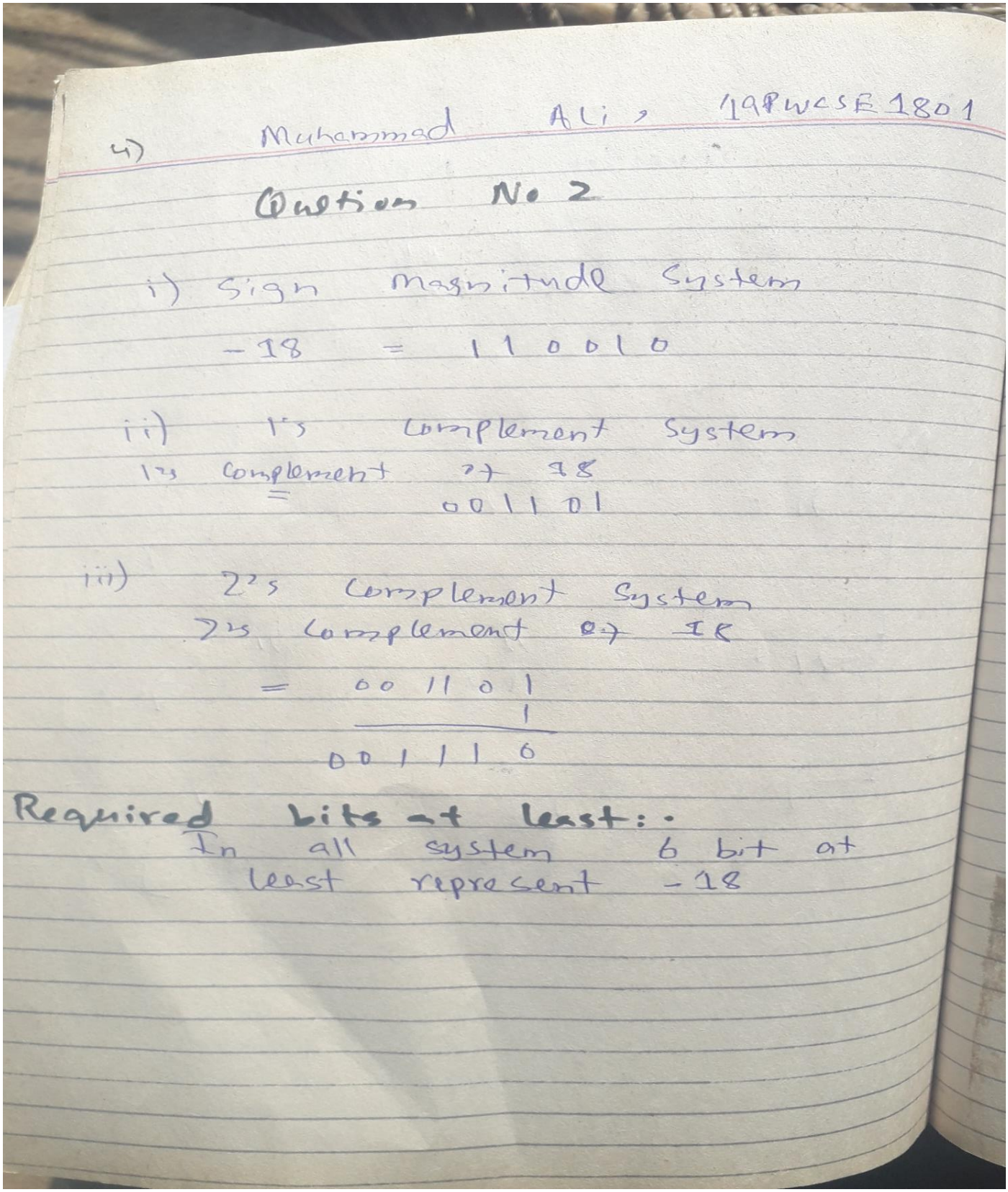
$\overline{01011000} = (88)$

$(-27)(-61) = (-88)$

Hence verified

Q. 2 At the least how many bits are needed to represent -18 (read as 3 minus 18) in

i. Sign-magnitude system
ii. 1's complement system iii. 2's complement system



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Question No 2

i) Sign Magnitude System

$-18 = 1\,1\,0\,0\,1\,0$

ii) 1's Complement System

1's Complement of 18

$= 0\,0\,1\,1\,0\,1$

iii) 2's Complement System

2's Complement of 18

$= 0\,0\,1\,1\,0\,1$

$+\quad\quad\quad 1$

$0\,0\,1\,1\,1\,0$

Required bits at least:

In all system 6 bit at least represent -18

Q. 3 In the following table fill the column B with an appropriate decimal 2 number corresponding to the equivalent unsigned binary number given in column A.

Column A	Column B
000	0
001	1
010	3
011	3
100	4
101	5
110	6
111	7

Q. 4 In the following table fill the column B with an appropriate decimal 2 number corresponding to the equivalent 1's complement number given in column A.

Column A	Column B
000	+0
001	+1
010	+2
011	+3
100	-3
101	-2
110	-1
111	-0

Q. 5 In the following table fill the column B with an appropriate decimal 2 number corresponding to the equivalent 2's complement number given in column A.

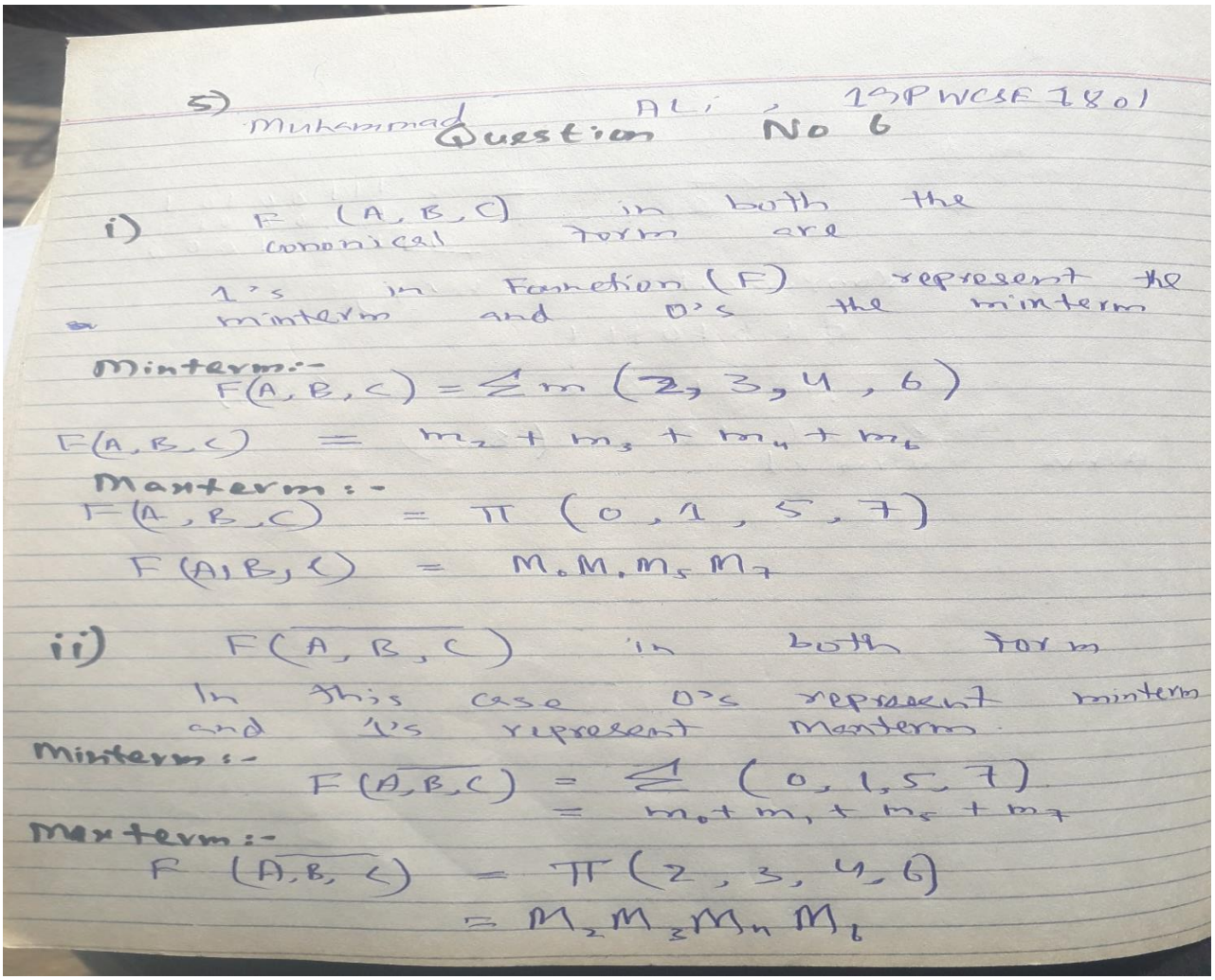
Column A	Column B
000	+0
001	+1
010	+2
011	+3
100	-4
101	-3
110	-2
111	-1

Q. 6 From the following truth table, directly write the Boolean expression for: 4

i. $F(A,B,C)$ in both the canonical forms.

ii. $\overline{F(A,B,C)}$ in both the canonical forms.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



Q. 7 Write the truth table for the following Boolean expression/function: 2

$$F(A,B,C) = \bar{B}.C + A.(\bar{B}+C) + \bar{A}.\bar{C}$$

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Q. 8 The following gates are available and the unit price is also listed. 4

- Price of 3-input AND gate = $ 2/-
- Price of 2-input OR gate = $ 2/-
- Price of NOT gate = $ 1/-

Implement the following Boolean function using the above gates. Draw its logic diagram and calculate its cost.

$$F(X,Y,Z)= \sum_m(1, 7)$$

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Question No 8

3-input AND gate = $2/-

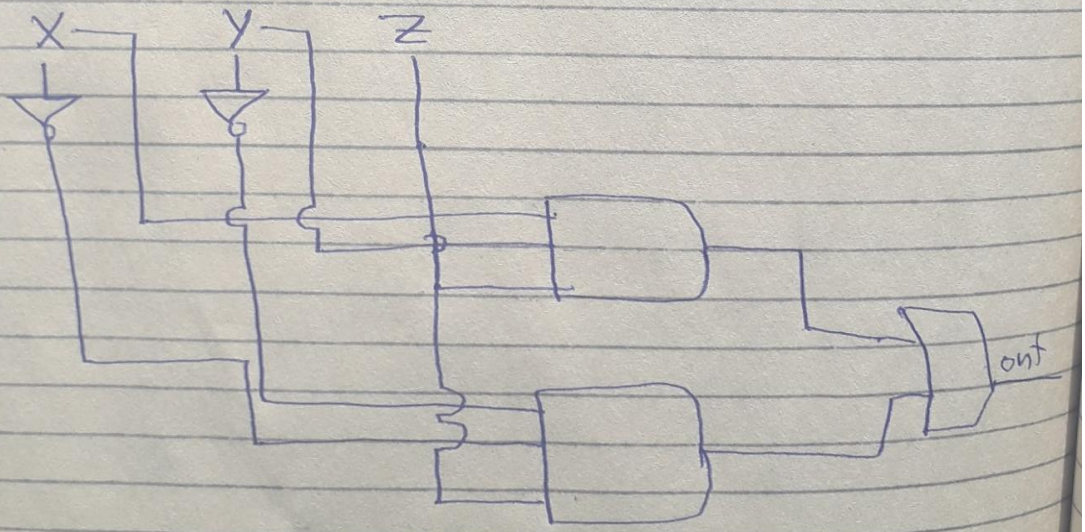
2-input OR gate = $2/-

Not gate = $1/-

$$F(X,Y,Z) = \Sigma_m(1,7)$$

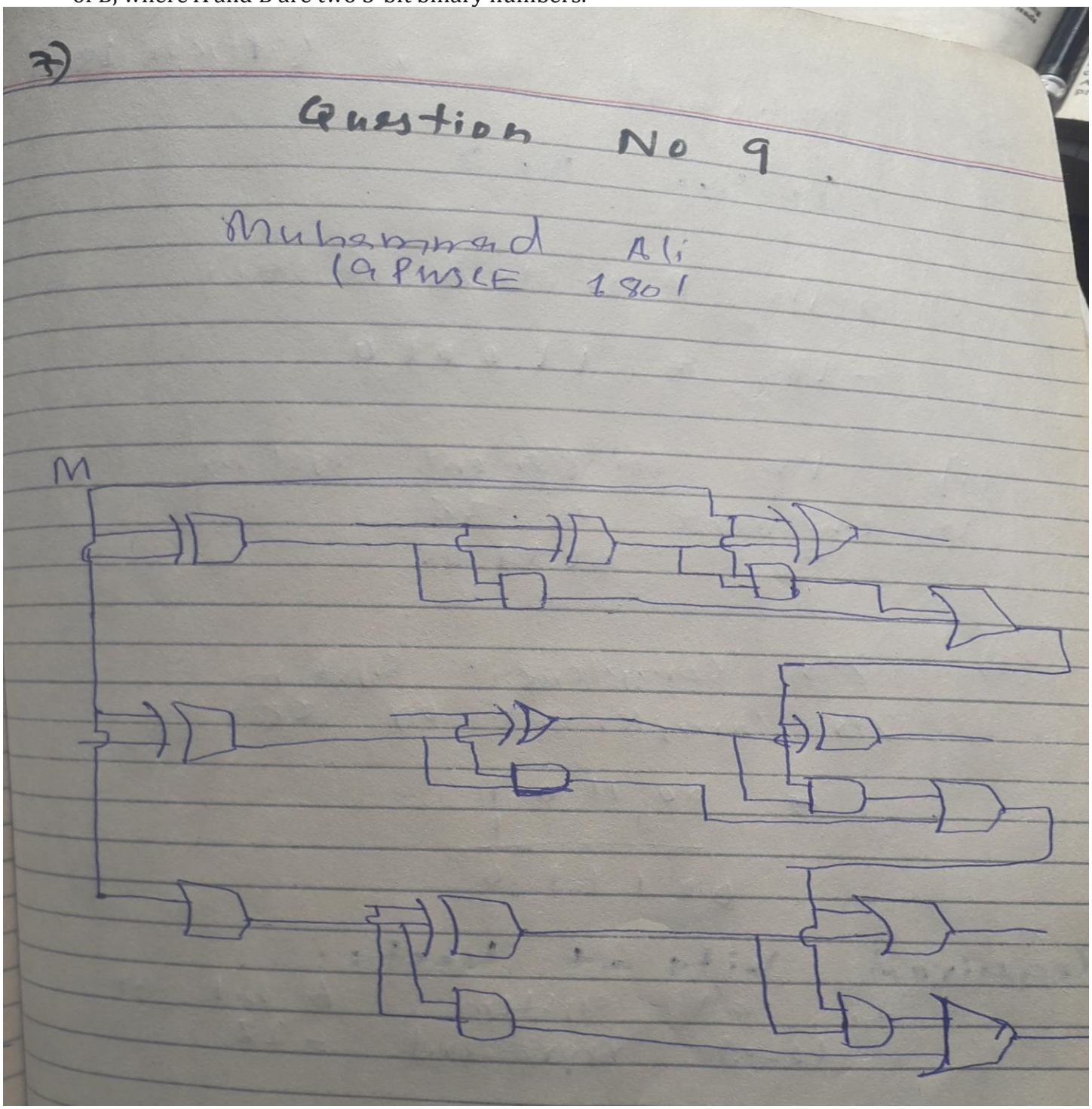
$$F(X,Y,Z) = m_1 + m_7$$
$$= X'Y'Z + XYZ$$

Logic diagram :-



Cost = 8 $

Q. 9 Design a 3-bit adder-subtractor circuit using 1-bit binary Full adders and 5 any necessary additional logic gates. The circuit has a mode/control input bit, M, that controls its operation. Specifically, when M=0, the circuit becomes a 3-bit adder, and when M=1, the circuit becomes a 3-bit subtractor that performs the operation A plus the 2's complement of B, where A and B are two 3-bit binary numbers.



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