University of Engineering and Technology (UET),
Peshawar, Pakistan

Lecture 3

CSE-304: Computer Organization and Architecture

BY:

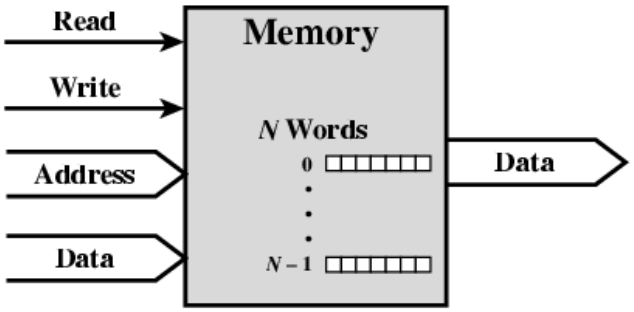
Dr. Muhammad Athar Javed Sethi

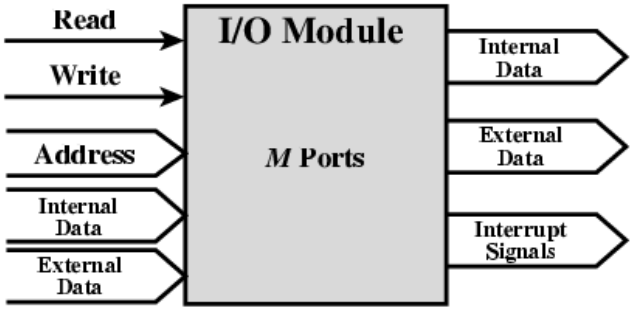
Slides are taken from student resources of William Stallings website

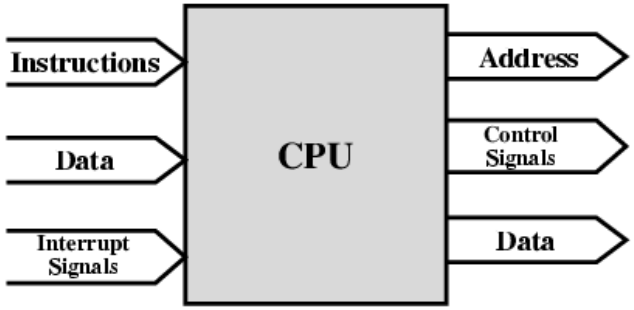
Connecting

- All the units must be connected
- Different type of connection for different type of unit
  - Memory
  - Input/Output
  - CPU

Computer Modules

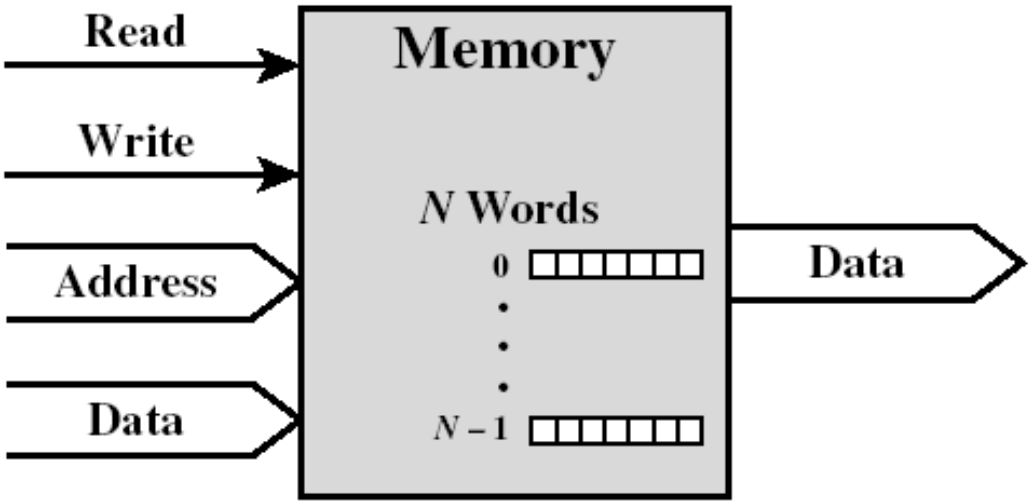






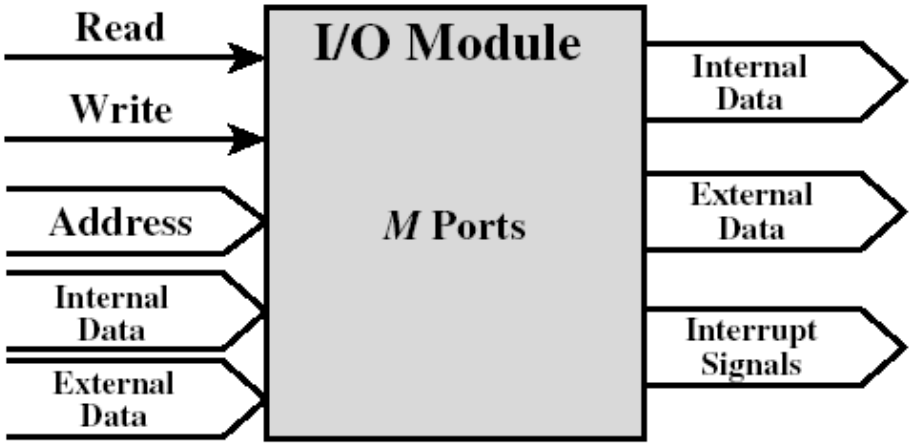
Memory Connection

- Receives and sends data
- Receives addresses (of locations)
- Receives control signals
  - Read
  - Write



Input/Output Connection(1)

- Similar to memory from computer's viewpoint
  - Receive data from computer
  - Receive data from peripheral
  - Send data to peripheral
  - Send data to computer

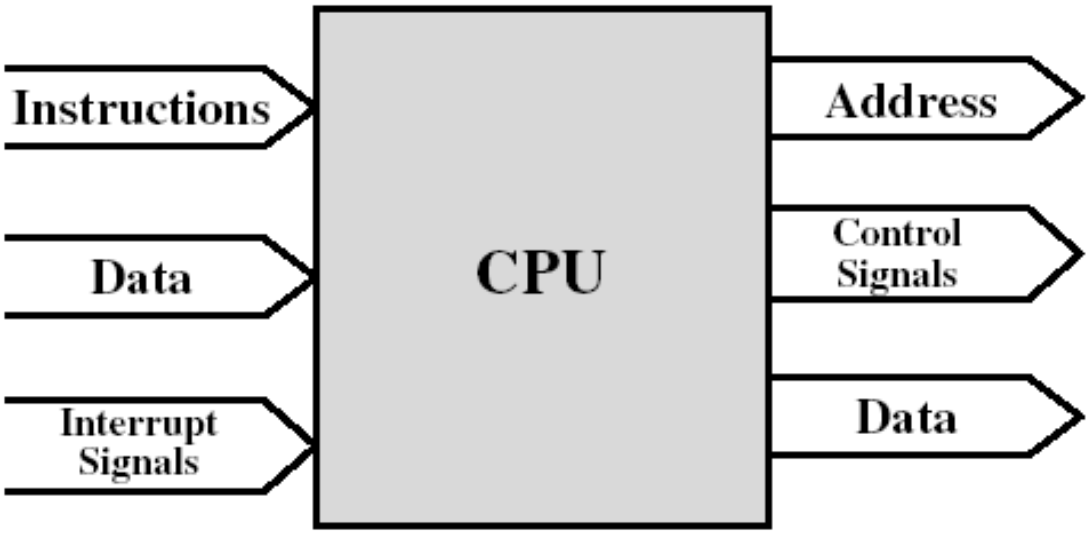


Input/Output Connection(2)

- Receive control signals from computer
- Send control signals to peripherals
- Receive addresses from computer
  - e.g. port number to identify peripheral
- Send interrupt signals (control)

CPU Connection

- Reads instruction and data
- Writes out data (after processing)
- Sends control signals to other units
- Receives (& acts on) interrupts



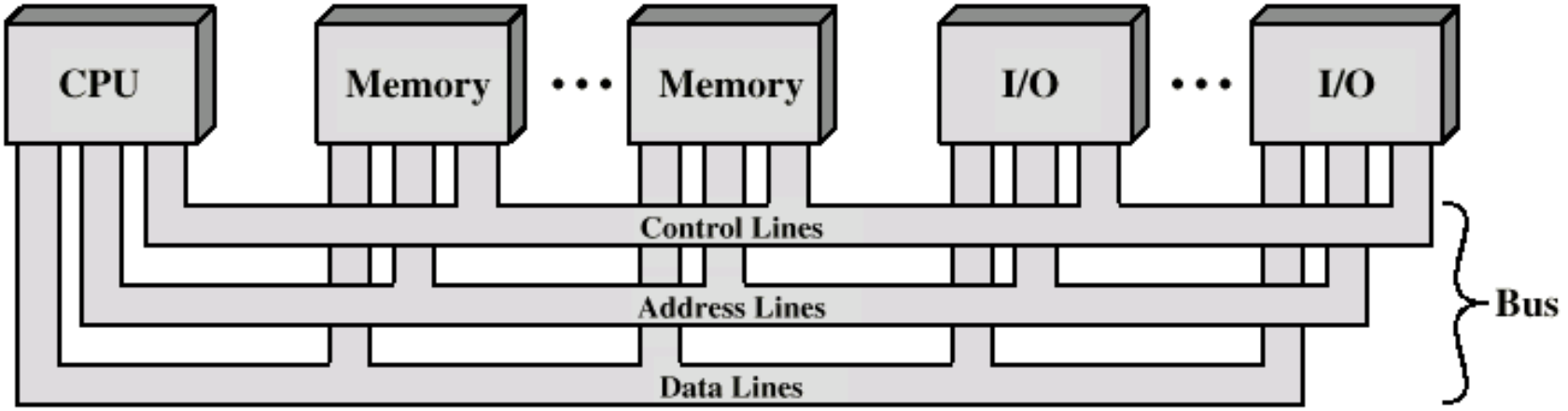
Buses

- There are a number of possible interconnection systems
- Single and multiple BUS structures are most common
- e.g. Control/Address/Data bus
- e.g. Unibus

What is a Bus?

- A communication pathway connecting two or more devices
- Usually broadcast (all components see signal)
- Often grouped
  - —A number of channels in one bus
  - —e.g. 32 bit data bus is 32 separate single bit channels

Bus Interconnection Scheme



Data Bus

- Carries data
  - Remember that there is no difference between “data” and “instruction” at this level
- Width is a key determinant of performance
  - 8, 16, 32, 64 bit

Address bus

- Identify the source or destination of data
- e.g. CPU needs to read an instruction (data) from a given location in memory
- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space

Control Bus

- Control and timing information
  - —Memory read/write signal
  - —Interrupt request
  - —Clock signals

Single Bus Problems

- Lots of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
- Most systems use multiple buses to overcome these problems

Bus Types

- Dedicated
  - —Separate data & address lines
- Multiplexed
  - —Shared lines
  - —Address valid or data valid control line
  - —Advantage - fewer lines
  - —Disadvantages
    - More complex control

Bus Arbitration

- More than one module controlling the bus
- Only one module may control bus at one time
- Arbitration may be centralised or distributed

Centralised Arbitration

- Single hardware device controlling bus access
  - —Bus Controller
  - —Arbiter

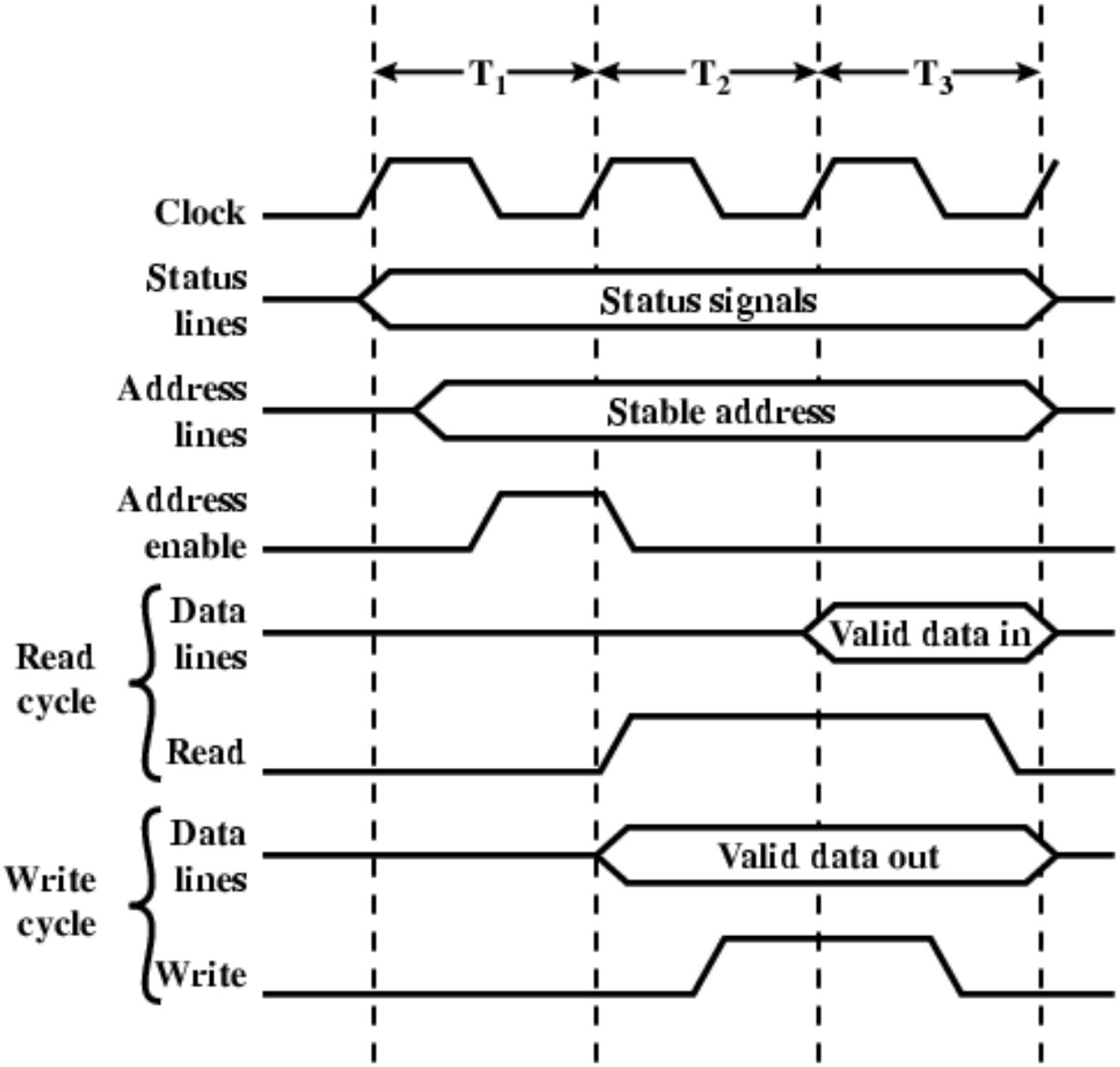
Distributed Arbitration

- Each module may claim the bus
- Control logic on all modules

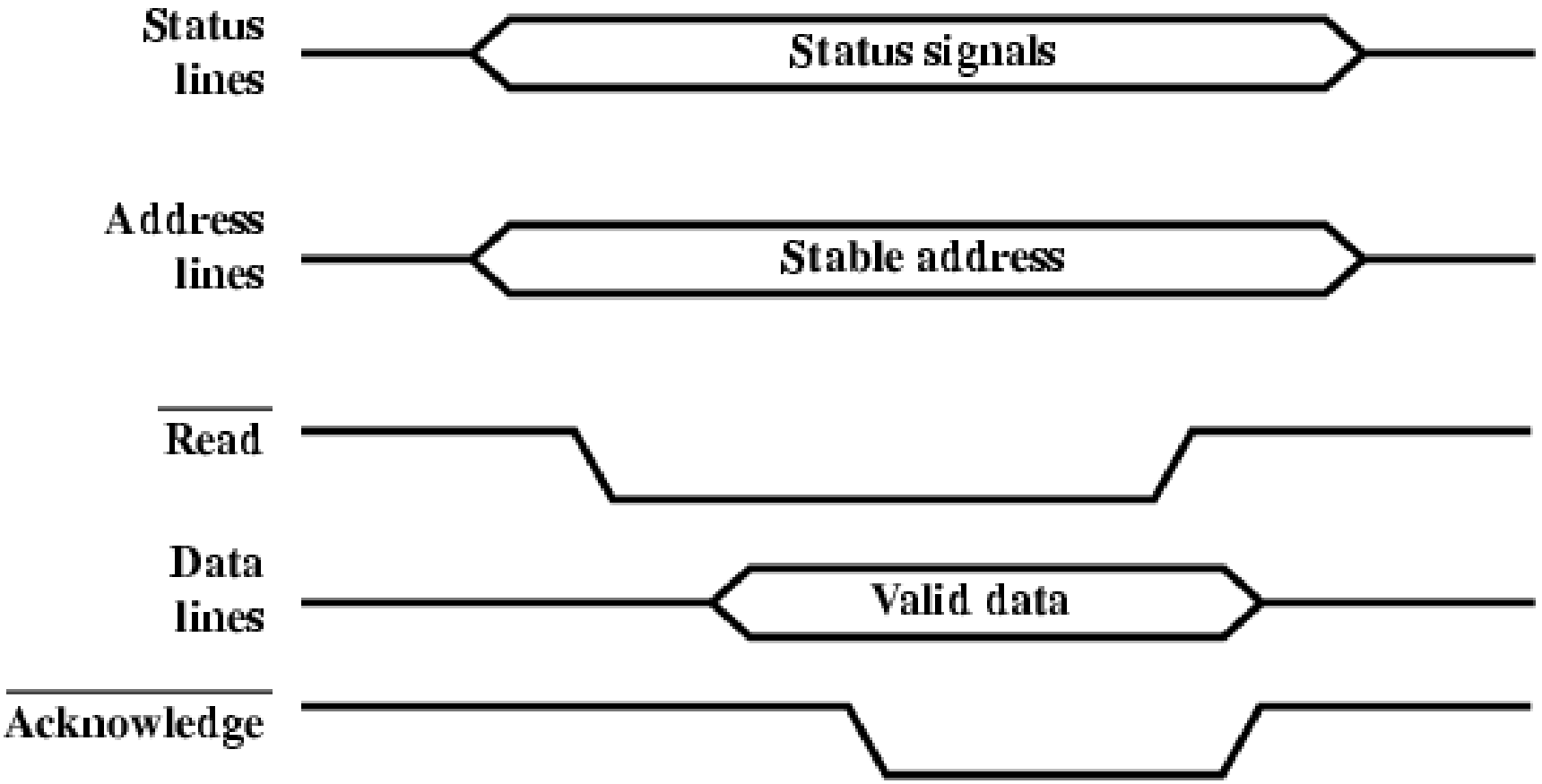
Timing

- Co-ordination of events on bus
- Synchronous
  - —Events determined by clock signals
  - —Control Bus includes clock line
  - —A single 1-0 is a bus cycle
  - —All devices can read clock line
  - —Usually sync on leading edge
  - —Usually a single cycle for an event

Synchronous Timing Diagram



Asynchronous Timing – Read Diagram



Asynchronous Timing – Write Diagram