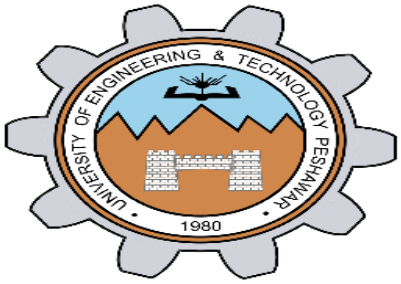
LAB REPORT NO 11



CSE-202L Digital logic design lab

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Class Section: A

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Submitted to:

Engr. Abdullah Hamid

Data:(24,2,2021)

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

Lab1

Ripple &ounters

OBJECTIVES

After completing this experiment, you will be able to:

- ③ Design and verify D4bit 5ipple &ounter
- ③ Design and verify 02'10DQG02'12 5ipple &ounter
- ③ Explain how D 5LSSOH&ounter FDQEHXVHGDV a frequency divider

COMPONENTS REQUIRED

- ③ Two 7476JK)lip)lop ICs
- ③ One 74002,QSXW NAND gate

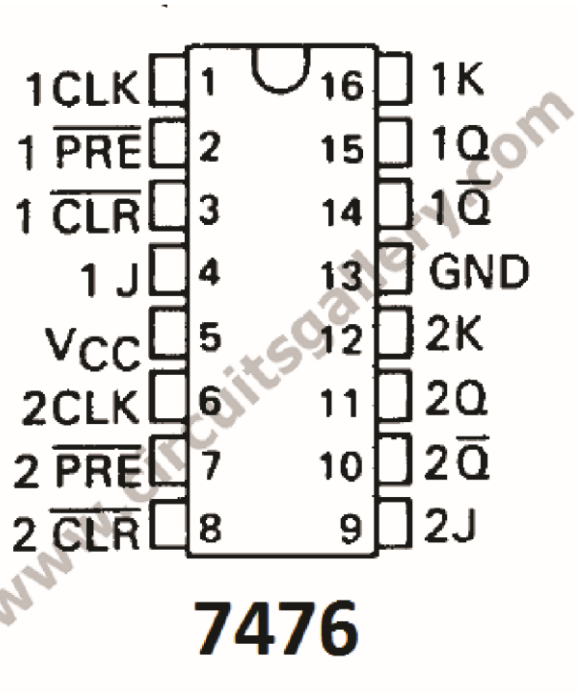
THEORY

$FLUFXLWXVHGIRUFRXQWLQJWKHSXOVHVLVNQRZQDV&RXQWHU%DVLFDOO\WKHUHDUHWZRW\SHVRI&RXQWHUV
$V\QFKURQRXV&RXQWHUV5LSSOH&RXQWHUVDQG6\QFKURQRXV&RXQWHUV

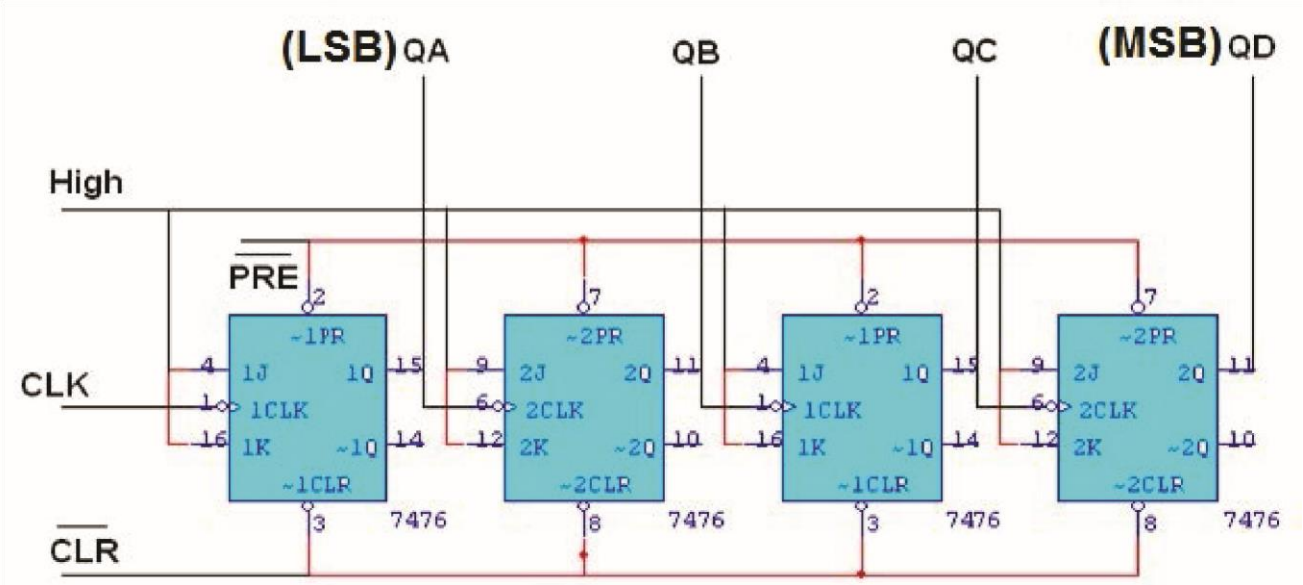
**$V\QFKURQRXV&RXQWHU**,QWKHFDVHRIDQ$V\QFKURQRXV&RXQWHUDOOWKH)OLS)ORSVDUHQRWFORFNHG
VLPXOWDQHRXVO\7KLV&RXQWHULVVLPSOHLQRSHUDWLRQ
UHTXLUHVDPLQLPXPRIKDUGZDUH%XWLWVVSHHGLV
VORZ(DFK))LVWULJJHUHGE\DSUHYLRXV))RS(DFK))WDNHVLWVRZQWLPHWRJLYHRSGXHWRSURSDJDWLRQ GHOD\6RILQDOVHWWOLQJWLPHLVKLJK

6\QFKURQRXV&RXQWHU,Q6\QFKURQRXV&RXQWHUDOOWKH))VDUHFORFNHGVLPXOWDQHRXVO\,WLVFRPSOH[LQ
FRQVWUXFWLRQEXWVSHHGLVPRUH,QWKLVFDVHVLQFHHDFK))LVFORFNHGVLPXOWDQHRXVO\WKXVVHWWOLQJWLPHLVWKH GHOD\WLPHRIVLQJOH))

PIN DIAGRAM FOR IC 7476



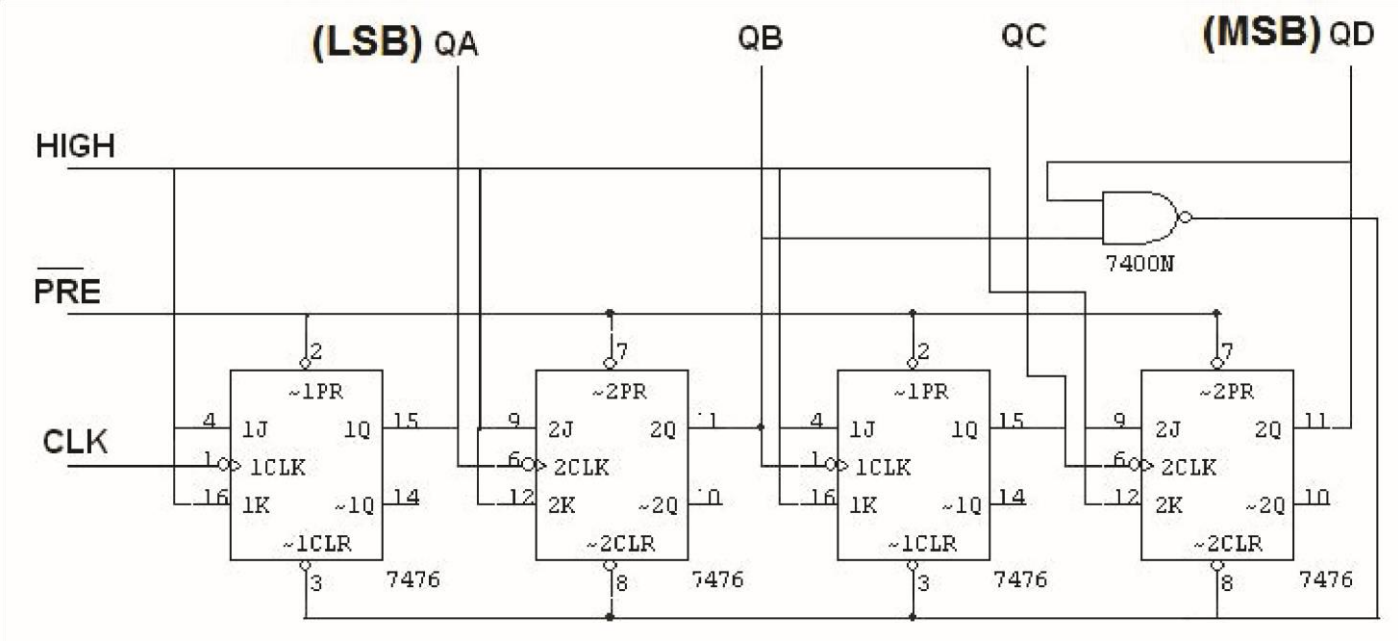
LOGIC DIAGRAM FOR 4BIT RIPPLE COUNTER



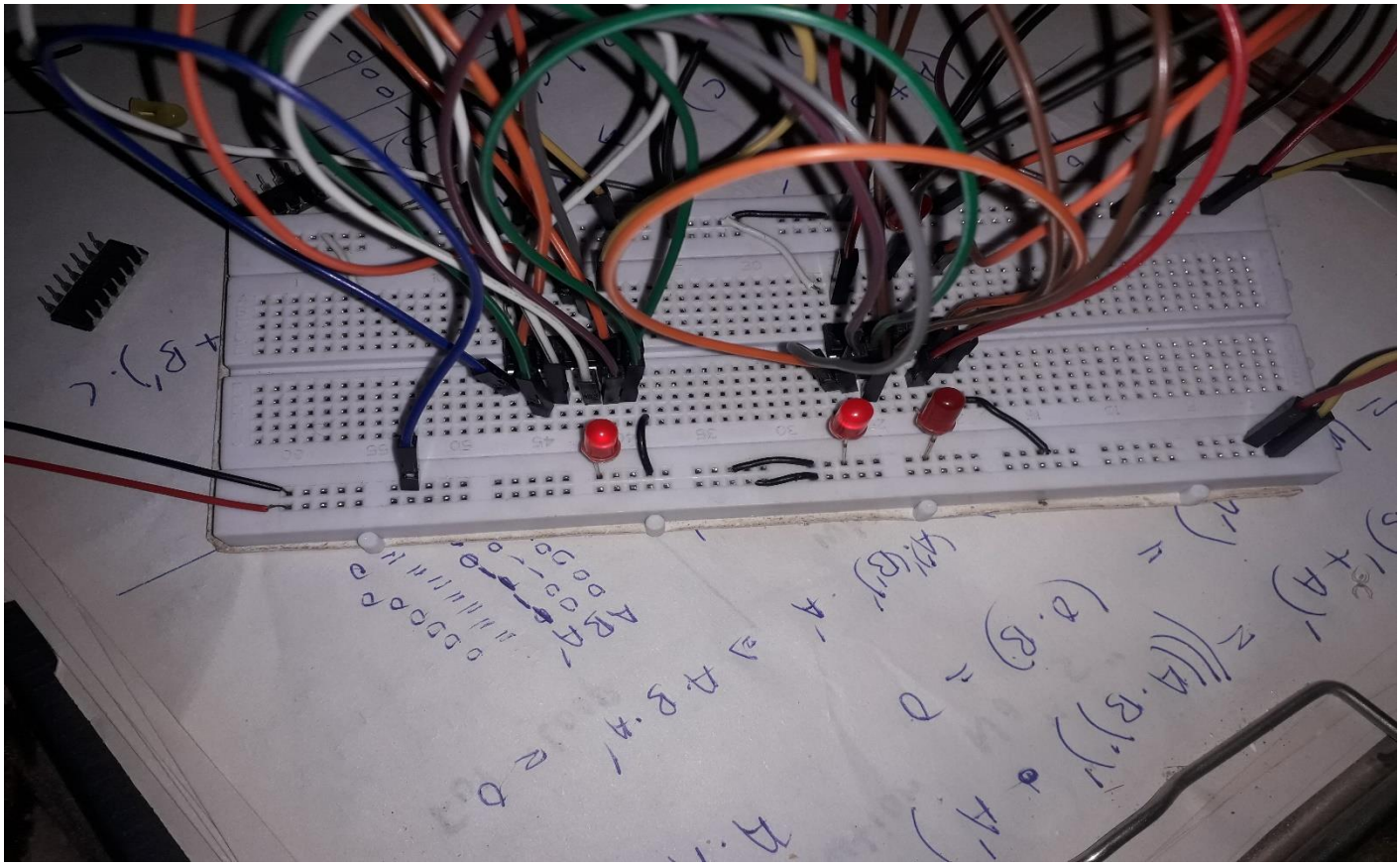
TRUTH TABLE

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

LOGIC DIAGRAM FOR MOD-10 RIPPLE COUNTER:



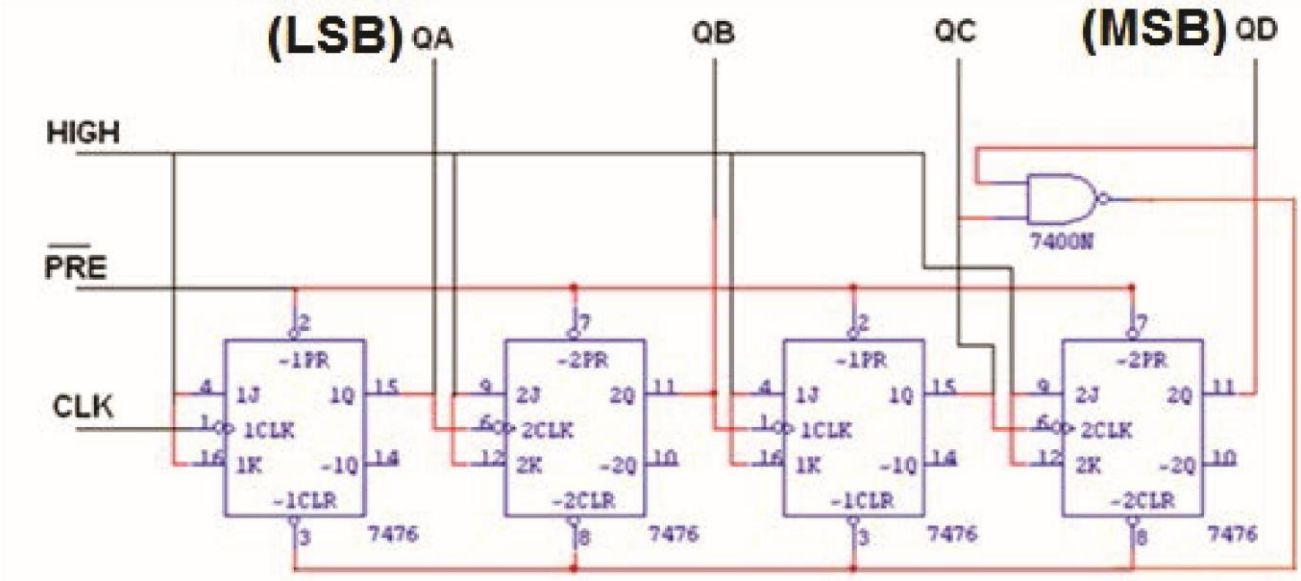
Experimental real pictures:-(For CLK=3)



TRUTH TABLE

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0

LOGIC DIAGRAM FOR MOD-12 RIPPLE COUNTER



Experimental real pictures:-For CLK=3

TRUTH TABLE

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	0	0

PROCEDURE

- ③ Connections are given as per circuit diagram.
- ③ Logical inputs are given as per circuit diagram.
- ③ Observe the output and verify the truth table. ③

REVIEW QUESTIONS

1.Counters can be used as frequency dividers. When the clock frequency in WKHELW 5LSSOH&RXQWHUJLYHQDERYHLV 1kHz, what ZLOOEH the output frequency of)lip-)lop A and)lip-)lop B?

Ans:

The answer will be

fA=half of one means

=0.5Hz

fb=quarter of one

means=0.25Hz

2.Would inverters on the clock inputs changethe count direction of a 5ipple &ounter?

Answer:- The count a ripple counter is not effected by inverter on the clock direction.

3.How many)lip-)lops are needed to build a 02'-5 &ounter?

The no of flipflops must be less than or equal to 2 power n where n is positive integer.so therefore 3 flipflops are required to madeup Mpd-5 counter.