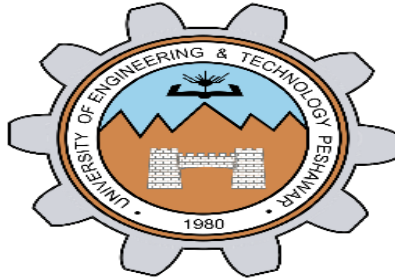


## LAB REPORT NO 8



### CSE-202L Digital logic design lab

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Class Section: A

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Submitted to:

**Engr. Abdullah Hamid**

Data:(31,1,2021)

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## Lab # 8: Magnitude comparators

### Objective:

- Realization of 1-bit comparator using logic gates.
- Realization and implementation of 2-bit comparator using logic gates on breadboard.
- Implementation of 4-bit magnitude comparator on breadboard using IC 7485.

### Components Required:

- Breadboard.
- IC Type 7486 Quadruple 2-input XOR gates.
- IC Type 7408 Quadruple 2-input AND gates.
- IC Type 7400 Quadruple 2-input NAND gates.
- IC Type 7410 Triple 3-input NAND gates.
- IC Type 74L85 4-bit magnitude comparator.
- Switches for inputs and
- LED displays for outputs.

### Theory:

Magnitude comparator is a combinational logic circuit that compares between two binary numbers A and B and determines their relative magnitudes. The output of the circuit is specified by three binary variables whether:  $A > B$ ,  $A = B$  or  $A < B$ .

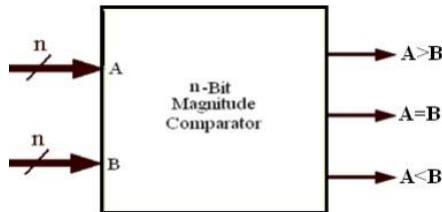


Figure 1: Block diagram of n-bit Magnitude Comparator. 1-

### 1-bit Magnitude Comparator:

A comparator used to compare two 1-bit binary numbers. It has two binary inputs A, B and three binary outputs: greater than, equal and less than relations. Figure 2 below shows the block diagram and truth table of a 1-bit magnitude comparator.



(a) Block diagram

A	B	A=B	A<B	A>B
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

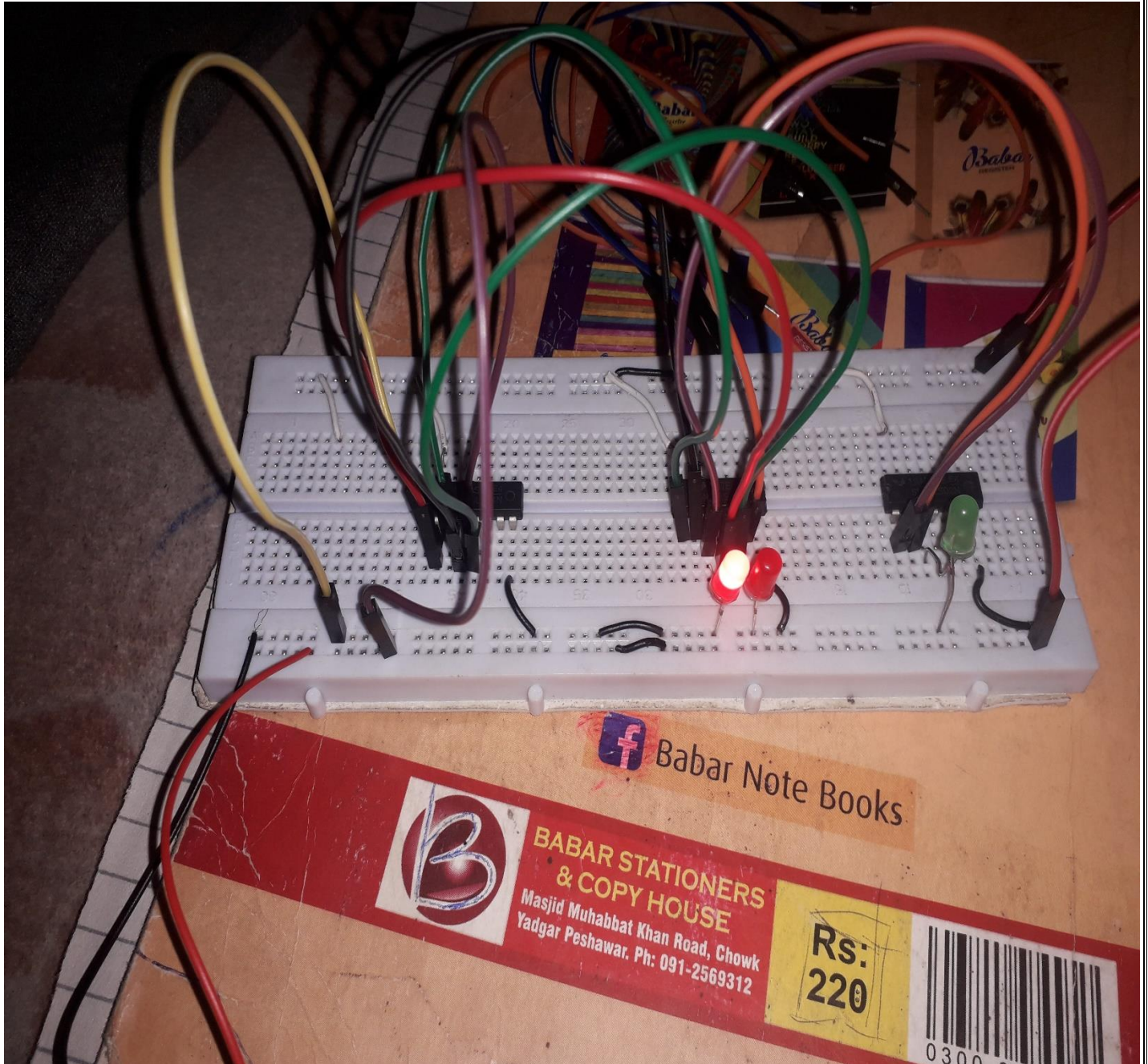
(b) Truth table

**Figure 2**

The Boolean functions describing the 1-bit magnitude comparator according to the truth table are:

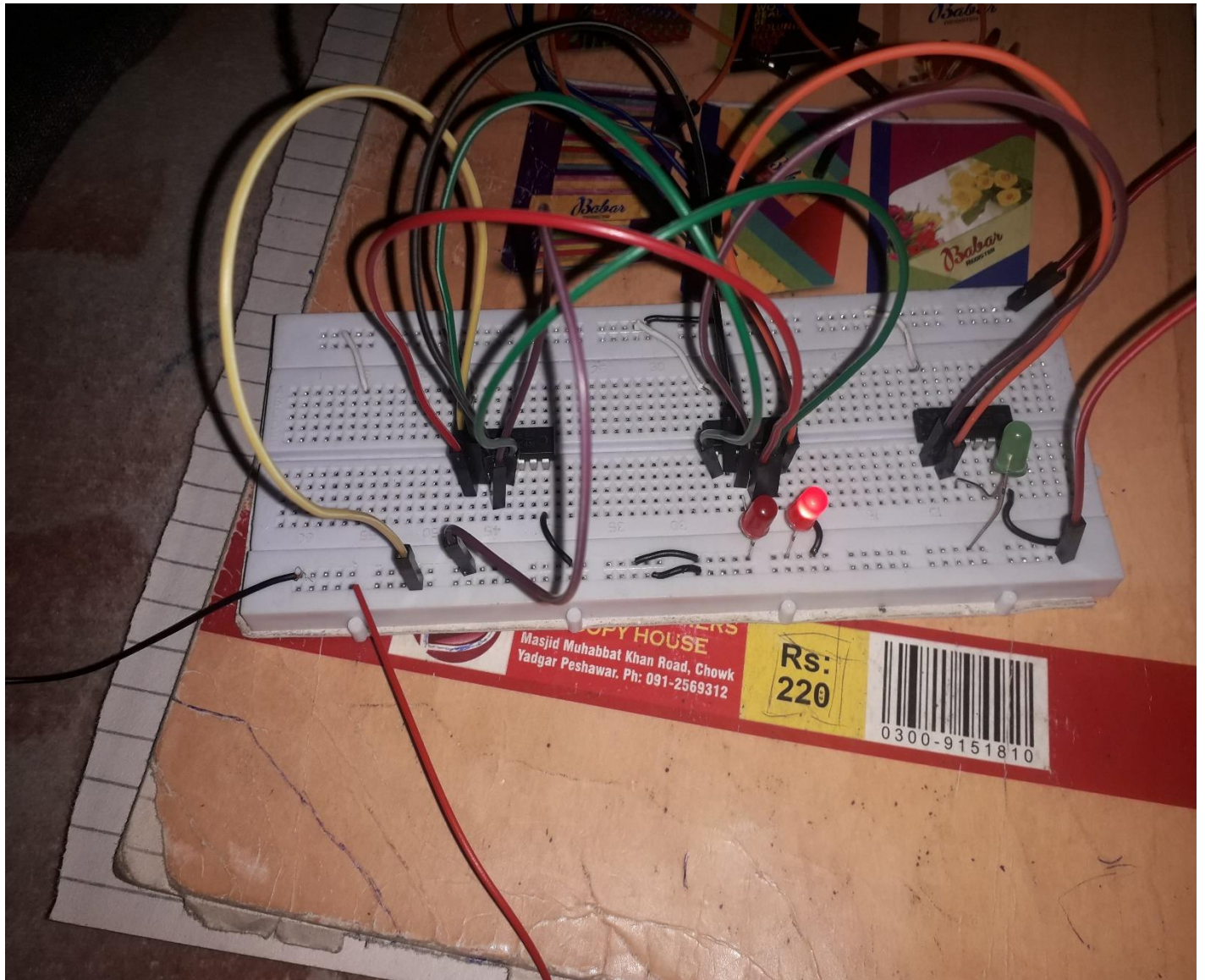
**Practical experimental circuit:-**

**For input (A=0 and B=1)**





**Practical experimental circuit:-**  
**For input (A=1 and B=0)**

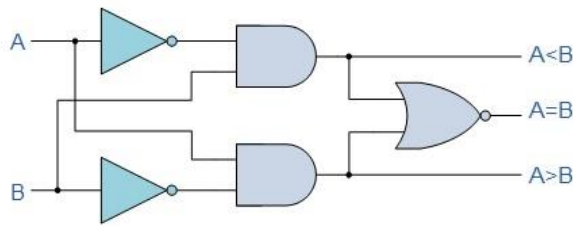


$$(A > B) = A'B$$

$$(A = B) = A'B' + AB = (A \oplus B)'$$

$$(A < B) = AB'$$

The logic diagram for 1-bit binary comparator implemented by XOR and basic logic gates is shown below



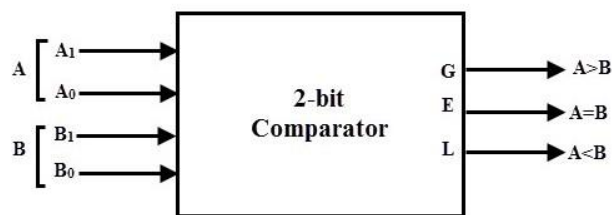
in figure 3.

Figure 3: Logic Diagram of 1-bit Comparator

So we conclude that digital comparators actually use **Exclusive-NOR** gates within their design for comparing their respective pairs of bits.

### 2-bit Magnitude Comparator:

A comparator used to compare two 2-bit numbers. It has 4 binary inputs (number A:  $A_1A_0$ , number B:  $B_1B_0$ ) and 3 binary outputs: greater than, equal and less than relations. Figure 4 below shows the block diagram and truth table of a 2-bit magnitude comparator.



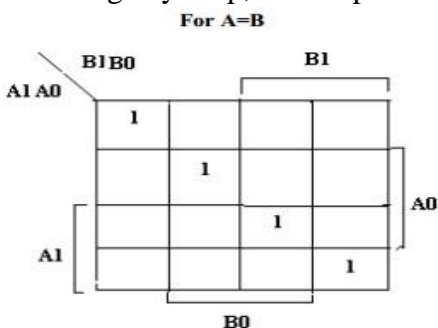
(a) Block diagram

Inputs				Outputs		
$A_1$	$A_0$	$B_1$	$B_0$	$A > B$	$A = B$	$A < B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

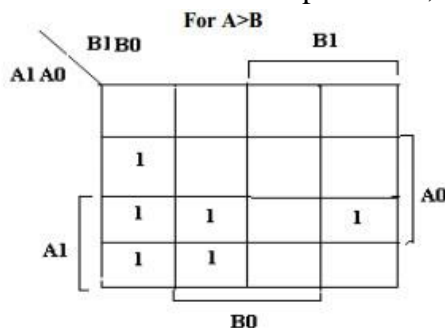
(b) Truth table Figure

4

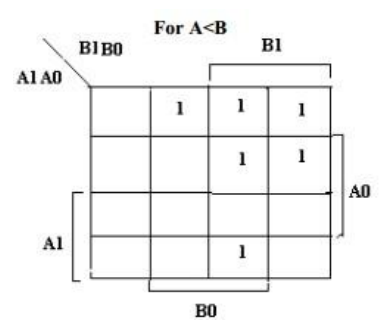
Using key-map, the simplified Boolean function for the outputs  $A > B$ ,  $A = B$  and  $A < B$  is shown below:



$A=B$ :



$A > B$ :



$A < B$ :

$$\begin{aligned}
 &= A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0'B_1B_0' + A_1A_0B_1B_0 \\
 &= A_1B_1' + A_1'A_0B_1'B_0' + A_1A_0B_1B_0' \\
 &= A_1B_1' + A_0B_0'(A_1'B_1' + A_1B_1) \\
 &= A_1'B_1 + A_1'A_0'B_1'B_0 + A_1A_0'B_1B_0 \\
 &= A_1'B_1 + A_0'B_0(A_1'B_1' + A_1B_1)
 \end{aligned}$$

$$\begin{aligned}
 &= (A_1'B_1' + A_1B_1)(A_0'B_0' + A_0B_0) \\
 &= (A_1 \oplus B_1)'(A_0 \oplus B_0)' \\
 &= X_1X_0 \\
 &= A_1B_1' + A_0B_0'(A_1 \oplus B_1)' \\
 &= A_1B_1' + X_1A_0B_0' \\
 &= A_1'B_1 + A_0'B_0(A_1 \oplus B_1)' \\
 &= A_1'B_1 + X_1A_0'B_0
 \end{aligned}$$

Based on the simplified Boolean functions for the three outputs  $A > B$ ,  $A = B$  and  $A < B$ , the logic diagram of the 2-bit magnitude comparator is shown below:

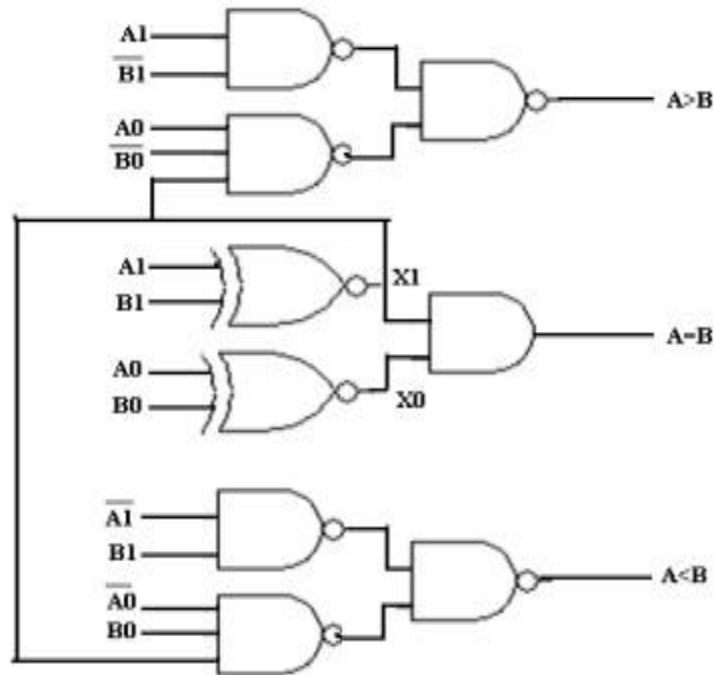
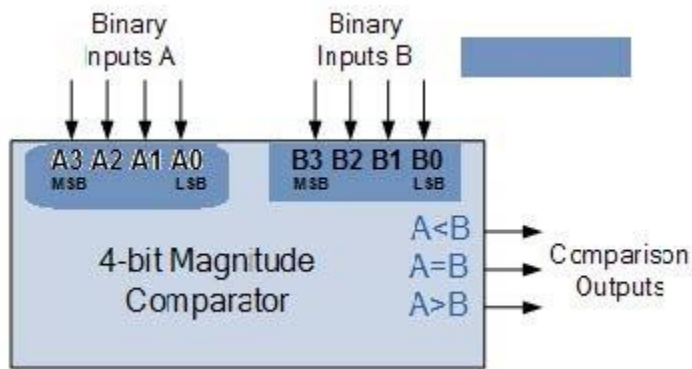


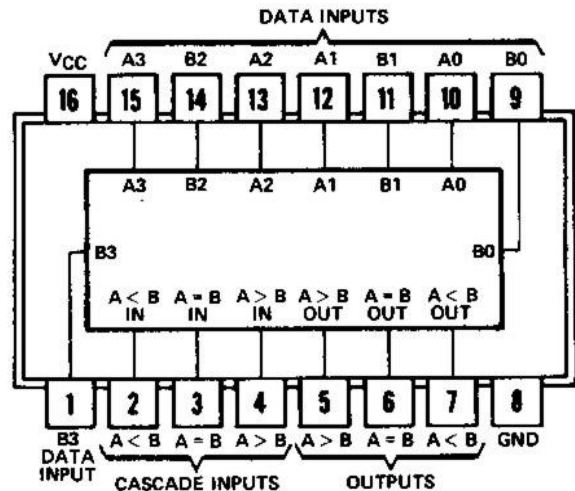
Figure 5: Logic Diagram of 2-bit Comparator

#### **4-bit Magnitude Comparator:**

A comparator used to compare two 4-bit words. The two 4-bit numbers are word A:  $A_3A_2A_1A_0$ , and word B:  $B_3B_2B_1B_0$ . So the circuit has 8 inputs and 3 binary outputs:  $A > B$ ,  $A = B$  and  $A < B$ .



(a) Block diagram



(b) Pin description for IC 7485

Figure 6

Figure 6 shows the block diagram and pin configuration of IC 7485 for 4-bit magnitude comparator. Three inputs are available for cascading comparators.

This comparator generates an output of 1 at one of three comparison outputs such that:

- If word A is bigger than word B;  $A > B$  output (pin 5) is “1”,
- If word A is smaller than word B;  $A < B$  output (pin 7) is “1”,
- If word A is equal to word B;  $A = B$  output (pin 6) is “1”.

This IC can be used to compare two 4-bit binary words by grounding the cascade inputs  $A < B$  (pin 2) and  $A > B$  (pin 4) and connecting the cascade input  $A = B$  (pin 3) to Vcc.

### How does a 4-bit comparator work?

#### Equality:

Word A equal word B iff:  $A_3=B_3, A_2=B_2, A_1=B_1, A_0=B_0$ .

#### Inequality:

- If  $A_3 = 1$  and  $B_3 = 0$ , then A is greater than B ( $A > B$ ). Or
- If  $A_3$  and  $B_3$  are equal, and if  $A_2 = 1$  and  $B_2 = 0$ , then  $A > B$ . Or
- If  $A_3$  and  $B_3$  are equal &  $A_2$  and  $B_2$  are equal, and if  $A_1 = 1$ , and  $B_1 = 0$ , then  $A > B$ . Or
- If  $A_3$  and  $B_3$  are equal,  $A_2$  and  $B_2$  are equal and  $A_1$  and  $B_1$  are equal, and if  $A_0 = 1$  and  $B_0 = 0$ , then  $A > B$ .
- If  $A_3 = 0$  and  $B_3 = 1$ , then A is less than B ( $A < B$ ). Or
- If  $A_3$  and  $B_3$  are equal, and if  $A_2 = 0$  and  $B_2 = 1$ , then  $A < B$ . Or
- If  $A_3$  and  $B_3$  are equal &  $A_2$  and  $B_2$  are equal, and if  $A_1 = 0$ , and  $B_1 = 1$ , then  $A < B$ . Or
- If  $A_3$  and  $B_3$  are equal,  $A_2$  and  $B_2$  are equal and  $A_1$  and  $B_1$  are equal, and if  $A_0 = 0$  and  $B_0 = 1$ , then  $A < B$ .

### Part A: Lab Tasks

#### Procedure:

1. Check all the components for their working.
2. Insert the appropriate ICs into the IC base.
3. Make connections as shown in the circuit diagram in figure 5.

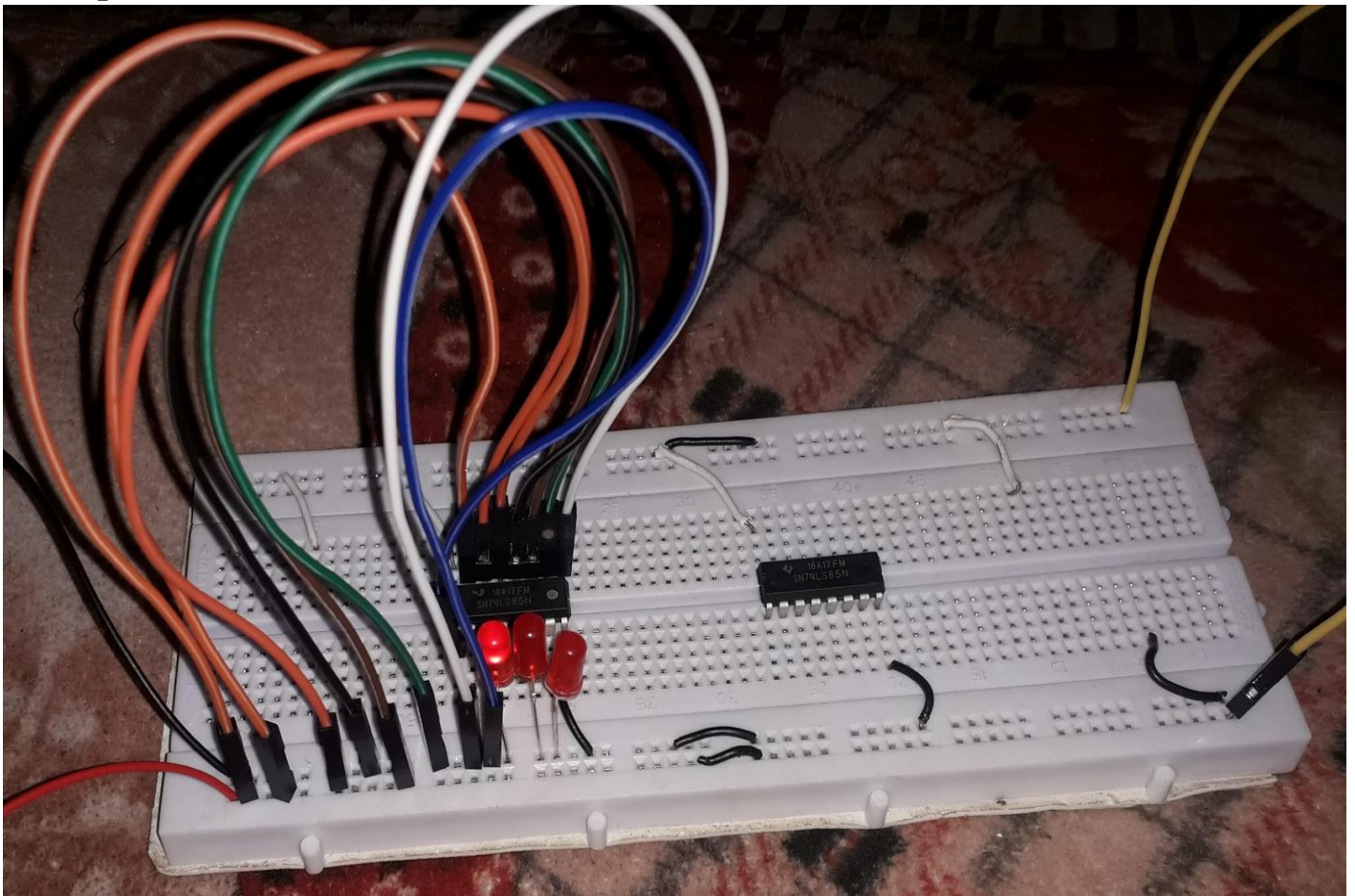


4. Verify the Truth Table and observe the outputs.
5. Repeat the same steps but for the circuit diagram in figure 6 and apply inputs in the following table.  
Record the outputs for the given values of A and B.

**TRUTH TABLE FOR 4 BITS CAMPARITOR:-**

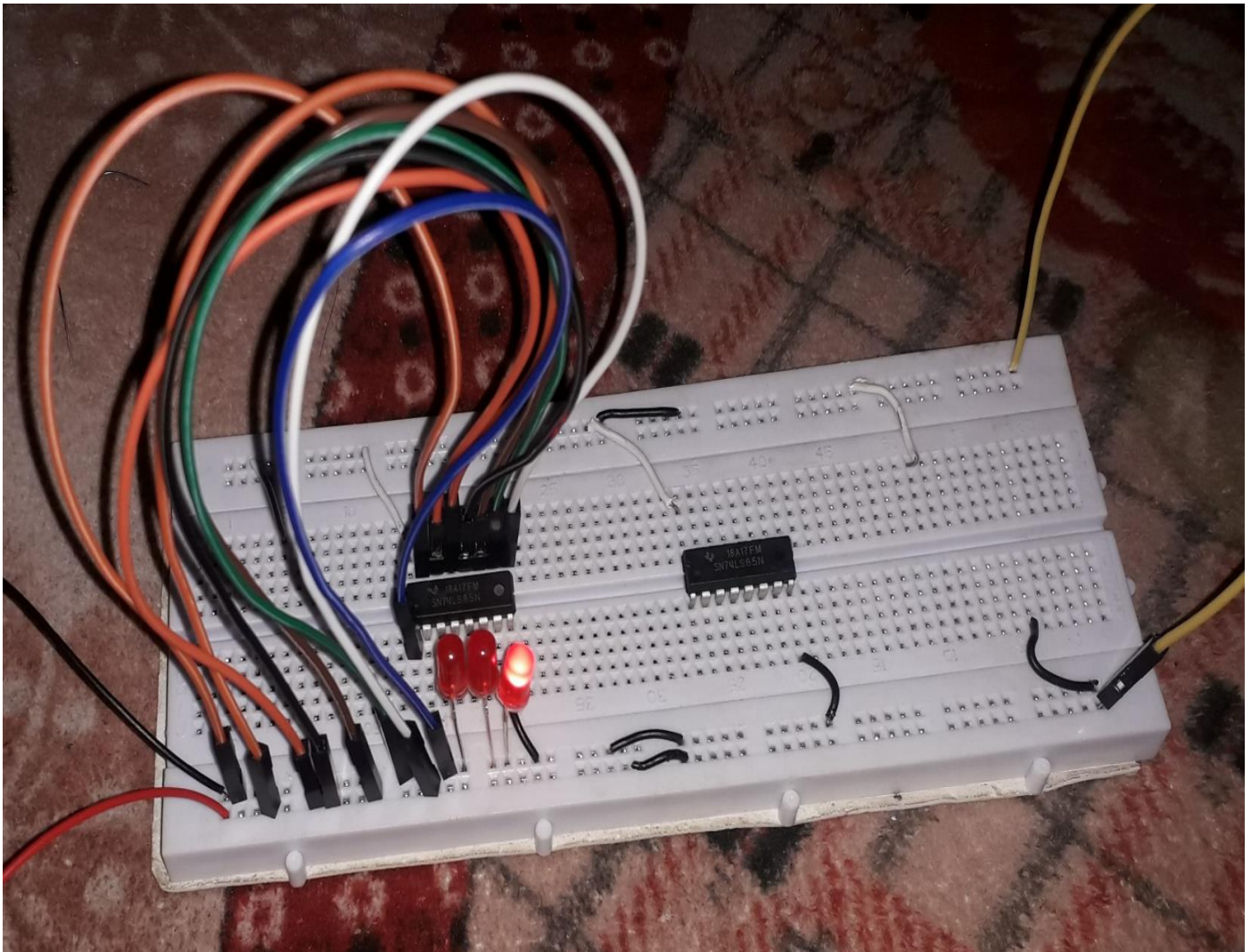
A	B	OUTPUTS
1001	0110	A>B
1100	1110	A<B
0011	0101	A<B
0101	0101	A=B

**Practical experimental circuit:-**  
**For input (A=1001 and B=0110)**

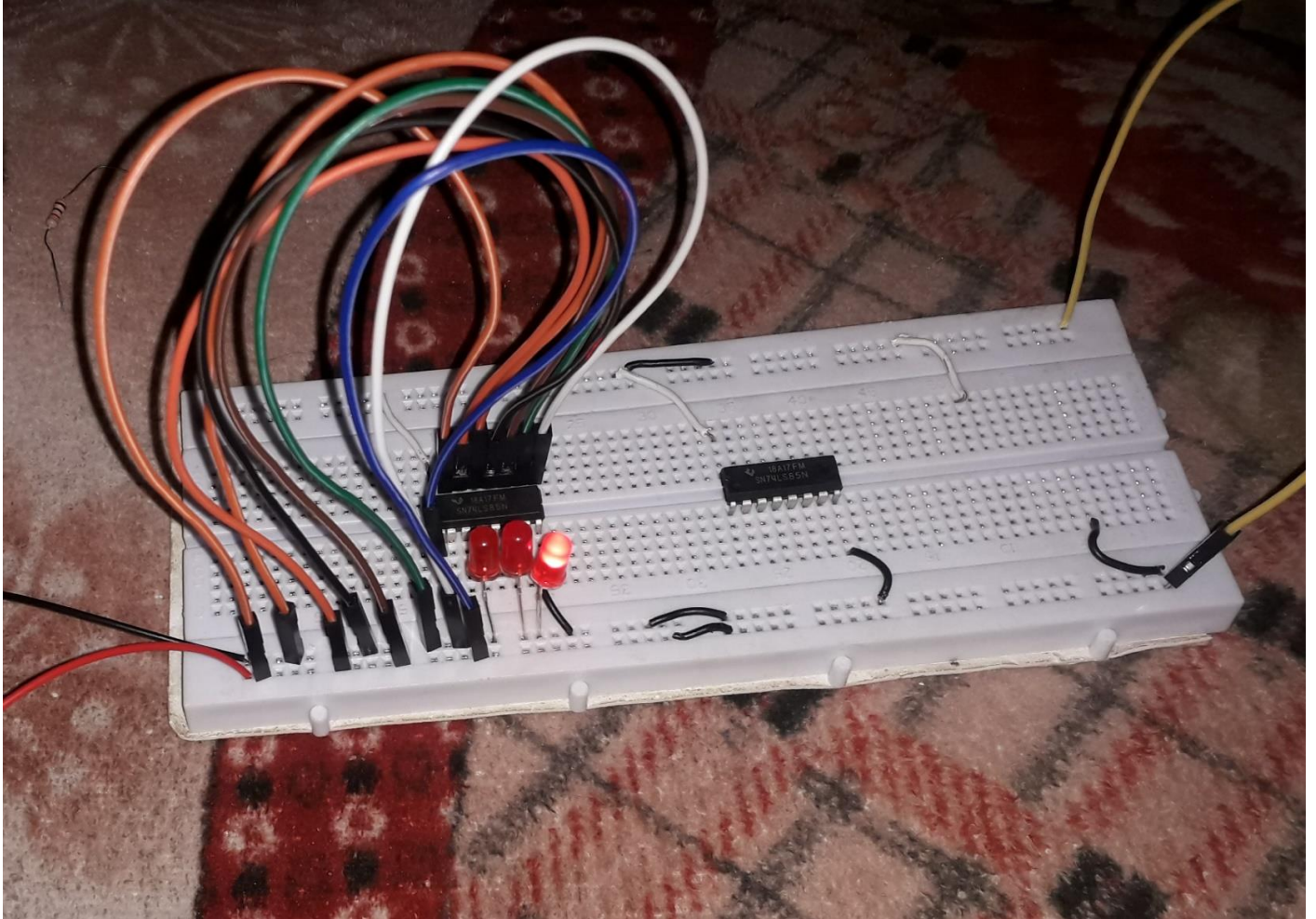




**Practical experimental circuit:-  
For input (A=1100 and B=1110)**

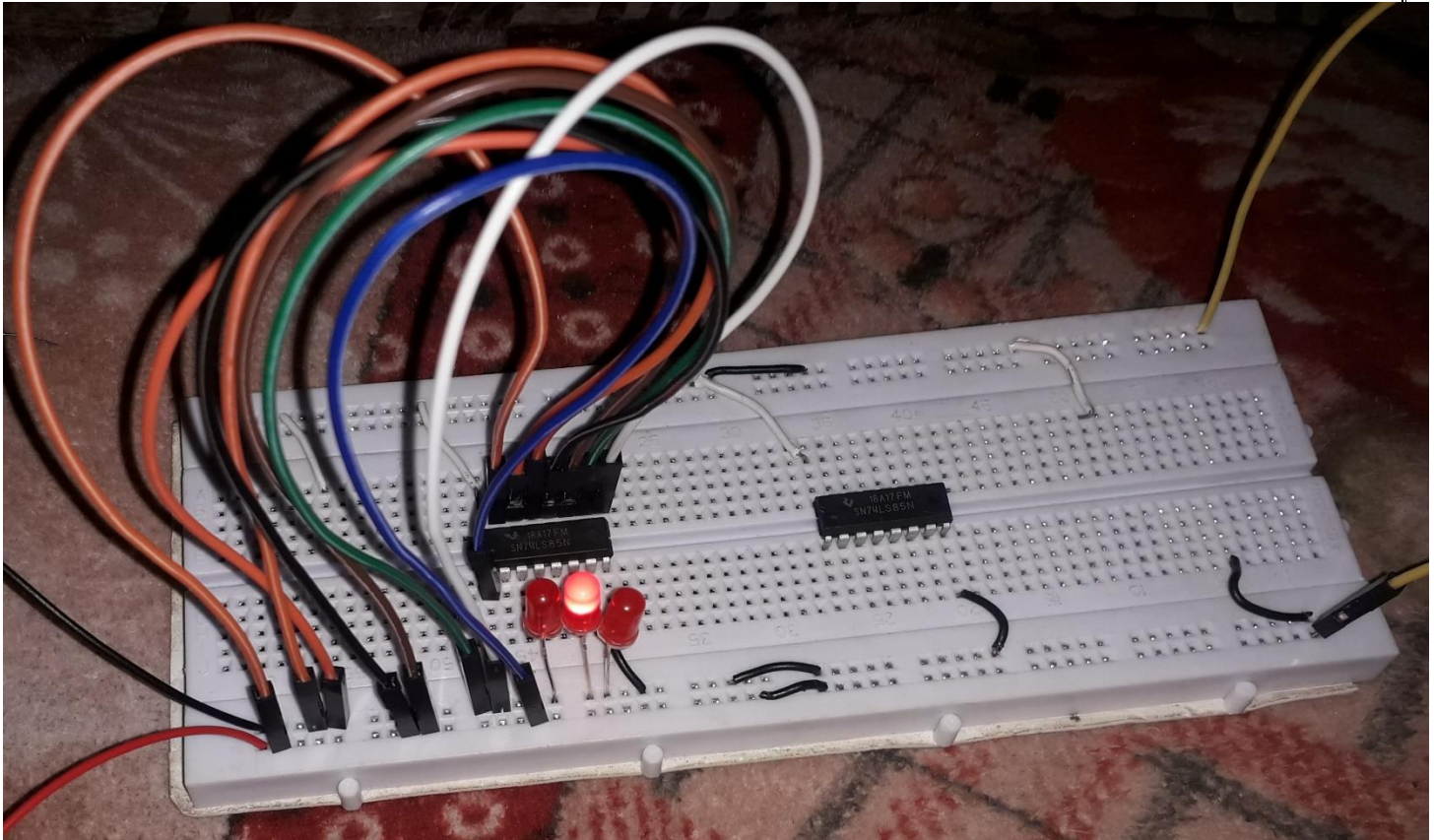


**Practical experimental circuit:-  
For input (A=0011 and B=0101)**





**Practical experimental circuit:-**  
**For input (A=0101 and B=0101)**



**Conclusions:** hence: 1,2 and 4 Magnitude comparator is studied.