University of Engineering & Technology Peshawar

Programme: B.Sc. Computer Systems Engineering

Semester: 3rd Semester

Paper: Digital Logic Design **Date: January 6, 2021**

Exam Type: Midterm

Allowed Time: 120 Minutes	**Max Marks: 30**
Student's Name:	**Student's Registration:**
Student's Signature:	

Instructions:

1- This exam is OPEN books/notes/Internet.
2- Sharing of books, notes and other materials during this exam is not permitted.
3- Answer ALL questions.
4- There are 9 questions in total. Some questions are harder than others. Answer the easy ones first to maximize your score.
5- Questions will not be interpreted during the exam.

Marks

Q. 1 Convert decimal +61 and +27 to binary using the signed-2's complement representation and enough digits to accommodate the numbers. Then perform the binary equivalent of (+27) + (-61), (-27) + (+61) and (-27) + (-61). Convert the answers back to decimal and verify that they are correct. 6

Q. 2 At the least how many bits are needed to represent **-18** (read as minus 18) in **3**

i. Sign-magnitude system
ii. 1's complement system
iii. 2's complement system

Q. 3 In the following table fill the column B with an appropriate decimal number corresponding to the equivalent unsigned binary number given in column A. **2**

Column A	Column B
000	
001	
010	
011	
100	
101	
110	
111	

Q. 4 In the following table fill the column B with an appropriate decimal number corresponding to the equivalent 1's complement number given in column A. **2**

Column A	Column B
000	
001	
010	
011	
100	
101	
110	
111	

Q. 5 In the following table fill the column B with an appropriate decimal number corresponding to the equivalent 2's complement number given in column A. **2**

Column A	Column B
000	
001	
010	
011	
100	
101	
110	
111	

Q. 6 From the following truth table, directly write the Boolean expression for: **4**

i. $F(A,B,C)$ in both the canonical forms.

ii. $\overline{F(A,B,C)}$ in both the canonical forms.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Q. 7 Write the truth table for the following Boolean expression/function: **2**

$$F(A,B,C) = \overline{B}.C + A.(\overline{B}+C) + \overline{A}.\overline{C}$$

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Q. 8 The following gates are available and the unit price is also listed. **4**

- Price of 3-input AND gate = $ 2/-
- Price of 2-input OR gate = $ 2/-
- Price of NOT gate = $ 1/-

Implement the following Boolean function using the above gates. Draw its logic diagram and calculate its cost.

$$F(X,Y,Z)= \Sigma_m(1, 7)$$

Q. 9 Design a 3-bit adder-subtractor circuit using 1-bit binary Full adders and any necessary additional logic gates. The circuit has a mode/control input bit, **M**, that controls its operation. Specifically, when **M=0**, the circuit becomes a 3-bit adder, and when **M=1**, the circuit becomes a 3-bit subtractor that performs the operation A plus the 2's complement of B, where A and B are two 3-bit binary numbers. **5**

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