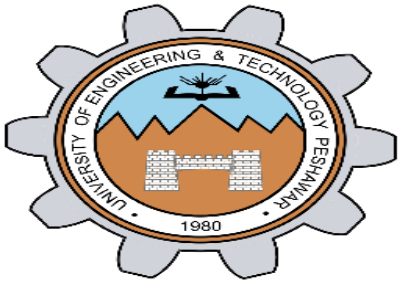
LAB REPORT NO 9



CSE-202L Digital logic

design lab

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Class Section: A

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Submitted to:

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Data:(7,2,2021)

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Lab # 9

Aim:

Verification of state tables of R-S and D flip-flops (with PRESET and CLEAR inputs) using NAND gates.

Apparatus:

IC 7410 (3-input NAND Gate).

Theory:

In case of sequential circuits the effect of all previous inputs on the outputs is represented by a state of the circuit. Thus, the output of the circuit at any time depends upon its current state and the input. These also determine the next state of the circuit. The relationship that exists among the inputs, outputs, present and next states can be specified by either the state table or the state diagram. The state table representation of a sequential circuit consists of three sections labelled present state, next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.

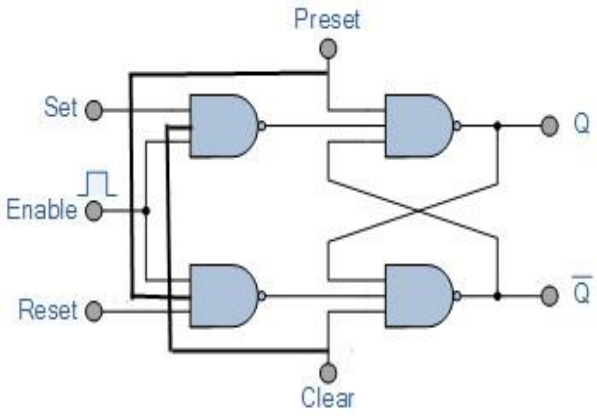
Flip-Flop:

The basic 1-bit digital memory circuit is known as flip-flop. It can store either 0 or 1. Flip-flops are classifieds according to the number of inputs.

R-S Latch vs R-S Flip-Flop:

The circuit is similar to R-S latch except enable signal is replaced by clock pulse.

Logic Diagram:



Truth Table:

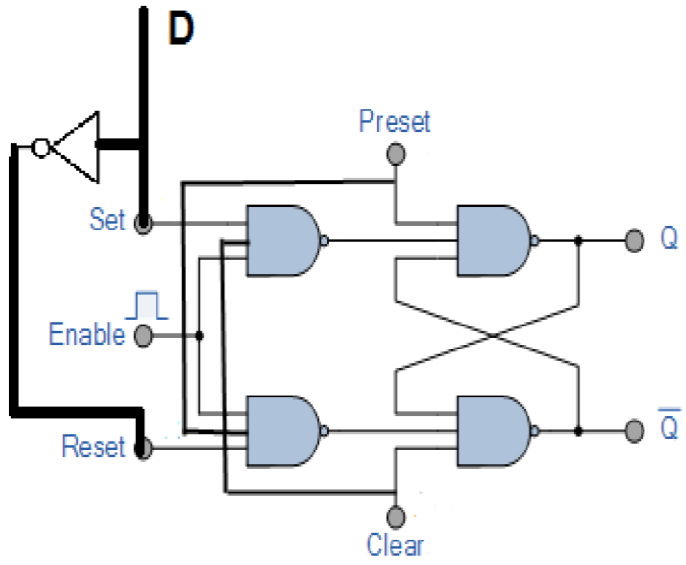
EN	S	R	PRE	CLR	Q(t+1)
x	x	x	0	1	1 (Set)
x	x	x	1	0	0 (Reset)
0	x	x	1	1	Qt (NC)
1	1	0	1	1	1 (Set)
1	0	1	1	1	0 (Reset)
1	0	0	1	1	Qt (NC)
1	1	1	1	1	Indeterminate

D Flip-Flop:

A D flip-flop has a single data input. This type of flip-flop is obtained from the R-S flip-flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked R-S flip-flop is known as D flip-flop and is shown below. From the truth table of R-S flip-flop we see that the output of the R-S flip-flop is in unpredictable state when the inputs are high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other.

Logic Diagram:

Truth Table:



EN	D	PRE	CLR	Q(t+1)
x	x	0	1	1 (Set)
x	x	1	0	0 (Reset)
0	x	1	1	Qt (NC)
1	0	1	1	0 (Reset)
1	1	1	1	1 (Set)

Procedure:

1. Connections are made as per circuit diagram.
2. Verify truth- tables for various combinations of input.

Precaution:

1. All the ICs should be checked before using the apparatus.
2. All LEDs should be checked.
3. All connections should be tight.
4. Always connect GROUND first and then VCC.
5. The circuit should be off before changing the connections.
6. After completing the experiment switch off the supply to apparatus.

Pre Lab Questions:

1) Differentiate between combinational and sequential circuits.

Ans. A circuit whose output is dependent only on the inputs at that instant is called combinational circuit. And a circuit whose output is dependent on present and past history of the inputs is called sequential circuit.

2) What is a latch?

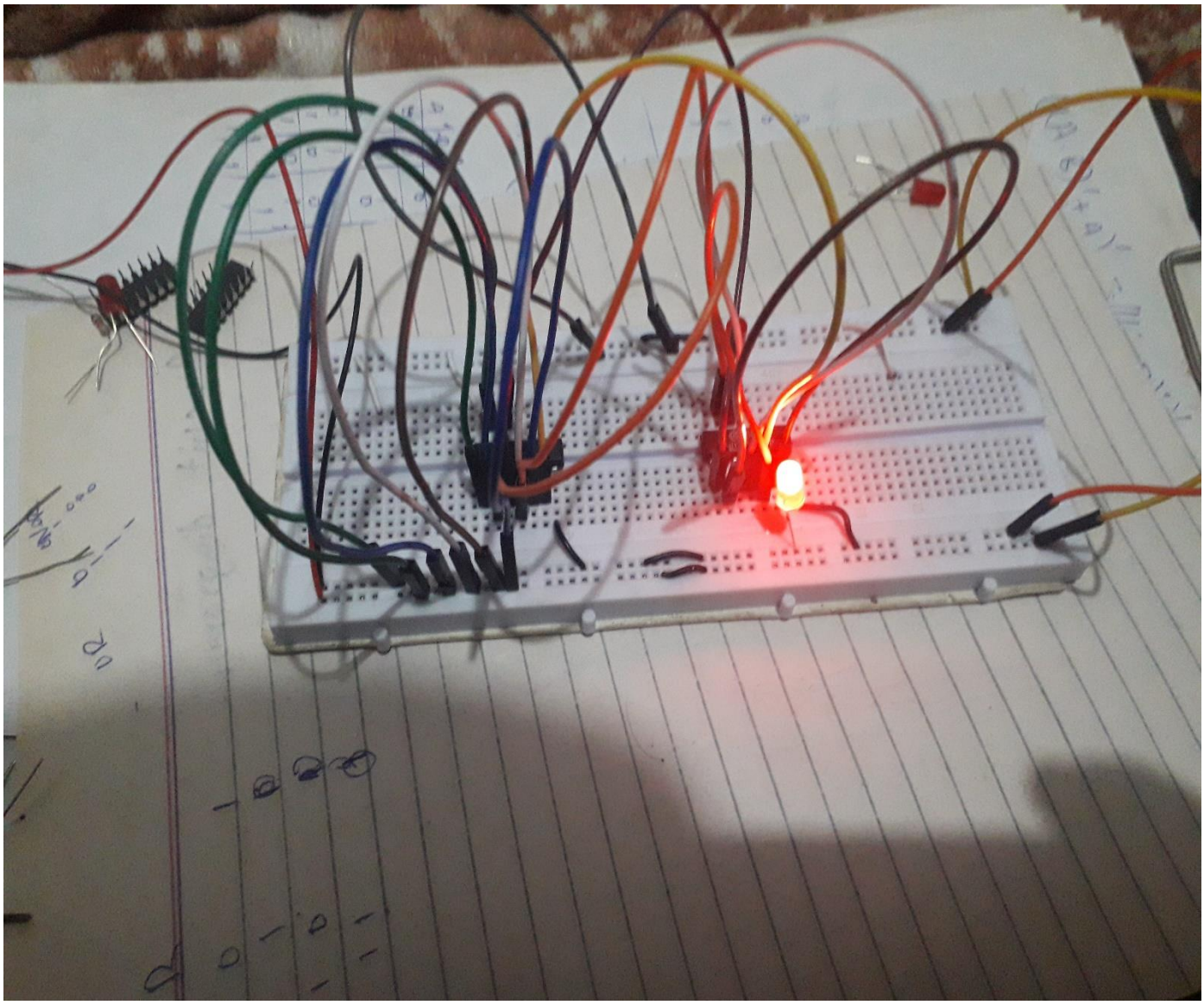
Ans. Storage elements that operate with signal levels are referred to as latches.

3) What is a flip-flop?

Ans. Storage elements controlled by clock transitions are called flip-flops.

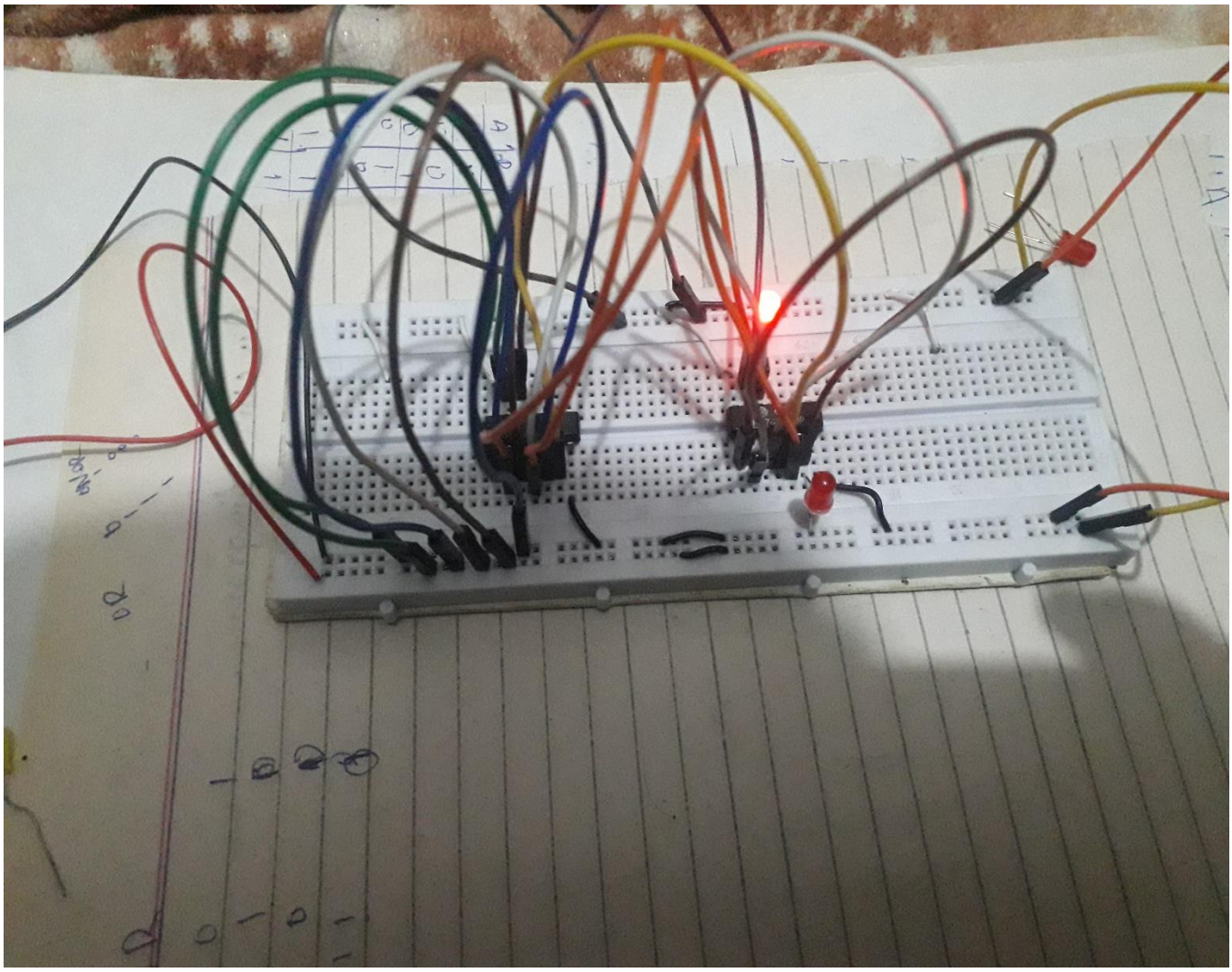
R-S Latch:-

For input: (EN=1, SET=0, RE=1, PRE=1, and CL=1)



R-S Latch:-

For input: (EN=1, SET=0, RE=0, PRE=1, and CL=1)



D Flip-Flop:

For input: (EN=1,S=1,D=0 and RE=1)