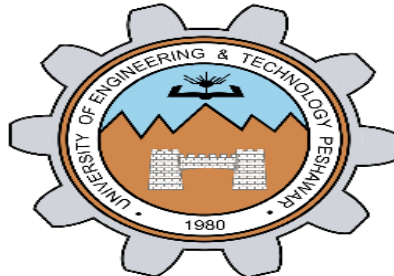


LAB REPORT NO 6



CSE-202L Digital logic design lab

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Registration No:- **19PWCSE1801**

Class Section: A

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Submitted to:

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Data:(15,1,2021)

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Lab 6

DECODER AND ENCODER

OBJECTIVES

After completing this experiment you will be able to:

- Design and construct Decoder and Encoder
- Verify their truth tables using logic gates

COMPONENTS REQUIRED

- Two 7410, 3 I/P NAND gate
- Three 7432, 2 I/P OR gate
- 7404 hex inverter

THEORY:-

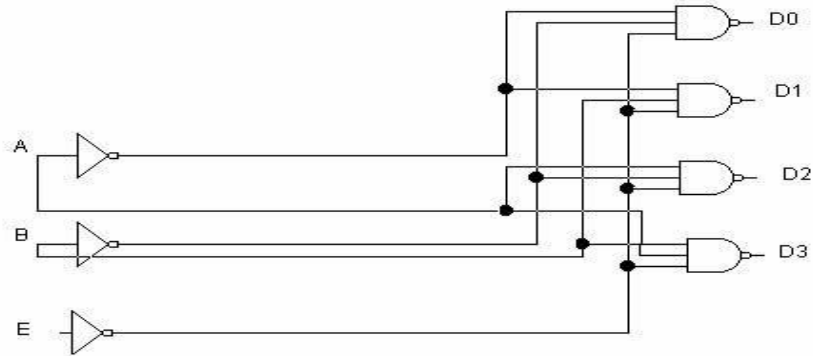
DECODER:

A Decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of Decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out $2^n - 1$.

ENCODER:

An Encoder is a digital circuit that perform inverse operation of a Decoder. An Encoder has 2^n input lines and n output lines. In Encoder the output lines generates the binary code corresponding to the input value. In octal to binary Encoder it has eight inputs, one for each octal digit and three outputs that generate the corresponding binary code. In Encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguity that when all inputs are zero the outputs are zero. The zero outputs can also be generated when $D_0 = 1$.

LOGIC DIAGRAM FOR DECODER

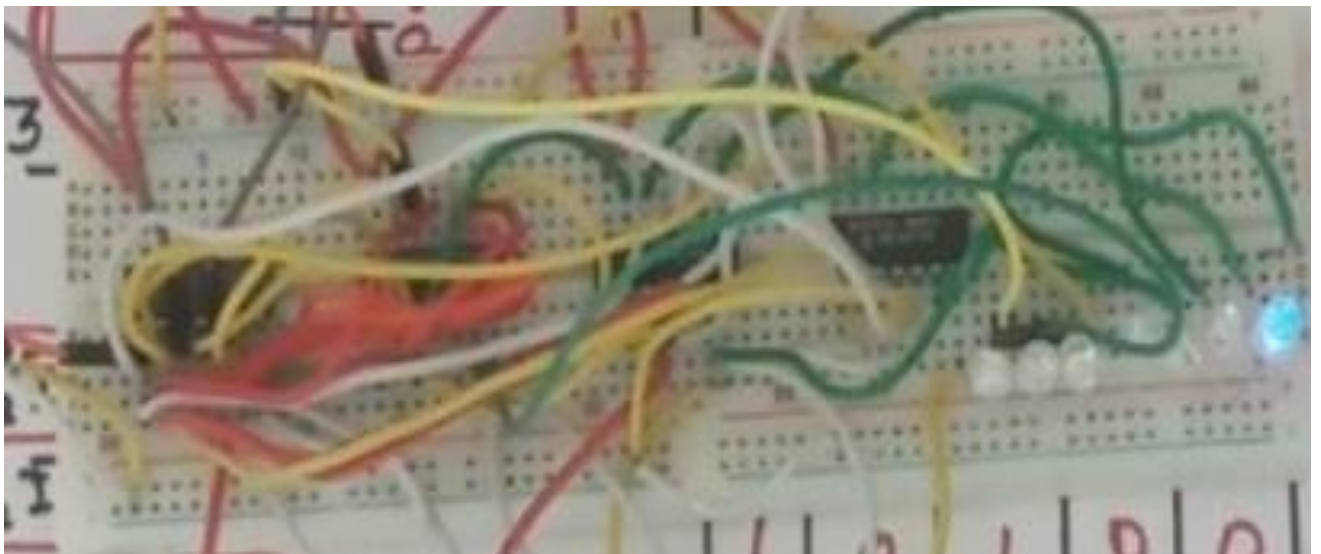


$$D0 = (A'B'E)'. \quad D1 = (A'BE')'. \quad D2 = (AB'E)'. \quad D3 = (ABE')'$$

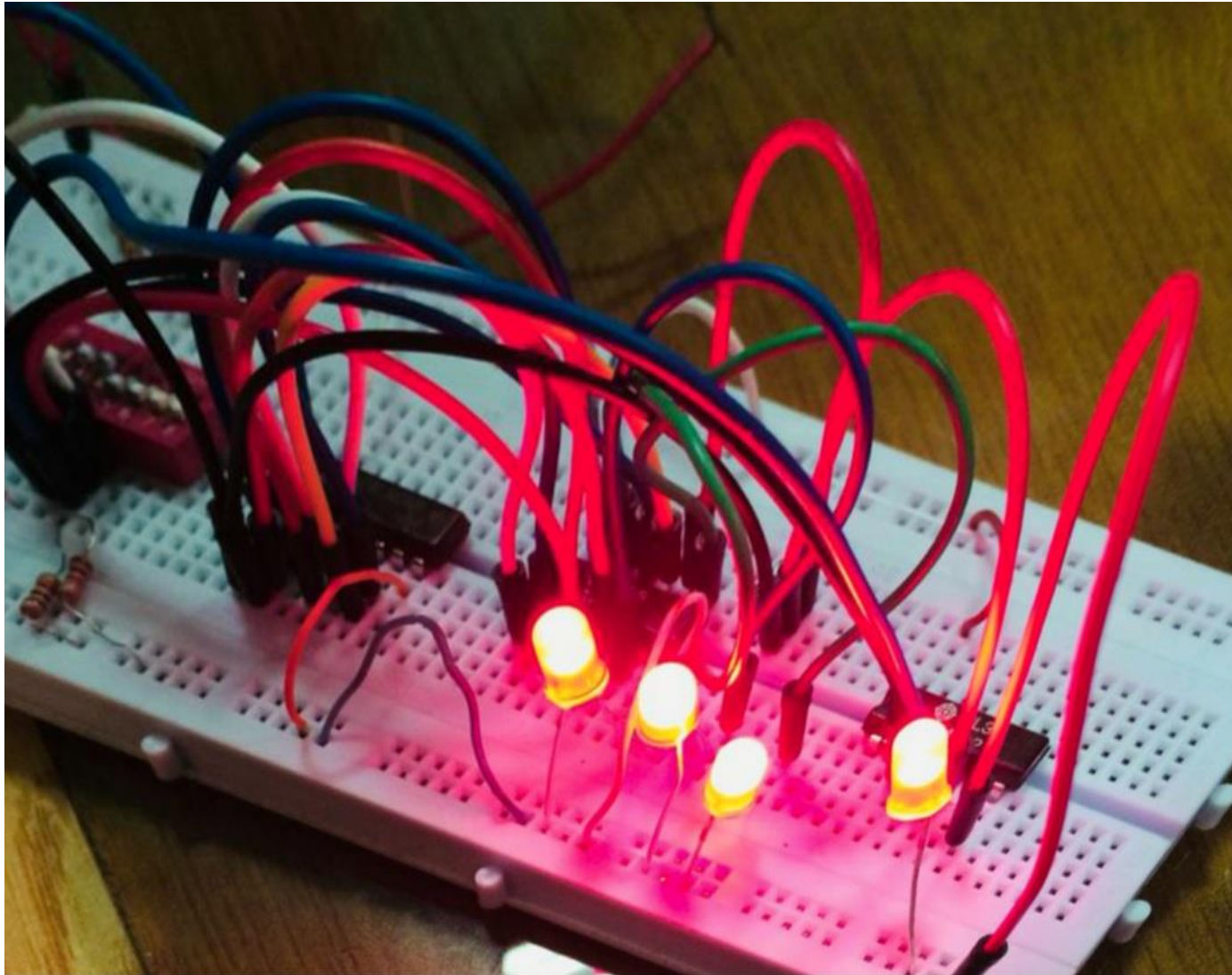
TRUTH TABLE

INPUT			OUTPUT			
E	A	B	D0	D1	D2	D3
1	x	x	x	x	x	x
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

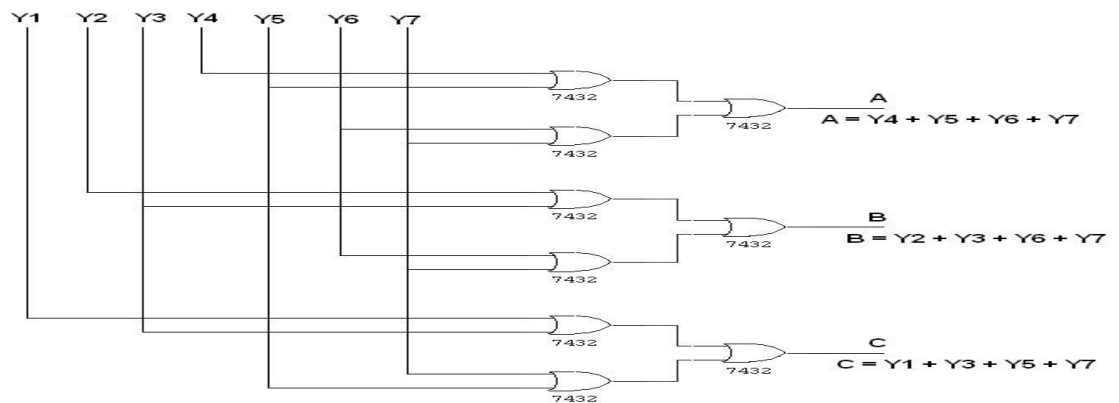
PRACTICAL DIAGRAM FOR DECODER:-



PRACTICAL DIAGRAM FOR ENCODER:-



LOGIC DIAGRAM FOR ENCODER:-



TRUTH TABLE

INPUT							OUTPUT		
Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

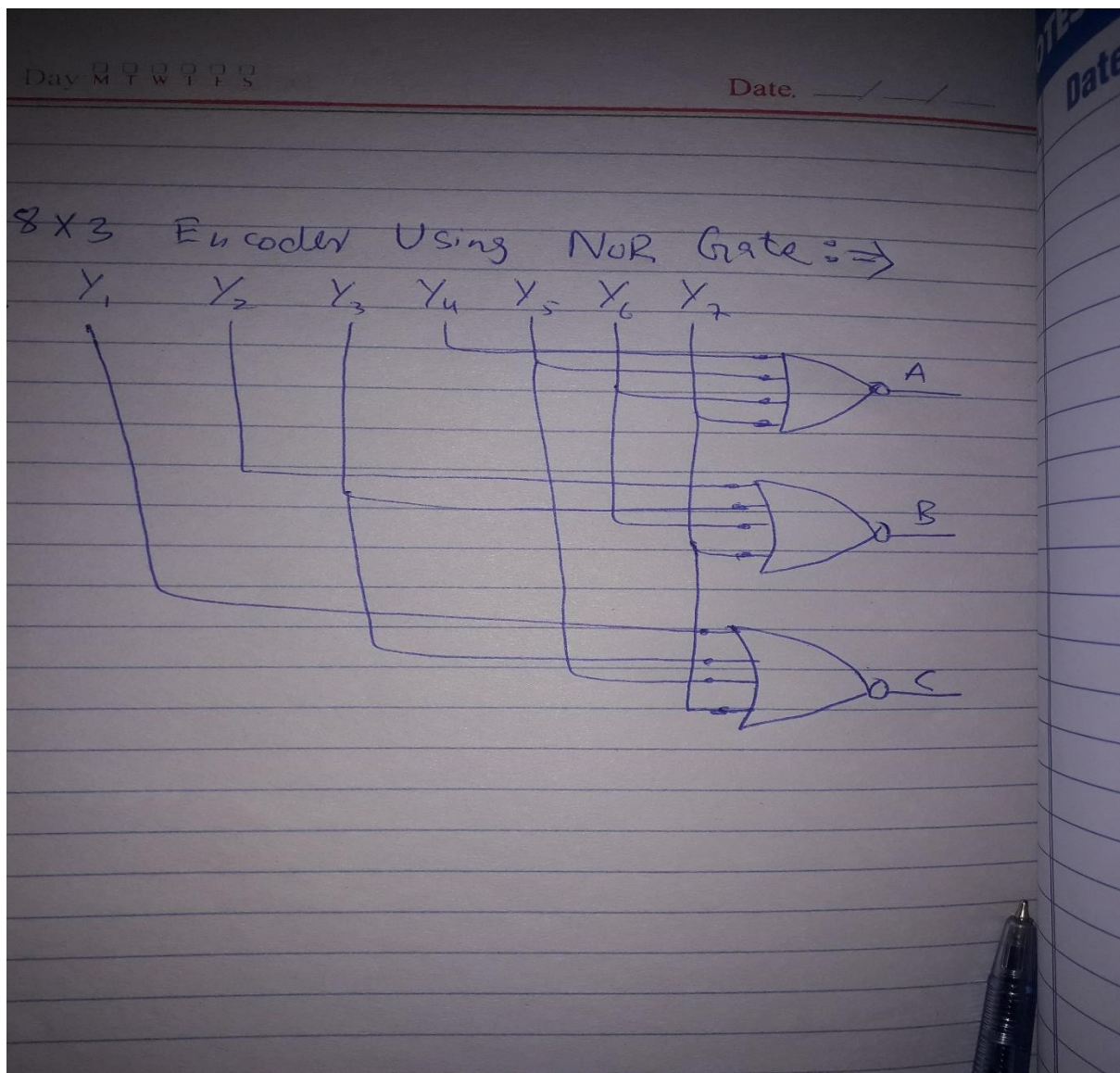
PROCEDURE

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

REVIEW QUESTIONS

- Design an Encoder using NOR gates only.

Answer:-



TRUTH TABLE:-

Input								Output		
Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
0	1	1	1	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	0	0	1
1	1	0	1	1	1	1	1	0	1	0
1	1	1	0	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	0	1	1	1	0	1
1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1

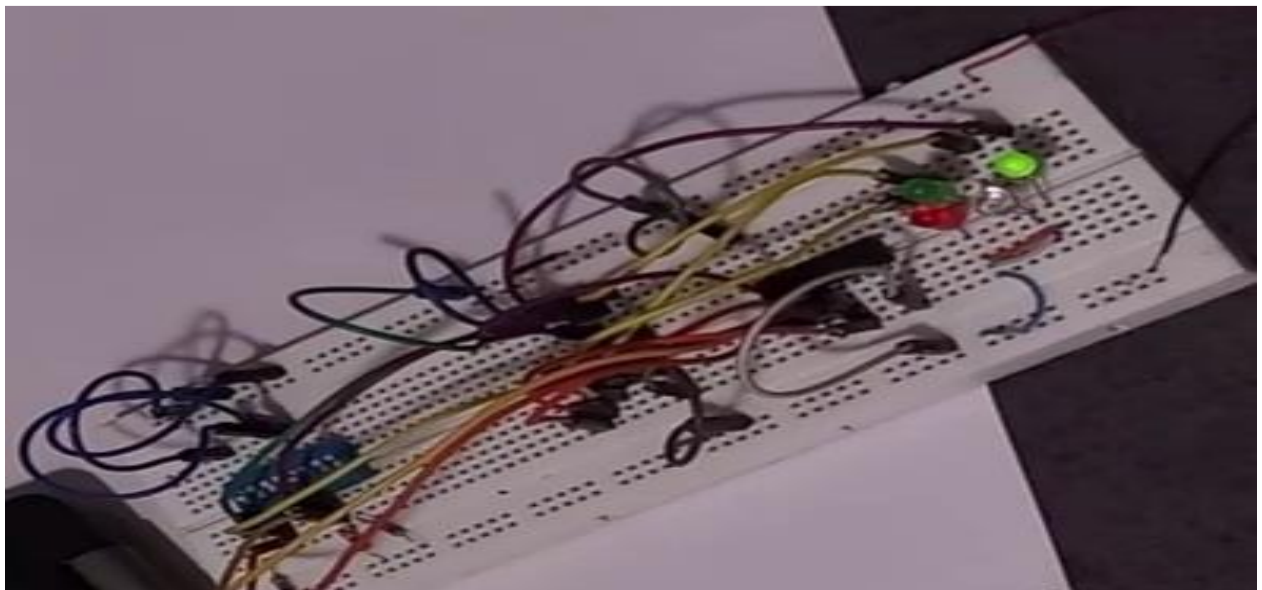
Q:-What will be the output of the Decoder circuit if NAND gates are replaced by AND gates?

Answer:-

The result of replacing NAND with AND gate will be inverted, as I show in the truth table.

D0 = (A'B'E'). D1 = (A'BE'). D2 = (AB'E'). D3 = (ABE')

INPUT			OUTPUT			
E	A	B	D0	D1	D2	D3
1	x	x	x	x	x	x
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1



- **What is the purpose of enable input in Decoder?**

Answer:-

A standard decoder typically has an additional input called Enable. Output is only generated when the Enable input has value 1; otherwise, all outputs are 0. Only a small change in the implementation is required, e.g. the Enable input is fed into the AND gates which produce the outputs.

- **Design a 3x8 Decoder using two 2x4 Decoders (74LS139).**

Answer:-

