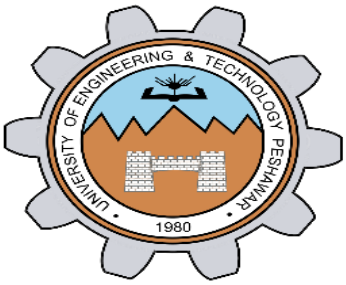
Lab report no 3



Fall 2022

CSE-308L Digital Systems Design Lab

Submitted By

Names	**Registration No**
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Section: **A**

Date:14,4,22

Submitted To: MAM. Madiha Sher

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LAB 03
INTRODUCTION TO XILINX ISE AND SPARTAN 6 BOARD

Objectives:

- Introduction to FPGA
- Introduction to Xilinx ISE

Software name:

Xilinx ISE

FPGA:

FPGAs are programmable digital logic circuits. It can be programmed to do almost any digital function. There are at least 5 companies making FPGAs in the world. Xilinx is the biggest name in the FPGA world.
The FPGA kits available in the lab are **Mimas V2 Spartan 6 FPGA Development Board**.

XILINX:

The Integrated Software Environment (ISE™) is the Xilinx® design software suite that allows you to take your design from design entry through Xilinx device programming. The ISE Project Navigator manages and processes your design through the following steps in the ISE design flow.

The code can be synthesized by the following steps.

1. First of all the Verilog module is created.
2. USER DEFINED CONSTRAINT file is created and added in the project
3. Verilog code is then synthesized
4. Design is implemented

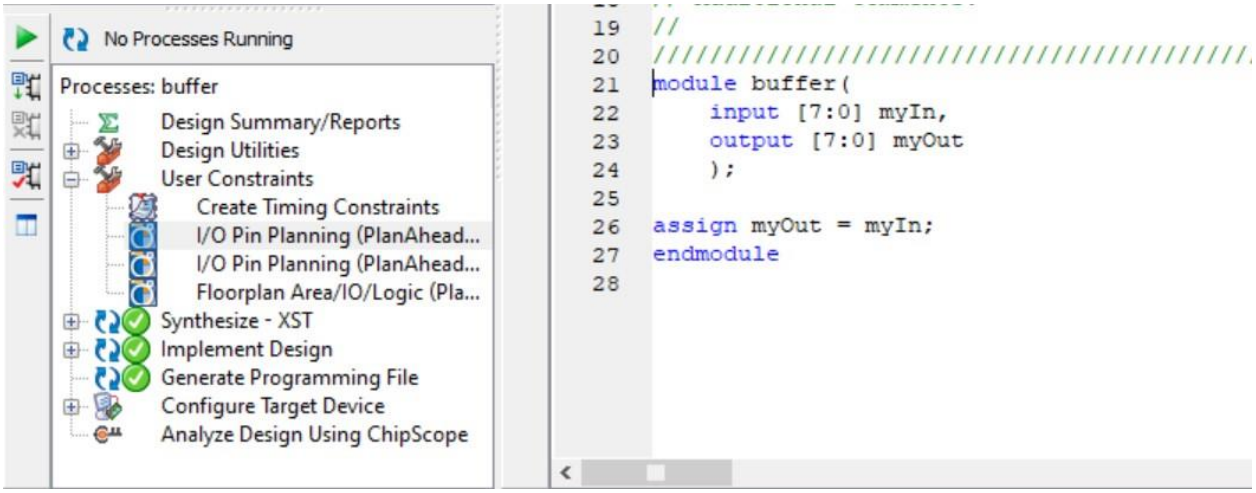
5. Programming file is then generated as binary file which can be downloaded into the FPGA The Process windows has all the above options
6. Programming file is downloaded to FPGA using Mimas V2 Configuration tool for windows

Lab Tasks:

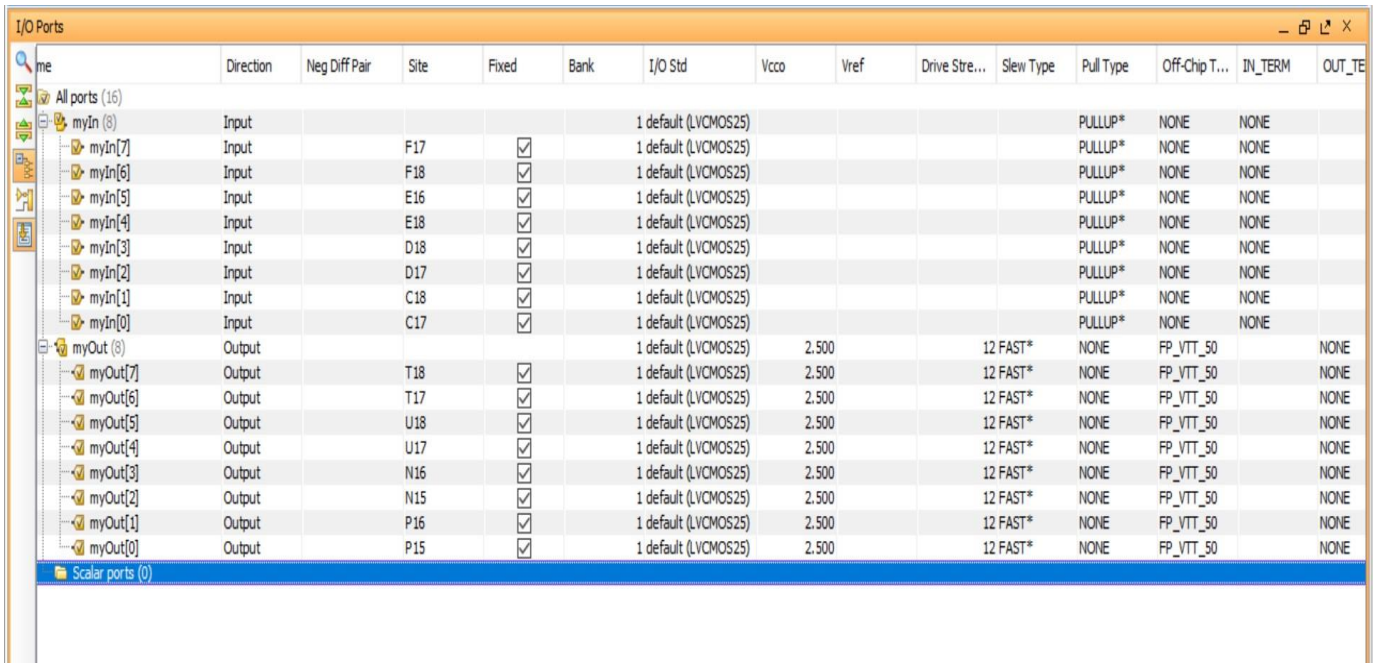
1- **Develop a program to control on Board LEDs using on board available switches.**

Buffer

Code :



I/O PORTS:



me	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Stre...	Slew Type	Pull Type	Off-Chip T...	IN_TERM	OUT_TE
All ports (16)														
myIn (8)	Input					1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myIn[7]	Input		F17	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myIn[6]	Input		F18	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myIn[5]	Input		E16	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myIn[4]	Input		E18	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myIn[3]	Input		D18	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myIn[2]	Input		D17	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myIn[1]	Input		C18	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myIn[0]	Input		C17	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	
myOut (8)	Output					1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
myOut[7]	Output		T18	☑		1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
myOut[6]	Output		T17	☑		1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
myOut[5]	Output		U18	☑		1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
myOut[4]	Output		U17	☑		1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
myOut[3]	Output		N16	☑		1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
myOut[2]	Output		N15	☑		1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
myOut[1]	Output		P16	☑		1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
myOut[0]	Output		P15	☑		1 default (LVCMOS25)	2.500		12	FAST*	NONE	FP_VTT_50		NONE
Scalar ports (0)														

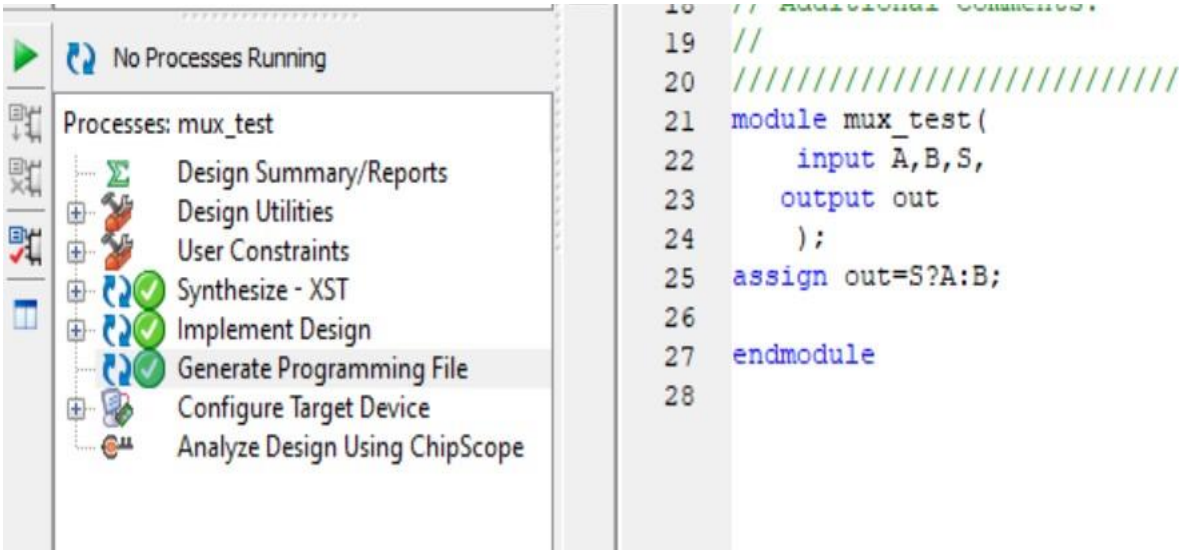
UCF File:

```
1
2
3   NET "myIn[0]" LOC = C17;
4   NET "myIn[1]" LOC = C18;
5   NET "myIn[2]" LOC = D17;
6   NET "myIn[3]" LOC = D18;
7   NET "myIn[4]" LOC = E18;
8   NET "myIn[5]" LOC = E16;
9   NET "myIn[6]" LOC = F18;
10  NET "myIn[7]" LOC = F17;
11
12
13  NET "myOut[0]" LOC = P15;
14  NET "myOut[1]" LOC = P16;
15  NET "myOut[2]" LOC = N15;
16  NET "myOut[3]" LOC = N16;
17  NET "myOut[4]" LOC = U17;
18  NET "myOut[5]" LOC = U18;
19  NET "myOut[6]" LOC = T17;
20  NET "myOut[7]" LOC = T18;
21
22
23  NET "myOut[7]" SLEW = FAST;
24  NET "myOut[6]" SLEW = FAST;
25  NET "myOut[5]" SLEW = FAST;
26  NET "myOut[4]" SLEW = FAST;
27  NET "myOut[3]" SLEW = FAST;
28  NET "myOut[2]" SLEW = FAST;
29  NET "myOut[1]" SLEW = FAST;
30  NET "myOut[0]" SLEW = FAST;
31  NET "myIn[7]" PULLUP;
32  NET "myIn[6]" PULLUP;
33  NET "myIn[5]" PULLUP;
34  NET "myIn[4]" PULLUP;
35  NET "myIn[3]" PULLUP;
36  NET "myIn[2]" PULLUP;
37  NET "myIn[1]" PULLUP;
38  NET "myIn[0]" PULLUP;
```

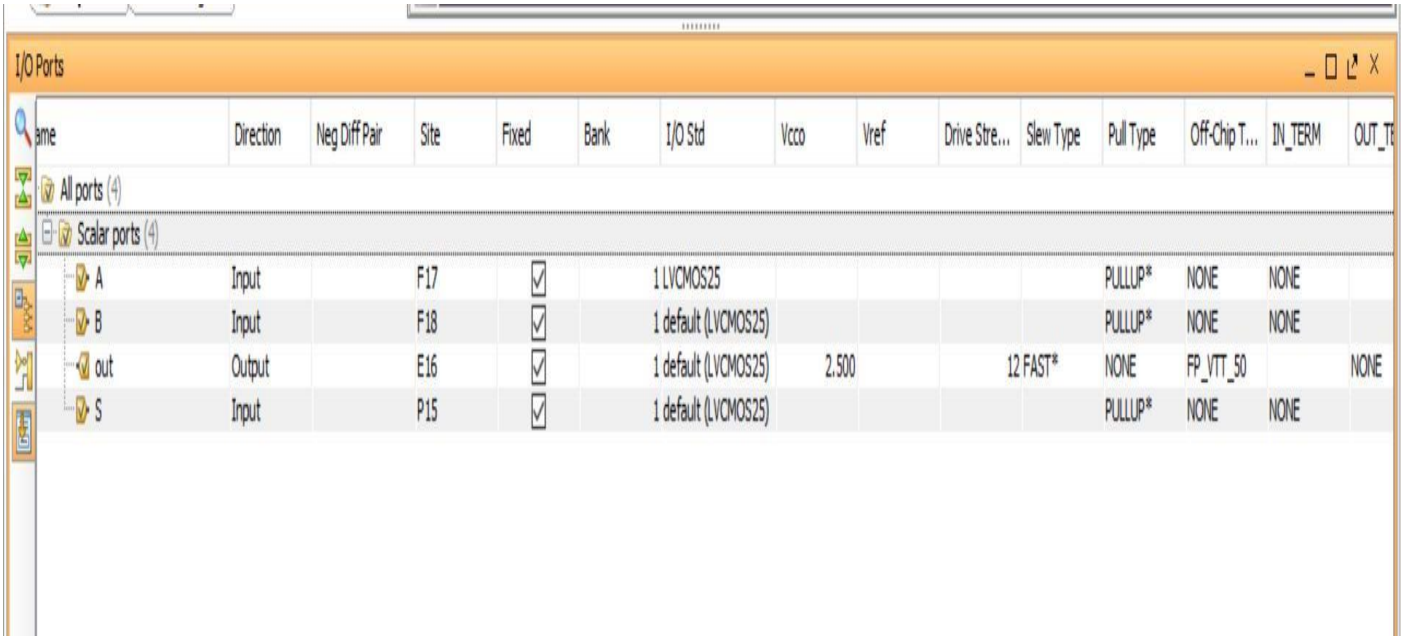
Lab Tasks:

2- **Develop a program that implements a 2x1 multiplexer on the board. Connect the inputs to switches and output to LEDs**.

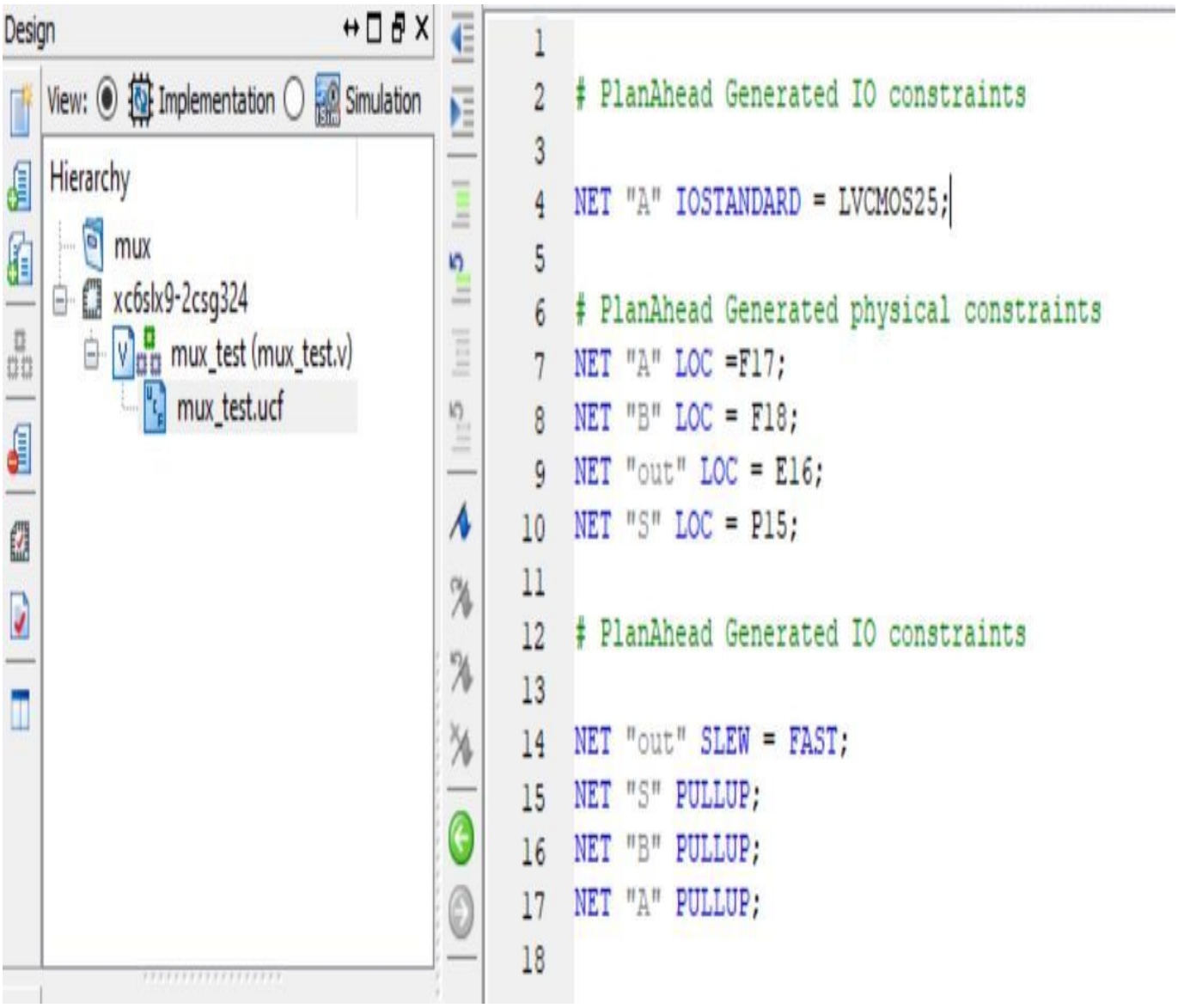
2X1 MUX CODE:-



I/O PORTS:



UCF File:


Design
View: Implementation Simulation
Hierarchy
mux
xc6slx9-2csg324
mux_test (mux_test.v)
mux_test.ucf
1
2 # PlanAhead Generated IO constraints
3
4 NET "A" IOSTANDARD = LVCMOS25;
5
6 # PlanAhead Generated physical constraints
7 NET "A" LOC =F17;
8 NET "B" LOC = F18;
9 NET "out" LOC = E16;
10 NET "S" LOC = P15;
11
12 # PlanAhead Generated IO constraints
13
14 NET "out" SLEW = FAST;
15 NET "S" PULLUP;
16 NET "B" PULLUP;
17 NET "A" PULLUP;
18