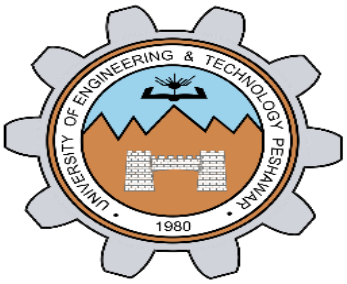
Lab report no 5



Fall 2022

CSE-308L Digital Systems Design Lab

Submitted By

Names	**Registration No**
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Section: **A**

Date:20,5,22

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Lab task (7 segment counter): -

```
module clk_div(clk100MHz,clk1Hz,rst);
input clk100MHz;
input rst;
output reg clk1Hz;
integer count;
always @(posedge clk100MHz)
if(rst)
begin
count=0;
clk1Hz=0;
end
else
begin
count=count+1;
if(count==1000000)
begin
clk1Hz=~clk1Hz;
count = 0;
end
end
endmodule
```

```
module counter(clk100MHz, reset, count);
```

```
        input clk100MHz, reset;
        output [7:0] count;

        reg [7:0] count;
        wire clk1Hz;
  clk_div div(clk100MHz,clk1Hz,reset);
        always @( posedge clk1Hz)
                if(reset)
                        count <= 8'b10000000;
                else
                begin
                        count <= count << 1; //Shift Left (Fill with Zero)
                        count[0] <= count[7];
                end
endmodule

# PlanAhead Generated physical constraints

NET "count[7]" LOC = P15;
NET "count[6]" LOC = P16;
NET "count[5]" LOC = N15;
NET "count[4]" LOC = N16;
NET "count[3]" LOC = U17;
NET "count[2]" LOC = U18;
NET "count[1]" LOC = T17;
```

NET "count[0]" LOC = T18;

NET "clk100MHz" LOC = V10;

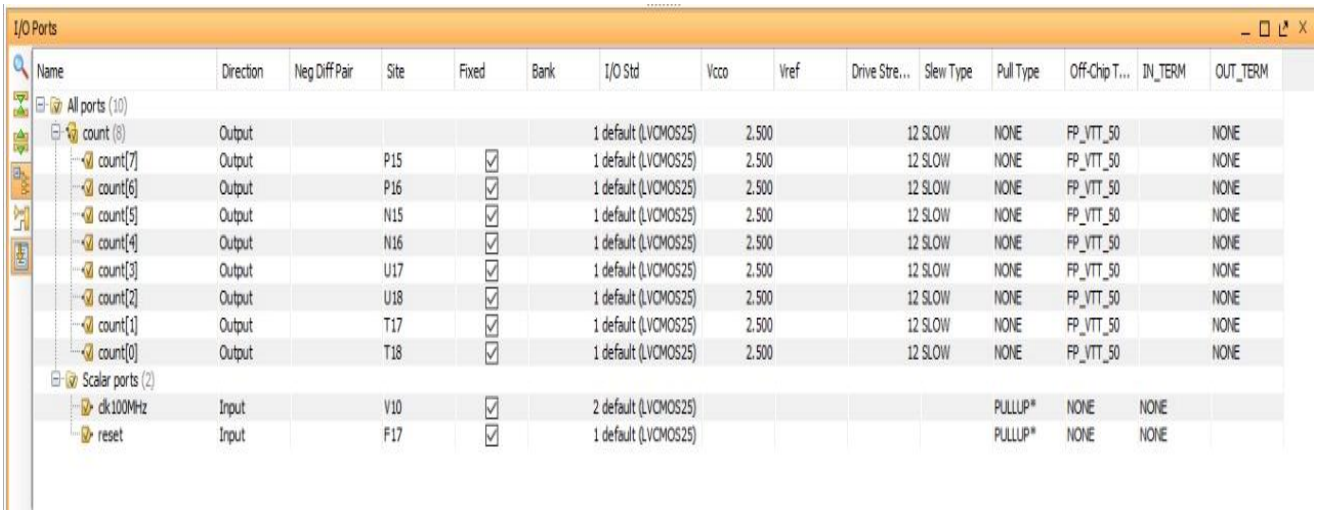
NET "reset" LOC = F17;

PlanAhead Generated IO constraints

NET "clk100MHz" PULLUP;

NET "reset" PULLUP;

Ports outputs: -



Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Stre...	Slew Type	Pull Type	Off-Chip T...	IN_TERM	OUT_TERM
All ports (10)														
count (8)	Output					1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
count[7]	Output		P15	☑		1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
count[6]	Output		P16	☑		1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
count[5]	Output		N15	☑		1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
count[4]	Output		N16	☑		1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
count[3]	Output		U17	☑		1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
count[2]	Output		U18	☑		1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
count[1]	Output		T17	☑		1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
count[0]	Output		T18	☑		1 default (LVCMOS25)	2.500			12 SLOW	NONE	FP_VTT_50		NONE
Scalar ports (2)														
clk100MHz	Input		V10	☑		2 default (LVCMOS25)					PULLUP*	NONE	NONE	
reset	Input		F17	☑		1 default (LVCMOS25)					PULLUP*	NONE	NONE	