

CHAPTER : 15

Integrated Circuits

Technologies

BASIC OPERATIONAL CHARACTERISTICS AND PARAMETERS:-

Example 15-1:

Determine the HIGH - level and LOW level noise margin for CMOS and for TTL by using the information.

Solution :

For 5 V CMOS ,

$$V_{IH(\min)} = 3.5 \text{ V}$$

$$V_{IL(\max)} = 1.5 \text{ V}$$

$$V_{OH(\min)} = 4.4 \text{ V}$$

$$V_{OL(\max)} = 0.33 \text{ V}$$

$$\Rightarrow V_{NH} = V_{OH(\min)} - V_{IH(\max)} \\ = 4.4V - 3.5V \\ = 0.9V$$

$$\Rightarrow V_{NL} = V_{IL(\max)} - V_{OL(\min)} \\ = 1.5V - 0.33V \\ = 1.17V$$

For TTL,

$$\Rightarrow V_{IH(\min)} = 2V \\ V_{OL(\max)} = 0.8V \\ V_{OH(\min)} = 2.4V \\ V_{OL(\max)} = 0.4V$$

$$\Rightarrow V_{NH} = V_{OH(\min)} - V_{IH(\max)} \\ = 2.4V - 2V \\ = 0.4V$$

$$\Rightarrow V_{NL} = V_{IL(\max)} - V_{OL(\min)} \\ = 0.8V - 0.4V \\ = 0.4V$$

A TTL gate is immune to up to 0.4V
of noise for both the HIGH and LOW
input states.

Example 15-2:

A certain gate draws 2 mA when its output is HIGH and 3.6 mA when its output is LOW. What is its average power dissipation if V_{cc} is 5V and the gate is operated on a 50% duty cycle?

Solution:

The average I_{cc} is
$$\Rightarrow I_{cc} = \frac{I_{ccH} + I_{ccL}}{2}$$

$$= \frac{2.0 \text{ mA} + 3.6 \text{ mA}}{2}$$
$$= 2.8 \text{ mA}$$

The average power dissipation is

$$\Rightarrow P_D = V_{cc} I_{cc}$$
$$= (5V) (2.8 \text{ mA})$$
$$= 14 \text{ mW}$$

Section 15-1:

- 1.** A certain logic gate has a $V_{OH(\min)} = 2.2\text{V}$ and it is driving a gate with a $V_{IH(\min)} = 2.5\text{V}$. Are these gates compatible for HIGH-state operation? Why?

No, because the $V_{OH(\min)}$ is less than the $V_{IH(\min)}$.

The gate may interpret 2.2V as a LOW.

- 2.** A certain logic gate has a $V_{OL(\max)} = 0.45\text{V}$, and it is driving a gate with a $V_{IL(\max)} = 0.75\text{V}$. Are these gates compatible for LOW-state operation? Why?

They are compatible because $V_{OL(\max)}$ is less than $V_{IL(\max)}$

3. A TTL gate has the following actual voltage level values;
 $V_{IH(\min)} = 2.25V$, $V_{IL(\max)} = 0.65V$
Assuming it is being driven by a gate with $V_{OH(\min)} = 2.4V$ and $V_{OL(\max)} = 0.4V$, what are the HIGH and LOW-level noise margin?

For TTL,

$$\Rightarrow V_{OH(\min)} = 2.4V$$

$$V_{IH(\min)} = 2.25V$$

$$\Rightarrow V_{OL(\max)} = 0.4V$$

$$V_{IL(\max)} = 0.65V$$

$$\begin{aligned}\Rightarrow V_{NH} &= V_{OH(\min)} - V_{IH(\min)} \\ &= 2.4V - 2.25V \\ &= 0.15V\end{aligned}$$

$$\begin{aligned}\Rightarrow V_{NL} &= V_{IL(\max)} - V_{OL(\max)} \\ &= 0.65V - 0.4V \\ &= 0.25V\end{aligned}$$

4. What is the maximum amplitude of noise spikes that can be tolerated on the inputs in both the HIGH state and the LOW state for the gate in Problem 3?

The maximum amplitudes equal the noise margins of 0.15V and 0.25V.

5. Voltage specifications for three types of logic gates are given in table. Select the gate that you would use in a high-noise industrial environment.

	V _{OH(min)}	V _{OL(max)}	V _{IH(min)}	V _{IL(max)}
Gate A	2.4V	0.4V	2V	0.8V
Gate B	3.5V	0.2V	2.5V	0.6V
Gate C	4.2V	0.2V	3.2V	0.8V

Gate A :

$$\Rightarrow V_{NH} = V_{OH} - V_{IH}$$
$$= 2.4V - 2V$$
$$= 0.4V$$

$$\Rightarrow V_{NL} = V_{IL} - V_{OL}$$
$$= 0.8V - 0.4V$$
$$= 0.4V$$

Gate B :

$$\Rightarrow V_{NH} = V_{OH} - V_{IH}$$
$$= 3.5V - 2.5V$$
$$= 1V$$

$$\Rightarrow V_{NL} = V_{IL} - V_{OL}$$
$$= 0.6V - 0.2V$$
$$= 0.4V$$

Gate C :

$$\Rightarrow V_{NH} = V_{OH} - V_{IH}$$
$$= 4.2V - 3.2V$$
$$= 1V$$

$$\Rightarrow V_{NL} = V_{IL} - V_{OL}$$

$$= 0.8V - 0.2V$$

$$= 0.6V$$

Gate C has the highest noise margins.

- 6.** A certain gate draws a dc supply current from a +5V source of 2mA in the LOW state and 3.5mA in the HIGH state. What is the power dissipation in the LOW state? What is the power dissipation in the HIGH state? Assuming a 50% duty cycle, what is the average power dissipation?

$$\Rightarrow P_D(\text{LOW}) = (5V)(2\text{mA})$$

$$= 10\text{mW}$$

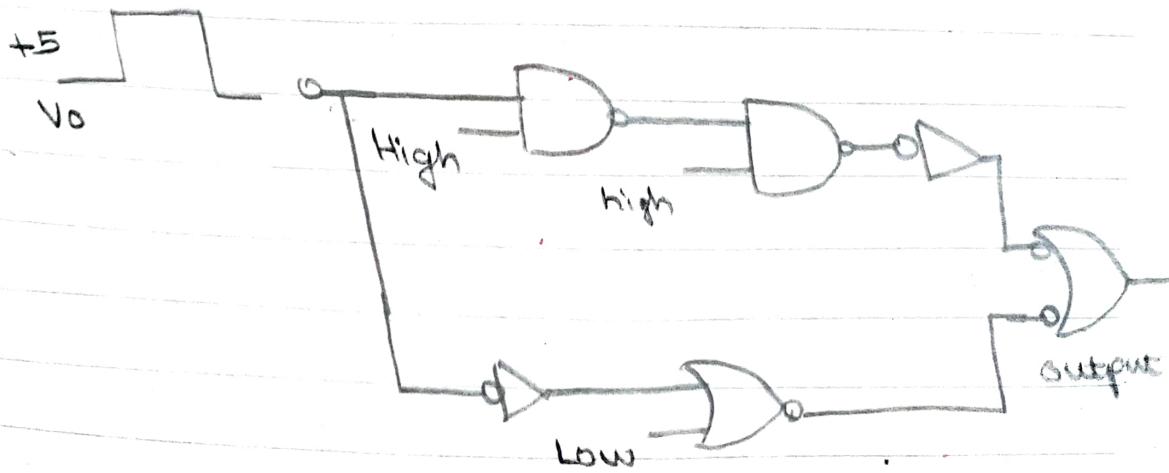
$$\Rightarrow P_D(\text{HIGH}) = (5V)(3.5\text{mA})$$

$$= 17.5\text{mW}$$

$$\begin{aligned}
 \Rightarrow P_D(\text{avg}) &= \frac{P_D(\text{low}) + P_D(\text{high})}{2} \\
 &= \frac{10\text{mW} + 17.5\text{mW}}{2} \\
 &= \frac{27.5\text{mW}}{2}
 \end{aligned}$$

$$\Rightarrow P_D(\text{avg}) = 13.75\text{mW}$$

7. Each gate in the circuit has a t_{PLH} and t_{PHL} of 4 ms. If a positive going pulse is applied to the input as indicated how long will it take the output pulse to appear?



The pulse goes through three gates in the shortest path.

$$\Rightarrow 3 \times 4 \text{ ns} = 12 \text{ ns.}$$

8. For a certain gate,
 $t_{PLH} = 3 \text{ ns}$ and $t_{PHL} = 2 \text{ ns}$,
what is the average propagation delay time?

$$\Rightarrow t_p(\text{avg}) = \frac{t_{PLH} + t_{PHL}}{2}$$

$$= \frac{2 \text{ ns} + 3 \text{ ns}}{2}$$

$$\Rightarrow t_p(\text{avg}) = 2.5 \text{ ns}$$

9. Table lists parameters for three types of gates. Basing your decision on the speed-power product, which one would you select for best performance?

	t_{PLH}	t_{PHL}	P_D
Gate A	1 ns	1.2 ns	15 mW
Gate B	5 ns	4 ns	8 mW
Gate C	10 ns	10 ns	0.5 mW

Gate A average propagation delay:

$$\begin{aligned}
 & \frac{t_{PLH} + t_{PHL}}{2} \\
 &= \frac{1 \text{ ns} + 1.2 \text{ ns}}{2} \\
 &= 1.1 \text{ ns}
 \end{aligned}$$

Speed / Power product =

$$\begin{aligned}
 &= (1.1 \text{ ns})(15 \text{ mW}) \\
 &= 16.5 \text{ pJ}
 \end{aligned}$$

gate B average propagation delay:

$$= \frac{t_{PLH} + t_{PHL}}{2}$$

$$= \frac{5\text{ns} + 4\text{ns}}{2}$$

$$= 4.5 \text{ ns}$$

Speed / Power product =

$$= (4.5 \text{ ns})(8 \text{ mW})$$

$$= 36 \text{ pJ}$$

gate C average propagation

delay:

$$= \frac{t_{PLH} + t_{PHL}}{2}$$

$$= \frac{10\text{ns} + 10\text{ns}}{2}$$

$$= 10 \text{ ns}$$

Speed / Power product =

$$= (10 \text{ ns})(0.5 \text{ mW})$$

$$= 5 \text{ pJ}$$

Gate C has the best speed / power

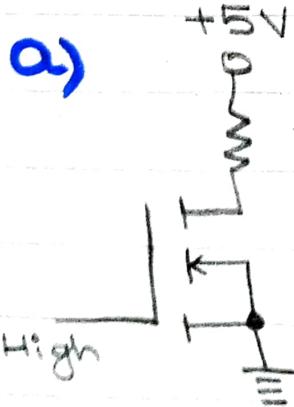
10. Which gate in table of Problem 9 would you select if you wanted the gate to operate at the highest possible frequency?

Gate A can be operated at the highest frequency because it has the shortest propagation delay.

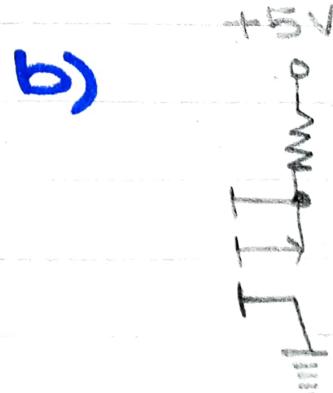
CMOS CIRCUITS

Section 15-2:-

13. Determine the state (on or off) of each MOSFET.

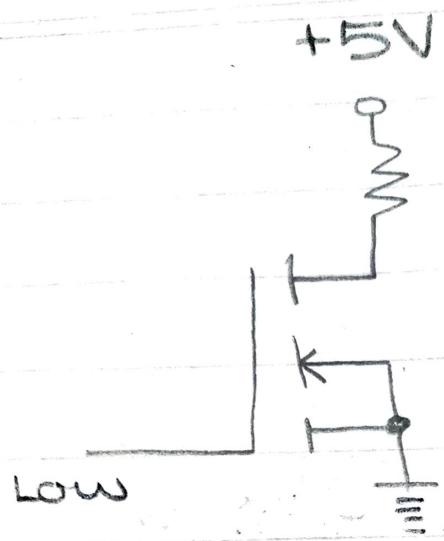


ON



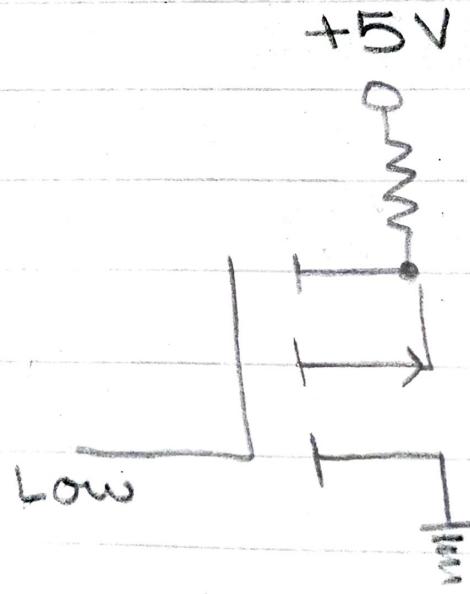
OFF

C)



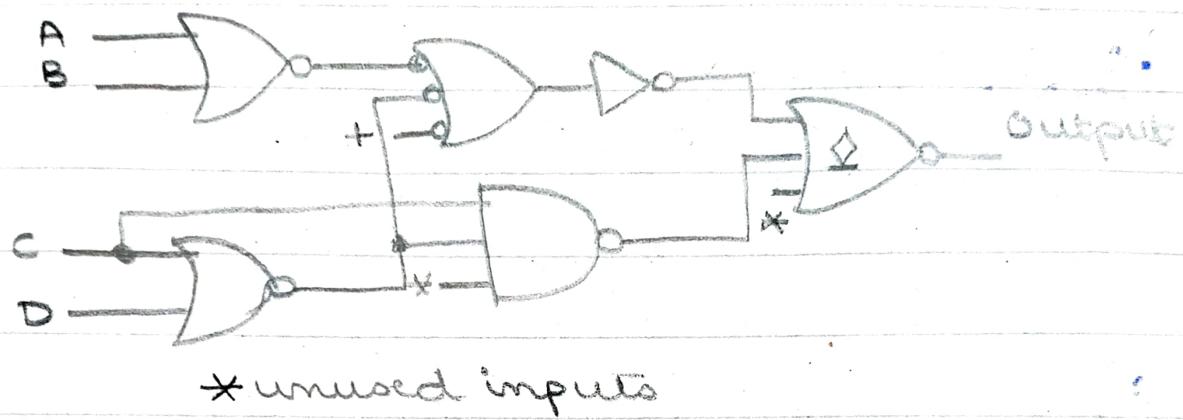
OFF

D)



ON

14. The CMOS gate network in figure is incomplete. Indicate the changes that should be made.



Unused inputs should be connected as follows:

→ Negative-OR gate (NAND) to V_{cc}

→ NAND gate to $+V_{cc}$

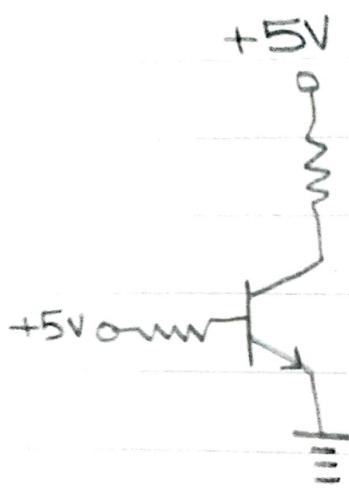
→ NOR gate to ground.

TTL (BIPOLAR) CIRCUITS

Section 15-3

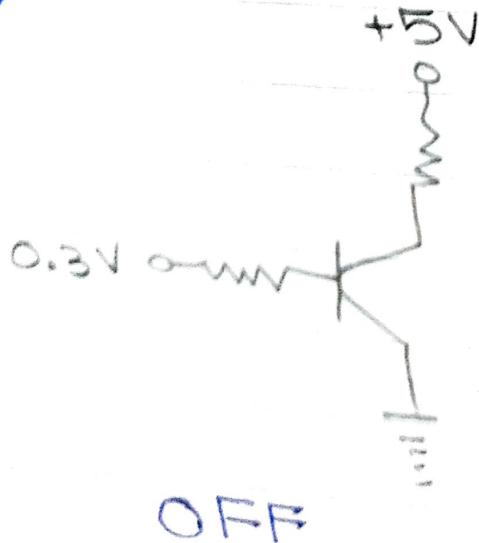
- 16.** Determine which BJT's in figure are off and which are on.

a)



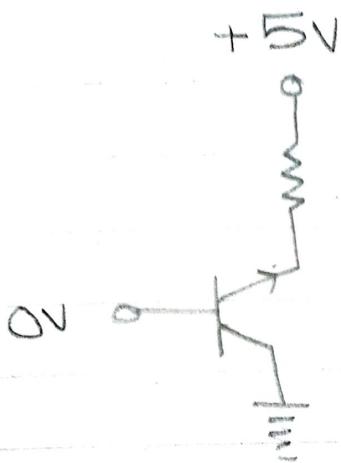
ON: high voltage on base forward-biases the base-emitter junction.

b)



Insufficient voltage on base to forward-bias the base-emitter junction.

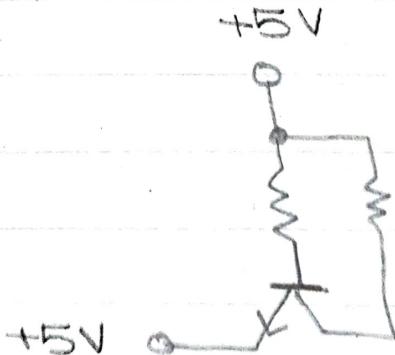
c)



OFF

Emitter is more positive than the base which reverse-biases the base-emitter junction.

d)



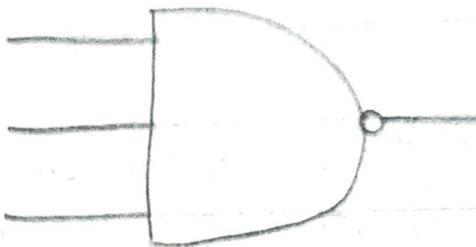
OFF

Base and emitter at same voltage. No forward bias.

17. Determine the output state
of each TTL gate

a)

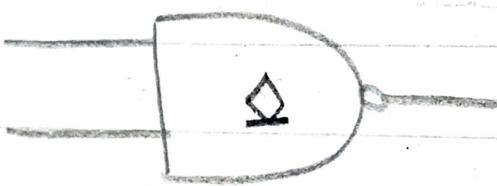
High
High
Low



HIGH

b)

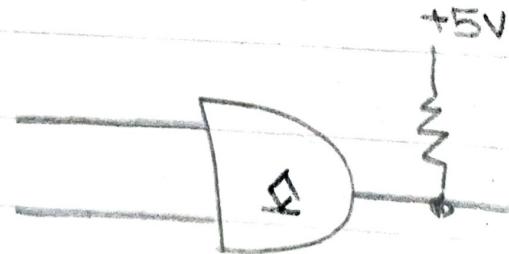
High
Low



Floating

c)

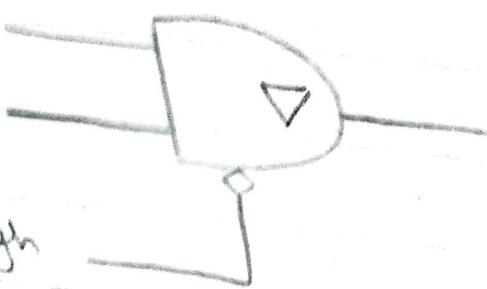
High
High



HIGH

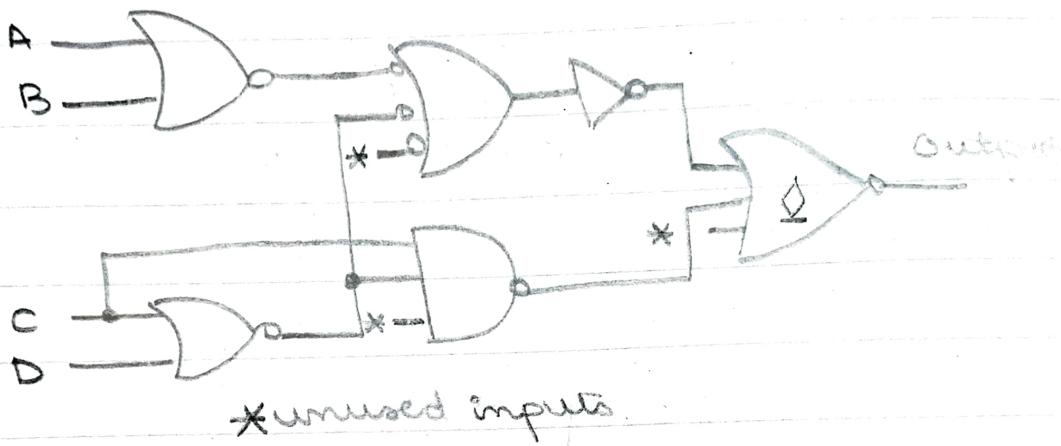
d)

High
High
High



High-Z

18. The TTL gate network in figure is incomplete. Indicate the changes that should be made.



Connect a $1\text{ k}\Omega$ pull-up resistor to the unused inputs of the two NAND gates. Connect the unused inputs of the NOR gate to ground. Connect a pull-up resistor to the open collector of the NOR gate (Value depends on load).

PRACTICAL CONSIDERATION IN THE USE OF TTL:-

Example 15-3

When a standard TTL NAND gate drives five TTL inputs, how much current does the driver output source, and how much it sink?

Solution:

Total source current (in HIGH output state):

$$\Rightarrow I_{IH(\text{max})} = 40 \mu\text{A} \text{ per input}$$

$$\begin{aligned}\Rightarrow I_T(\text{source}) &= (5 \text{ inputs}) (40 \mu\text{A}/\text{inputs}) \\ &= 5 (40 \mu\text{A}) \\ &= 200 \mu\text{A}\end{aligned}$$

Total sink current (in low output state):

$$\Rightarrow I_{IL(\max)} = -1.6 \text{ mA per input}$$

$$\begin{aligned}\Rightarrow I_T(\text{sink}) &= (\text{5 inputs}) \\ &\quad (-1.6 \text{ mA/input}) \\ &= 5(-1.6 \text{ mA}) \\ &= -8.0 \text{ mA.}\end{aligned}$$

Example 15-4

Refer to the datasheet available at www.ti.com and determine the fan-out of the 7400 NAND gate.

Solution:

According to the data sheet, the current parameters are as follows:

$$\Rightarrow I_{IH(\max)} = 40 \mu\text{A}$$

$$I_{OH(\max)} = -400 \mu\text{A}$$

$$I_{IL(\max)} = -1.6 \text{ mA}$$

$$I_{OL(\max)} = 16 \text{ mA}$$

Fan-out for the HIGH output state is calculated as follows,

Current $I_{OH(\text{max})}$ is the maximum current that the gate can source to a load. Each load input requires an $I_{IH(\text{max})}$ of 40 mA. The HIGH state fanout is

$$\left| \frac{I_{OH(\text{max})}}{I_{IH(\text{max})}} \right| = \frac{400 \text{ mA}}{40 \text{ mA}} = 10 \text{ unit loads}$$

For the LOW output state, fanout is calculated as follows:

$I_{OL(\text{max})}$ is the maximum current that the gate can sink. Each load input produces an $I_{IL(\text{max})}$ of -1.6 mA. The LOW-state fanout is:

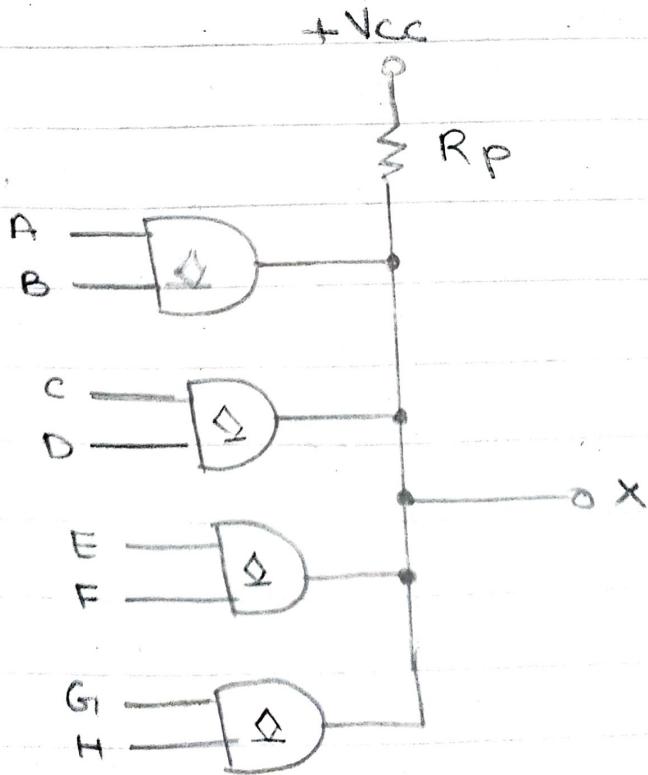
$$\left| \frac{I_{OL(\text{max})}}{I_{IL(\text{max})}} \right| = \frac{16 \text{ mA}}{1.6 \text{ mA}}$$

= 10 units load

In this case both the HIGH-state fan-out and the LOW-state fan-out are the same.

Example 15-5

Write the output expression ~~that~~ for the wired-AND configuration of open-collector AND gate.



Solution:

The output expression is

$$X = ABCDEF GH$$

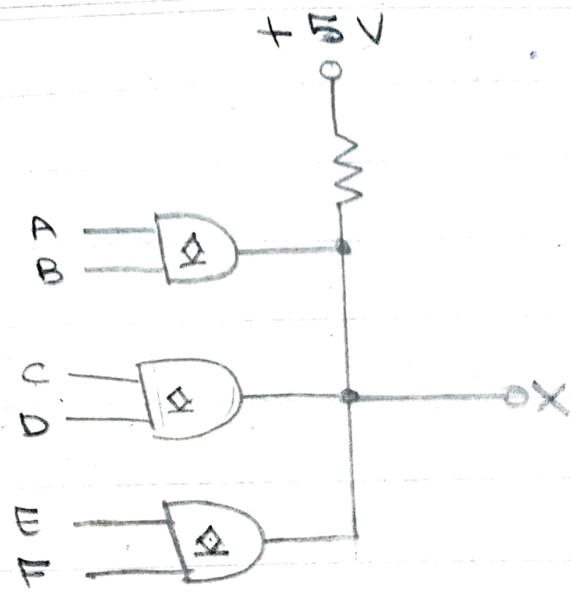
The wired - AND connection
of the four 2-input AND gate
creates an 8-input AND gate.

Example 15-6

Three open-collector AND gates
are connected in a wired - AND
configuration. Assume that the
wired - AND circuit is driving
four standard TTL inputs.
(-1.6 mA each)

a) Write the logic expression
for X

b) Determine the minimum value of
 R_P if $I_{OL(max)}$ for each gate is
30 mA and $V_{OL(max)}$ is 0.4V



Solution :

$$(a) X = ABCDEF$$

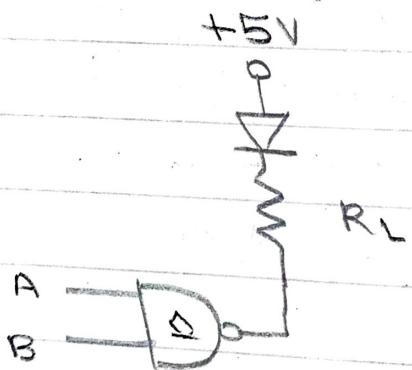
$$(b) 4(1.6 \text{ mA}) = 6.4 \text{ mA}$$

$$\begin{aligned} I_{RP} &= I_{OL(\text{max})} - 6.4 \text{ mA} \\ &= 30 \text{ mA} - 6.4 \text{ mA} \\ &= 23.6 \text{ mA} \end{aligned}$$

$$\begin{aligned} R_P &= \frac{V_{CC} - V_{OL(\text{max})}}{I_{RP}} \\ &= \frac{5V - 0.4V}{23.6 \text{ mA}} \\ &= 195 \Omega \end{aligned}$$

Example 15-7

Determine the value of the limiting resistor, R_L in the open-collector circuit if the LED current is to be 20 mA. Assume a 1.5 V drop across the LED when it is forward-biased and a LOW-state output voltage of 0.1 V at the output of the gate.



Solution:

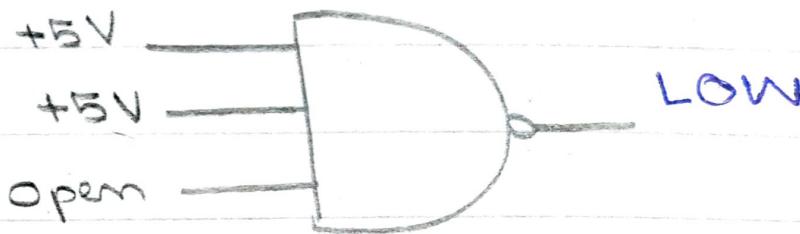
$$\Rightarrow V_{RL} = 5V - 1.5V - 0.1V \\ = 3.4V$$

$$\Rightarrow R_L = \frac{V_{RL}}{I} = \frac{3.4V}{20\text{mA}} \\ = 170\Omega$$

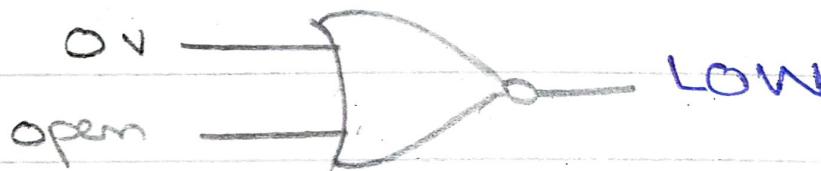
Section 15-4

19. Determine the output level of each TTL gate

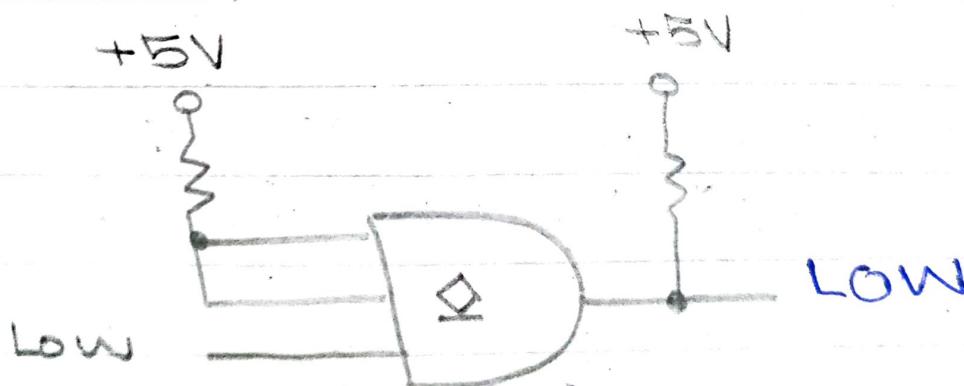
a)



b)

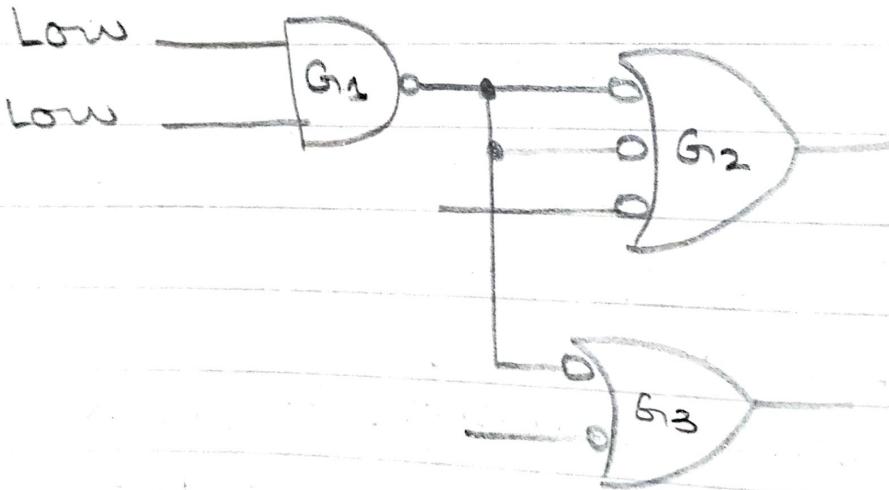


c)



20. For each part, tell whether each driving gate is sourcing or sinking current. Specify the maximum current out of or into the output of the driving gate or gates in each case. All gates are standard TTL.

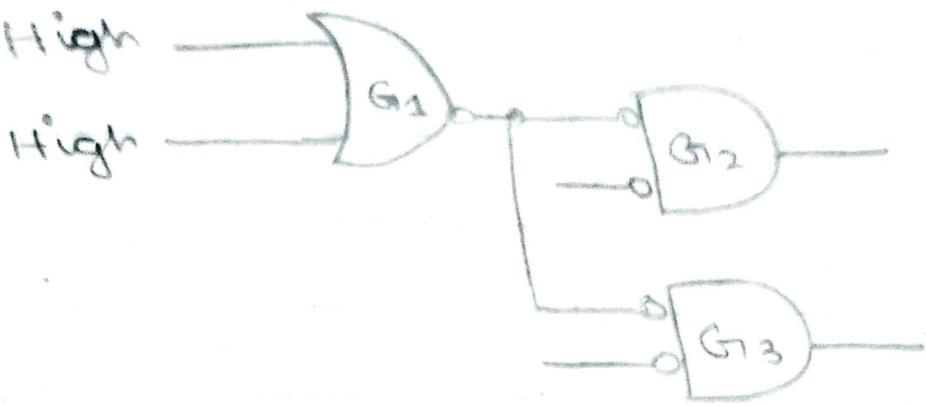
a)



The driving gate output is HIGH, it is sourcing 3 unit loads

$$\Rightarrow I_T = 3(40 \text{ mA}) \\ = 120 \text{ mA}$$

b)



The driving gate output is LOW, it is sinking current from 2 unit loads.

$$\Rightarrow I_T = 2(-1.6 \text{ mA}) \\ = -3.2 \text{ mA}$$

c)



Gate 1 output is HIGH, it is sourcing 6 unit loads.

$$\Rightarrow I_T = 6(40 \mu\text{A}) \\ = 240 \mu\text{A}$$

Gate 2 output is LOW, it is sinking current from 2 unit loads.

$$\Rightarrow I_T = 2(-1.6 \text{ mA}) \\ = -3.2 \text{ mA}$$

gate 3 output is HIGH, it
is sourcing 2 unit loads.

$$\Rightarrow I_T = 2(40 \text{ mA}) \\ = 80 \text{ mA}$$

23. Determine the minimum value for the pull-up resistor in each circuit if $I_{OL(\max)} = 40 \text{ mA}$ and $V_{OL(\max)} = 0.25V$ for each gate. Assume that 10 standard TTL unit loads are being driven from output X and the supply voltage is 5V.

Worst case for determining minimum R_P is when only one gate is sinking all of the current (40 mA maximum)

For 10 UL:

$$I_L = 10(1.6 \text{ mA}) \\ = 16 \text{ mA}$$

For each gate:

$$I_{RP(\text{max})} = I_{OL(\text{max})} - 16 \text{ mA} \\ = 40 \text{ mA} - 16 \text{ mA} \\ = 24 \text{ mA}$$

$$\Rightarrow V_{RP} = 5V - 0.25V \\ = 4.75V$$

$$R_P(\text{min}) = \frac{V_{RP}}{I_{RP(\text{max})}} \\ = \frac{4.75V}{24 \text{ mA}} \\ = 198 \Omega$$