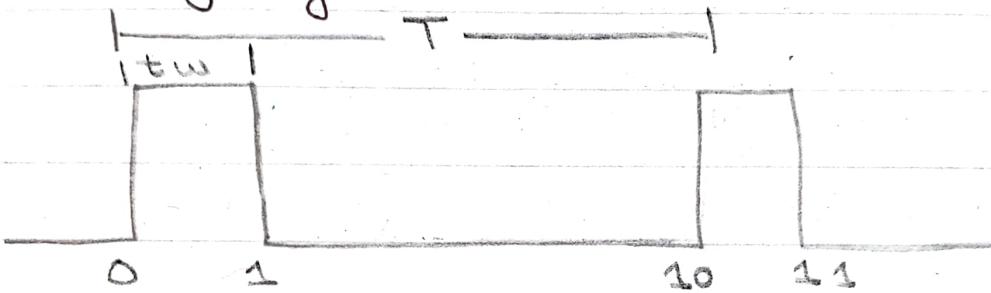


Chapter :01

Example 1.1

A portion of a periodic digital waveform is figure below. The measurements are in milliseconds. Determine the following a) period b) frequency c) duty cycle.



a) The period (T) is measured from the edge of one pulse to the corresponding edge of the next pulse. In this case T is measured from leading edge to leading, as indicated. T equals 10 ms.

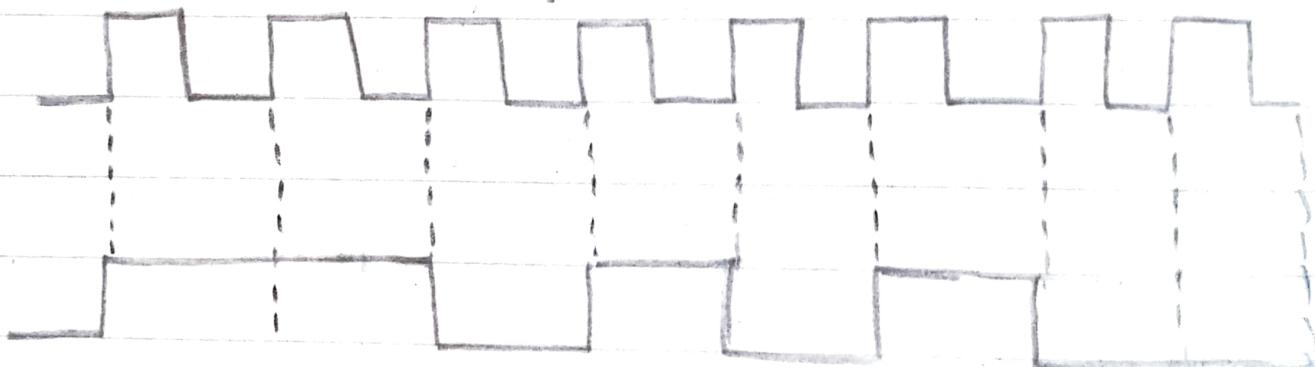
$$b) f = \frac{1}{T} = \frac{1}{10 \text{ ms}} = 100 \text{ Hz}$$

$$c) \text{Duty cycle} = \left(\frac{tw}{T} \right) 100\% = \left(\frac{1 \text{ ms}}{10 \text{ ms}} \right) 100\% = 10\%$$

Example 1.2

- a) Determine the total time required to serially transfer the eight bits contained in waveform A of figure and indicate the sequence of bits. The left-most bit is the first to be transferred. The 1 MHz clock is used as reference.

- b) What is the total time to transfer the same eight bits in parallel?



a) since the frequency of the clock is 1 MHz the period is

$$T = \frac{1}{f} = \frac{1}{1 \text{ MHz}} = 1 \mu\text{s}$$

It takes 1 μs to transfer each bit in the waveform. The total transfer time for 8 bits is

$$8 \times 1 \mu\text{s} = 8 \mu\text{s}$$

To determine the sequence of bits, examine waveform in figure during each bit time. If waveform A is HIGH during the bit time, a 1 is transferred.

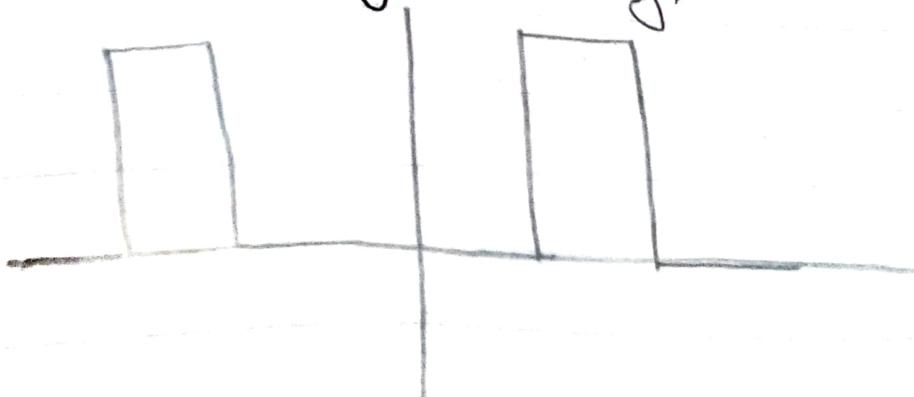
If waveform A is low during the bit time, a 0 is transferred. The bit sequence in figure. The left-most bit is the first to be transferred.

1	1	0	1	0	1	0	0
---	---	---	---	---	---	---	---

b) A parallel transfer would take 1 us for all eight bits.

Example 1.3

Based on the readout, determine the amplitude and the period of the pulse waveform on the screen of a digital oscilloscope as shown in figure. Also, calculate the frequency.



The Volts/div setting is 1V. The pulses are three divisions high. Since each division represents 1V, the pulse amplitude is

$$\Rightarrow \text{Amplitude} = (3 \text{ div}) (1V/\text{div}) = 3V$$

The sec/div setting is 10 μs. A full cycle of the waveform covers four division; therefore, the period is

$$\Rightarrow \text{Period} = (4 \text{ div}) (10 \mu\text{s}/\text{div}) = 40 \mu\text{s}$$

The frequency is calculated as

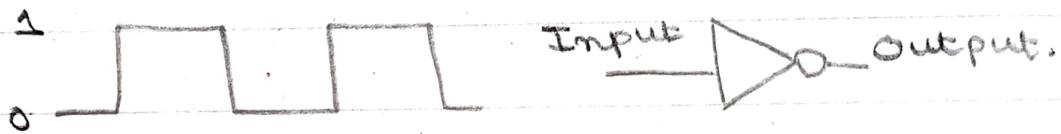
$$\Rightarrow f = \frac{1}{T} = \frac{1}{40 \mu\text{s}} = 25 \text{ KHz}$$

Chapter: 03

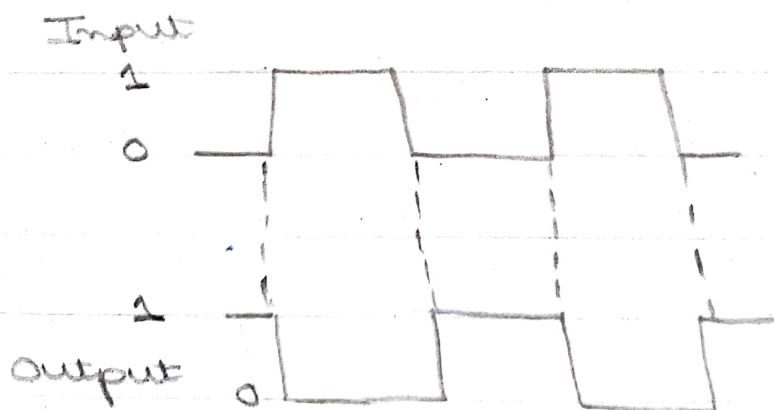
THE INVERTER

Example 3.1

A waveform is applied to an inverter in figure. Determine the output waveform corresponding to the input and show timing diagram. According to the placement of the bubble, what is the active output state?

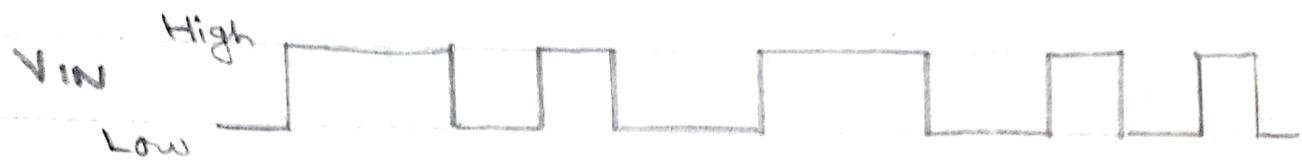


The output waveform is exactly opposite to the input (inverted) which is basic timing diagram. The active or asserted output state is 0.

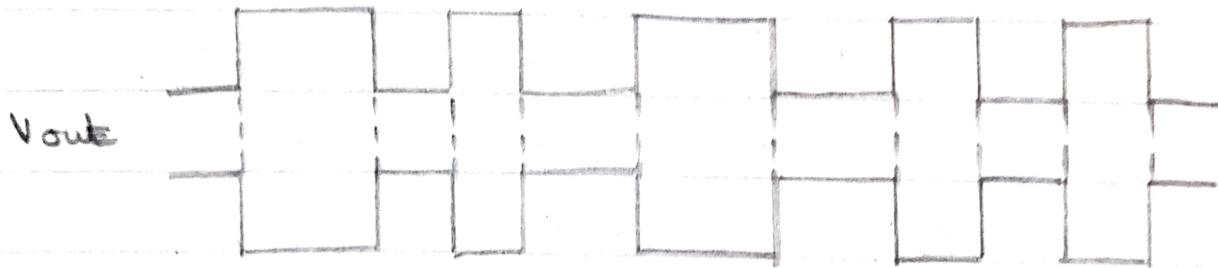


Section 3.1

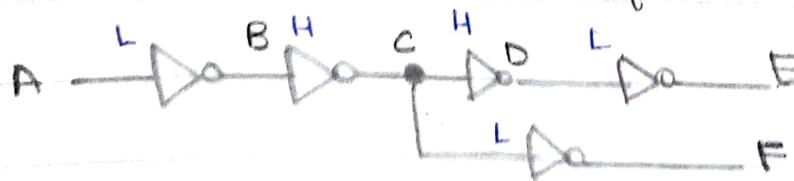
1. The input waveform shown in figure is applied to a system of two inverters connected in series. Draw the output waveform across each inverter



Solution:



2. A combination of inverters is shown in figure. If a LOW is applied to point A, determine net output at point E and F.



Solution-

Point E : HIGH

Point F : LOW

THE AND GATE:-

Example 3.2

a) Develop ~~the~~ truth table for 3-input AND gate

$$\Rightarrow N = 2^n \Rightarrow N = 2^3 = 8$$

Inputs			Outputs
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

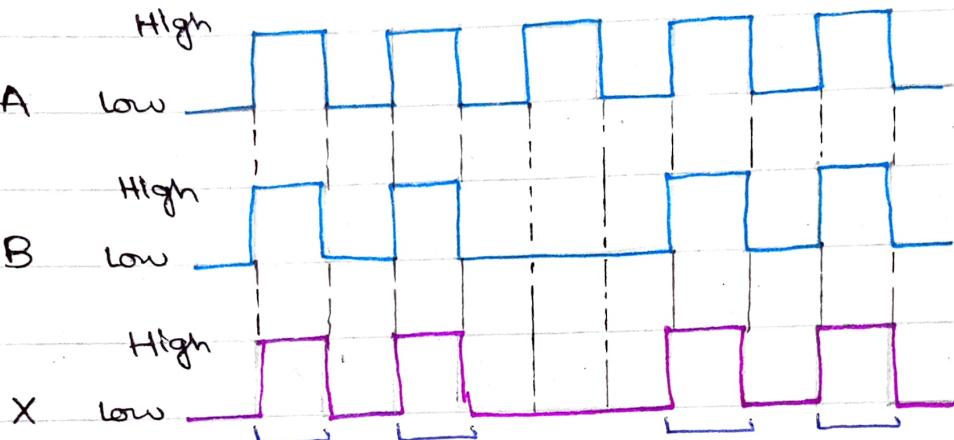
b) Determine total number of possible inputs combinations for a 4-input AND gate.

$$\Rightarrow N = 2^n = 2^4 = 16$$

There are 16 possible combinations of input bits for a 4-input AND gate.

Example 3.3

If two waveforms A and B are applied to the AND gate inputs as in figure what is the resulting output waveform?

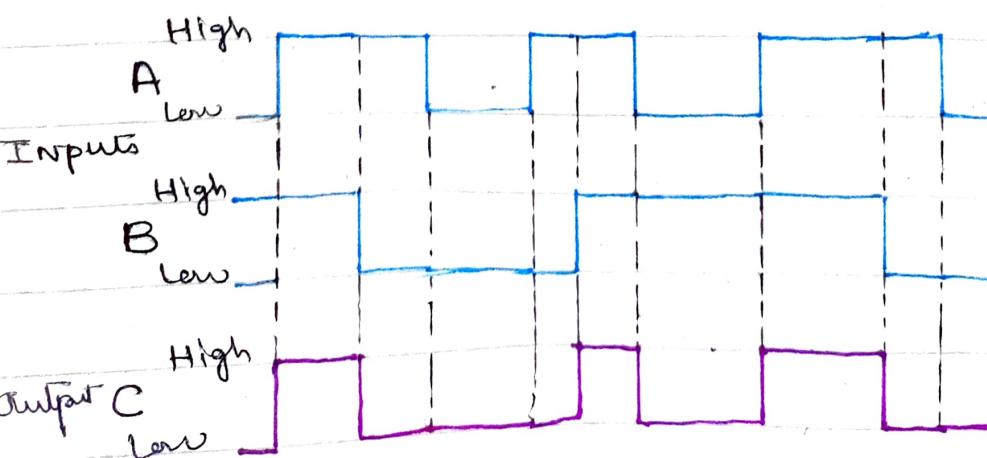


A and B are high at four intervals.

The output waveform X is HIGH only when both A and B waveform are high.

Example 3.4

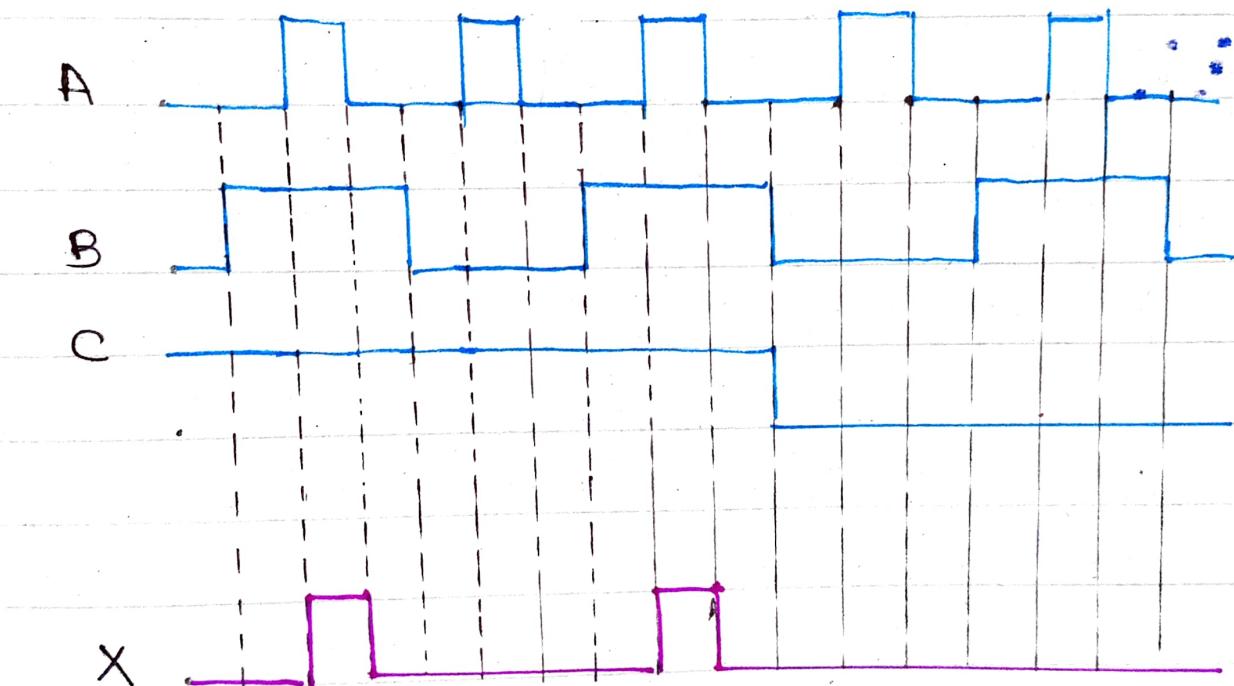
For two input waveforms, A and B show the output waveform with proper relation to the inputs.



The output waveform is HIGH only when both of input waveforms are HIGH.

Example 3.5

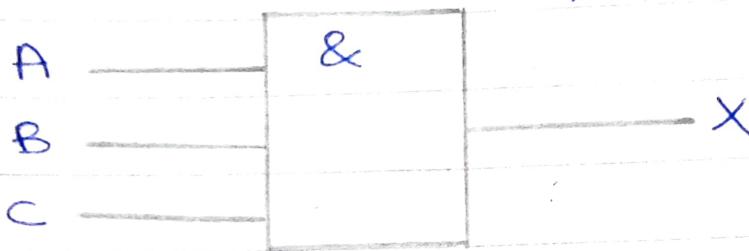
For 3-input AND gate in figure, determine the output waveform in relation to the inputs.



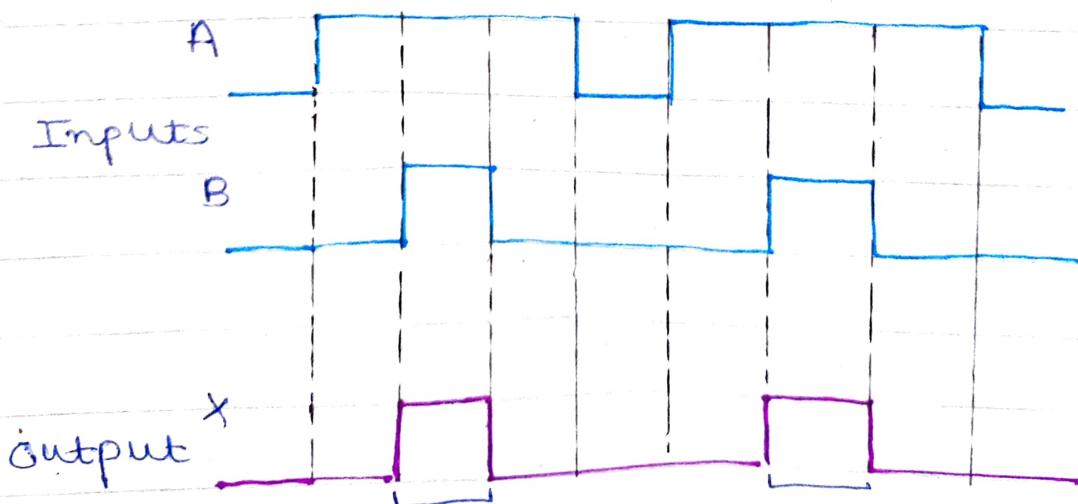
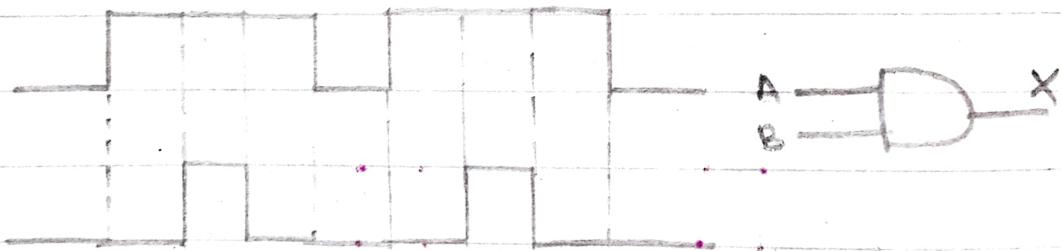
The output waveform X of 3-input AND gate is HIGH only when all three inputs waveforms A, B and C are HIGH.

Section 3.2

4. Draw the rectangular outline symbol for a 3-input AND gate.



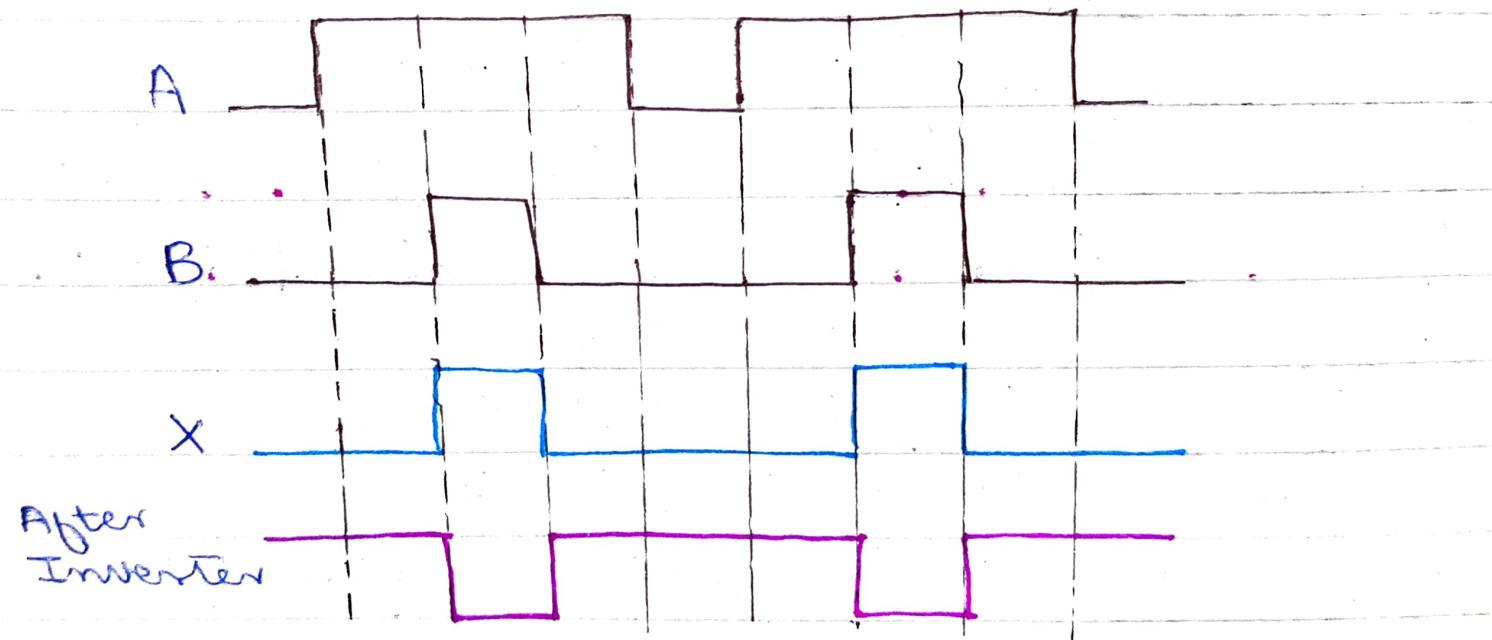
5. Determine the output X, for a 2-input AND gate with input waveform. Show proper relationship of output to inputs with timing diagram.



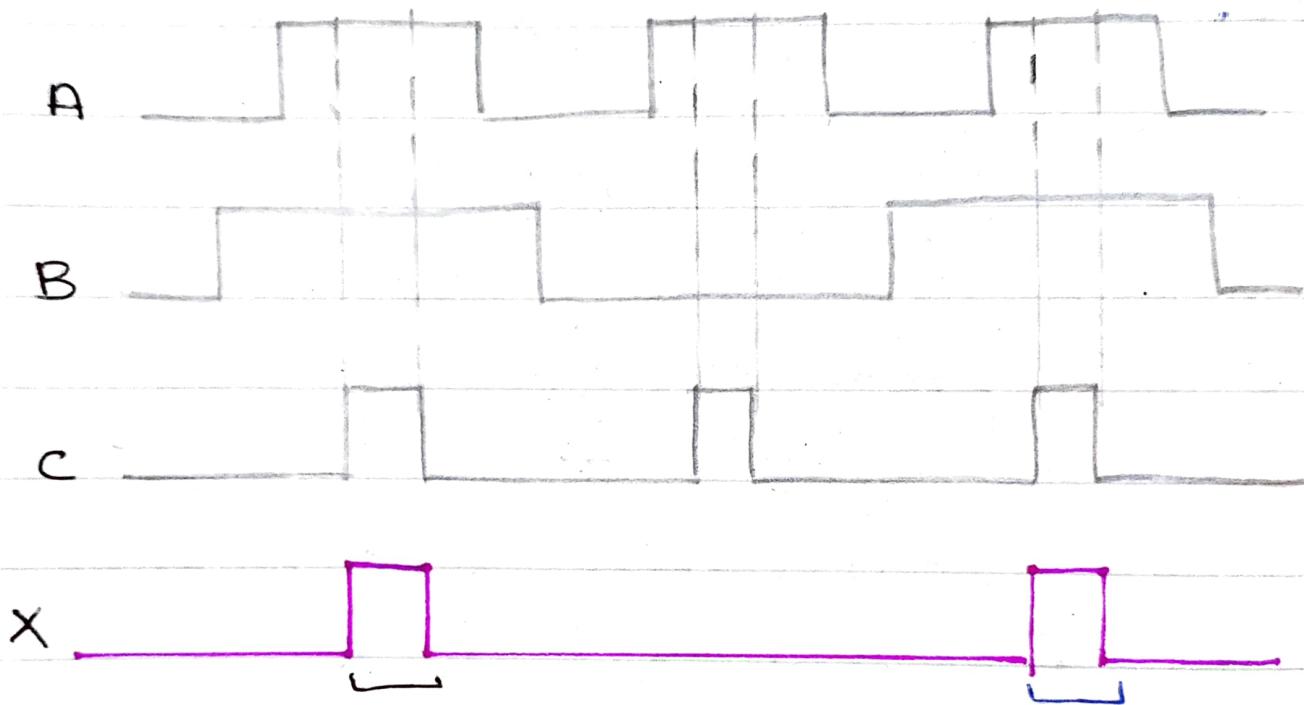
Output is HIGH on two intervals.

The output waveform is HIGH only when the two inputs A and B are HIGH.

6. The waveforms in figure applied to points A and B of a 2-input AND gate followed by an inverter. Draw output waveform.



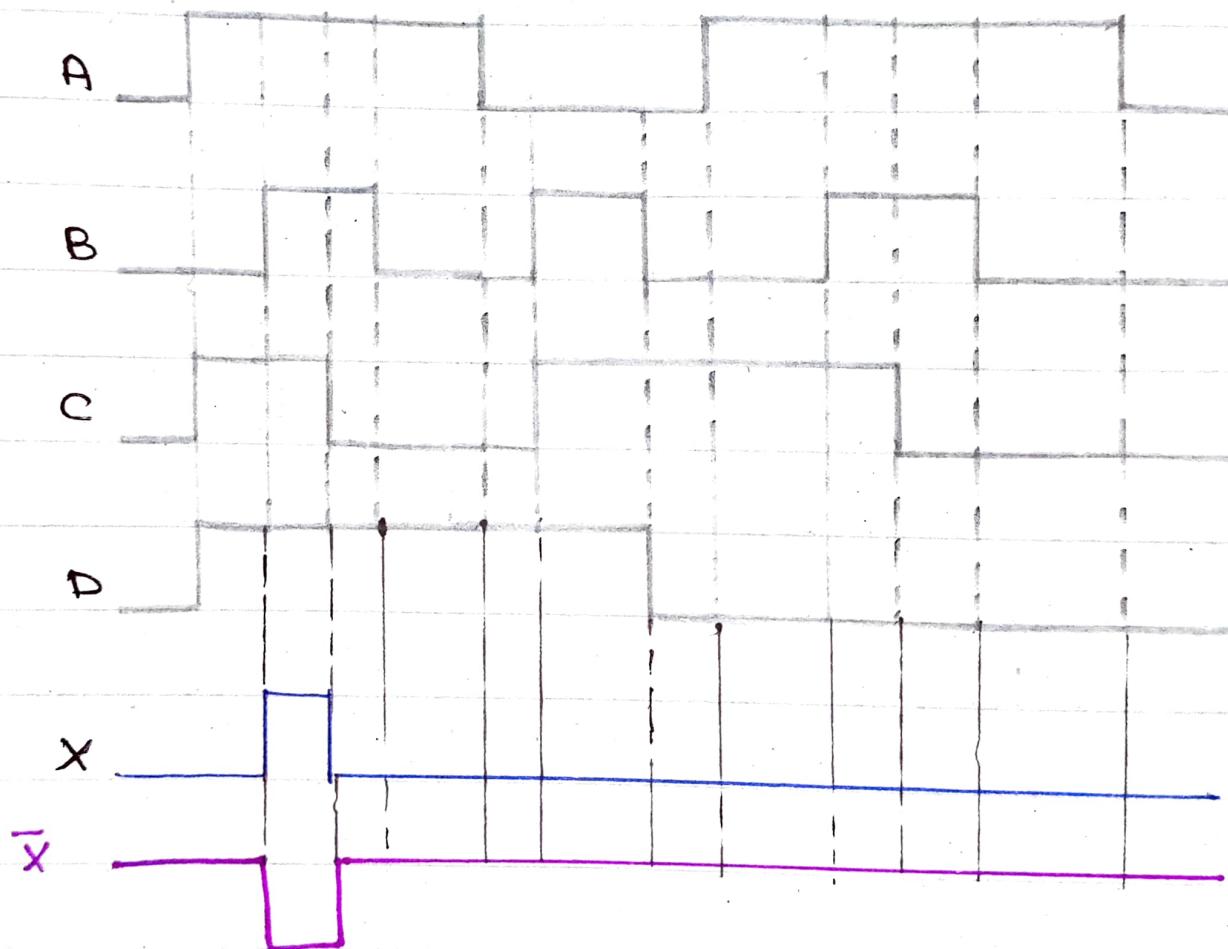
7. The input waveform applied to a 3-input AND gate. Show the output waveform in proper relation to the inputs with a timing diagram.



Output is HIGH on two intervals.

The output waveform is HIGH only when inputs A, B and C are HIGH.

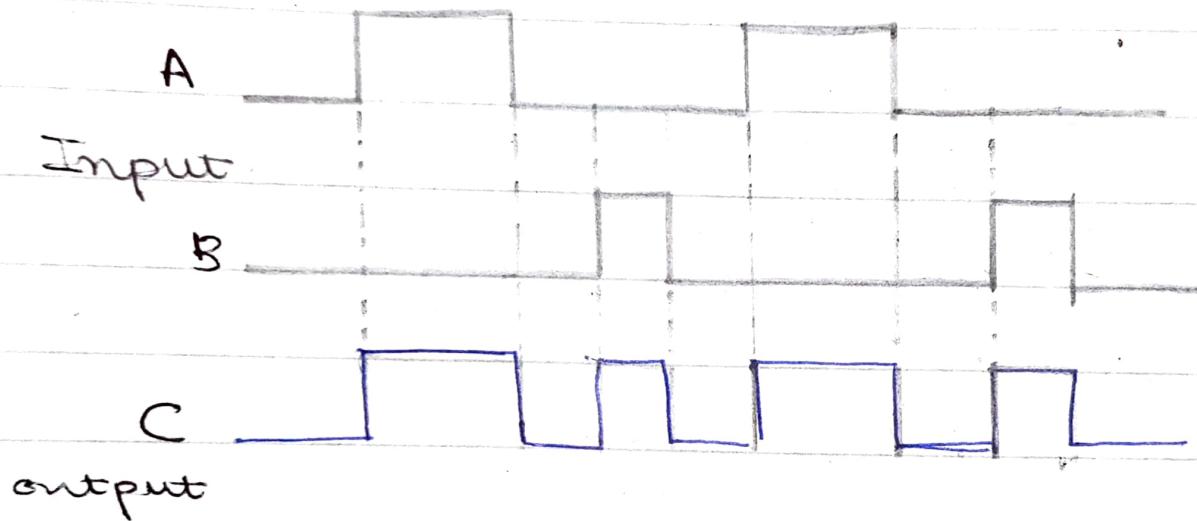
8. The input waveforms applied to a 4-input AND gate are as indicated. The output of the AND gate is fed to an inverter. Draw the net output waveform of this system.



THE OR GATE:-

Example 3.7

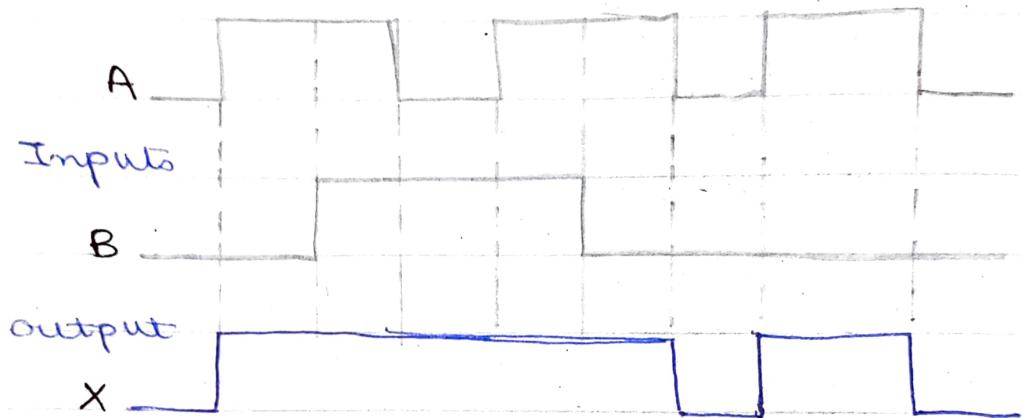
If two output waveforms A and B are applied to OR gate, what is resulting output waveform?



The output waveform X of a 2-input OR gate is HIGH when either or both input waveforms are HIGH.

Example 3.8

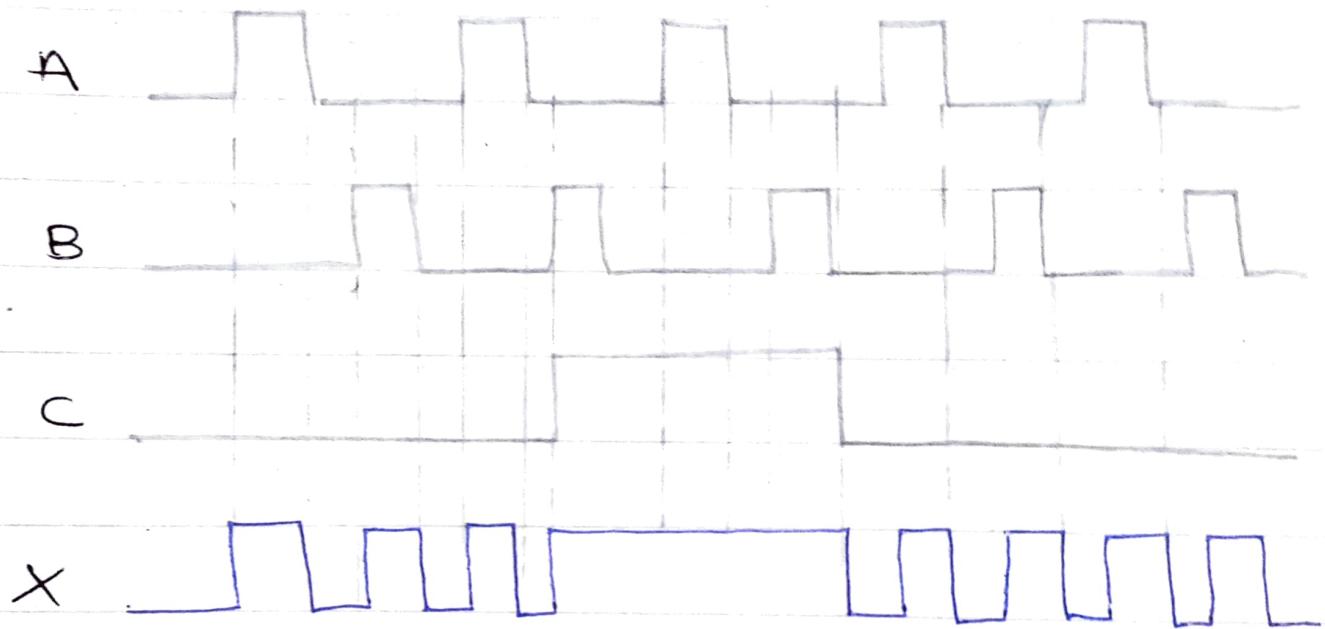
For the two input waveforms, A and B, show the output waveform with its proper relation to the inputs.



When either or both input waveforms are HIGH the output is HIGH as shown by the output waveform X in the timing diagram.

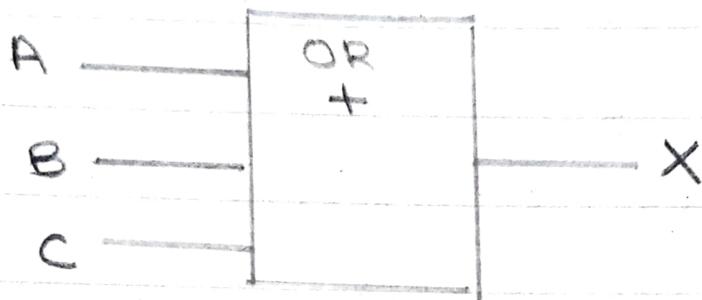
Example 3.9

For the 3-input OR gate in figure determine the output waveform in proper time relation to the inputs.



The output is HIGH when one or more of the inputs waveforms are HIGH as indicated by the output waveform X in the timing diagram.

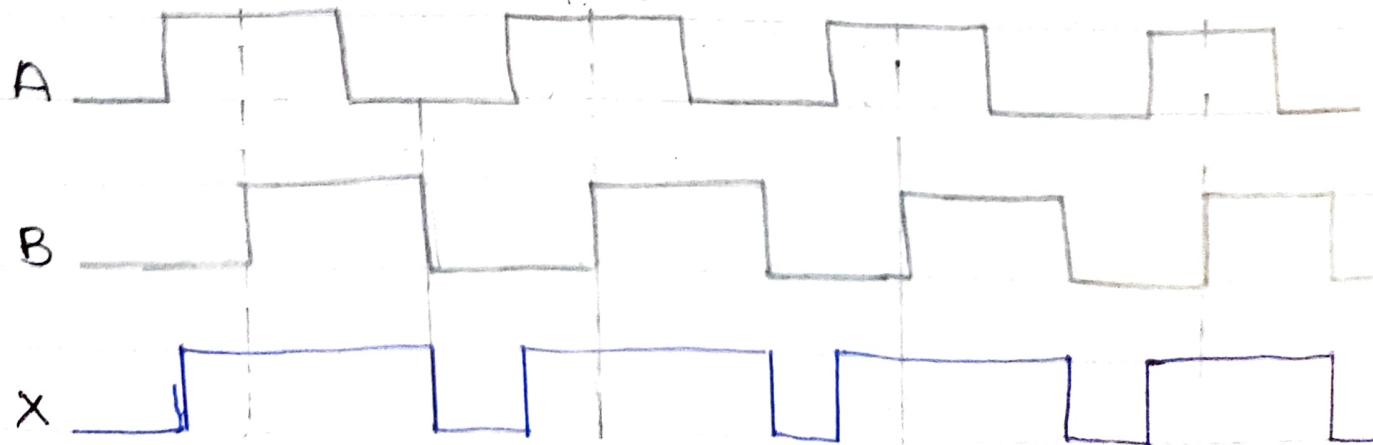
9. Draw the rectangular outline symbol for a 3-input OR gate.



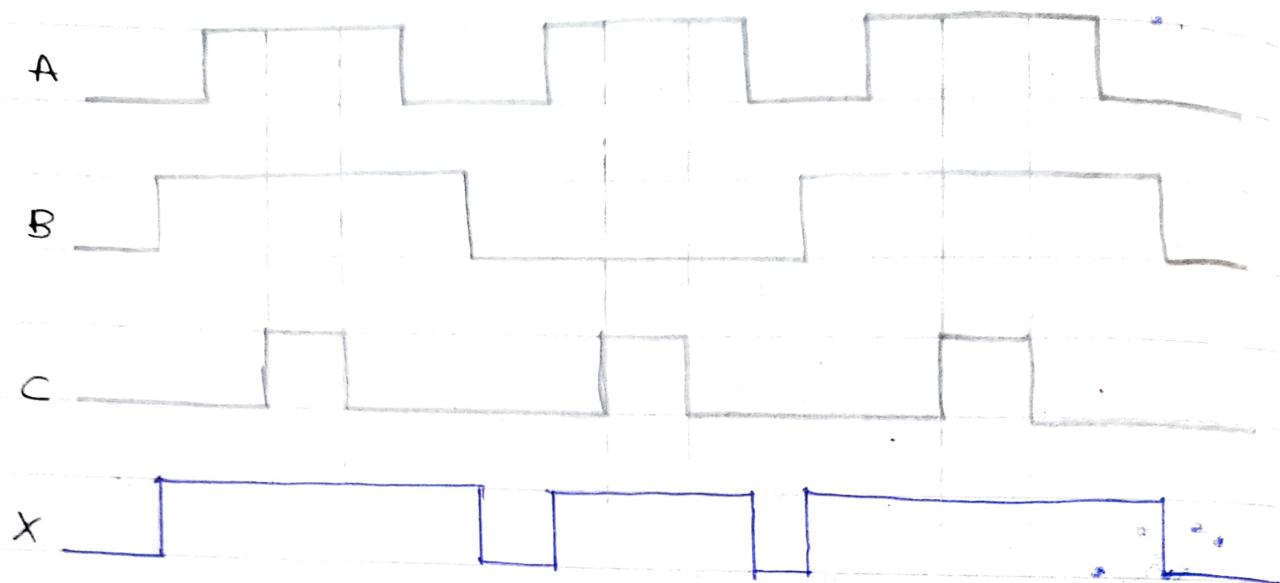
10. Write the expression for a 4-input OR gate with inputs A, B, C, D and output X.

$$\Rightarrow X = A + B + C + D$$

11. Determine output for 2-input OR gate and draw timing diagram.

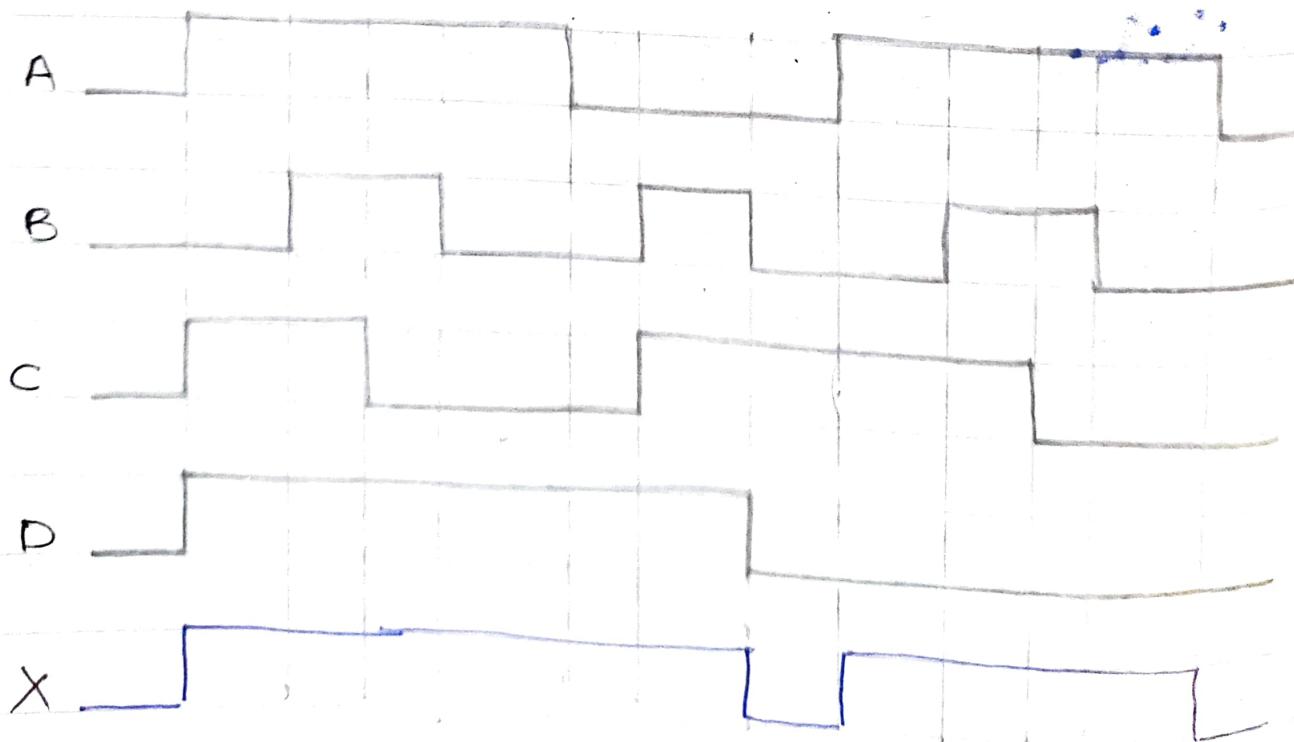


12. Repeat problem 7 for 3-input OR gate.



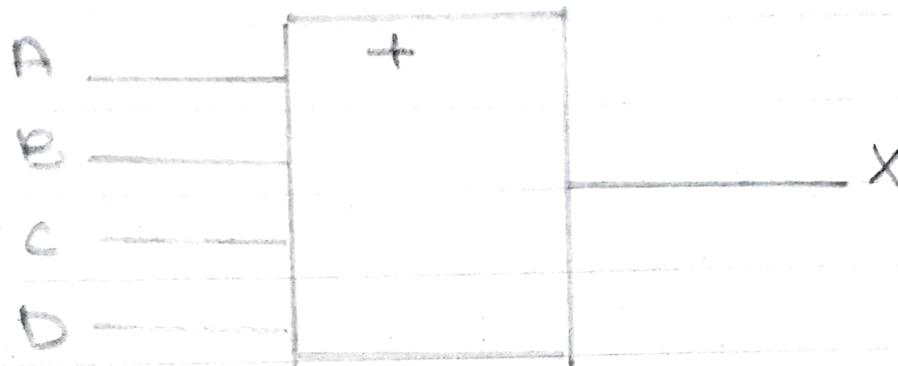
Where either input A, B ~~and~~ OR C are HIGH the output waveform is HIGH.

13. Repeat problem 8 for 4-input OR gate.



Output waveform X is HIGH where input A, B, C or D are HIGH.

15. Draw rectangular outline symbol for a 4-input OR gate.



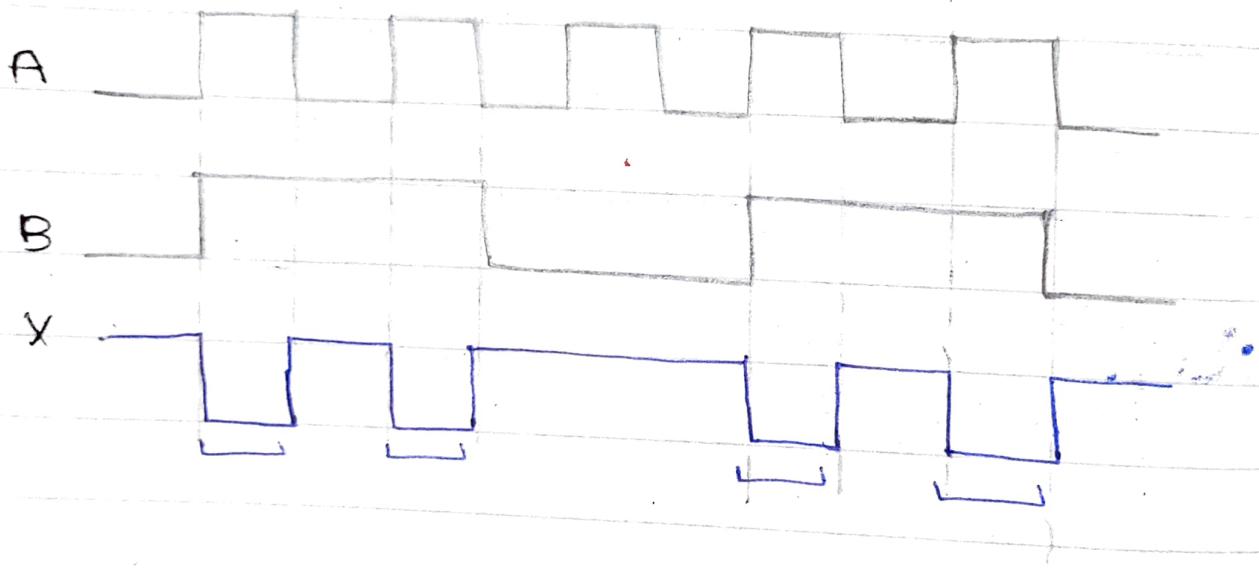
16. Show the truth table for a system of a 3-input OR gate followed by an inverter.

A	B	C	$A+B$	$\overline{A+B}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

THE NAND GATE:-

Example 3.10:

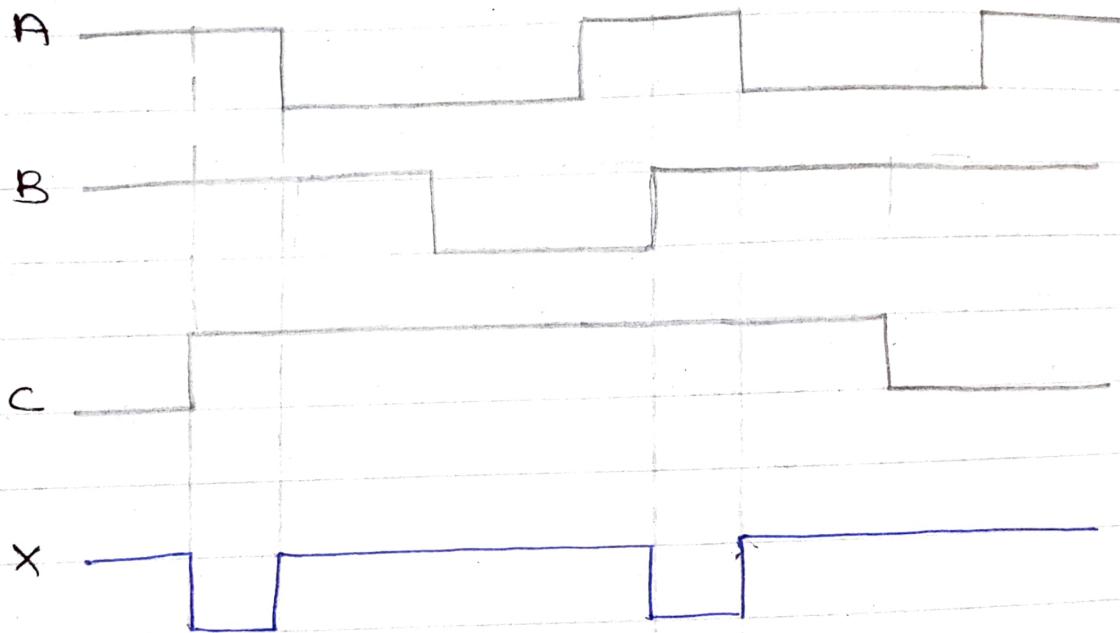
If the two waveforms A and B are applied to the NAND gate inputs, determine the resulting output waveform.



Output waveform X is LOW only during the four time intervals when both input waveforms A and B are HIGH as shown in timing diagram.

Example 3.11

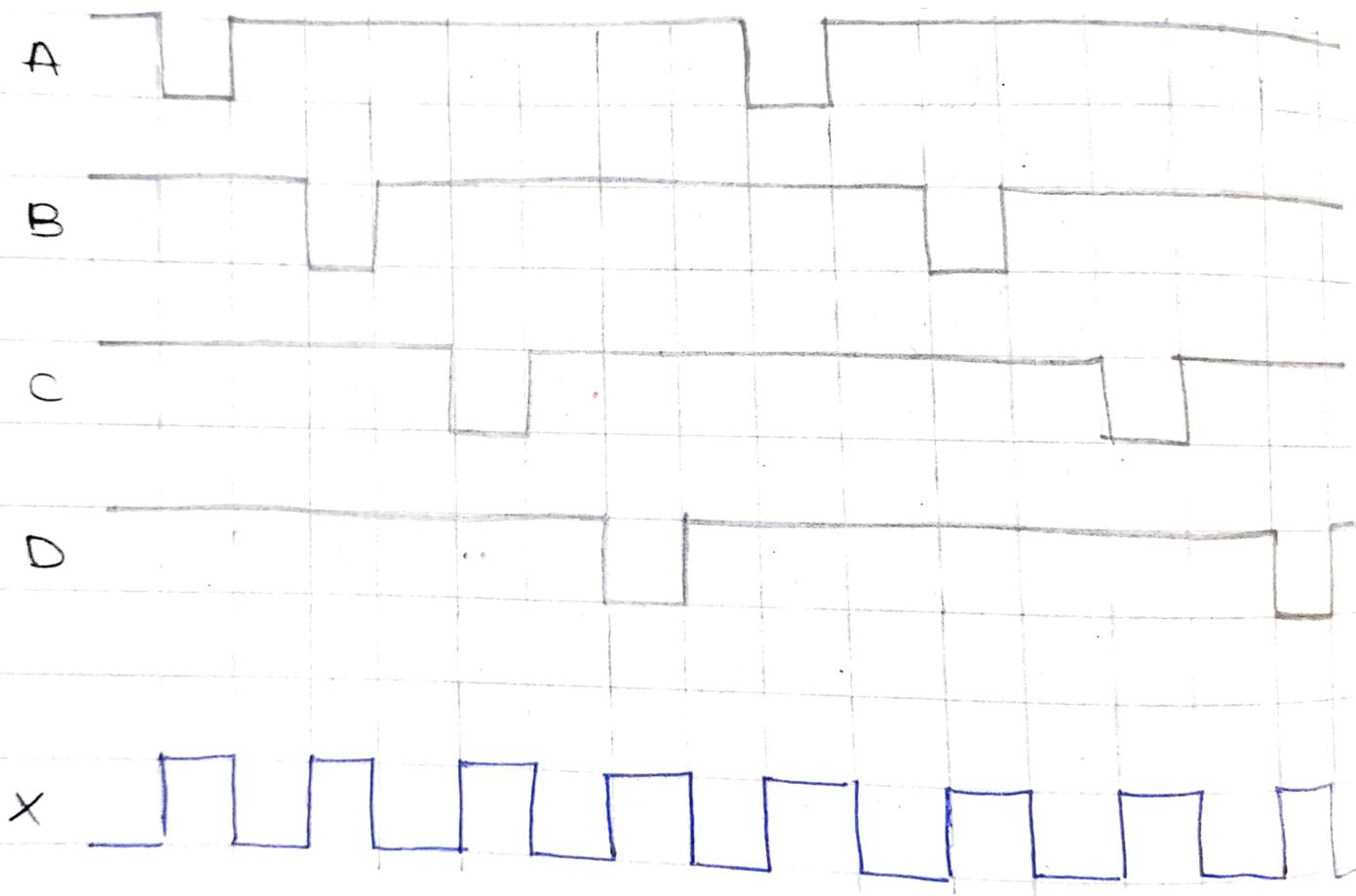
Show the output waveform for the 3-input NAND gate with its proper time relationship to the inputs.



The output waveform X is LOW only when all three inputs waveforms are HIGH as shown in timing diagram.

Example 3.14

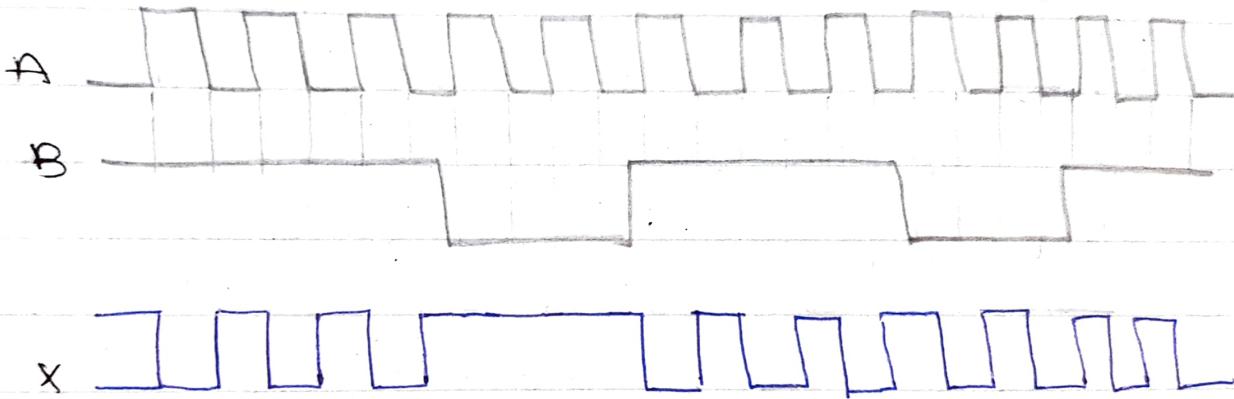
For 4-input NAND gate, operating as a negative OR gate, determine the output with respect to inputs.



The output waveform X is HIGH any time an input waveform is LOW as shown in the timing diagram.

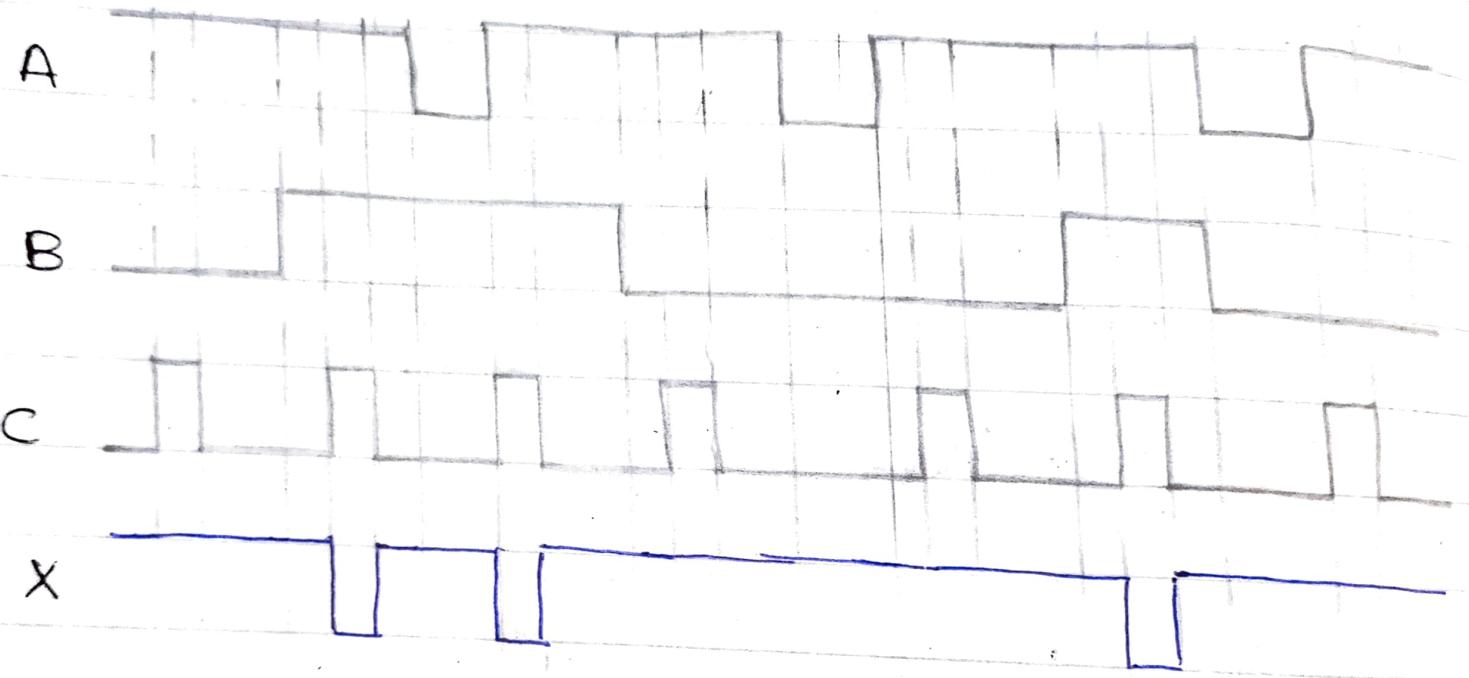
Section 3.4

17. For the set of input waveforms, determine the output for the gate and draw the timing diagram.



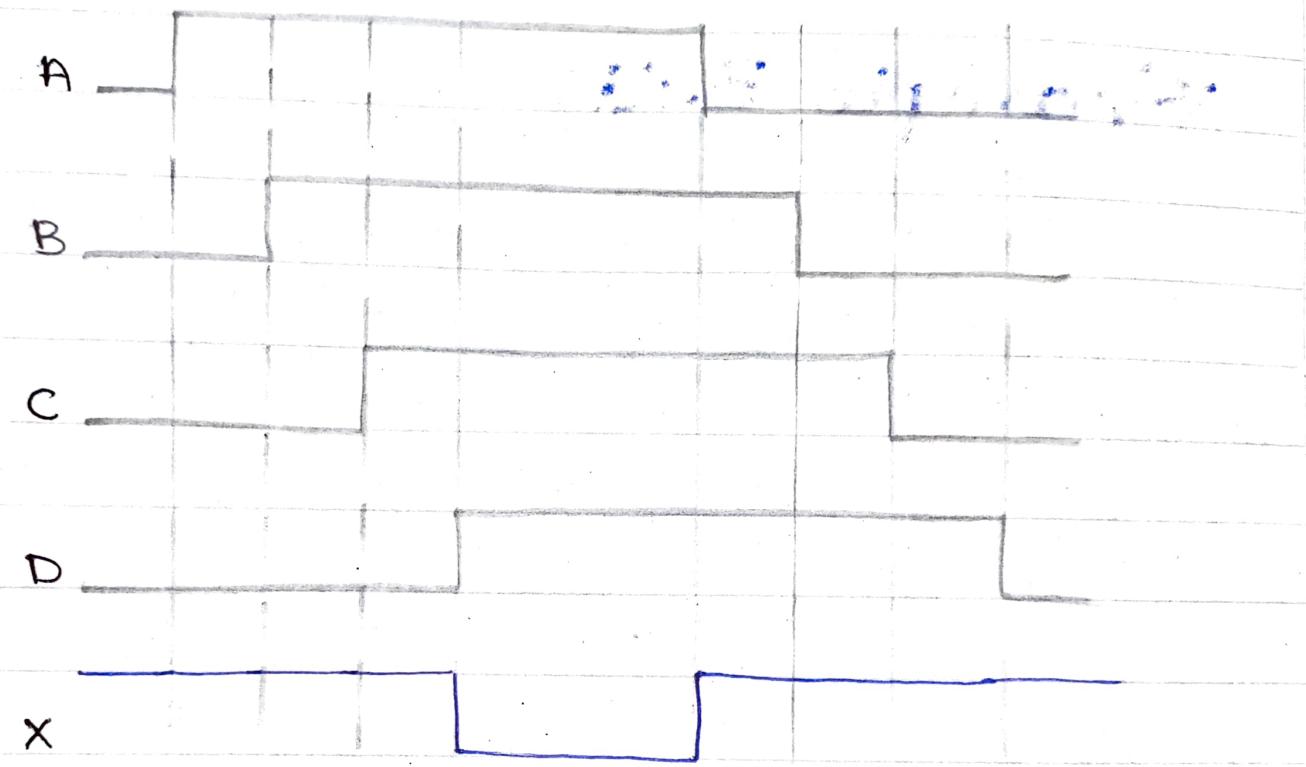
The output waveform is HIGH any time any input waveform has LOW as shown in timing diagram.

18. Determine the gate output for the input waveform and draw timing diagram.



The output waveform is HIGH anytime the input waveforms are LOW as shown in the timing diagram.

19. Determine the output waveform.

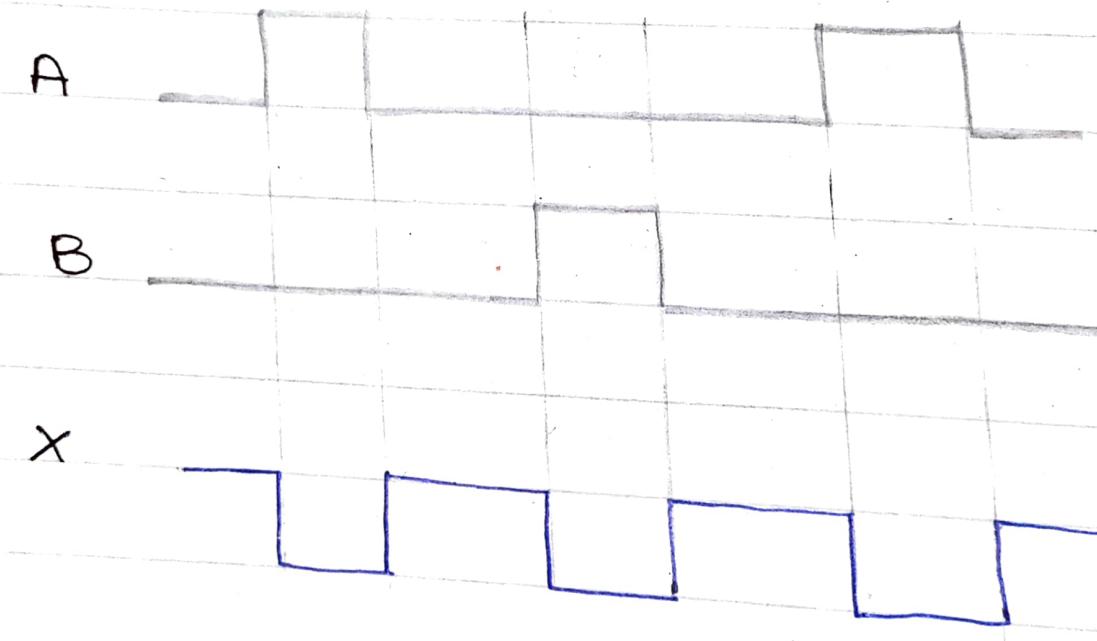


The waveform X is HIGH anytime the input waveforms are LOW.

THE NOR GATE :-

Example 3.15

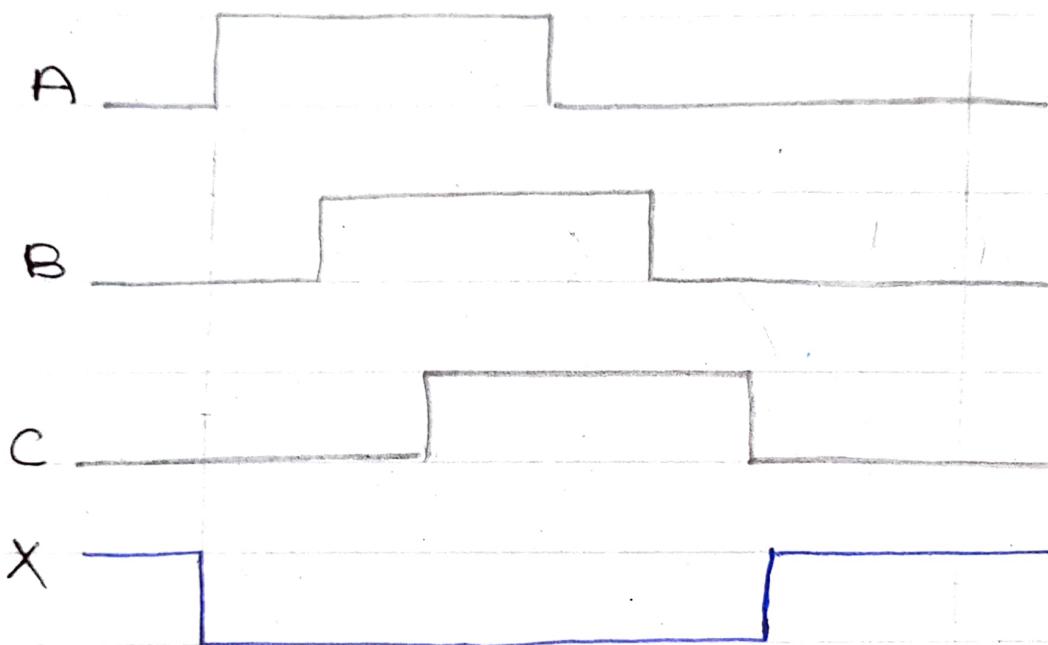
If two waveforms are applied to a NOR gate, what is the resulting output waveform?



Whenever any input of NOR gate is HIGH, the output is LOW as shown by the output waveform X in the timing diagram.

Example 3.16.

Show the output waveform for the 3-input NOR gate with the proper time relation to the inputs.

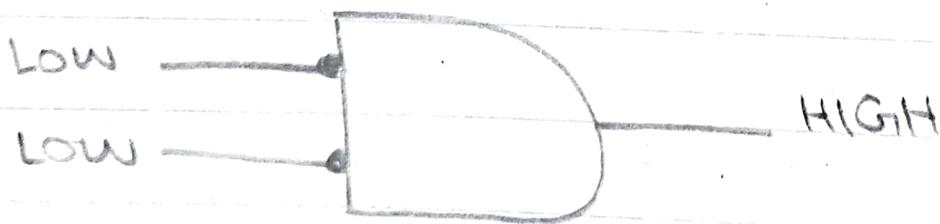


The output X is LOW when any input is HIGH as shown by the output waveform X in the timing diagram.

Example 3.17.

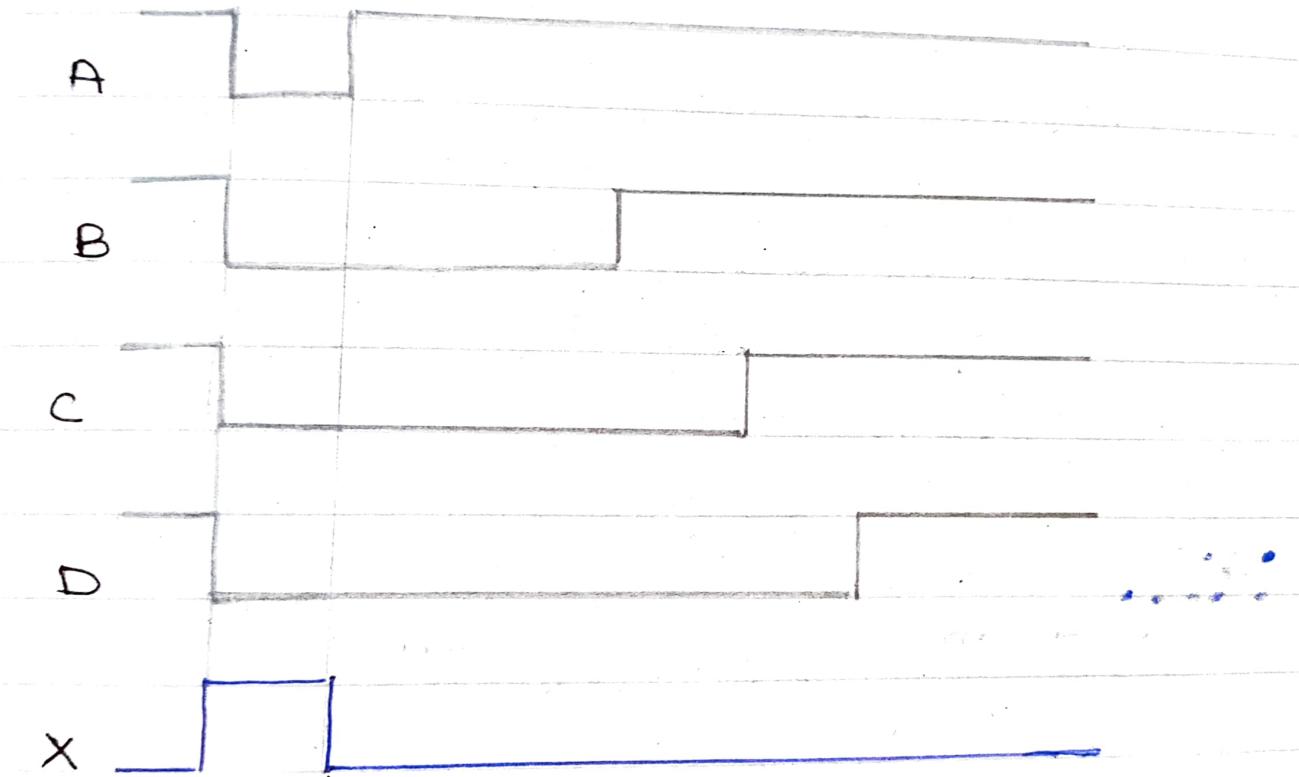
A device is needed to indicate when two LOW levels occur simultaneously on its input and to produce a HIGH output as an indication. Specify the device.

A 2-input NOR gate operating as a negative AND gate is required to produce a HIGH output when both inputs are LOW.



Example 3.19

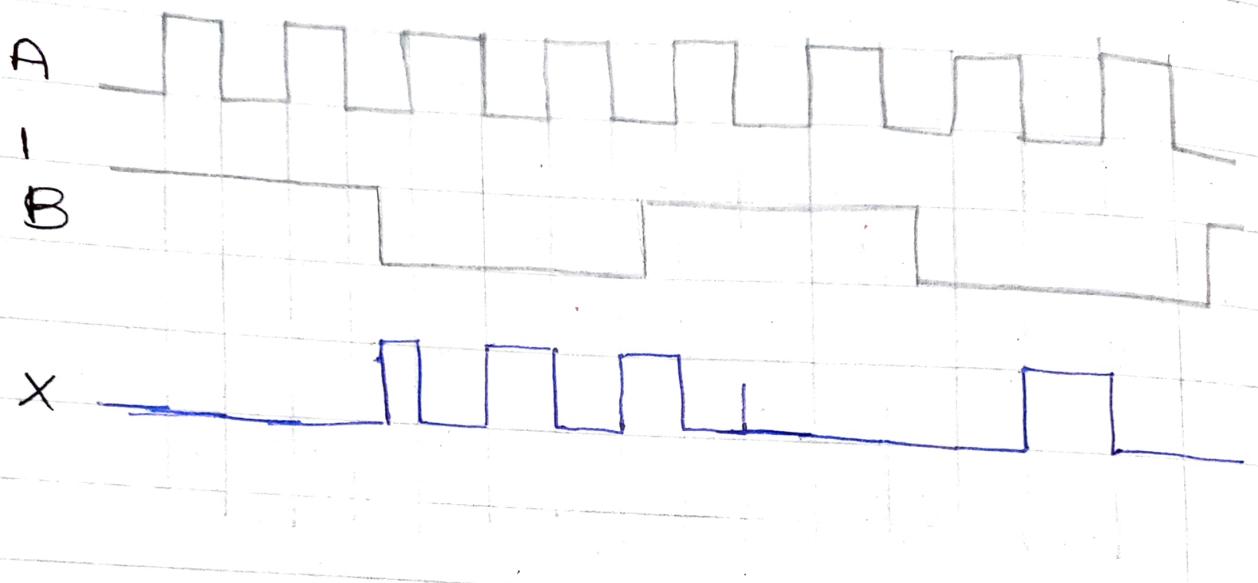
For the 4-input NOR gate operating as a negative-AND, determine the output relative to the input.



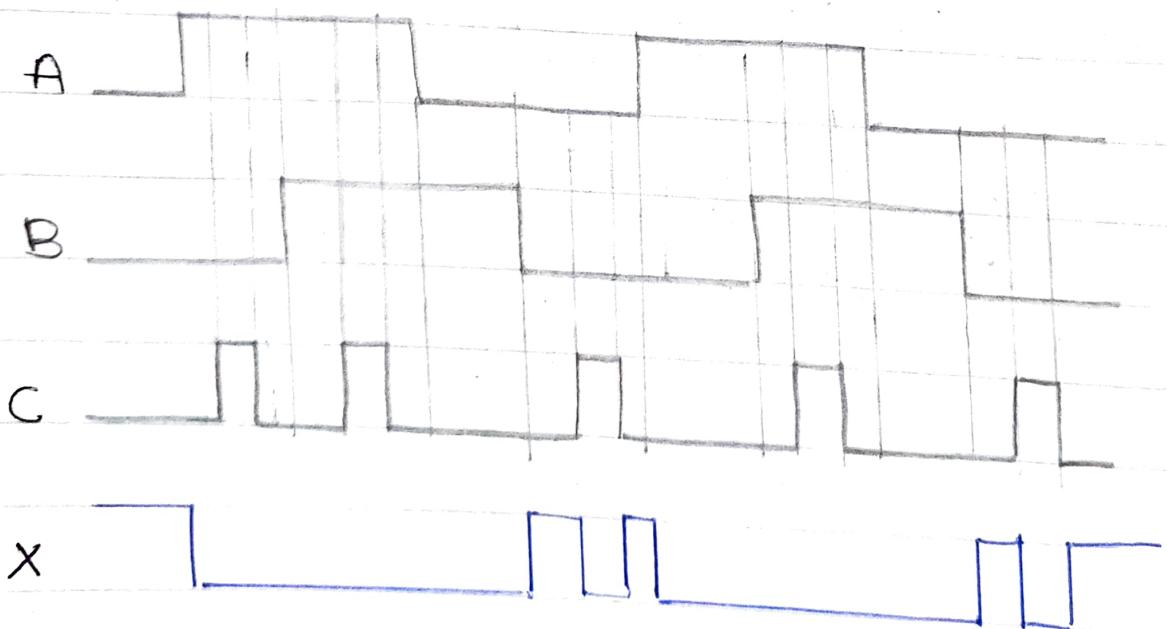
Anytime all of the input waveforms are LOW, the output is HIGH as shown by the output waveform X in the timing diagram.

Section 3.5

- 21.** Repeat problem 17 with 2-input NOR gate.

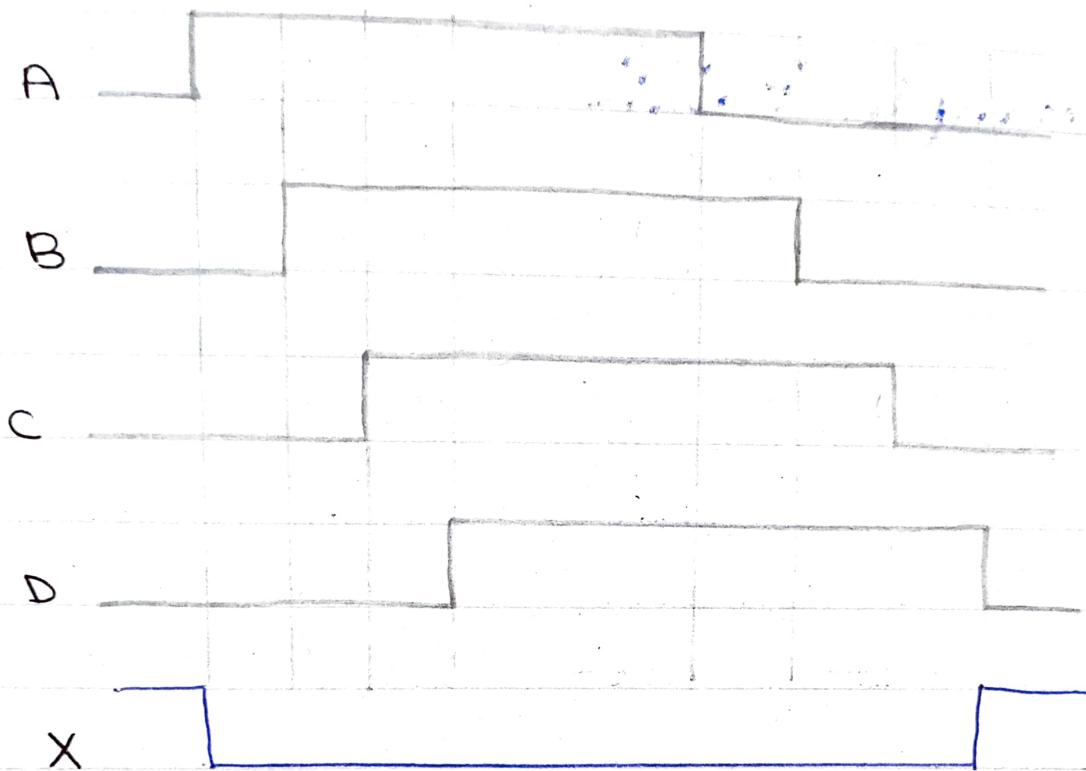


- 22.** Determine the output waveform and draw timing diagram.



The output waveform X is low where any of input waveform is HIGH.

23. Repeat problem 19 for a 4-input NOR gate.

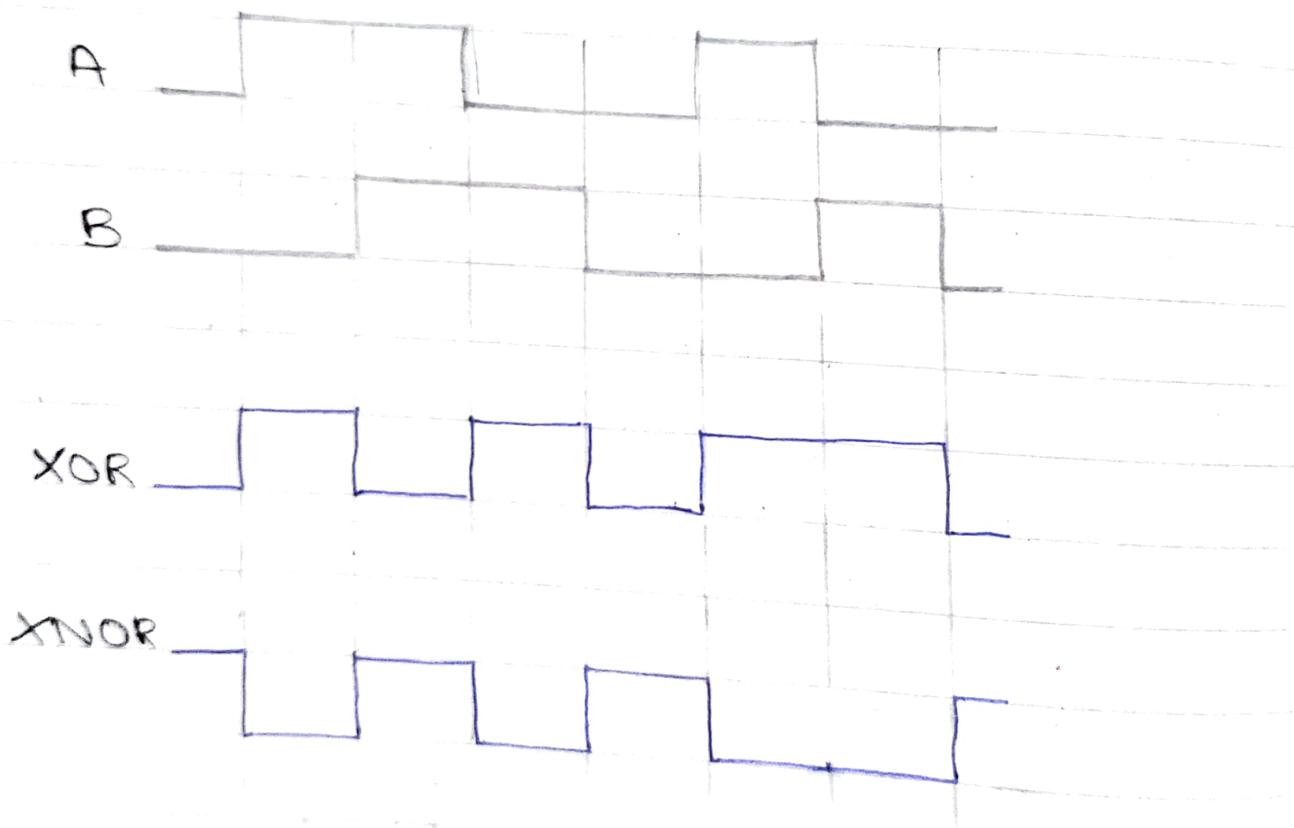


The output waveform X is LOW where any of the input waveforms is HIGH.

EXCLUSIVE-OR AND EXCLUSIVE-NOR GATE:-

Example 3.21

Determine the output waveforms for the XOR gate and for XNOR gate given input waveforms A and B.



The XOR output is HIGH only when both inputs are at opposite levels.

The XNOR output is HIGH only when both inputs are same.

Section 3.6

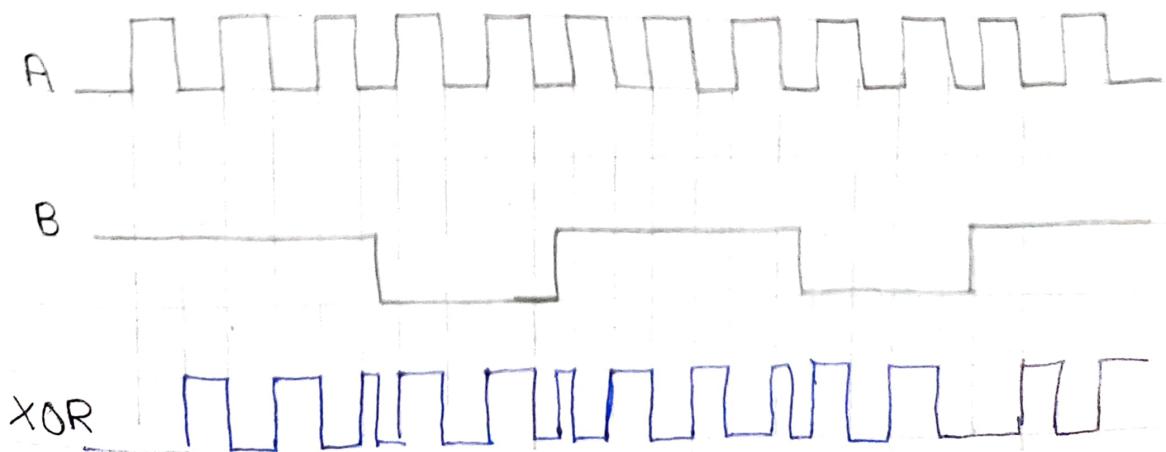
25. How does an exclusive OR gate differ from an OR gate in its logical operation?

- Exclusive OR gate is applied on only 2 - inputs but OR gate can be applied for more than 2 - inputs.
- Exclusive OR gate output is HIGH when ~~any~~ only one input is HIGH. OR gate is applied HIGH when any one of inputs is HIGH.

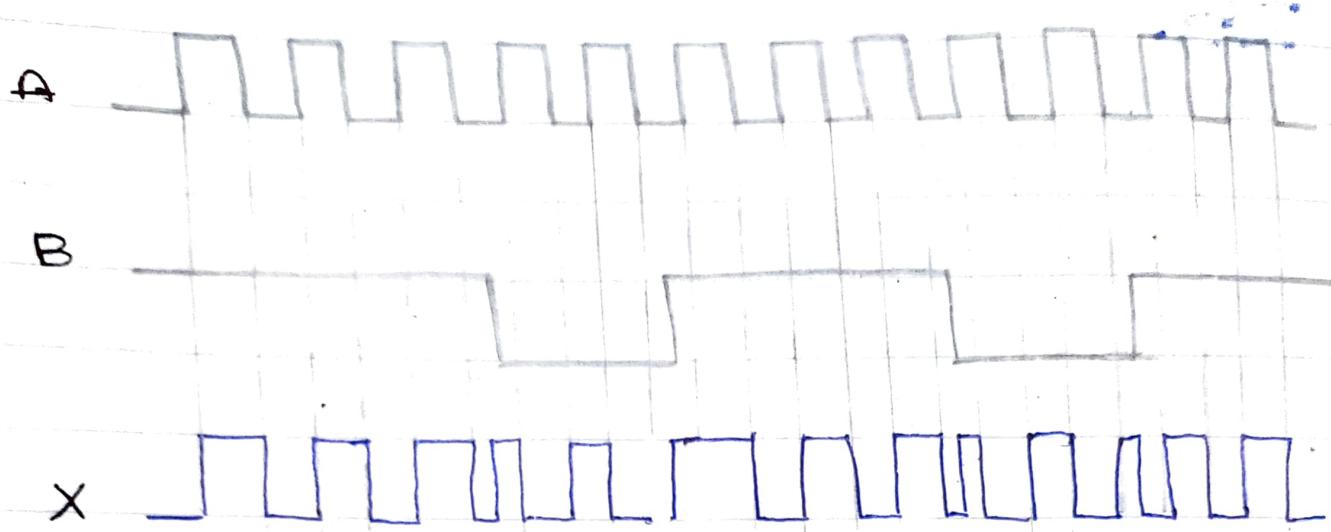
$$\Rightarrow \text{XOR} = A\bar{B} + \bar{A}B$$

$$\text{OR} = A + B$$

26. Repeat problem 17 with an exclusive OR gate.

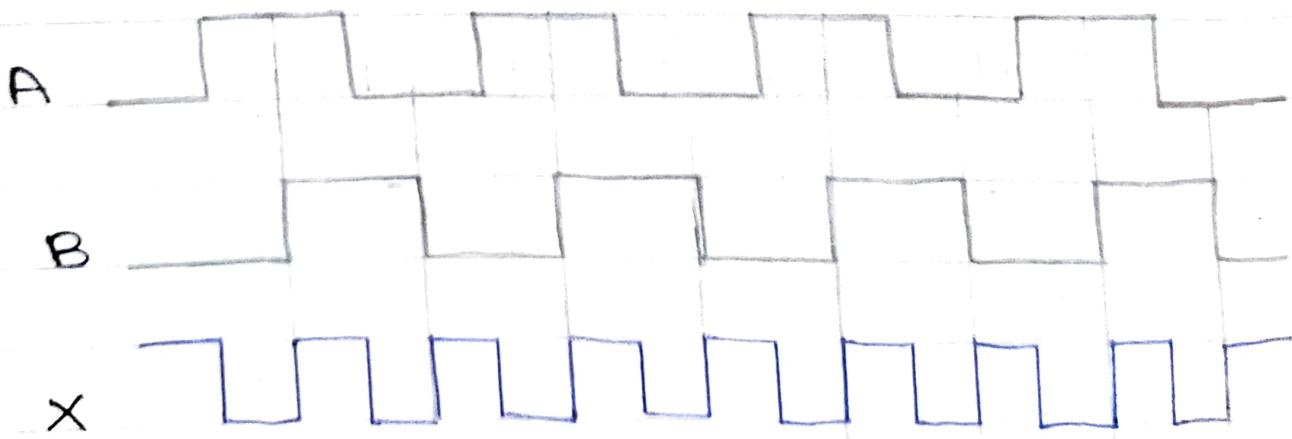


27. Repeat problem 17 for an exclusive - NOR gate.



The output is HIGH when both inputs A and B are HIGH.

28. Determine output of an exclusive NOR gate for the inputs and draw timing diagram.



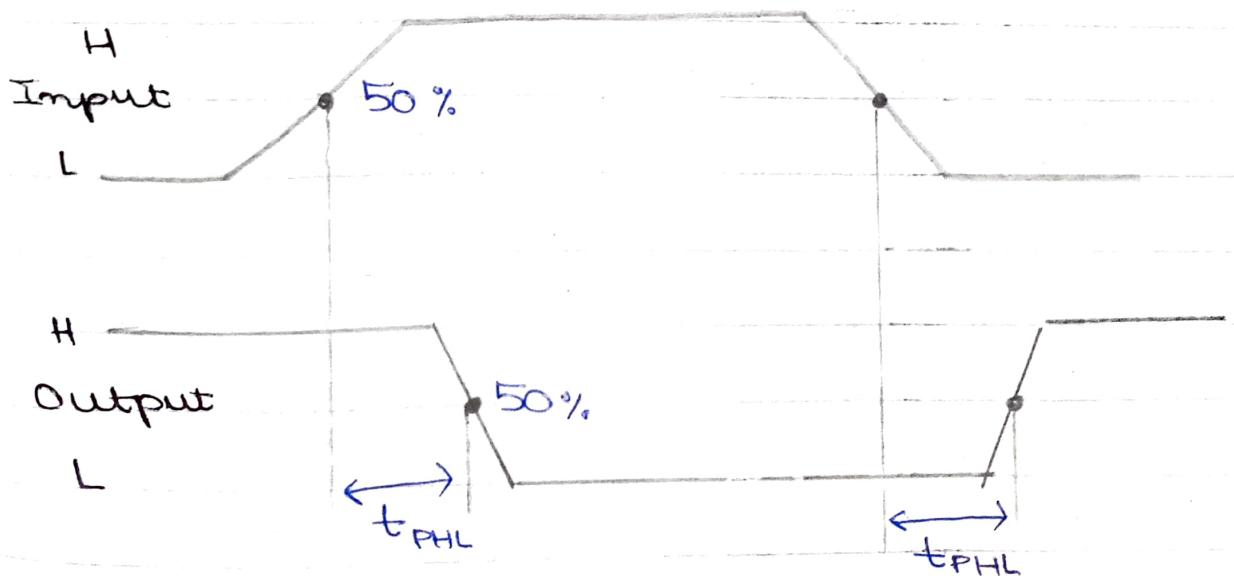
The output is HIGH when both inputs are HIGH.

FIXED FUNCTION LOGIC GATES :-

Example 3.23

Show the propagation delay times of an inverter.

An input/output pulse of an inverter is shown in figure and the propagation delay times t_{PHL} and t_{PLH} are indicated. In this case, the delays are measured between the 50% points of the corresponding edges of the input and output pulses. The values of t_{PHL} and t_{PLH} are not necessarily equal but in many cases they are same.



Example 3.24

A certain gate has a propagation delay of 5ns and $I_{CCH} = 1\text{ mA}$ and $I_{CCL} = 2.5\text{ mA}$ with a dc supply voltage of 5V. Determine the speed power product.

$$\begin{aligned}\Rightarrow P_D &= V_{cc} \left(\frac{I_{CCH} + I_{CCL}}{2} \right) \\ &= 5\text{V} \left(\frac{1\text{mA} + 2.5\text{mA}}{2} \right) \\ &= 5\text{V} (3.75\text{ mA}) \\ P_D &= 8.75\text{ mW}\end{aligned}$$

$$\begin{aligned}\Rightarrow SPP &= t_p P_D \\ &= (5\text{ ns})(8.75\text{ mW})\end{aligned}$$

$$\Rightarrow \boxed{SPP = 43.75\text{ pJ}}$$

Section 3.8

- 36.** Gate A has $t_{PLH} = t_{PHL} = 6 \text{ ns}$.
Gate B has $t_{PLH} = t_{PHL} = 10 \text{ ns}$.
Which gate can be operated at a higher frequency?

Gate A can be operated at the highest frequency because it has shorter propagation delay times than gate B.

- 37.** If a logic gate operates on a dc supply voltage of +5V and draws an average current of 4mA what is its power dissipation?

$$\Rightarrow P_D = V_{CC} \left(\frac{I_{CCH} + I_{CCL}}{2} \right)$$
$$= 5V (4mA)$$

$$\Rightarrow P_D = 20 \text{ mW}$$