Complex Engineering Problem

1 Implementation of the RISC-V Instruction Set

In this lab, we are going to implement a single-cycle implementation of the datapath and controller for a RISC-V processor.

1.1 Tasks

You are required to describe a single-cycle data path and controller for the following RV32I insruction set:

(a) R Type: `ADD, SUB, OR, XOR, AND, SLT, SLTU.`

(b) I Type: `ADDI, ORI, ANDI, SLTI, LW.`

(c) B Type: `BEQ, BNE.`

A reference for different machine code fields corresponding to different instructions is given on page 130 of https://github.com/riscv/riscv-isa-manual/releases/download/Ratified-IMAFDQC/riscv-spec-20191213.pdf . Refer page 13 onwards for explanation.

Chapter 7 of your textbook covers single cycle in detail.

First write the assembly code and then the machine code for a program that computes the greatest common divisor (GCD) of two numbers present in the main memory (not the register file) using the algorithm given in Listing 1 and stores the GCD in the register file only.

```
done = 0;
A = First Number;
B = Second Nubmer;
while(!done ){
        if ( A < B ) swap A and B;s
        else if ( B != 0 ) A = A - B;
        else done = 1;
}
Y = A;
```

Listing 1: Algorithm for calculating GCD of two numbers A and B.

Use `initial` blocks with `readmemh` in the behavioral models of instruction memory and main memory to initialize them to your machine code for the GCD algorithm and two input numbers, respectively. (It can also be done in an always block but that would happen again and again rather than just at the start).

```
reg [7:0] example_memory [7:0];
initial
$readmemh("example.mem", example_memory);
```

Listing 2: Verilog code for loading a example.mem to a memory named *example_memory*

Test the assembly code in QuestaSim and check the register file's contents in QuestaSim's memory view section. You will find the memories under the *Memory List* tab of your simulation window. If it is not visible go to *View* and check the *Memory List (w)*. In the *Memory List* tab, double click the memory you want to view and it will open.

1.2 Deliverables

(a) Diagram for single cycle datapath and controller.

(b) Simulation of your processor in Questasim.

The collaboration between students is encouraged, but blind code sharing/copying is not allowed. If you are unable to explain anything in your code, it will be assumed you have copied it. So make sure you know everything you have written in your code. I am least concerned about how you have learnt something as long as you have learnt it well.

2 Acknowledgements

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