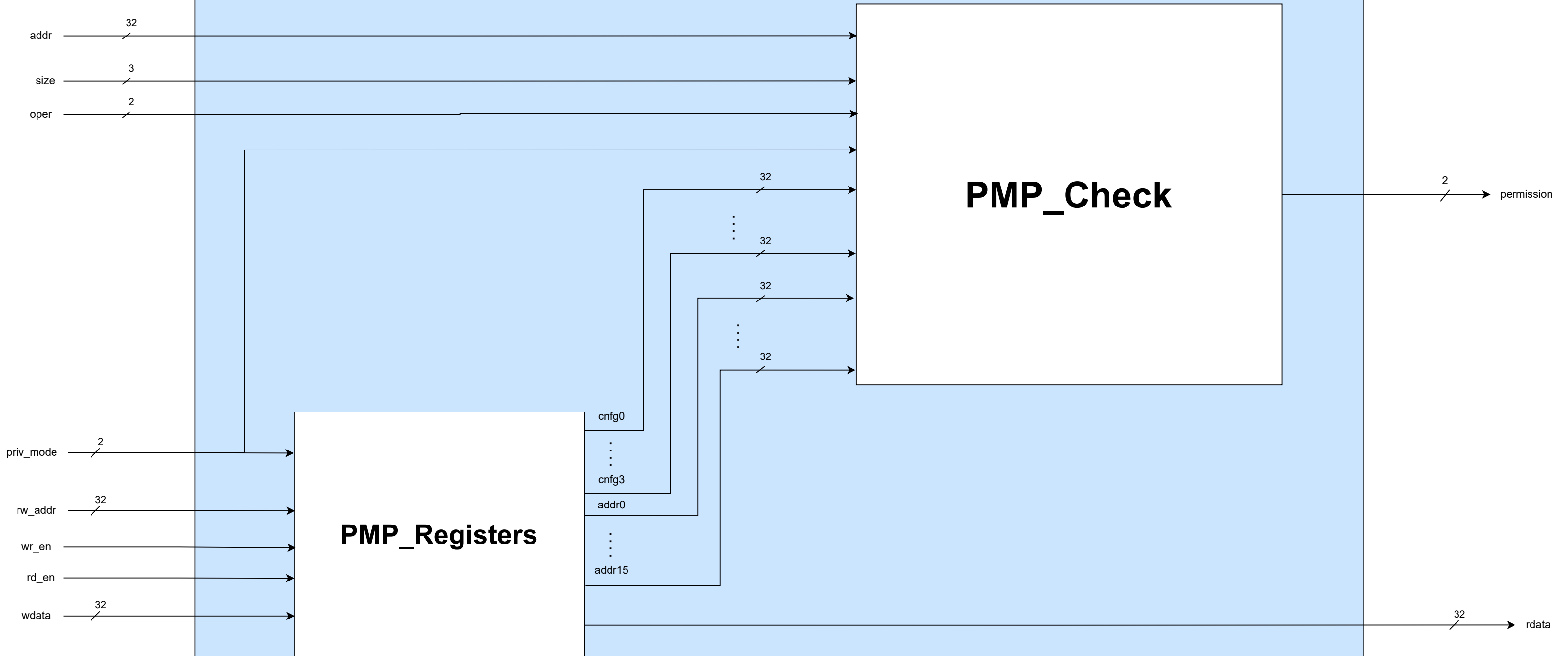


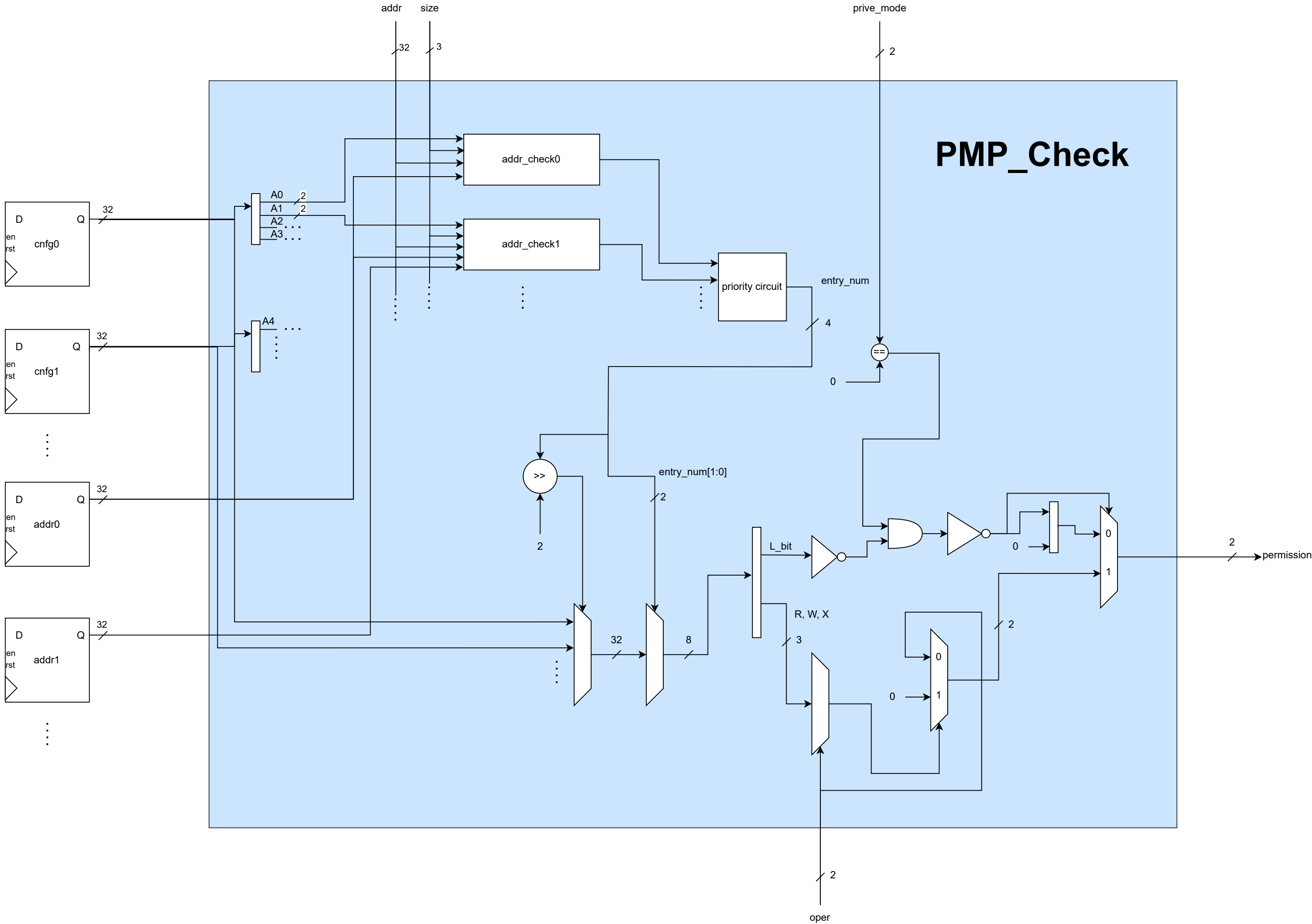
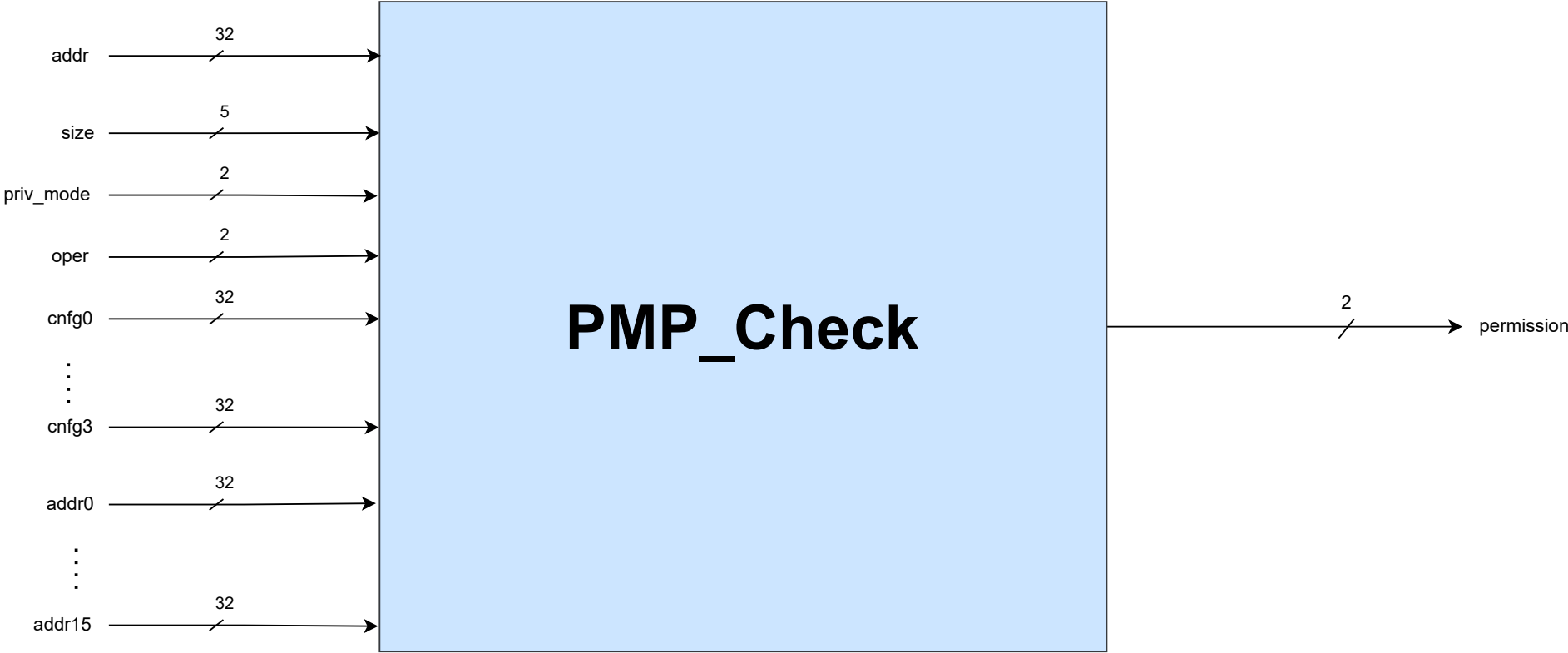
The diagram illustrates the Physical Memory Protection (PMP) architecture. It features two main functional blocks: **PMP\_Registers** and **PMP\_Check**.

- PMP\_Registers**: This block receives five external inputs from the left. It outputs four 32-bit configuration registers (`cnfg0`, `cnfg3`, and two intermediate registers indicated by vertical dots) and one 32-bit address register (`addr0`, with intermediate registers indicated by vertical dots up to `addr15`). A fifth output line from the bottom of the block represents a global enable or status signal.
- PMP\_Check**: This block receives five external inputs from the top. It also receives four 32-bit configuration registers (`cnfg0`, `cnfg3`, and two intermediate registers indicated by vertical dots) and one 32-bit address register (`addr0`, with intermediate registers indicated by vertical dots up to `addr15`) from the **PMP\_Registers** block. The `addr0` signal is specifically labeled with a '32' and a slash, indicating its width.

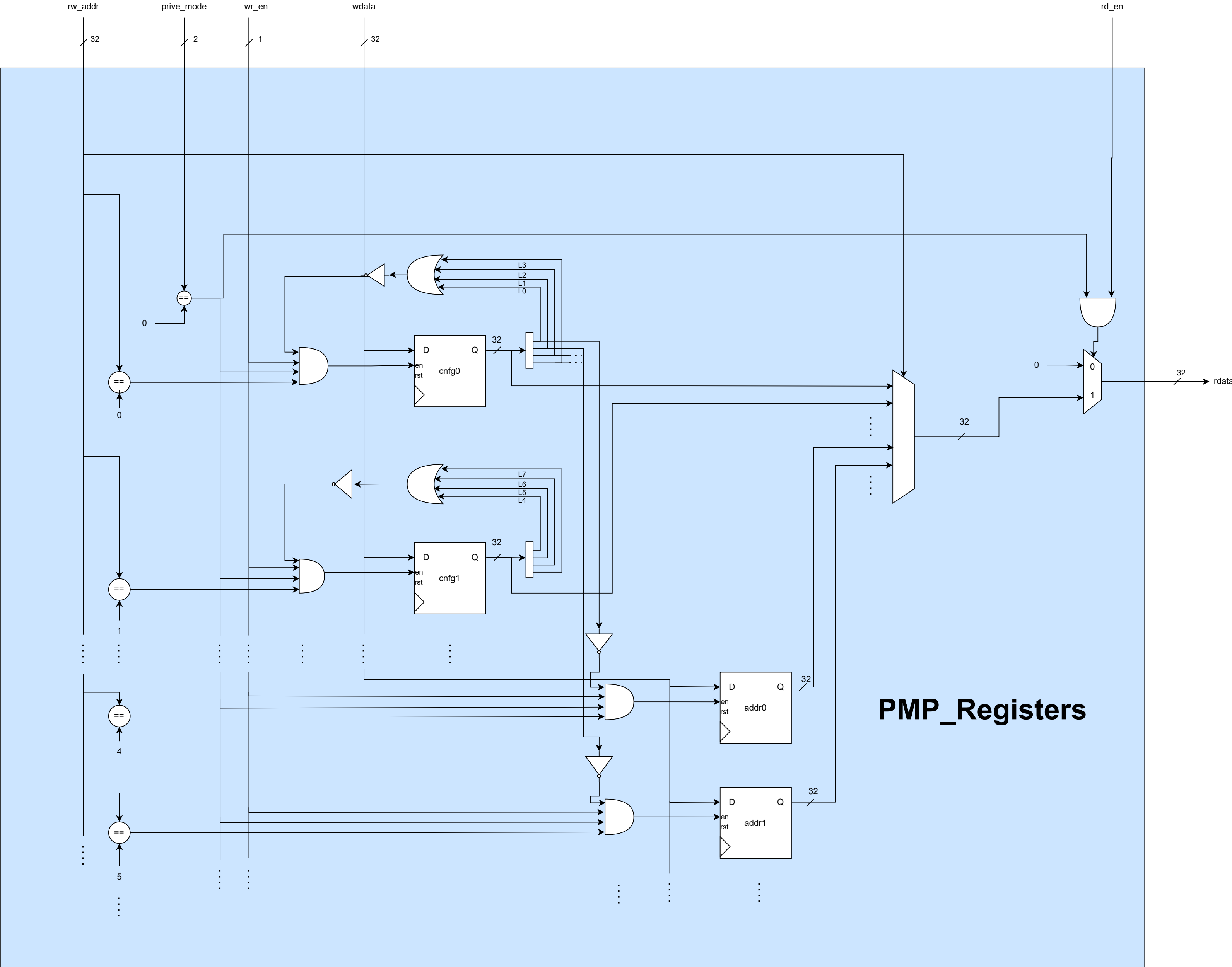
The overall system is titled **Physical Memory Protection**.



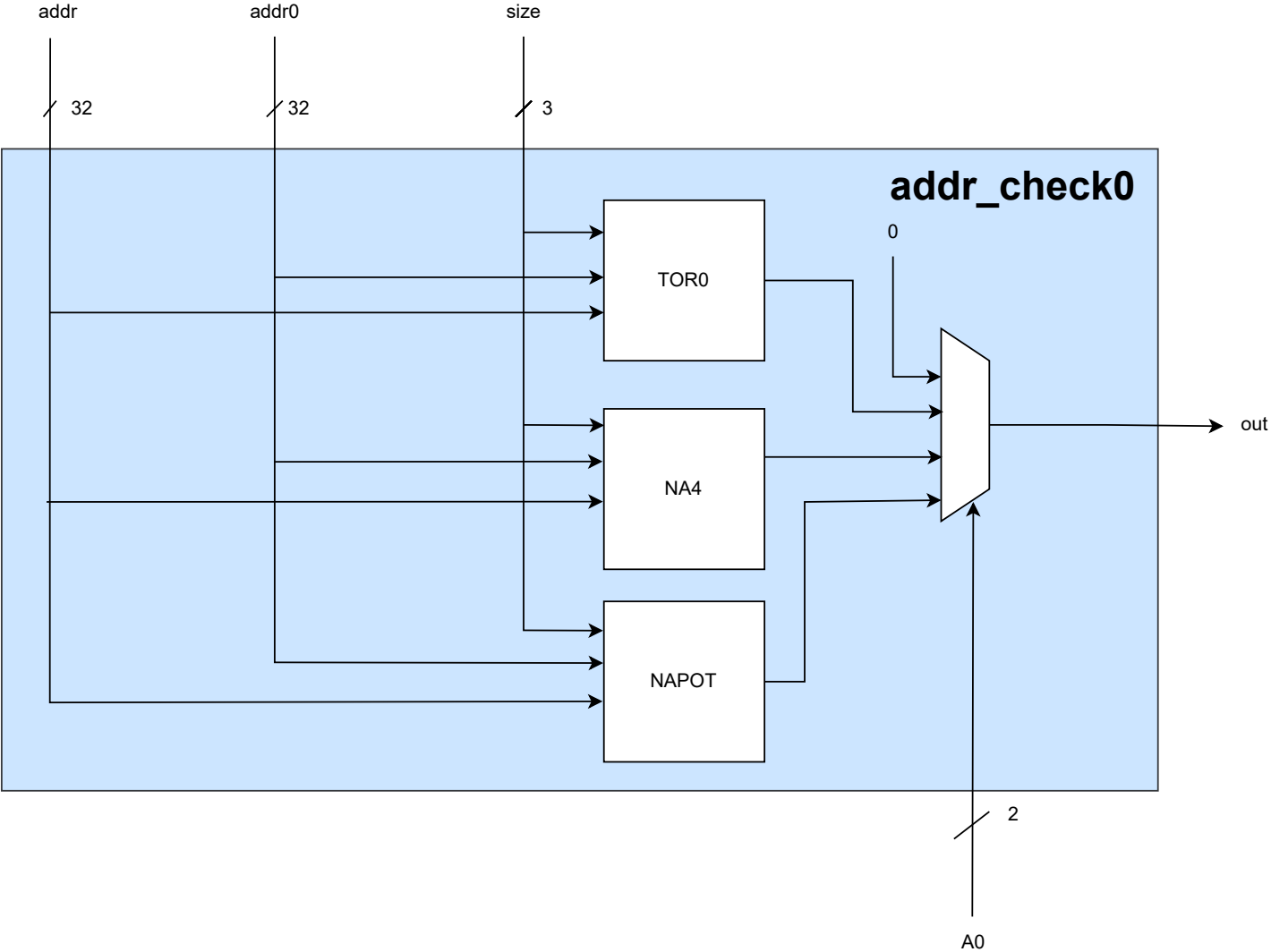
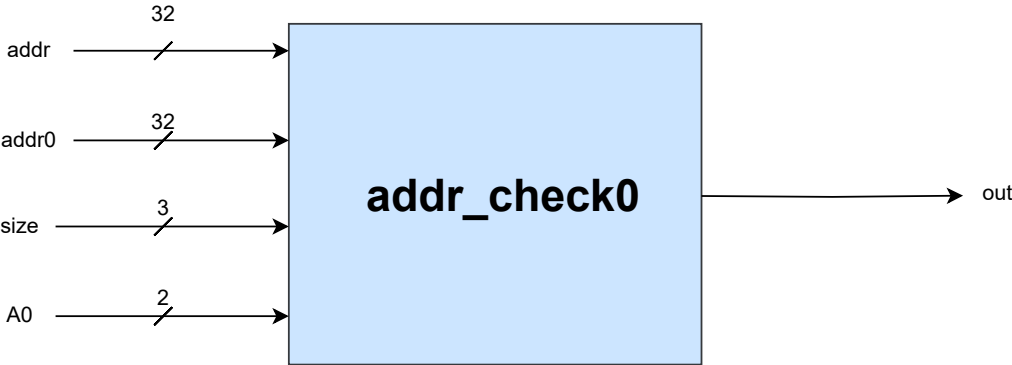
Pinout Diagram



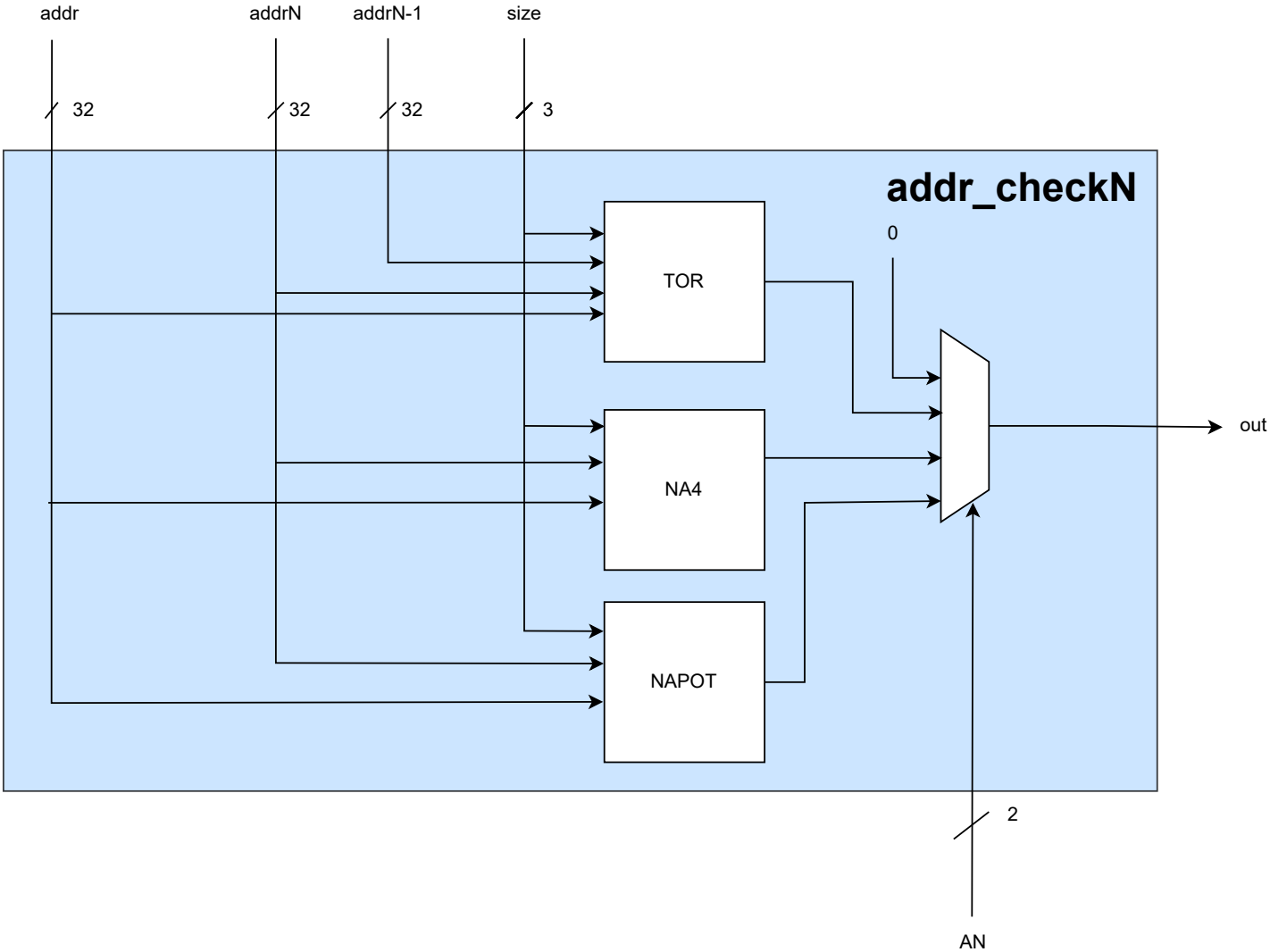
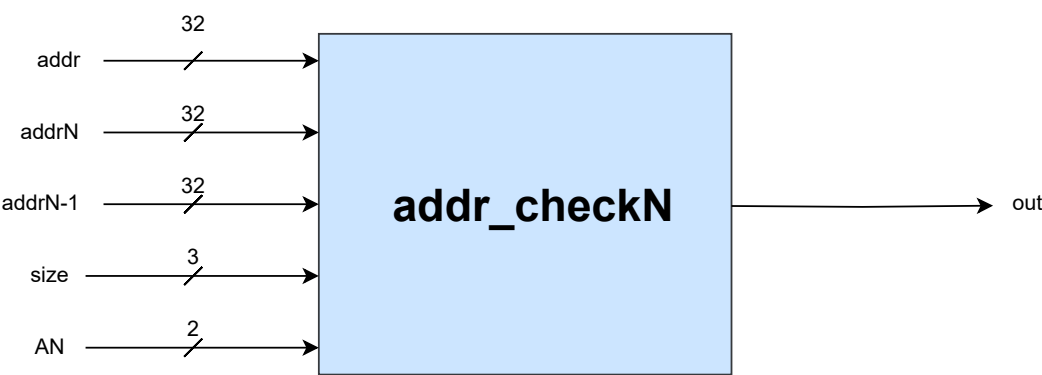
# Pinout Diagram



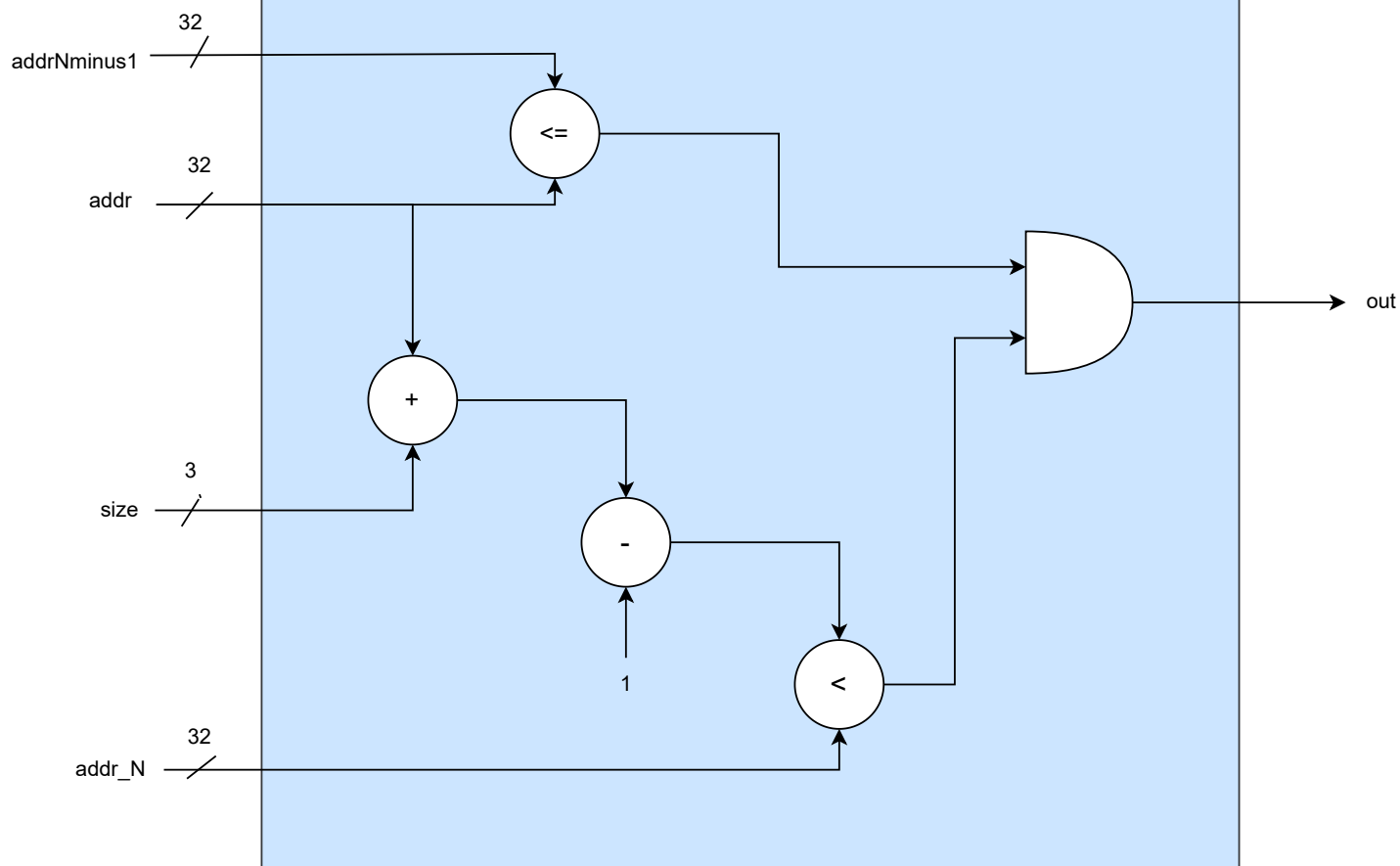
# Pinout Diagram



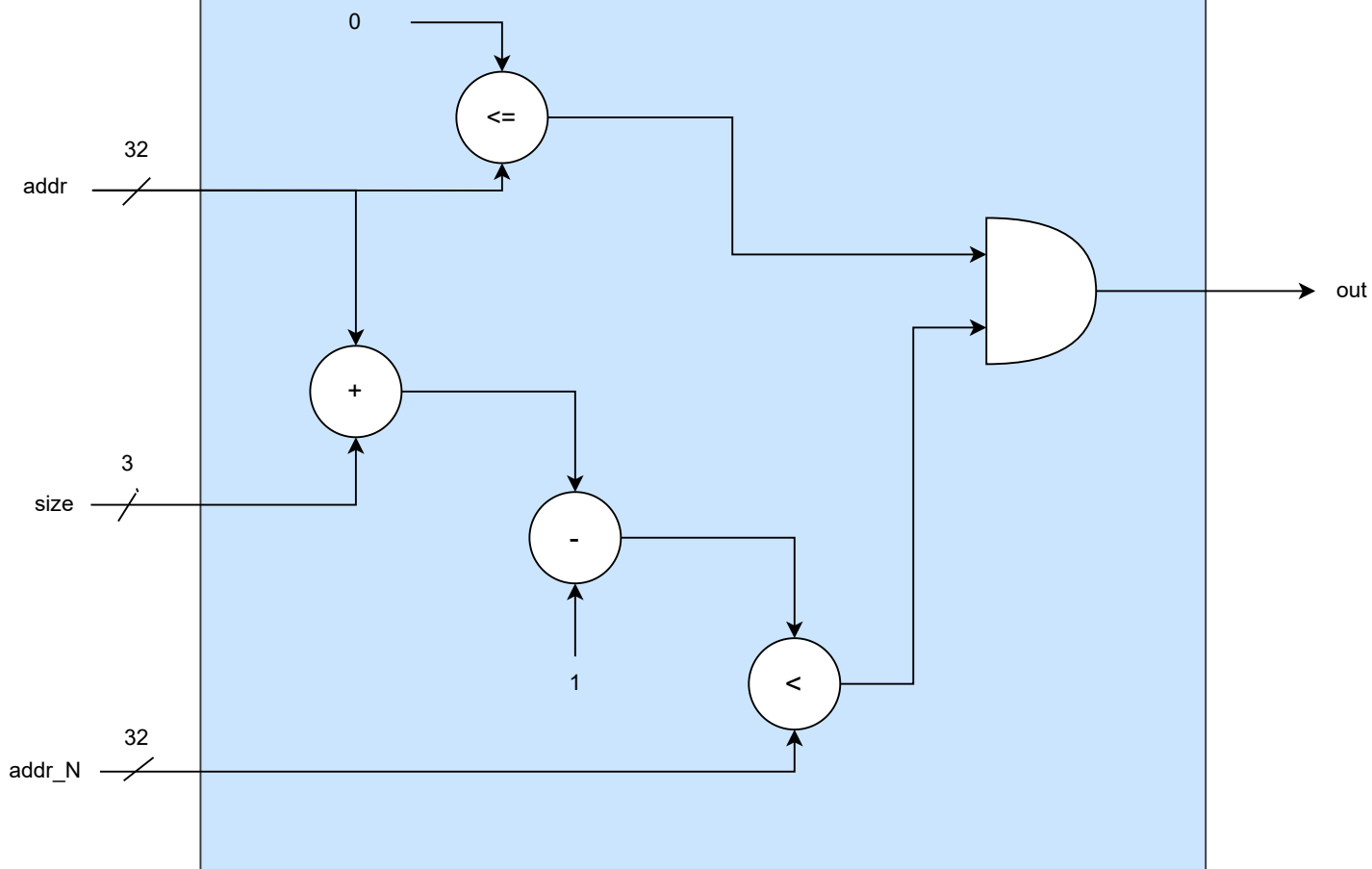
# Pinout Diagram



# TOR



# TOR0



# NA4

