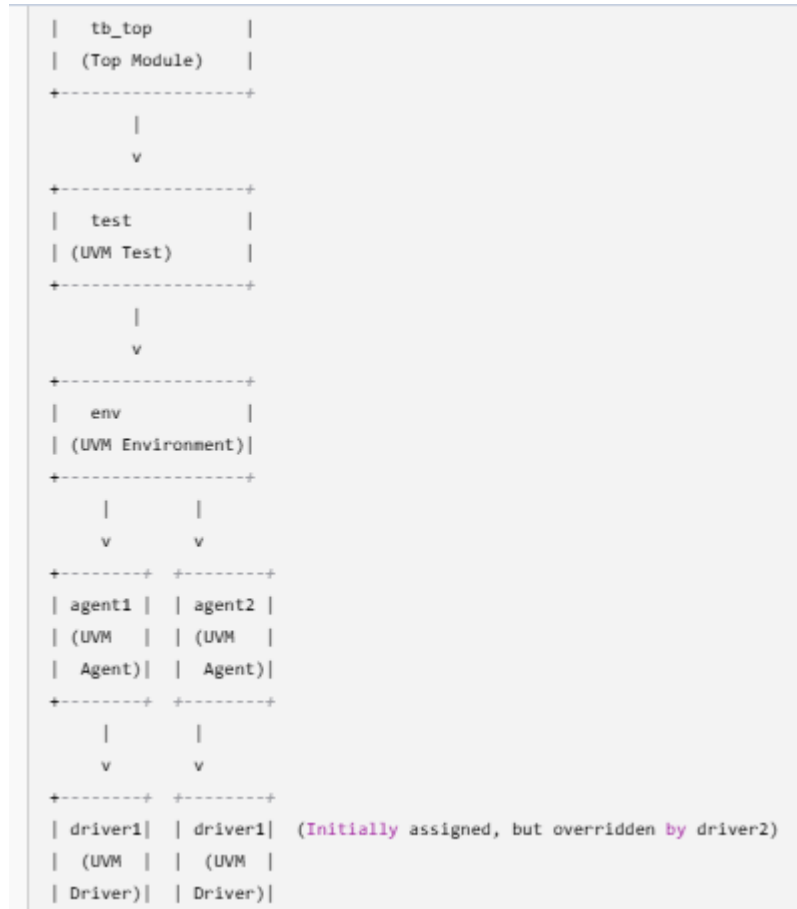


Lab 04: Understanding Dynamic Construction using UVM Factory and Component Overriding

Objective: To learn how to dynamically construct components using the UVM factory and override components at runtime



Step 1: Create Driver1 and Extend Driver2

- Create a file named **driver1.sv**.
- Extend from **uvm_driver** and print a message inside **build_phase()**.
- Create another file named **driver2.sv**.
- Extend **driver2** class from **driver1** class and override **build_phase()** to print a different message.

Step 2: Build Two Agents

- Create two files: **agent1.sv** and **agent2.sv**.

- Extend both classes from `uvm_agent`.
- Inside each agent, instantiate and create driver1 using build phase.

Step 3: Build the Environment

- Create a file named **env.sv**.
- Extend from `uvm_env`.
- Instantiate and create two agent classes (agent1 and agent2) using the build phase.

Step 4: Create a Basic UVM Test Without Sequences

- Create a file named `test.sv`.
- Extend from `uvm_test`.
- Register with UVM factory
- Inside `build_phase()`, create environment using `type_id::create`, use `set_type_override_by_type()` to replace driver1 with driver2.
- Print the test topology using
function `void end_of_elaboration_phase(uvm_phase phase);`

```

        super.end_of_elaboration_phase(phase);

        `uvm_info("TEST", "Printing UVM Topology:", UVM_NONE)

        uvm_top.print_topology();

    endfunction

```

Step 5: Create the Top-Level Module

- Create a file named **tb_top.sv**.
- Use `run_test("test")` to execute the testbench.
- Draw the block diagram of developed code.

- Expected output

Name	Type
-----	-----
uvm_test_top	test
e	env
a1	agent1
d	driver2
rsp_port	uvm_analysis_port
seq_item_port	uvm_seq_item_pull_port
a2	agent2
d	driver2
rsp_port	uvm_analysis_port
seq_item_port	uvm_seq_item_pull_port
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- Comment the override line to observe the difference.
- Use `set_inst_override_by_type()` to override only one instance of driver1 inside a specific agent. Observe the result.