Wishbone-Compliant Slave Memory

1. Overview

This document specifies the Wishbone-compliant slave memory module, which acts as a memory storage unit in a Wishbone bus system. The module follows the Wishbone B4 specification, supporting single read/write cycles with data granularity control.

2. Compliance with Wishbone Standard

The module is designed to comply with the **Wishbone B4 Specification**, supporting **Classic and Pipelined Bus Cycles** and including signal-handling requirements as per the **Wishbone Slave Interface**.

2.1 Supported Features

- Classic Read/Write Cycles
- Pipeline Read/Write Cycles
- Configurable Data Width (8, 16, 32, or 64-bit)
- Byte-Enable Signal (SEL) for partial-word selection
- Error Signaling (ERR_O)
- Acknowledgment Signal (ACK_O)
- Stall Signaling (STALL_O)
- Supports up to 32 Register Memory Locations

3. Interface Signals

Signal Name	Direction	Width	Description
clk_i	Input	1-bit	System clock signal
rst_i	Input	1-bit	Active-high reset signal
adr_i	Input	ADDR_WIDTH	Address input (4-bit, selects register)
dat_i	Input	DATA_WIDTH	Data input bus (width: 8, 16, 32, or 64-bit)
dat_o	Output	DATA_WIDTH	Data output bus (width: 8, 16, 32, or 64-bit)
sel_i	Input	SEL_WIDTH	Byte-enable selection mask

we_i	Input	1-bit	Write enable (1: write, 0: read)
stb_i	Input	1-bit	Strobe signal indicating a valid transfer
cyc_i	Input	1-bit	Cycle valid signal (indicates ongoing transaction)
ack_o	Output	1-bit	Acknowledge signal (indicates successful transfer)
err_o	Output	1-bit	Error signal (1: invalid address access)
stall_o	Output	1-bit	Stall signal (1: slave is busy)

4. Functional Description

4.1 Reset Behavior

- When rst_i is asserted, the module enters **IDLE state**.
- All registers are initialized to 0.

4.2 Master/Slave Architecture

- The DUT is slave, your testbench must act as master.

4.3 Read Cycles

- See the protocol waveforms in Wishbone Specification Document B4.

4.4 Write Cycle

- See the protocol waveforms in Wishbone Specification Document B4.

5. Address and Data Organization

- The module supports **16 registers (REGISTER_NUM = 32)**.
- Each register can store data of width **DATA_WIDTH** (default: 32-bit).
- **Granularity (GRANULE)** defines access size:
    - DATA_WIDTH = 32 → SEL_WIDTH = 4 (byte select granularity)

6. Error Handling

- If adr_i exceeds the number of registers (REGISTER_NUM), err_o = 1.
- If stb_i is deasserted before completion, the operation is aborted.

7. Parameterization

Parameter	Default	Description
ADDR_WIDTH	4	Address bus width
DATA_WIDTH	32	Data bus width
GRANULE	8	Data granularity
REGISTER_NUM	16	Number of registers
SEL_WIDTH	DATA_WIDTH / GRANULE	Byte select width

8. Summary

- This Wishbone-compliant memory module serves as a slave device that processes read and write operations efficiently.
- It supports variable data widths, granularity selection, and error handling.
- The module follows the Wishbone B4 standard ensuring compatibility with standard Wishbone masters.

References

- OpenCores Wishbone Specification B4

  https://cdn.opencores.org/downloads/wbspec_b4.pdf