Name: Total Time: 30 Mins
Student ID: Total Marks: 10

Q1. Given a processor that executes instruction in 5 stages and time taken by each stage is: IF=ID=EX=MA=30nsec and WB is divided into two half cycle, each half is of 15ns (first half cycle for write and second half cycle for read). If this processor is pipelined, what should be the clock cycle time and clock frequency of the pipeline processor? What is the speed up of pipelined processor over its non-pipelined counterpart? **(3 Marks)**.

Q2. Consider the following RISC-V assembly code:

1. lw $10, ($1)
2. lw $11, ($2)
3. add $12, $10, $11
4. and $08, $09, $05
5. add $09, $11, $12
6. sub $15, $09, $14

Assume a five-stage pipeline, answer the following questions:

a) Write name and type of all hazards with line numbers and underlying causes. **(3 Marks)**.

b) Draw a timing diagram (not the logical circuit) of pipelined execution of instructions on line number 2, 3, and 4. Assume every stage takes one clock cycle. **(2 Marks).**

Solution 1:

Clock Cycle Time= Max (Ti) = 30ns (WB)

Frequency= 1/clock cycle time= 1/30ns=33.3 MHz

Speed up= (30+30+30+30+30) /30 = 5.

Solution 2:

(a) Line 2-3 Load Delay

(b) Line 5-6 RAW

(c) Line 3-5 RAW

(d) Line 1-2 Structural Hazard

Inst. 2	**IF**	**D**	**EX**	**MA**	**WB**	
Inst. 3		**IF**	**D**	**EX**	**WB**	
Inst. 4			**IF**	**D**	**EX**	**WB**