



National University of Computer & Emerging Sciences, Karachi

Fall-2017 CS-Department

Term Examination No. 1



20th September 2017, 11:00 am – 12 noon

Course Code: EE 204	Course Name: Computer Architecture
Instructor Names: Dr. Hasina Khatoon + Faraz Idris	
Student Roll No:	Section No:

Instructions:

- Read each question completely before answering it. There are **3 questions on 2 pages**
- **Attempt all questions**
- In case of any ambiguity, you may make assumptions, but your assumption should not contradict any statement in the question paper.

Time: 1 Hr (60 minutes).

Max Marks: 60

Q1 (i) A byte **A9h** is loaded into a 32-bit register of a MIPS-like architecture. Give the contents of the register (in hexadecimal) after the load operation, if the operand is (1) signed and (2) unsigned. (3)

- (ii) What are the major characteristics of Personal Mobile Devices (PMDs)? (4)
- (iii) Why are benchmarks not valid indefinitely? (4)
- (iv) Differentiate between ILP (Instruction Level Parallelism) and TLP (Thread Level Parallelism). (4)
- (v) What do you understand by temporal and spatial locality? (4)
- (vi) State the operation performed by each of the following description language expressions: (4)

Regs [R1] $\leftarrow_{64} [0]^{32} \# Mem[40 + Regs[R2]]$

Mem[50 + Regs[R4]] $\leftarrow_{64} Regs[R3]$

(vii) Name three most frequently used addressing modes in processors. (2)

(viii) Why are RISC processors referred to as load/store architecture? (4)

(ix) Mention a compiler optimization technique that is referred to as a high-level compiler optimization and is not machine dependent. (4)

Q2 (a) A processor is enhanced by a graphics unit that achieves a speedup of 15 for graphics instructions. If the observed overall speedup of a program is 2 when run

$$\frac{1}{\left(1 - \frac{\text{fraction enhanced}}{\text{speed enhanced}}\right) + \frac{\text{fraction enhanced}}{\text{speed enhanced}}}$$

on the enhanced processor, what is the percentage of graphics instructions in the example application? (7)

Q2 (b) A computer M runs at 5 GHZ and executes an application program that has 5000 instructions. The program comprises of instructions of types ALU, Load/store, control flow and others in the following proportions: ALU instructions are 24%, Load/store instructions are 25%, Control flow instructions are 20%. The clock cycles required to execute each type of instruction are: ALU = 1.8, Load/store = 2.5, Control flow = 2.7, and others = 2.5. Give the average CPI of M. What is the execution time of the program that has 5000 instructions? (9)

Q3(a) What are the instruction set properties that help the compiler writer? (6)
Jump, Procedure call, Procedure return

Q3(b) What are the advantages of fixed length and fixed field encoding of instructions? (5)