

Computer Architecture (EE-3009)
Assignment#1
Submission Deadline: 5th March, 25

Submission Guidelines: Max mark: 60

Hand written Assignment on standard A4 sheet should be submitted.

- Write your name, roll number and section on top of the first page of the assignment.
- **Plagiarism will be treated strictly.**
- 50% reduction will be applied for late submissions

Q1 a) Describe the components of multicore computer layout. (5)

b) Illustrate and explain the processor chip for the IBM z13 processing unit. You also need to illustrate and explain the components of instruction set of z/architecture. (5+5)

Q2 a) Differentiate between microprocessor and micro-controller chip.(5)

b) Draw the block diagram of EFM32 micro-controller from Silicon Labs with Cortex-M3 processor and core components. Briefly explain all components of micro-controller and Cortex-M3 processor. (5+5)

Q3 a) Some microprocessors today are designed to have adjustable voltage, so a 20% reduction in voltage may result in a 20% reduction in frequency. What would be the impact on dynamic energy and on dynamic power? (5)

b) The owner of a shop observes that on average 20 customers per hour arrive and there are typically 10 customers in the shop. What is the average length of time each customer spends in the shop using Little's Law? (5)

c) Availability is the most important consideration for designing servers, followed closely by scalability and throughput. (2.5+2.5)

- i. We have a single processor with a failure in time (FIT) of 100. What is the mean time to failure (MTTF) for this system?
- ii. If it takes one day to get the system running again, what is the availability of the system?

Q4 Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs: Determine the effective CPI, MIPS rate, and execution time for each machine. (5+5+5)

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine B		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3