National University of Computer and Emerging Sciences

Karachi Campus

Computer Architecture (EE-3009)

Sessional-II Exam

Date: April 10th 2025

Course Instructor(s)

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Total Time (Hrs):	**1**
Total Marks:	**30**
Total Questions:	**3**

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Roll No Section Student Signature

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INSTRUCTION: Attempt all the questions in-order.

CLO # 2 **Solution**

Q1: Logical Reasoning **[3x 2=6 Marks]**

a. In load –store Architecture, what is the maximum number of operands allowed in an instruction? Does it support memory addressing?

3 operands allowed in an instruction. No it does not support memory addressing.

b. In RISC-V ISA, which encoding format is used for ALU operations and for branches?

R – Type for ALU operations (R-R) , I- Type for ALU immediate.

S/B- Type for Branches.

c. Why memory alignment restrictions are significant in architecture design?

Misalignment causes hardware complications, because the memory is typically aligned on a multiple of a word or double-word boundary. A misaligned memory access may, therefore, take multiple aligned memory references. Thus, even in computers that allow misaligned access, programs with aligned accesses run faster.

CLO # 3 **Solution**

Q2: You are given a non-pipelined processor design which has a 5 GHz clock and it uses 3 cycles for ALU operations, 2 cycles for branch operations and 4 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, and 40%, respectively. **[3x3=09 Marks]**

a. What is the best speedup you can get by pipelining it into 5 stages?

b. If the 5 stages are 1ns, 1.5ns, 4ns, 3ns, and 0.5ns, what is the best speedup you can get compared to the original processor?

c. If each pipeline stage added also adds 2ns due to register setup delay, what is the best speedup you can get compared to the original processor?

Q No: 2

Clock = 5 GHz → 0.2 ns.

3 cycles for ALU → 40%.

2 cycles for Branches → 20%.

4 cycles for Memory → 40%

Part a

Best Speed up ⇒ no. of Stages i.e 5x (ideal)

Part b

$$\text{CPU time} = \text{Clock time} \times \left(\sum_{i=1}^{n} IC_i \times CPI_i\right)$$

$$= 0.2\,ns \times [(3\times0.4) + (2\times0.2) + (4\times0.4)]$$

$$= 0.2\,ns \times [1.2 + 0.4 + 1.6]$$

$$\text{CPU time}_{old} \Rightarrow 0.64\,ns.$$

New Cycle time ⇒ Slowest Stage i.e. 4 ns.

$$\text{Speedup} \Rightarrow \frac{old}{New} \Rightarrow \frac{0.64\,ns}{4\,ns} \Rightarrow 0.16x$$

Part c

Adding Register delay → 4 ns + 2 ns ⇒ 6 ns

$$\text{Speedup} \Rightarrow \frac{old}{New} = \frac{0.64\,ns}{6\,ns} \Rightarrow 0.106x$$

***CLO # 3* Solution**

Q3: Consider the following code sequences,

- Identify the type of Dependencies (Hazards).
- Suggest a possible solution to resolve the hazard.
- Draw Pipeline diagram for each case to support your answer.

[3.5x4=15 Marks]

A)	**B)**

ld x1,45(x2)
add x5,x1,x7
sub x8,x6,x7
or x9,x6,x7
	ld x1,45(x2)
	add x5,x6,x7
	sub x8,x1,x7
	or x9,x6,x7

C)	**D)**

ld x1,45(x2)
add x5,x6,x7
sub x8,x6,x7
or x9,x1,x7
	Ld x1,0(x4)
	Ld x2,4(x4)
	add x3,x2,x1
	sd x3,8(x4)
	addi x4,x4,4

(A)

Instruction	C1	C2	C3	C4	C5	C6	C7	C8	C9
LD	IF	ID	EX	MEM	WB				
ADD		IF	ID	Stall	EX	MEM	WB		
SUB			IF	Stall	ID	EX	MEM	WB	
OR				Stall	IF	ID	EX	MEM	WB

→ RAW HAZARD B/W LD & ADD
→ Solution Stall.

(B)

Instruction	C1	C2	C3	C4	C5	C6	C7	C8	C9
LD	IF	ID	EX	MEM	WB				
ADD		IF	ID	EX	MEM	WB			
SUB			IF	ID	EX	MEM	WB		
OR				IF	ID	EX	MEM	WB	

→ RAW HAZARD B/W LD & SUB
→ Solution → Forwarding

(C)

INSTRUCTION	C1	C2	C3	C4	C5	C6	C7	C8	C9
LD	IF	ID	EX	MEM	WB				
ADD		IF	ID	EX	MEM	WB			
SUB			IF	ID	EX	MEM	WB		
ORI				IF	ID	EX	MEM	WB	

→ NO HAZARD → Read & Write of X1 takes place in different half of cycles.

→ NO ACTION Required.

(D)

HAZARDS → RAW B/W instruction 3 and 1
RAW B/W instruction 4 and 3.

Solution → Rescheduling

	C1	C2	C3	C4	C5	C6	C7	C8	C9
LD X1	IF	ID	EX	MEM	WB				
LD X2		IF	ID	EX	MEM	WB			
Addi			IF	ID	EX	MEM	WB		
Add				IF	ID	EX	MEM	WB	
SD					IF	ID	EX	MEM	WB

========== **Good Luck** ==========