1. How does performance of a system be change by increasing or decreasing time quanta. How does this time quanta would change the performance of a system when system hires only I/O bound processes.

2. What will be the impact on resource utilization if number of levels in multilevel feedback queue would be increased?

3. How does the internal fragmentation would be effected by having large fixed equal partitions?

4. Consider a system demands reduced search time compromise for storage space utilization. Which algorithm will you consider first fit, best fit or worst fit? Give reason.

5. You are given the available holes 50k , 200k, 300k, 10k. Process P1, p2, p3, p4 and p5 arrives in first come first serve order demands storage of 100, 250, 95, 270 with turnaround time 3, 4 , 2 , 5. At what time instant request of all jobs will be satisfied using best fit strategy?

6. Consider the following segment table:

Segment	base	length
0	100	200
1	345	50

What are the physical addresses for the following logical address:
a. 0, 150
b. 1, 100

7. Consider the following inverted hashed page table:

hash table index	**Index**	**pid**	**vpn**	**Next**
0x234	0x0	1	0xcvb	0x456
0x456	0x345	0	0x567	-
0x0	0x456	2	0xrtc	0xghj
0xa	0xghj	0	0x1	-

What will be the physical address for the virtual address if the hash function for given address would be 0x0.

pid	**vpn**	**offset**
0	0x1	0x123

8. Assume three process P1, P2 and P3. Process P1 uses compile time address binding while others uses execution time address binding. Show allocation of memory after compaction(You don't need to recompile processes).

p1(200K)
300K
p2(50)
100k
500k
p3(100k)

9. System supports 2251799813685248 total number of pages and 32 total frames with 8Kb page size and 1 byte entry size.

1. You are required to compute virtual address space and physical address space.
2. How much time would be required to load page table if each entry takes 100nanoseconds to bring in memory.
3. In order to reduce the search time to access the page table, you are required to breakup the page table into multiple hierarchies. Draw virtual address space after incorporating maximum hierarchies.
4. Is there any way to reduce page table size? Calculate reduced page table size.
5.Calculate memory access time for process p1, if it takes 10seconds to access main memory. (Assume that instructions of process P1 will fit in 10 pages.)
6. How much percent TLB would be effected in this case, If it supports total 32 entries.(Assume that instructions of process P1 will fit in 10 pages.)