Computer Architecture (EE-3009) Sessional-II Exam

Date: April 10th 2025

Course Instructor(s)

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Section

Mr. Shoaib Rauf

Roll No

Total Time (Hrs):	1
Total Marks:	30
Total Questions:	3

Student Signature

INSTRUCTION: Attempt all the questions in-order.

CLO # 2 Solution

Q1: Logical Reasoning

[3x 2=6 Marks]

- a. In load –store Architecture, what is the maximum number of operands allowed in an instruction?
 Does it support memory addressing?
 - 3 operands allowed in an instruction. No it does not support memory addressing.
- b. In RISC-V ISA, which encoding format is used for ALU operations and for branches?
 R Type for ALU operations (R-R), I- Type for ALU immediate.
 S/B- Type for Branches.
- c. Why memory alignment restrictions are significant in architecture design?

Misalignment causes hardware complications, because the memory is typically aligned on a multiple of a word or double-word boundary. A misaligned memory access may, therefore, take multiple aligned memory references. Thus, even in computers that allow misaligned access, programs with aligned accesses run faster.

CLO #3 Solution

Q2: You are given a non-pipelined processor design which has a 5 GHz clock and it uses 3 cycles for ALU operations, 2 cycles for branch operations and 4 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, and 40%, respectively. [3x3=09 Marks]

a. What is the best speedup you can get by pipelining it into 5 stages?

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- b. If the 5 stages are 1ns, 1.5ns, 4ns, 3ns, and 0.5ns, what is the best speedup you can get compared to the original processor?
- c. If each pipeline stage added also adds 2ns due to register setup delay, what is the best speedup you can get compared to the original processor?

Clock =
$$SGHZ \rightarrow 0.2 \text{ ms}$$
.

3 cycles for ALU $\longrightarrow 40\%$.

2 cycles for Brenches $\rightarrow 20\%$.

4 cycles for Memory $\longrightarrow 40\%$.

Part 6.

Best speed up \Rightarrow no: of Stayes i.e. SX (ideal)

Part b

CPU time = $Clock$ time X ($\sum_{i=1}^{\infty} IC_i \times CPI_i$)

= $0.2 \text{ ms} \times \left[(3x0.4) + (2x0.2) + (4x0.4) \right]$

= $0.2 \text{ ms} \times \left[(1.2 + 0.4 + 1.6) \right]$

CPU time $\Rightarrow 0.64 \text{ ms}$.

New Cyle time $\Rightarrow Slowest$ Staye i.e. 4 ms .

 $Speedup \Rightarrow Old = 0.64 \text{ ms} \Rightarrow 0.16 \times \frac{1}{2}$

Part c

Adding Register delay $\Rightarrow 4 \text{ ms} + 2 \text{ ms} \Rightarrow 6 \text{ ms}$
 $Speedup \Rightarrow Old = 0.64 \text{ ms} \Rightarrow 0.106 \times \frac{1}{2}$

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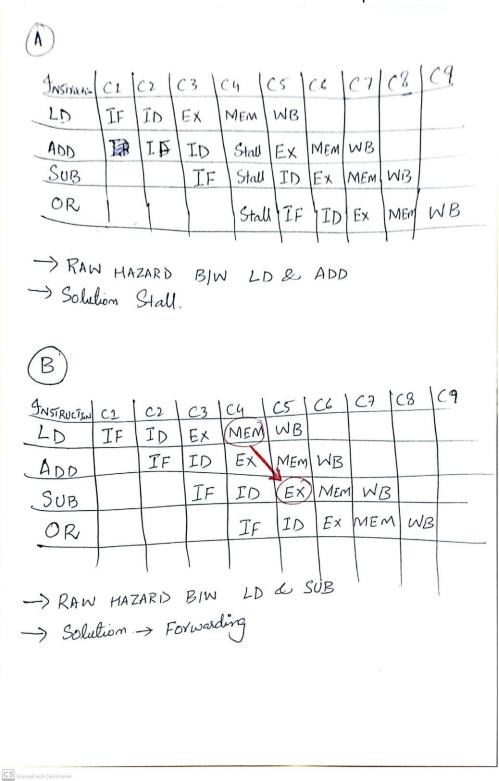
CLO #3 Solution

Q3: Consider the following code sequences,

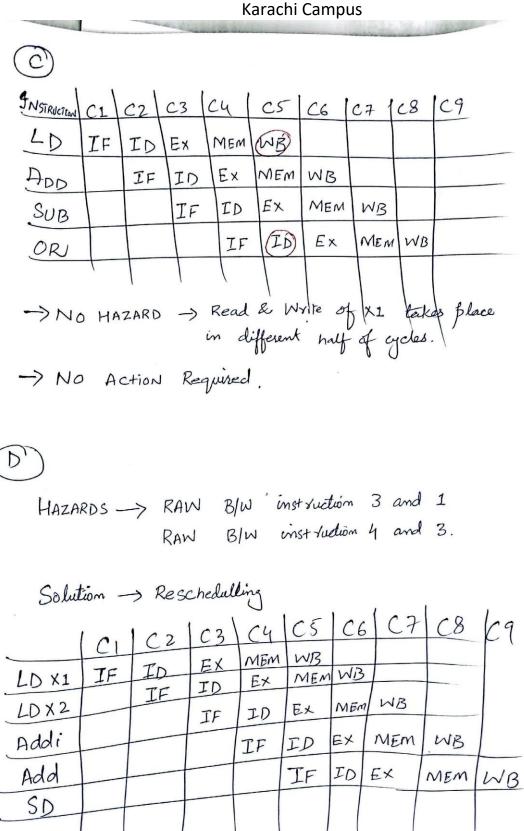
- Identify the type of Dependencies (Hazards).
- Suggest a possible solution to resolve the hazard.
- Draw Pipeline diagram for each case to support your answer.

[3.5x4=15 Marks]

<u>A)</u>	<u>B)</u>
1d x1,45(x2)	1d x1,45(x2)
add x5,x1,x7	add x5,x6,x7
sub x8,x6,x7	sub x8,x1,x7
or x9,x6,x7	or x9,x6,x7
<u>C)</u>	<u>D)</u>
$\begin{array}{ c c } \hline C) \\ Id & x1,45(x2) \end{array}$	Ld $x1,0(x4)$
add x5,x6,x7	Ld $x2,4(x4)$
sub x8,x6,x7	add x3,x2,x1
or $x9, x1, x7$	sd x3,8(x4)
	addi x4,x4,4



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=========== Good Luck ==========

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