

Computer Architecture : Assignment 01

BCS-4T

23K-2001

Answer#01:

a.) Components of multicore computer layout:

Cores: each core has its own ALU, registers & cache memory.
control unit &

L1, L2 & L3 cache:

Cache reduce memory access time and improve performance.

Memory controller:

manages access to main memory (RAM) and caches.

Bus interconnection:

facilitates communication between cores, caches, and memory.

Power management:

adjusts power usage to optimize efficiency.

Input/Output interface:

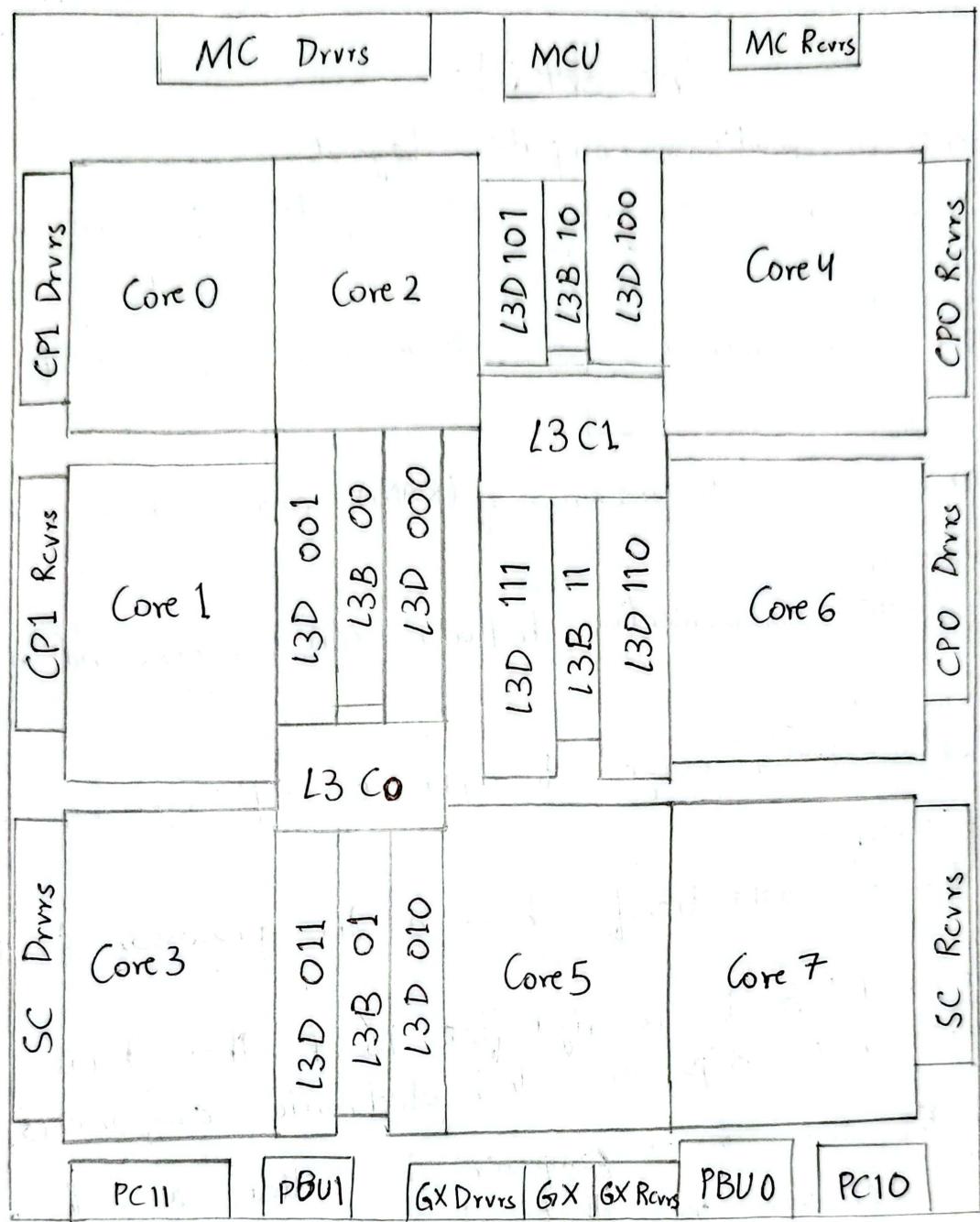
handles data transfer between the processor & peripherals.

Printed circuit board: PCB is a rigid, flat board that holds & interconnects chips and other electronic components.

Motherboard: the PCB in a computer is called a motherboard, while smaller ones that plug into the slots are called expansion boards.

b.) Processor chip of IBM z13 processing unit:

- contains 3.99 billion transistors.
- chip has 8 cores
- substantial portion of the chip is dedicated to L3 cache.
- L3 control logic controls traffic between L3 cache and the cores.
- storage control logic manages the cores and L3 cache
- memory controller controls access to memory external to the chip.

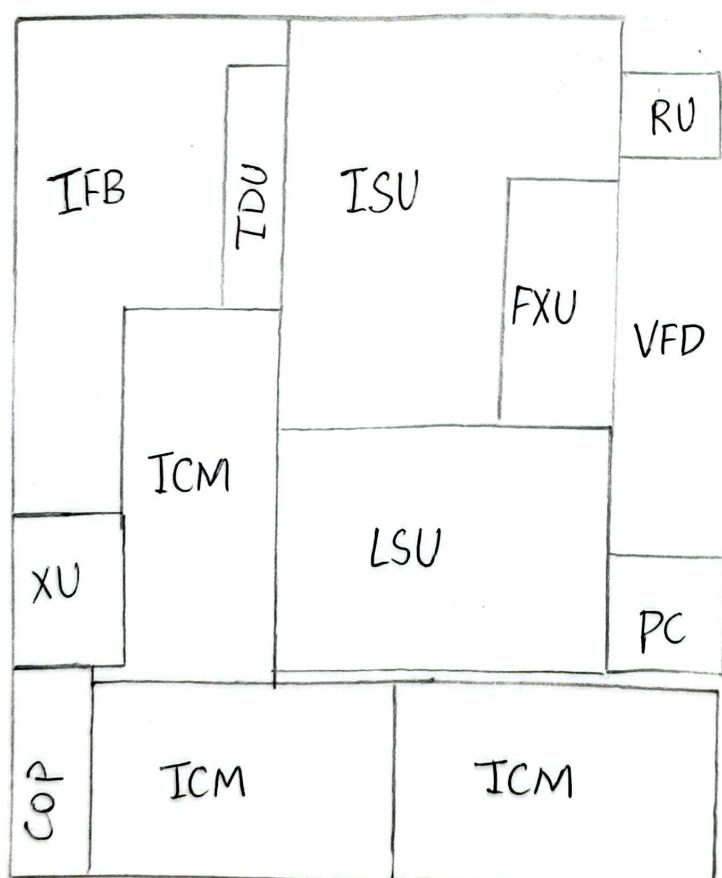


IBM z13 Processor Unit Chip

Components of Instruction set of z/architecture:

- Instruction Sequence Unit: (ISU) determines the sequence in which instructions are executed.
- Instruction Fetch & Branch (IFB) & Instruction Cache & Merge (ICM): these two components contain the 128KB instruction cache, branch prediction logic, instruction fetching, controls & buffers.
- Instruction Decode Unit: (IDU) parses & decodes instruction for execution.

- Load store unit: (LSU) manages data transfer between L1 cache and L2/3 cache.
- Translation Unit: (TU) converts logical addresses into physical addresses using translation look-aside buffer (TLB).
- Fixed point unit (FXU) & Vector & floating-point unit (VFD): handle integer and floating point operations.
- Recovery Unit (RU): maintain system state and faulty system mechanism.
- L2 Data Cache (L2D) & L2 instruction cache (L2I): 2mB L2D for data storage and 2mB L2I for instruction storage.
- Dedicated Co-processor: (COP) responsible for data compression and encryption functions for each core.

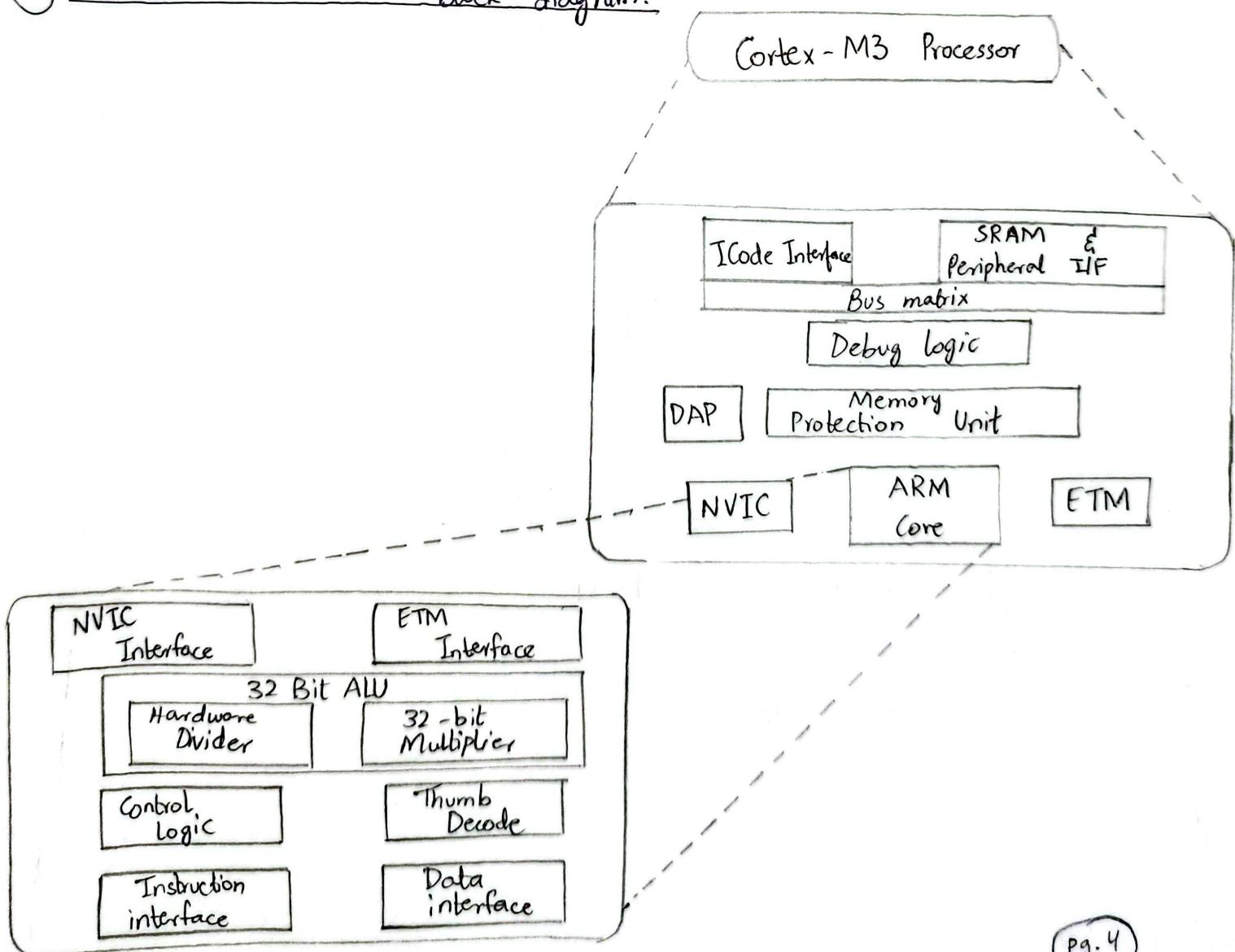


IBM z13 layout

Answer#02:

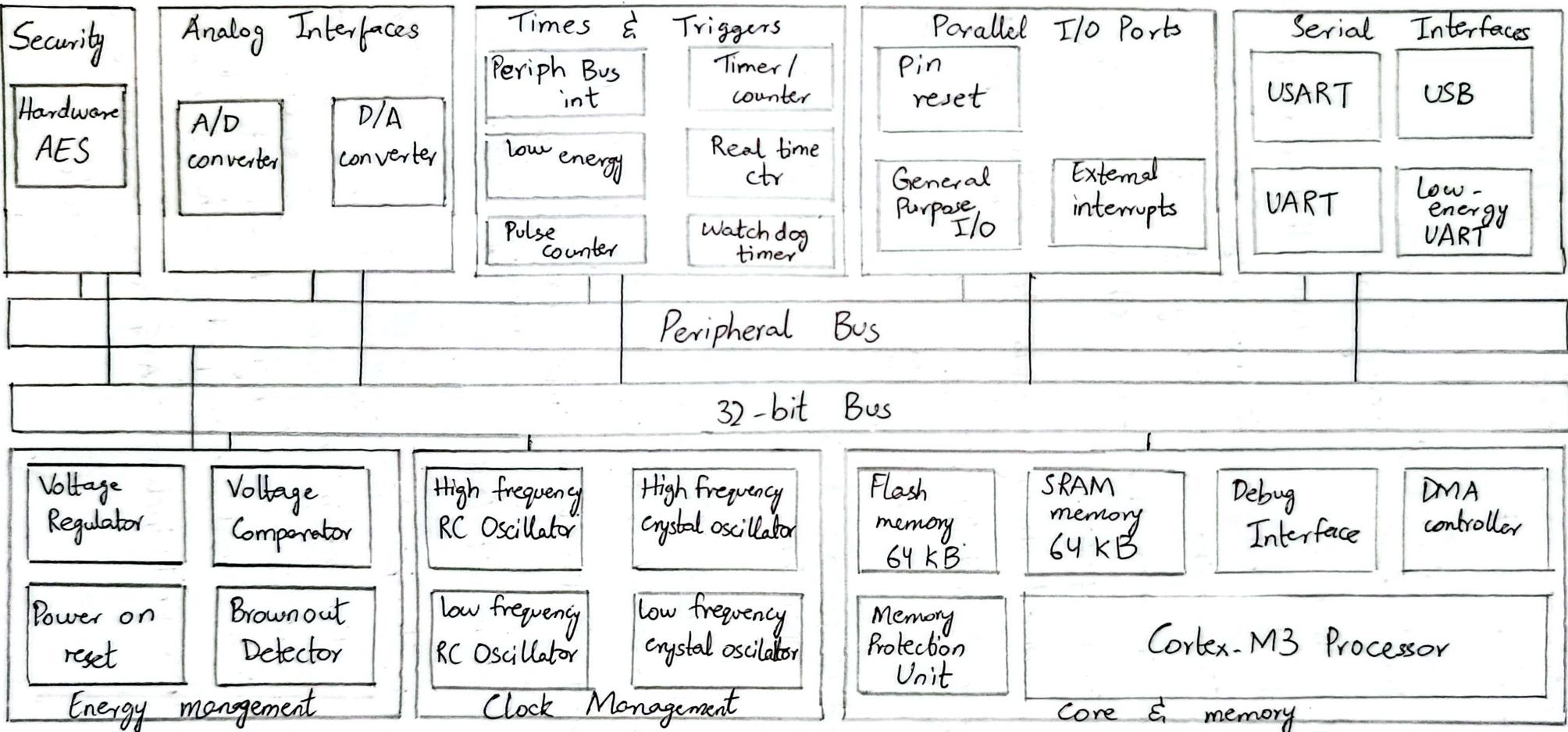
a.)	<u>Micro Processor</u>	<u>Micro Controller</u>
	<ul style="list-style-type: none"> - A CPU designed for general computing tasks. - Requires external RAM/ROM for storage. - Used in computers, servers, and high performance systems. - Has high power consumption. - Highly flexible and can be programmed for various tasks. 	<ul style="list-style-type: none"> - A compact IC with CPU, memory, and I/O on a single chip. - Has built-in RAM and ROM. - Used in embedded systems, appliances and automation. - Has low power consumption. - Optimized for specific instructions.

b.) Cortex-M3 Processor block diagram:



EFM 32 microcontroller

Block Diagram



Components of microcontroller:

- CPU: executes instructions and performs computation and controls all internal components.
- Memory:
 - > Flash memory stores program code permanently.
 - > Static RAM stores temporary data.
- EEPROM: Stores small amount of data that must be preserved.
- I/O Ports: Digital & Analogue I/O pins allow connection with external devices like sensors, displays & motors.
- Timers & Counters: used for event scheduling, generating delays & counting external pulses.
- ADC & DAC: converts analog signals to digital signals & vice versa.
- Power management unit: (PMU) controls low power mode to optimize battery life.
- Clock generator: provides timing signals for synchronization of operation.

Components of Cortex M3 processor:

- Processor core: executes instructions using a 3-stage pipeline.
- Nested Vectored Interrupt Controller: handles upto 240 interrupt priority levels.
- Memory protection unit: (MPU) controls access to memory regions.
- Instruction Set Thumb2 technology: uses a mix of 16 bit and 32 bit instruction optimizing code size & speed.
- Bus system:
 - > AHB-Lite: ensures high speed data transfer
 - > APB: Connect lower-speed peripherals such as UART & timers.
- Debug and Trace unit: includes TATG and serial wire debug for debugging.

Answer #03

a.) 20% reduction in f & v:

$$\frac{\text{energy new}}{\text{energy old}} = \frac{(\text{voltage} \times 0.8)^2}{\text{voltage}^2} = 0.8^2 = 0.64 \Rightarrow 64\% \text{ of original energy}$$

$$\frac{P_{\text{new}}}{P_{\text{old}}} = \frac{0.64 \times (f_{\text{switched}} \times 0.8)}{f_{\text{switched}}} = 0.512 \Rightarrow 51.2\% \text{ of original power}$$

Conclusion:

→ dynamic power reduces by 48.8%

→ dynamic energy reduces by 36%. Ans.

b.) Data:

$$L = \lambda W \Rightarrow W = \frac{L}{\lambda} = \frac{10}{20} \Rightarrow 0.5 \text{ hours}$$

⇒ 30 minutes Ans.

c.)

(i)

$$\text{MTTF} = \frac{1}{\text{FIT}} \quad \text{FIT} = 100$$

$$\Rightarrow \frac{10^9}{100}$$

$$\text{MTTF} = 10^7 \text{ hours}$$

(ii)

$$A = \frac{\text{MTTF}}{\text{MTTF} + \text{MTTR}} \quad : \text{MTTF} = 10^7 \\ \text{MTTR} = 24$$

$$A = \frac{10^7}{10^7 + 24}$$

$$A = 0.9999976$$

$$\text{Availability} = 99.9998\% \quad \text{Ans.}$$

Answer #04:

For machine A:

$$CPI = \frac{\text{total cycles}}{\text{instruction count}}$$

$$CPI_A = \frac{(8 \times 1) + (4 \times 3) + (2 \times 4) + (4 \times 3)}{8+4+2+4}$$

$$CPI_A = 2.22 \quad \text{Ans.}$$

$$MIPS = \frac{\text{clock rate}}{CPI}$$

$$MIPS_A = \frac{200}{2.22} = 90.09 \quad \text{Ans.}$$

$$\text{Execution time} = \frac{\text{total cycles}}{\text{clock rate}} = \frac{40}{200}$$

$$ET_A = 0.2 \text{ sec} \quad \text{Ans.}$$

For machine B:

$$CPI_B = \frac{(10 \times 1) + (8 \times 2) + (2 \times 4) + (4 \times 2)}{(10+8+4+2)}$$

$$CPI_B = 1.92 \quad \text{Ans.}$$

$$MIPS_B = \frac{200}{1.92} = 104.17 \quad \text{Ans.}$$

$$ET_B = \frac{46}{200} = 0.23 \text{ sec} \quad \text{Ans.}$$

Conclusion:

	Machine A	Machine B
CPI	2.22	1.92
MIPS	90.09	104.17
ET	0.2s	0.23s