NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCE

CS205-SESSIONAL II

QUESTION # 1 MARKS: 20

Consider a single level page table having following characteristics:

- System has 2251799813685248 total number of pages with 8196 byte size each and 64 total number of frames.
- Page table entries are 8bytes each, containing physical page frame number, plus additional control bits including the valid bit.

You are required to compute page table size for above. To avoid excessively large page tables, many virtual memory systems have multi-level page tables. You are required to find following information:

- Number of levels in a system
- How many bits are required for each level
- Number of bits of offset
- Number of page table entries in outermost level

After changing page table data structure into multiple hierarchies' designer observed tremendous overhead for translating virtual address space into physical address space. So, you are required to change the data structure of a page table to further optimize space and time. Mention the scheme?? Show calculations for reduced page table size. Also compute amount of memory you will save by using the proposed technique.

(No partial grading is there. Show proper calculations for each and every step)

QUESTION 2: MARKS 10

Consider a system having memory of total 3 frames available. A process needs to be executed which requires total 6 frames. After loading 3 pages into memory operating system needs to apply replacement algorithms. You are given the time when page has been referenced and when it was loaded into memory. You are required to mention which page will be replaced first for the following algorithms (FIFO, LRU, 2nd chance algorithm)

Load time	Reference time	Modify bit	Reference bit
230	285	1	0
400	265	0	0
140	270	0	1

QUESTION 3: MARKS 10

Consider a memory system having 3 frames and 8 virtual pages. You are required to compute number of page fault for the reference string 01232304523143263212 when optimal algorithm is used.

QUESTION 5:

What happens when required entry does not find in the associative register?

QUESTION 6:

What is the purpose of address id's in associative register?

QUESTION 7:

Can we have a super cache instead of having a separate cache TLB?

QUESTION 8:

Calculate physical address for the following logical address

0,512
3,400

SEGMENT	BASE	LIMIT
0	512	600
1	300	400
2	350	450
3	200	300