Computer Architecture (EE-3009)
Assignment_02
Spring 2025

Due Date: Thursday, April 10,2025 **Total Points: 45**

Instruction:

- You need to submit the **neat and clean handwritten scan copy** of the assignment **on classroom** before due date
- In case of plagiarism, **zero marks** will be awarded to the students.

Q# 01

Calculate the clock period of the pipeline, considering a RISC pipeline having stages taking 2,3,4,2,2 units of time. Also calculate throughput. [5 points]

Q# 02

Consider two pipelined processors, P1 with five stages with execution time of 4,3,5,3 and 4ns. P2 possess eight stages each having 3ns execution time. Calculate the amount of time saved comparing P2 to P1 for executing 200 items. [10 points]

Q# 03

Why RAR data hazard is not possible in RISC architecture? [5 Points]

Q# 04

Why WAW data hazard is not possible in RISC architecture? [5 Points]

Q# 05

The time delay of various segments in a 4 stage pipeline are t1=35 ns, t2= 30ns, t3= 40ns and t4= 45 ns. The interface register delay time is t= 5ns. How long would it take to complete 100 instructions in the pipeline? (Assuming all instructions are independent.) [10 Points]

Q# 06

The 5 stages of the processor have the following latencies: [10 Points]

	Fetch	Decode	Execute	Memory	Writeback
a.	300ps	400ps	350ps	550ps	100ps
b.	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages.

a). Non-pipelined processor: what is the cycle time? What is the latency of an instruction? What is the throughput?

b) Pipelined processor: What is the cycle time? What is the latency of an instruction? What is the throughput?