Activity 2

Multilevel paging

Consider a system using multilevel paging scheme. The page size is 16 KB. The memory is byte addressable and virtual address is 48 bits long. The page table entry size is 4 bytes.

Find-

1. How many levels of page table will be required?
2. What will be the size of inner page table?
3. What will be the size of outer page table?
4. Give the divided physical address and virtual address illustrated by a diagram of address translation.

Activity 3

Inverted Page table Problem:

Consider a machine with 64 MB physical memory and 34 bit virtual address space.If the page size is 4 KB ,the approximate size of conventional and inverted page table will be??

Activity 4:

Translation Lookaside Buffer

Consider a single level paging scheme with a TLB. Assume no page fault occurs. It takes 20 ns to search the TLB and 100 ns to access the physical memory. If TLB hit ratio is 80%, the effective memory access time is _____ msec.

Activity 5:

LRU and optimal page replacement

Consider the page references

6 5 1 2 5 3 5 4 2 3 5 3 2 1 2 5 1 6 5 1

with 4 page frame. Find number of page fault using the given schemes:

1. FIFO
2. LRU
3. Optimal page replacement