School of Electrical Engineering and Computer Science
NationalUniversity of Sciences & Technology (NUST)

Home Assignment No-3

Subject:	**Digital Logic Design**	Marks:	**50**
Course:	**BSCS-10AB**	Issue:	**May 02, 2021**
Teacher:	**Engr. Arshad Nazir**	Due:	**May 09, 2021**
Note:			*(10:00 PM)*

- ✓ *Attempt the given problem set in a sequential order.*
- ✓ *Make an index showing summary of the problems solved with page numbers and also specify the missing ones.*
- ✓ *No late submissions will be accepted and the assignments submitted after the due date/time will be graded **zero**.*
- ✓ *No copying is allowed and assignments found copied will be marked **zero**.*
- ✓ *The students will submit a certificate with the assignment work stating the originality of their efforts and no copying from others.*
- ✓ ***Five** marks are reserved for neat and clean work, table of contents, and certificate to be attached with the assignment work.*

Problem No-1

Optimize the following Boolean functions together with the don't care conditions d in the forms indicated using map method by finding all the prime implicants and essential prime implicants and apply the selection rule:

a. $F(W,X,Y,Z)=\pi_M\,(0,1,6,8,11,12).\pi_D\,(3,7,14,15)$ **SOP**
b. $g=(a'+c+d)(a'+b+e)(a+c'+e')(c+d+e')(b+c+d'+e)(a'+b'+c+e')$ **SOP**
c. $h(a,b,c,d,e)=\sum_m(1,5,12,13,14,16,17,21,23,24,30,31)+\sum_d(0,2,3,4)$ **POS**
d. $f(w,x,y,z)=\sum_m(0,1,3,7,8,11,12,13,15)$ **SOP & POS**

Problem No-2

Braille is a system which allows a blind person to read alphanumeric by feeling a pattern of raised dots. Design a circuit that converts BCD to Braille. The table shows the correspondence between BCD and Braille.

				W	X
A	B	C	D	Z	Y
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		

Implement your design with two-level (a) NAND-AND, (b) OR-NAND forms. Assume that double rail inputs are available.

Problem No-3 Implement the following two-level function using multi-level NOR gates:

$f(x_1,x_2,x_3,x_4,x_5,x_6,x_7)=x_1x_4x_5+x_1x_4x_6+x_1x_7+x_2x_3x_4x_5+x_2x_3x_4x_6+x_2x_3x_7$

Assume that logic gates have a maximum fan in of 2 and the input variables are available in uncomplemented form only.

"**Stay Home, Stay Safe"**