COMPUTER ARCHITECTURE PROJECT

Team14

Team Members

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1. Instruction Set Architecture (ISA)

1.1 Instruction Format

The processor design utilizes a fixed 32-bit instruction word. The instruction format is structured as follows:

Field	Bits	Description
Unused	[31:30]	Reserved for future use.
OPCODE	[29:25]	5 bits, identifies the instruction operation.
RDST	[24:22]	3 bits, destination register.
RSRC1	[21:19]	3 bits, first source register.
RSRC2	[18:16]	2 bits, second source register limited
Unused	[15:0]	
IMM	[31:0]	32 bits, Immediate Value (used for instructions like LDM, ADD, etc., when specified).

1.2 Instruction Details and Opcode Mapping

Instruction	OPCODE	RDST	RSRC1	RSRC2	UnUsed	IMM (32 bit)
NOP	00000	x	x	x	x	
HLT	00001	x	x	x	x	
SETC	00010	x	x	x	x	
RET	00011	x	x	x	x	
RTI	00100	x	x	x	x	
PUSH	01000	x	x	Rdst	x	
POP	01001	Rdst	x	x	x	
OUT	01010	x	Rsrc1	x	x	
IN	01011	Rdst	x	x	x	

CALL	01100	x	x	x	x	Use
INT	01101	x	x	x	x	Use
INC	01110	x	Rsrc1	x	x	
NOT	01111	x	Rsrc1	x	x	
MOV	10000	Rdst	Rsrc1	x	x	
SWAP	10010	x	Rsrc1	Rsrc2	x	
ADD	10011	Rdst	Rsrc1	Rsrc2	x	
SUB	10100	Rdst	Rsrc1	Rsrc2	X	
AND	10101	Rdst	Rsrc1	Rsrc2	X	
JZ	11000	x	x	x	X	Use
JN	11001	x	x	x	X	Use
JC	11010	x	x	x	X	Use
JMP	11011	x	x	x	X	Use
IADD	11100	Rdst	Rsrc1	x	X	Use
LDM	11101	Rdst	x	x	x	Use
LDD	11110	Rdst	Rsrc1	x	x	Use
STD	11111	x	Rsrc1	Rsrc2	x	Use

2. Control unit Design

Input is the Instruction OPCODE

Output Signals: RET, POP, RTI, PUSH, INT1, INT2, CALL, Mem (load,store), MemSel, Swap, HLT, IsIMM, RegWriteEN, MemWrite, JmpZ, JmpC, JmpN, Jmp, LoadUse, outEn, NOT/INC, WBSel

3. Pipelined Processor Design

IF/ID Register (96 bits): Stores program counter (PC1F), fetched instruction (PSPF), and read data for the next stage.

- PSPF: 32 bits
- PC1F: 32 bits
- ReadData: 32 bits

ID/EX Register (198 bits): Passes operands (RD1, RD2), immediate values (IMMF), PC (PC1D), and control signals to the EX-stage.

- **Control Signals (1 bit each**): RETD, POPD, RTID, PUSHD, INT1D, INT2D, CALLD, MemD (load/store), MemSelD, RegWriteEND, MemWriteD, JmpZD, JmpCD, JmpND, JmpD, LoadUseD, OutEnD
- **Control Signals (2 bits):** SwapD, WBSelD, ExOutSelD
- **Register Fields (3 bits):** RSrc1D, RSrc2D, Rdst
- **ALU Control (3 bits):** AluOpD, AluSrcD
- **Data/Immediate (32 bits):** RD1, RD2, PC1D, PSPD, IMMF

EX/MEM Register (177 bits): Carries ALU results, memory addresses, and control signals to the MEM stage.

- **Control Signals (1 bit each):** RETE, POPE, RTIE, PUSHE, INT1E, INT2E, CALLE, MemE (load/store), MemSelE, RegWriteEND, MemWriteE, OutEnE
- **Control Signals (2 bits):** WBSelE
- **Register Fields (3 bits):** Rdst

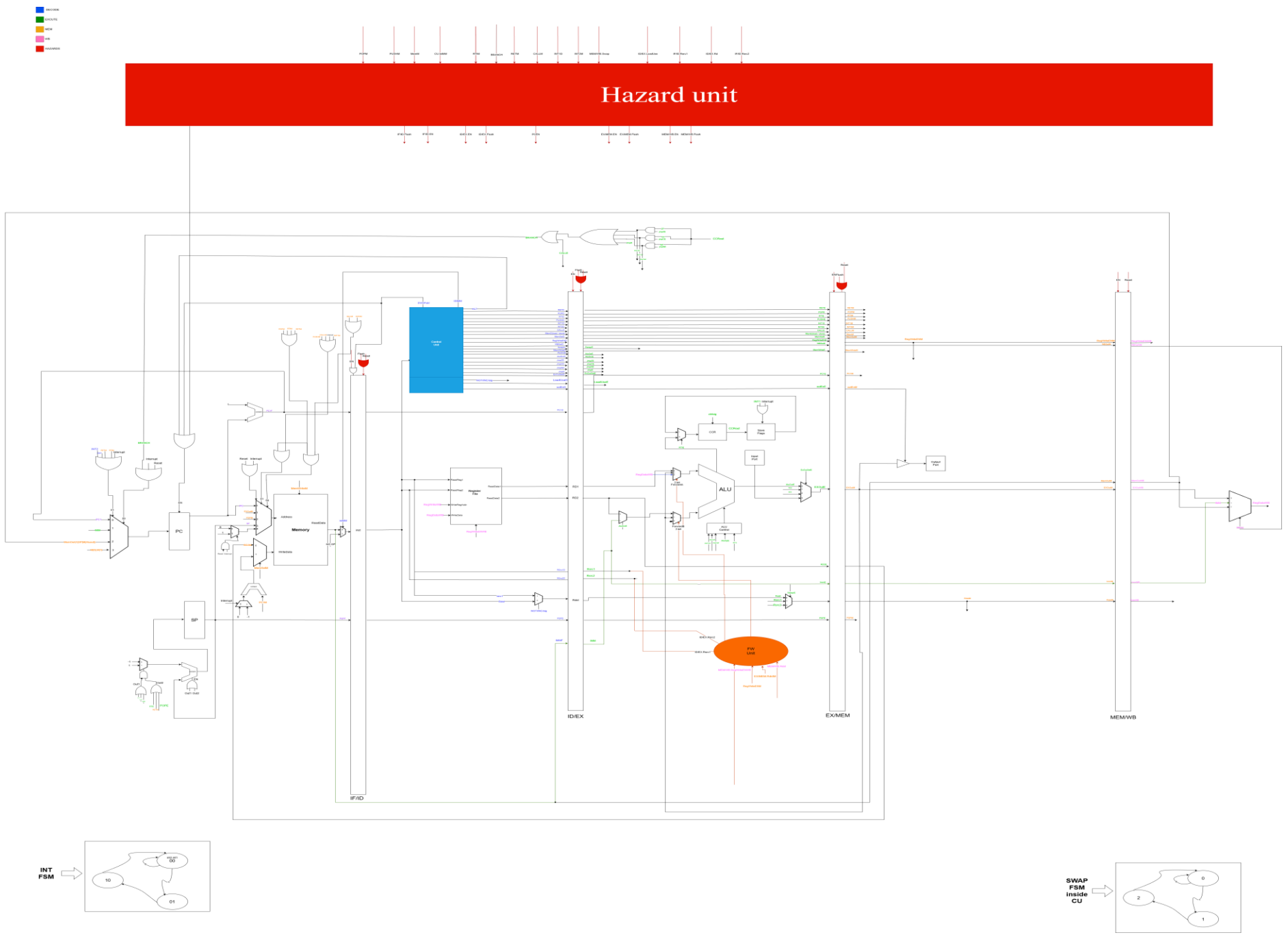
- **Data/Immediate (32 bits):** PC1E, ExOutE, IMME, PSPE, RD2E (for stores)

MEM/WB Register (102 bits): Holds data from memory or ALU, ready for the WB stage.

- **Control Signals (1 bit):** RegWriteEnM
- **Control Signals (2 bits):** WBSelM
- **Data (32 bits):** ExOutM, MemOutM, ImmM
- **Register Fields (3 bits):** RdstM

Link of the Diagram from the tool:

https://drive.google.com/file/d/168NWHNYzl6bViFPiPO2LuSlhblBrivq4/view?usp=drive_link


DECODE
EXCUTE
MEM
WB
HAVARDS
Hazard unit
Control Unit
Memory
Register File
ALU
FW Unit
IF/ID
ID/EX
EX/MEM
MEM/WB
INT FSM
SWAP FSM inside CU