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University of Engineering & Technology Peshawar

Digital System Design
CSE 308

Finalterm Examination Spring 2024
11 June 2024, Duration: 120 Minutes

Exam Rules

Please read carefully before proceeding.

- This exam is CLOSED books/notes/Internet/laptops/phones.
- No calculators/phones of any kind are allowed.
- Attempt all problems on the answer sheet.
- Some problems are harder than others. Answer the easy ones first to maximize your score.
- Problems will not be interpreted during exam. Please note!
- This exam booklet contains 5 pages, excluding this cover page. Count them to be sure you have them all.

Problem 1	_____	(40 pts.)
Problem 2	_____	(20 pts.)
Problem 3	_____	(35 pts.)
Total	_____	(95 pts.)

Good luck!

PROBLEM 1 (MEMORIES).....(40 pts., CLO-2)

1(a) (10 pts.) Given the following partial module for a 4Kx16 RAM chip, fill in the blanks to complete the module.

```
module RAM_4Kx16 (addr, CS, RW, idata, odata);  
  
    input CS, RW;  
    input [____ : ____] addr;  
    input [____ : ____] idata;  
    output [____ : ____] odata;  
    reg [____ : ____] d_out;  
    reg [____ : ____] Mem1 [____ : ____];  
  
    assign odata = (CS && RW)?d_out:16'b0;  
  
    always @ (addr or idata or CS or RW)  
        if (CS && !RW)  
            Mem1 [____] = ____;  
    always @ (addr or CS or RW)  
        if (CS && RW)  
            d_out = Mem1 [____];  
  
endmodule
```

1(b) (10 pts.) Write a top-level module to combine four 4Kx16 RAM chips (given in 1(a)) to form a 16Kx16 RAM. Use the below skeleton module.

```
module RAM_16Kx16 (addr, CS, RW, idata, odata);  
  
endmodule
```

1(c) (10 pts.) Draw the block diagram of the RAM_16Kx16 from 1(b). Label all the inputs and outputs appropriately.

1(d) (10 pts.) Simulate the RAM_16Kx16 in 1(b) using the below testbench. And write the output in the format specified by \$display.

```

module RAM_16Kx16_testbench();

    reg [13:0] address;
    reg CS, RW_enable;
    reg [15:0] data_in;
    wire [15:0] data_out;

    RAM_16Kx16 r1 (
        .addr(address),
        .CS(CS),
        .RW(RW_enable),
        .idata(data_in),
        .odata(data_out));

    initial begin

        $display("RAM test bench...");

        #10 RW_enable = 0;
        CS = 1;
        address = 1050;
        data_in = 16'hAF09;
        →#10 address = 2057;
        data_in = 16'h55AB;
        →#10 address = 256;
        data_in = 16'hFFC0;
        →#10 address = 4028;
        data_in = 16'hD0AB;
        #10 RW_enable = 1;
        →#10 $display($time, " Mem[%d] = %h", address, data_out);
        →#10 address = 0;
        →#10 $display($time, " Mem[%d] = %h", address, data_out);
        #10 address = 1050;
        →#10 $display($time, " Mem[%d] = %h", address, data_out);
        ||#10 RW_enable = 0;
        address = 0;
        data_in = 16'h2A6B;
        #10 RW_enable = 1;
        →#10 $display($time, " Mem[%d] = %h", address, data_out);
        #10 RW_enable = 0;
        address = 4028;
        #10 $display($time, " Mem[%d] = %h", address, data_out);

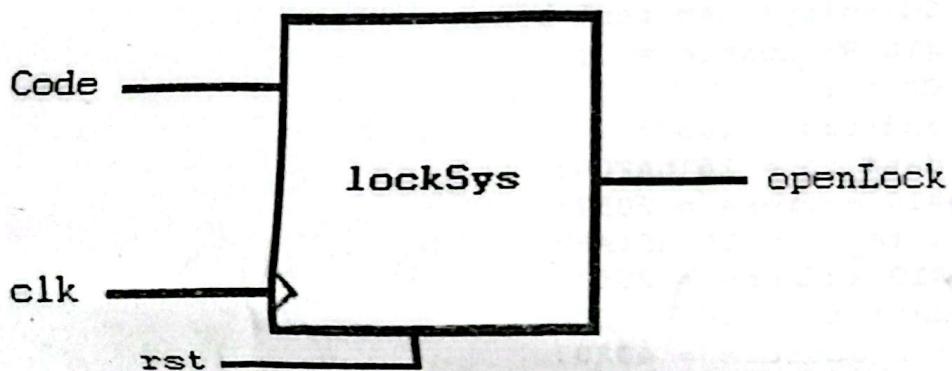
    end

endmodule

```

PROBLEM 2 (FINITE STATE MACHINES).....(20 pts., CLO-2)

In this problem, design an electronic lock system (**lockSys**, see Figure) for a garage door lock. The electronic lock accepts a 4-bit user code input, one bit at a time. If the input code sequence exactly matches 1010, the electronic lock is opened (**openLock** is asserted). If any part of the 4-bit code input sequence is incorrect, the user is forced to restart code entry i.e. all backward arcs go back to the initial state if a "wrong" bit is entered. When **openLock** is asserted after the correct code has been entered, the lock stays open. And the lock shuts itself (**openLock** is de-asserted) if the asynchronous input signal **rst** is asserted or a 0/1 is entered after the correct input code sequence until the correct input code is again entered.



2(a) (10 pts.) Design a Mealy FSM for **lockSys**.

2(b) (10 pts.) Implement the FSM in 2(a) in Verilog. Use the below skeleton module and the same standard format as was presented in the class. (Define your states; use one **always** block to model the state register; use second **always** block for state transitions and output.)

```

module sysLock (code, clk, rst, openLock);

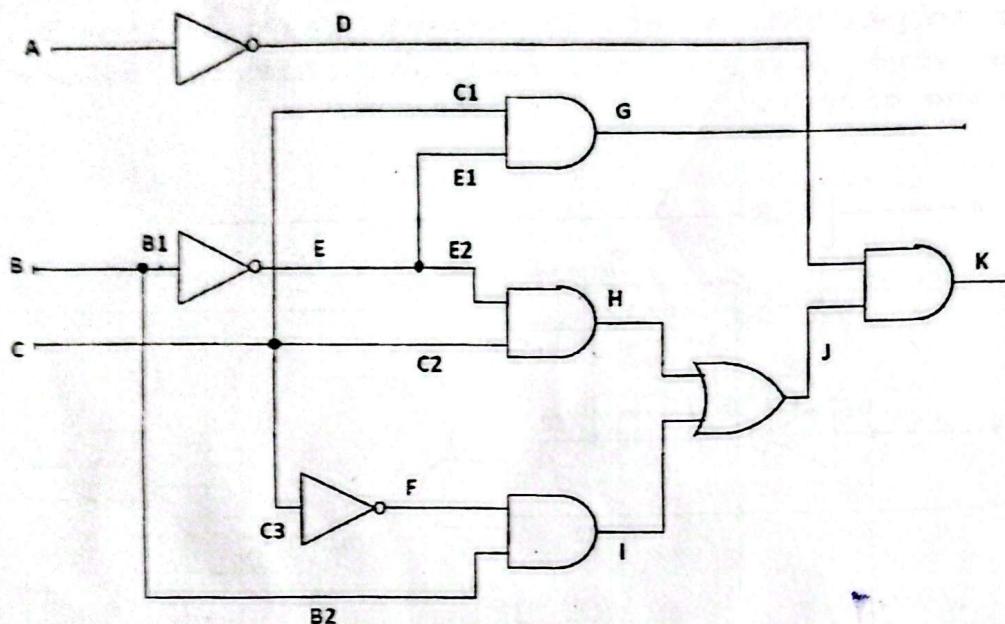
    // Your Verilog implementation here

endmodule

```

PROBLEM 3 (TESTING).....(35 pts., CLO-3)

Consider the below given circuit based on the single stuck-at faults assumption and answer the questions related to this.



3(a) (4 pts.) What is the number of all possible faults?

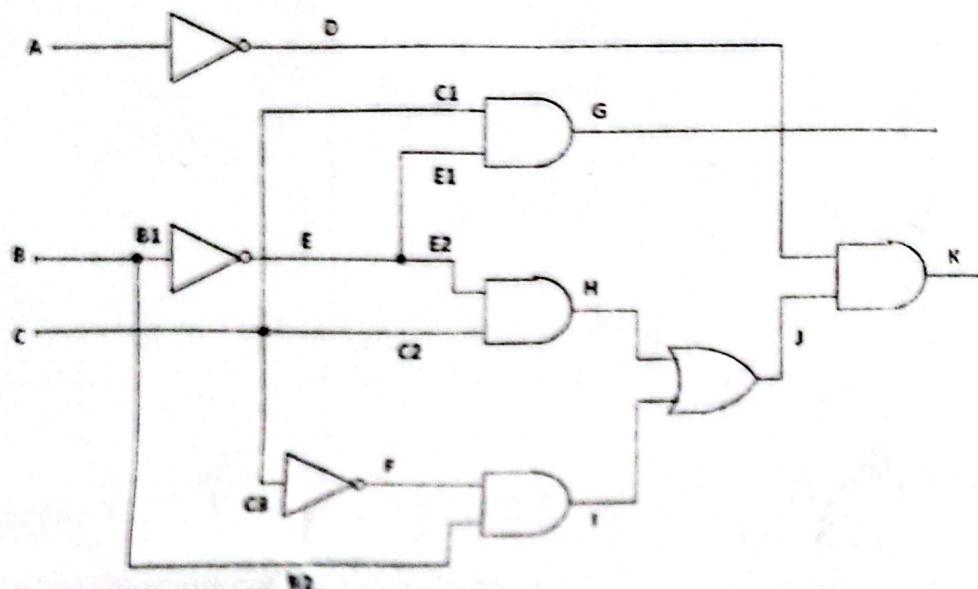
3(b) (3 pts.) How many checkpoint faults are in the circuit?

3(c) (10 pts.) Write the reduced fault list using the method of fault equivalence and fault dominance reduction. What is the collapse ratio after you perform fault collapsing (based on the equivalent and dominant faults you find)?

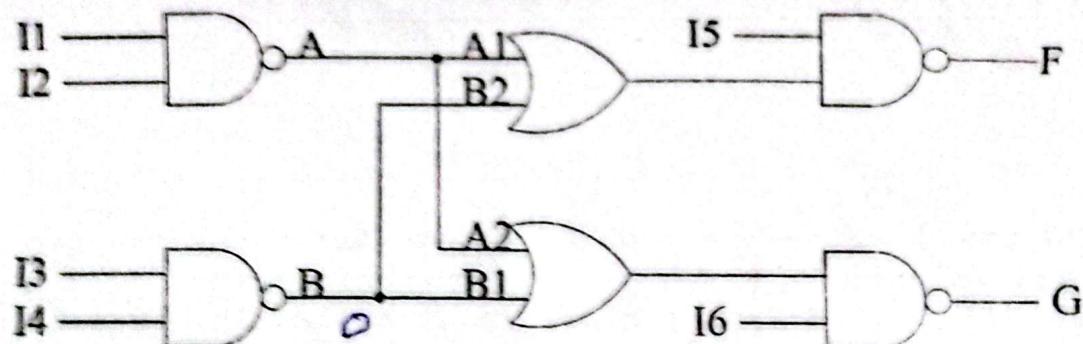
RFL = {
 }
 }

CR = _____

3(d) (10 pts.) Label the sequence of assignments made by the D algorithm to generate a test for the **sa1** fault on line **E** indicated below. Be sure to give the order and show the values for all nodes in the circuit.



3(e) (8 pts.) Consider the circuit given below.



Tests shown in the table below are applied to this circuit. State if the single faults **A sa0** and **B sa0** will be detected or not by these tests. Give reasons.

Test #	I1	I2	I3	I4	I5	I6	A sa0	B sa0
1	0	1	1	1	0	1		
2	1	1	0	1	1	0		
3	0	1	0	1	1	1		
4	0	1	1	1	1	0		



Final Exam (Spring 2024)

Time: 2 Hours (6th Semester)

Paper: CSE-403 Database Management System

Marks: 50

Note: Attempt all questions on the answer sheet.

Question No. 1

Marks (5+5) (CLO-3)

- a). Convert the following ERD to relations showing referential integrity constraints.

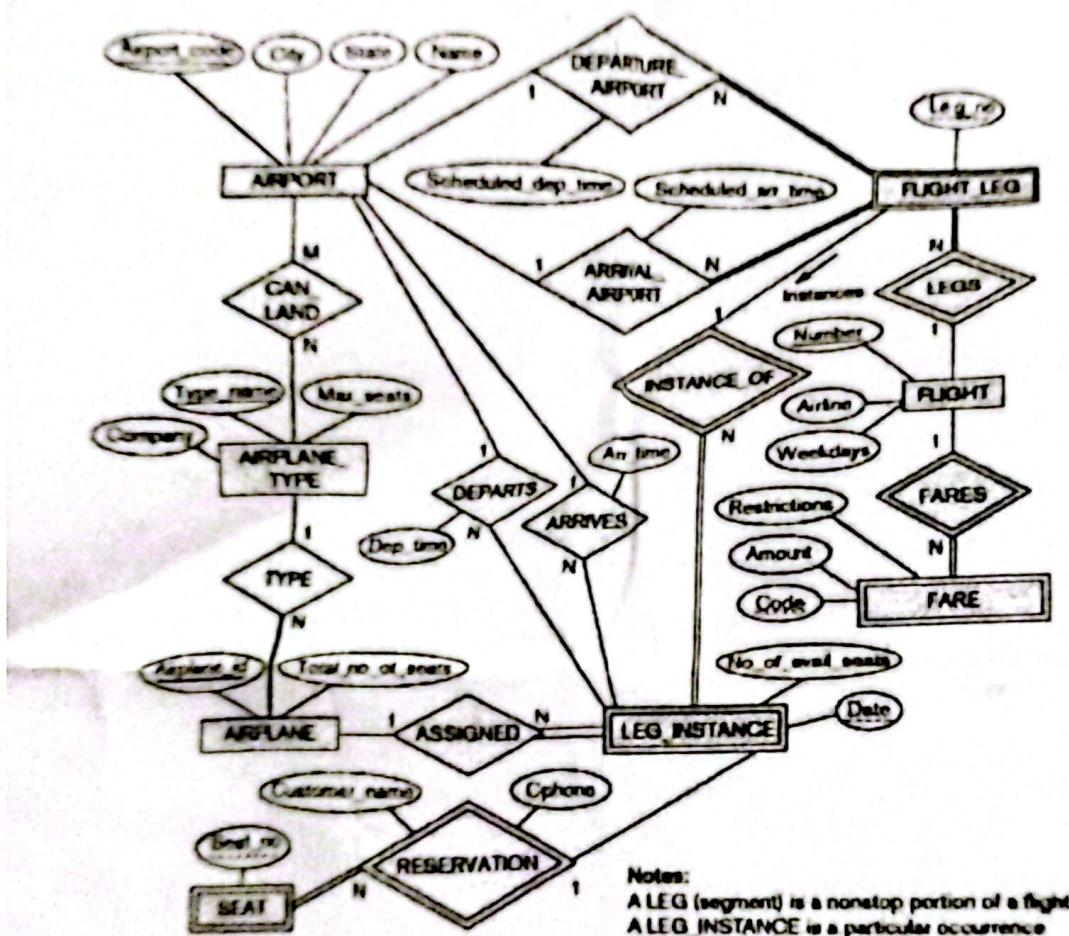


Figure 1: E-R Diagram for an Airline Booking Application

- b). Identify the functional and transitive dependencies in the following relation and convert it to 2nd and 3rd Normal form. (Identify/assume appropriate primary/foreign keys)

Product_Sales (Order_ID, Product_ID, Product_Name, Customer_ID, Customer_Name, Quantity, Price, Total_Amount)

REGISTRATION_CARD (Student-ID, S-Name, HomeAddr, Advisor, Ofc-Phone, Course-ID, Course-Days/Time, Credit-hours, Room/Bldg, Instructor, Email, Phone, RegisDate, TotalFees, FeesPaid)

LIBRARY_CHECKOUT (Checkout_ID, Book_ID, Book_Title, Author, Member_ID, Member_Name, Checkout_Date, Due_Date, Fine_Amount)

Patient_Records (Patient_ID, Patient_Name, Age, Gender, Date_Admitted, Doctor_ID, Doctor_Name, Department, Diagnosis, Medication, Dosage)

Question No. 2

(Marks=2+2+2+2+2) (CLO-4)

Consider the following tables:

*Order (OrderId, CustomerId, ProductId, Qty, Amount, SalRepId, Date)**SalesRep (SalRepId, SalRepName, OfficeId, Title, Age, HireDate, Manager, Quota, Sales, Target)**Office (OfficeId, City, Region, Target, Sales)**Customer (CustomerId, customerName, Company, CreditLimit, Address, salRepId)**Product (ProductId, Description, Price, Manufacturer, Qty_On_Hand)*

Write the SQL statements for the following queries:

- List the name and hire date of anyone with sales over 50000
- List the names of Sales persons and their corresponding Customer names
- List sales people whose sales are not between 50000 to 80000
- List all the customers whose name starts with 'A' or 'a'
- List orders over 2500, including the name of the sales person who took the order

Question No. 3

Marks (4+4+4+4)

Consider the following table:

staffNo	dentistName	patientNo	patientName	appointment date	time	surgeryNo
S1011	Tony Smith	P100	Gillian White	12-Aug-03	10.00	S10
S1011	Tony Smith	P105	Jill Bell	13-Aug-03	12.00	S15
S1024	Helen Pearson	P108	Ian MacKay	12-Sept-03	10.00	S10
S1024	Helen Pearson	P108	Ian MacKay	14-Sept-03	10.00	S10
S1032	Robin Plevin	P105	Jill Bell	14-Oct-03	16.30	S15
S1032	Robin Plevin	P110	John Walker	15-Oct-03	18.00	S13

- Provide examples of Insertion, Deletion and Modification anomalies in the table.
- Draw a dependency diagram that shows all functional dependencies in the relation, based on the sample data shown.
- Develop a set of relations in third normal form.
- Develop an E-R diagram with the appropriate cardinality notations.

Question No. 4

(Marks=4+4)

Consider the following table:

Trans_ID	Date	Product_ID	Product_Name	Category	Supplier_ID	Supplier_Name	Quantity_Sold	Unit_Price	Total_Price	Stock_Quantity	Reorder_Level
1	2024-05-01	101	Laptop	Electronics	501	ABC Electronics	5	1200	6000	10	5
2	2024-05-02	102	Smartphone	Electronics	502	XYZ Tech	8	800	6400	15	5
3	2024-05-03	103	Shirt	Apparel	503	Fashion Store	10	30	300	30	20

- Diagram the functional dependencies and determine the normal form of the above table.
- Convert the given table to 3rd normal form, and identify referential integrity constraints.

Question No. 5 a). How the three application logics (Presentation, Processing and storage) are distributed in a three-tier architecture? (Marks: 3)

b). What are the possible threats to Data Security in a Database Environment? (Marks: 3)



**Department of Computer Systems Engineering
University of Engineering & Technology Peshawar
6th Semester Final-term Examination, Spring 2024**

Course Title: Technical Writing

Course Code: CSE311

Total Marks: 50

Maximum Weightage: 50%

Time allowed: 02 Hours

Name: Ali Asghar

Reg #: 21PWCSE 2050

- Attempt all five questions; the marks for each part of the question are written there in parenthesis.
- Do not write anything on this question paper except your name and registration number.
- Electronic gadgets are strictly prohibited.

Q1 – What is a skill (2)? Is interviewing a skill (1)? If yes, how can you improve it (1)? Pick a job/title of your choice in an organization of your choice. What are the skills and competencies that make you best fit for this job (3)? What is the STAR method used for improving interviewing skills (3)?

Affective-2 (Responding)

Q2 – What is plagiarism (2)? Why do people plagiarize (2)? In your candid opinion, how can Generative AI tools be used in an ethical and responsible manner (3)? With respect to the Generative AI tools, devise a process for encouraging creativity and critical thinking (3).

Q3 – What is Latex and why do the people in scientific community usually prefer it over MS Word (2)? Why do we read research papers (2)? Where can we find relevant and quality research papers (2)? What are the ingredients of a quality research paper (4)?

Affective-3 (Valuing)

Q4 – Write guidelines for writing a good quality

- a) Title (2)
- b) Abstract (2)
- c) Introduction (3)
- d) Literature Review (3)

Q5 – What are the essential ingredients of a good proposal? Explain/Justify with the help of your own FYP proposal that you wrote as an assignment for this course. (10)

Affective-4 (Organization)



Department of Computer Systems Engineering,
University of Engineering and Technology Peshawar,
Pakistan

Finalterm Exam (6th Semester, Spring 2024)

Paper: MBSD
Marks: 80

Time: 2 Hours

Note: Attempt all questions on the answer sheet.

Question No. 1 (Marks=10+5+5) (CLO-2)

1. Design an efficient assembly language program to generate a 500 Hz signal on P1.0 using Timer 0. The waveform should have a 30% duty cycle (duty cycle = high-time / period).
2. Assuming that XTAL = 11.0592 MHz, indicate when the TF0 flag is raised for the following program.

```
MOV TMOD, #01
MOV TL0, #12H
MOV TH0, #1CH
SETB TR0
```

3. Who provides clock pulses to 8051 timers if C/T = 0?

Question No. 2 (Marks=10+10)

1. For XTAL = 11.0592 MHz, find the TH1 value (in both decimal and hex) for each of the following baud rates.
(a) 9,600 (b) 4,800 (c) 150
2. Write a program for the 8051 to transfer "YES" serially at 9600 baud, 8-bit data, 1 stop bit, do this continuously.

Question No. 3 (Marks=10+10)(CLO-1)

1. Describe Interrupts Vs Polling, Interrupt Service Routing, Steps in executing an Interrupt, six interrupts in the 8051, Enabling and Disabling an interrupt, steps in enabling an interrupt.
2. Comment each line of the following program and describe its purpose/output if LED is connected to pin P1.3 of the 8051 microcontroller.

```
ORG 0000H
LJMP MAIN
ORG 0013
SETB P1.3
MOV R3, #255
BACK: DJNZ R3, BACK
       CLR P1.3
       RETI
       ORG 30H
MAIN:  MOV IE, #10000100B
HERE:  SJMP HERE
END
```

Question No. 4 (Marks=20)(CLO-3)

Assuming that we need an 8031 system with 16KB of program space, 16KB of data ROM starting at 0000H, and 16k NV-RAM starting at 8000H. show the design using a 74LS138 for the address decoder. (Note: write and comment the address map, describe the design and its implementation)