

```
module Memory_2Kx8 (addr, CS, RW, idata, odata);
  input CS, RW;
  input [10:0] addr;
  input [7:0] idata;
  output [7:0] odata;

wire [7:0] odata1, odata2;

wire D0, D1;

assign D0 = CS && ~addr[10]; //Output D0 of the 2x1 decoder assign D1 = CS && addr[10]; //Output D1 of the 2x1 decoder

RAM1 rc1 (addr[9:0], D0, RW, idata, odata1);
  RAM2 rc2 (addr[9:0], D1, RW, idata, odata2);

assign odata = (CS && RW)?(odata1 | odata2):8'bz;
endmodule
```

```
module RAM1 (addr, CS, RW, idata, odata);
     input CS, RW;
     input [9:0] addr;
     input [7:0] idata;
     output [7:0] odata;
     reg [7:0] d out;
     reg [7:0] Mem1 [0:1023];
     assign odata = (CS && RW)?d_out:8'b0;
     always @(addr or idata or CS or RW)
               if (CS && !RW)
                    Mem1 [addr] = idata;
          always @(addr or CS or RW)
               if (CS && RW)
                    d out = Mem1 [addr];
        initial
               $readmemh ("memory1.dat", Mem1);
endmodule
```

//memoryl.dat. The data file must be in the same directory as design and testbench. Otherwise you will need to specify the complete path.

	ca to specify		COIL	PICCC	Pati
memo	ry1 - Notepad		_		×
File Edit	Format View Help				
25	//reg 0				^
3A	//reg 1				
7B	//reg 2				
AA	//reg 3				
DD	//reg 4				
88	//reg 5				
FF	//reg 6				
AC	//reg 7				
ВВ	//reg 8				
00	//reg 9				
11	//reg 10	)			
88	//reg 11				
77	//reg 12				
99	//reg 13				
CC	//reg 14				
BC	//reg 15		4 60	on	
BC	meg 13	all	u 30	, OII	

```
module RAM2 (addr, CS, RW, idata, odata);
     input CS, RW;
     input [9:0] addr;
     input [7:0] idata;
     output [7:0] odata;
     reg [7:0] d out;
     reg [7:0] Mem2 [0:1023];
     assign odata = (CS && RW)?d_out:8'b0;
     always @(addr or idata or CS or RW)
               if (CS && !RW)
                    Mem2 [addr] = idata;
          always @(addr or CS or RW)
               if (CS && RW)
                    d out = Mem2 [addr];
        initial
               $readmemh ("memory2.dat", Mem2);
endmodule
```

//memory2.dat. The data file must be in the same directory as design and testbench. Otherwise will you need to specify the complete path.

	a neca to specify			
memo	ry2 - Notepad	_		×
File Edit	Format View Help			
BB	//reg 0			^
30	//reg 1			
99	//reg 2			
AC	//reg 3			
FF	//reg 4			
99	//reg 5			
00	//reg 6			
9C	//reg 7			
ВС	//reg 8			
77	//reg 9			
22	//reg 10			
AF	//reg 11			
AD	//reg 12			
BD	//reg 13			
CD	//reg 14			
AF	//reg 15 an	nd so	o on	
	mog io ai	iu 30	, OII	V

```
module tst Memory 2Kx8 ();
     reg [10:0] address;
     reg CE, RW;
     reg [7:0] data in;
    wire [7:0] data out;
    Memory 2Kx8 m1 (
        .addr(address),
        .CS (CE),
        .RW(RW),
        .idata(data in),
        .odata(data_out));
     initial begin
              $display("Reading from Memory (already initialized/populated using $readmemh)...");
               CE = 0;
               RW = 0;
               #5 address = 15;
               #5 RW = 1;
               #5 CE = 1;
               #10 address = 1;
               #10 address = 2;
               #10 address = 3;
               #10 address = 1024;
               #10 address = 6;
               #10 address = 1025;
               #10 address = 1030;
               #10 address = 8;
               #10 address = 9;
               #10 address = 10;
               #10 address = 11;
               #10 address = 0;
```

```
#10 address = 14;
#10 address = 13;
#10 address = 12;
#500 $finish;
```

end

## endmodule

