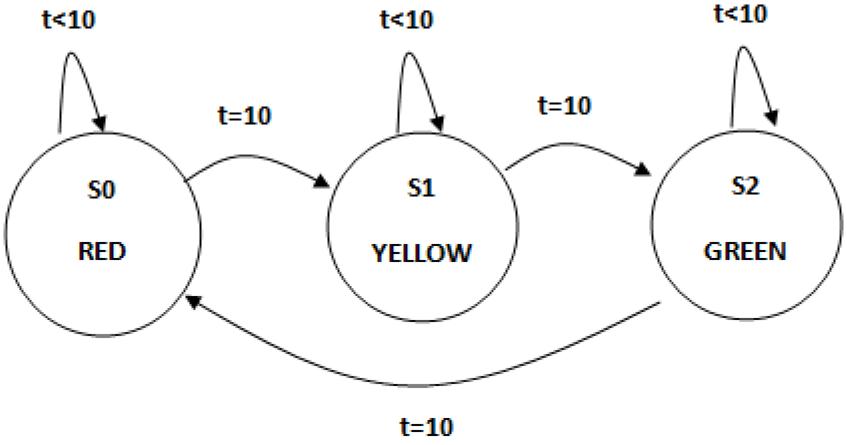
Name: ****Solution****______________________________

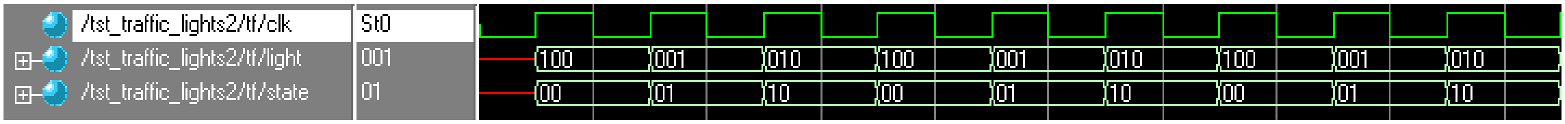
Registration: ________________________

Design and implement the following traffic light controller in Verilog.
(Simulation: 50% pts., FGPA Implementation: 50% pts.)



```
module traffic_lights2 (clk, light);

     input clk;
     output [2:0] light; reg [2:0] light;

     parameter S0 = 0, S1 = 1, S2 = 2;
     parameter RED = 3'b100, GREEN = 3'b010, YELLOW = 3'b001;

     reg [0:1] state;

     always @(posedge clk)
          case (state)
               S0: state <= S1;
               S1: state <= S2;
               S2: state <= S0;
               default: state <= S0;
          endcase

     always @(state)
          case (state)
               S0: light = RED;
               S1: light = YELLOW;
               S2: light = GREEN;
               default:  light = RED;
          endcase

endmodule
```

```
`timescale 1s/1s
module tst_traffic_lights2;

     reg clk;
     wire [2:0] light;

     traffic_lights2 tf (clk, light);

     initial
          clk = 0;

     always
          #5 clk = ~clk;

endmodule
```



/tst_traffic_lights2/tf/clk St0
/tst_traffic_lights2/tf/light 001
/tst_traffic_lights2/tf/state 01