

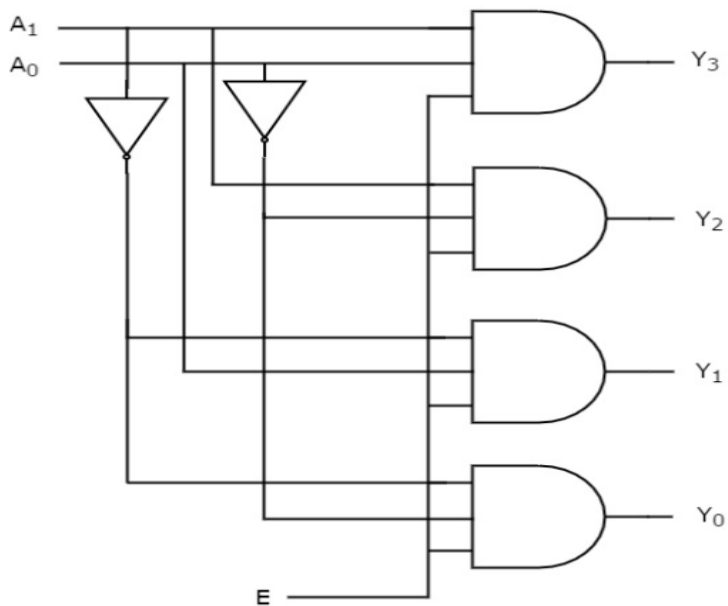
COA

DCSE, UET Peshawar

LAB 8

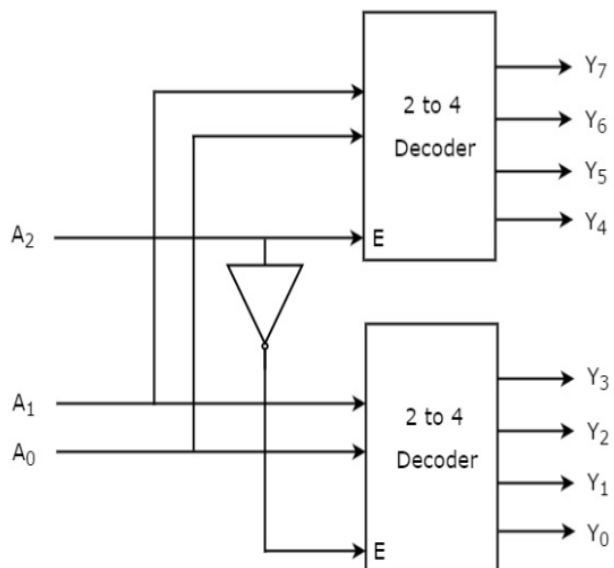
DECODERS IN VERILOG:

Q NO 1: implement 2X4 Decoder using gate level modeling in Verilog.



Q NO 2: Implement 3X8 Decoder using gate level modeling in Verilog.

Q NO 3: Implement 3X8 Decoder using 2X4 Decoder.



Q NO 4: Implement 4X16 Decoder using 3X8 Decoder.

