CSE-308: Digital System Design **Lecture 1** Introduction

**warm-up**

**quiz…**

DLD (also DSD) is basically a design course. List all the steps involved in capturing a real-world phenomenon and converting it to the simplest digital logic circuit using discrete gates.

Note: You just have to list the steps. Don’t write unnecessary details.

Instructor:

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Course Newsgroups:

A: https://classroom.google.com/c/NzYwMzQwMTY1MDA4 B: https://classroom.google.com/c/NzUwMDM0NjExNTIy C: https://classroom.google.com/c/NzUwMDM0MjgxOTk5

Check the group often for announcements related to the course

**marks**

**distribution…**

Final

Examination

50%

Midterm

Examination

25%

Sessional Work

25%

Sessional Work (25%)

• Homeworks 5% • Quizzes 15% – (50% announced + 50% unannounced) • Class Participation + Attendance 5%

Homeworks (5%)

• Almost one every two weeks

• Late homework policy: Late submission of homeworks will result in "zero" grade

Homeworks (contd…)

• Done on an individual basis

• Collaboration is fine, but it should be you alone who writes up the answers

• Copying of homework is allowed as long as it goes through the head

Midterm Exam (25%)

• During the 7th/8th week

• Duration: Two hours

• Will cover all material covered during the first 7/8 weeks

Final Exam (50%)

• During the 16th/17th week

• Will cover the whole of the course before and after midterm

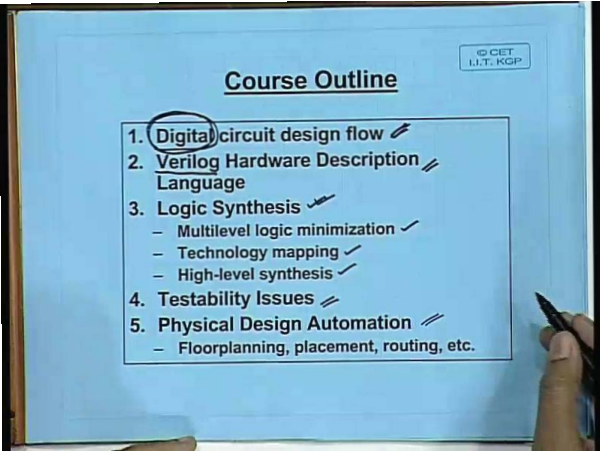
• Duration: Two hours

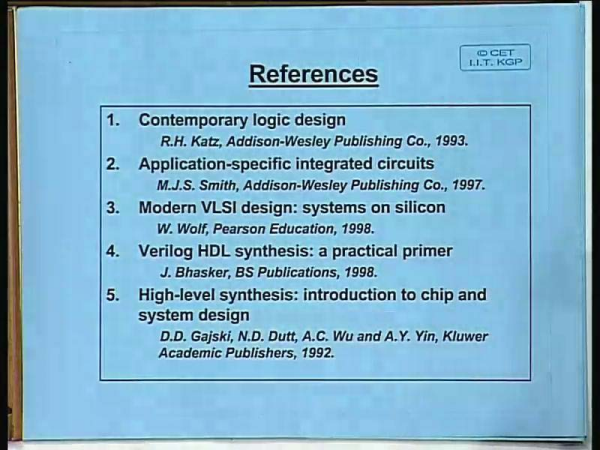
What I don’t want?

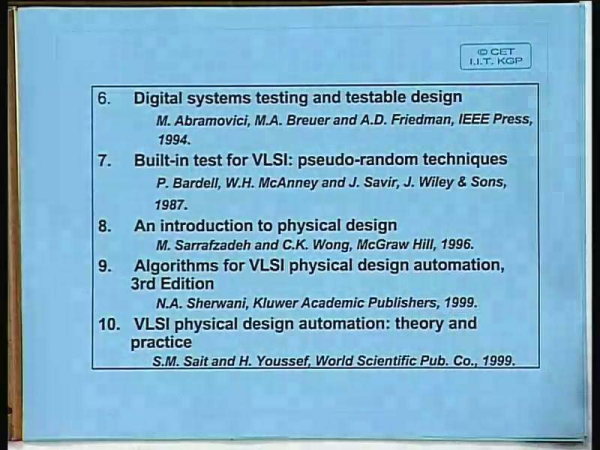
That you fail such an easy course Essential ingredient to pass is "HARD WORK"

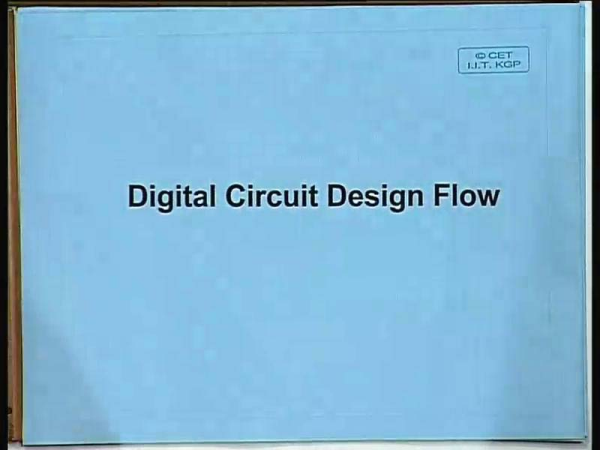
**attendance policy…**

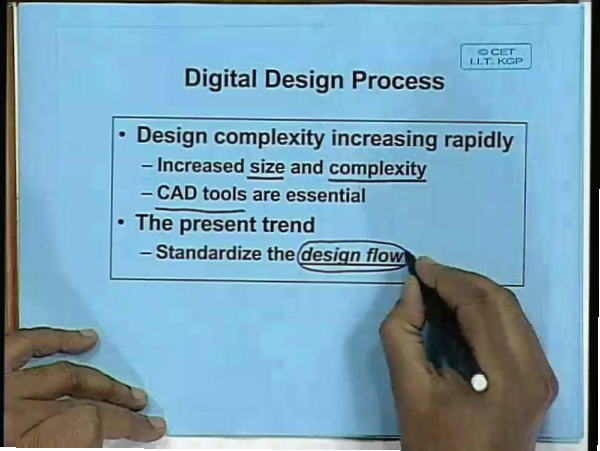
Students with attendance less than 75% will NOT be allowed to sit in the "FINAL EXAM"

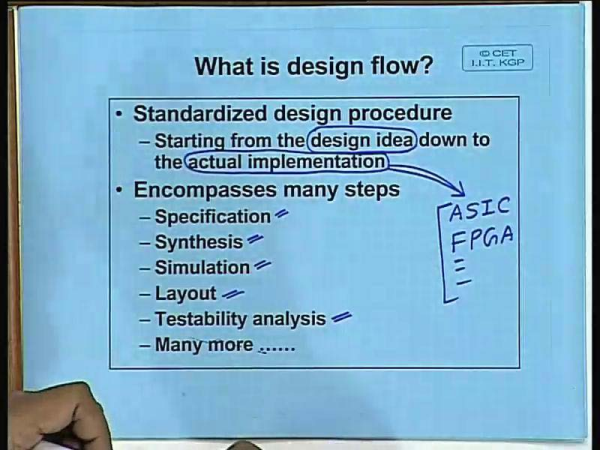


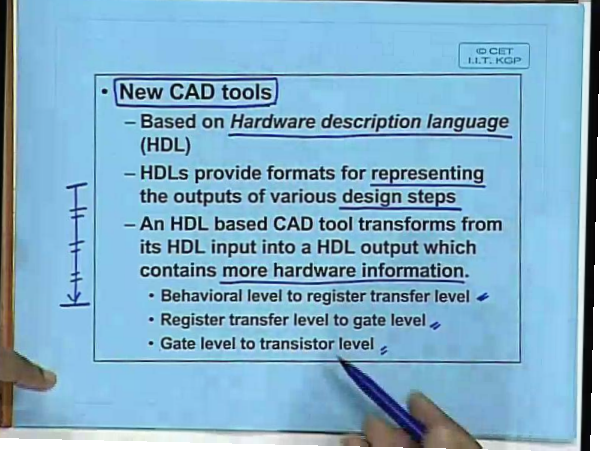


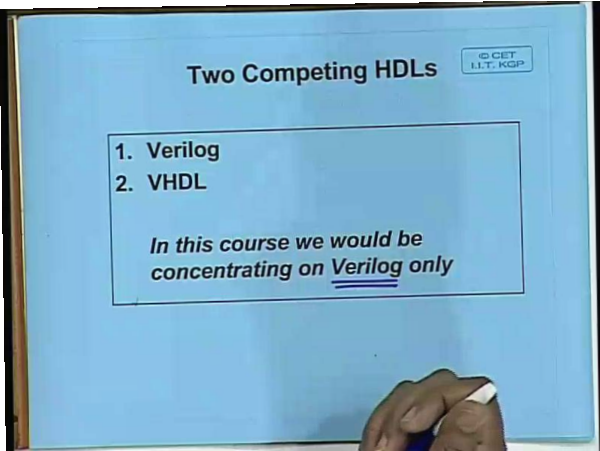


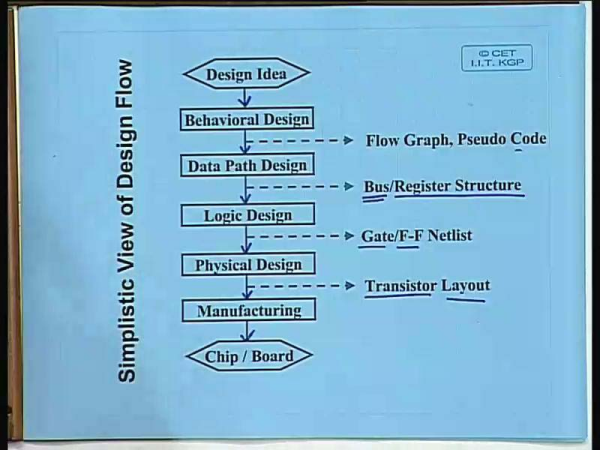


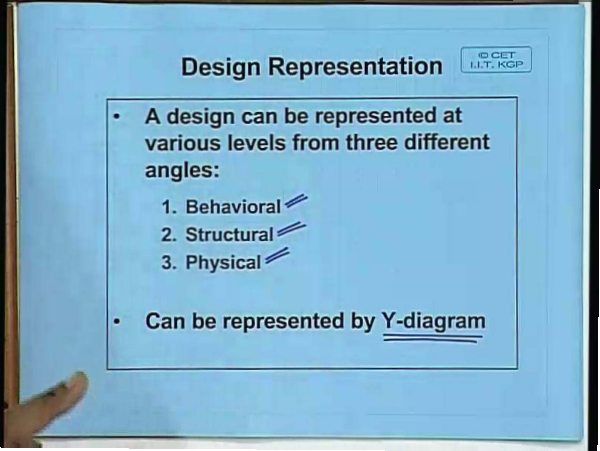


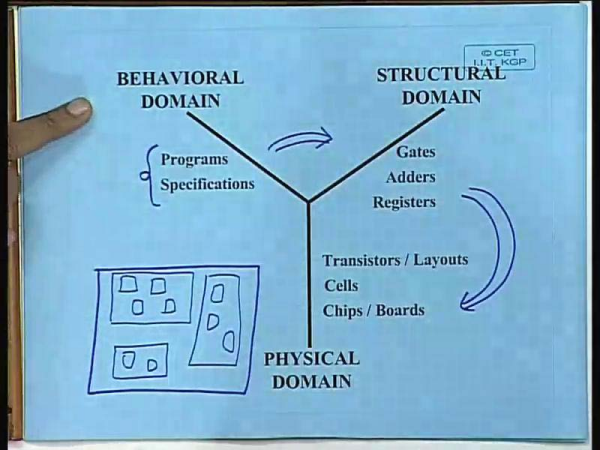


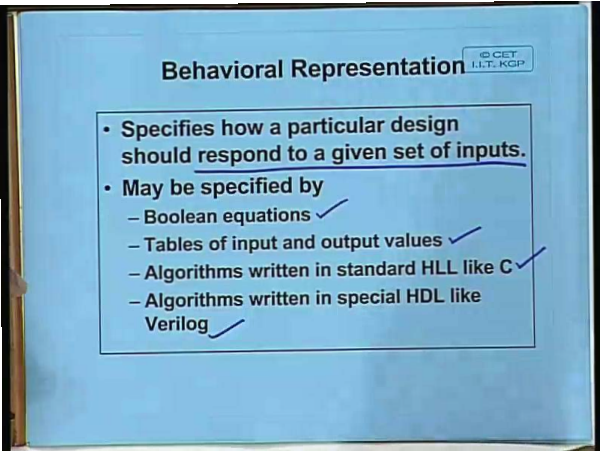


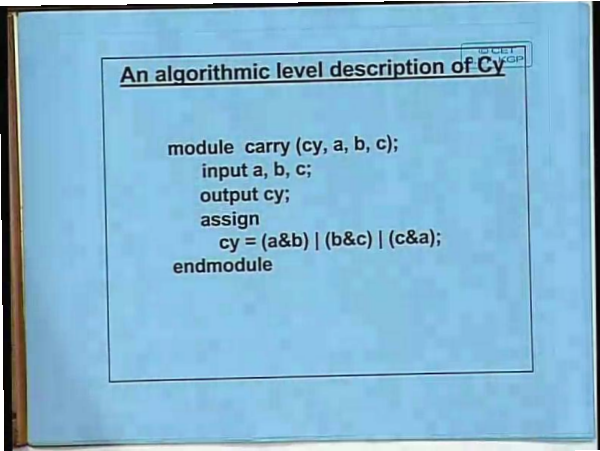


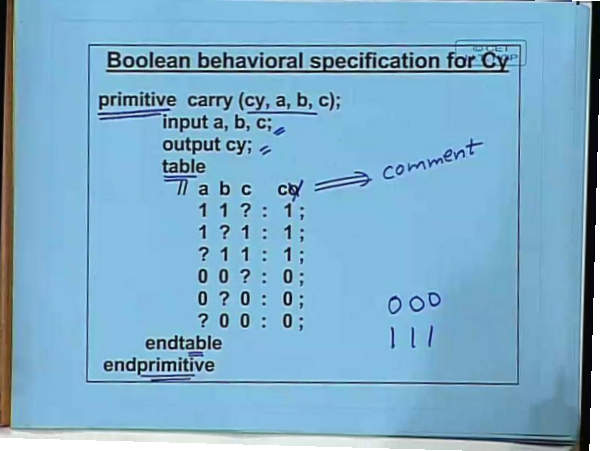


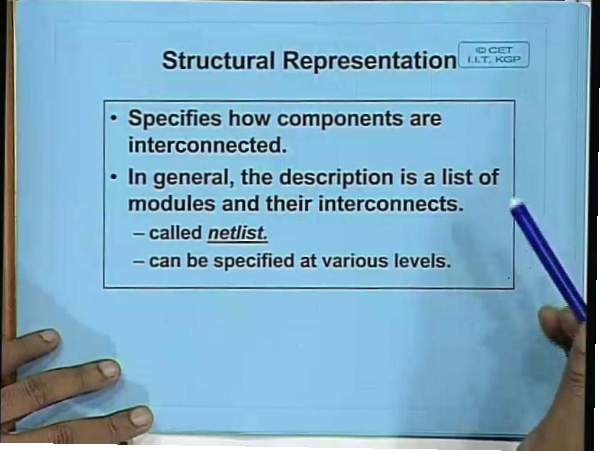




















**2x4 Decoder**

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**2x4 Decoder Structural/Gate Level Modeling**

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**2x4 Decoder in Behavioral Modeling using a case statement**

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**4x16** 

**Decoder using**

**five 2x4 Decoders**

**4x16 Decoder using five 2x4 Decoders**

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**4x1 Multiplexer using 2x1 Multiplexers**

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**4x1 Multiplexer using 2x1 Multiplexers**

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**4x1 Multiplexer**

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**Gate Level Modeling**

**Behavioral Modeling**

**Data Flow Modeling**

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