**COA**

**DCSE, UET Peshawar**

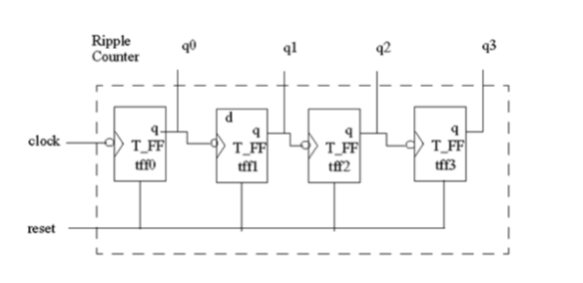
**LAB 10**

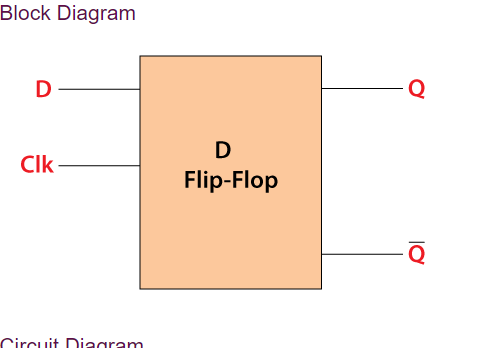
**COUNTERS IN VERILOG:**

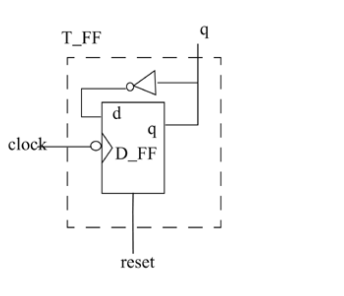
Q NO 1: Write a Verilog code to implement 4 BIT counter.

Q NO 2: Write a Verilog code to implement 8 BIT counter.

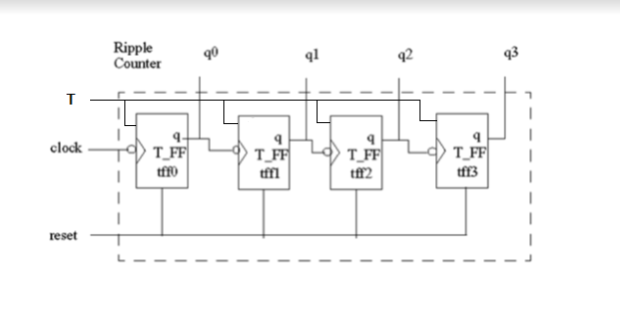
Q NO 3: Implement 4 BIT Uncontrolled Asynchronous UP COUNTER in Verilog using T FLIP FLOP:

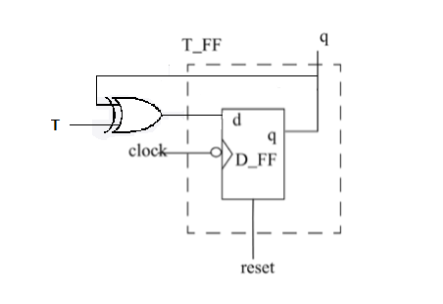






Q NO 4: Implement 4 BIT Controlled Asynchronous UP COUNTER in Verilog using T FLIP FLOP:

****

****

Q NO 5: Implement 16\*8 RAM in Verilog.