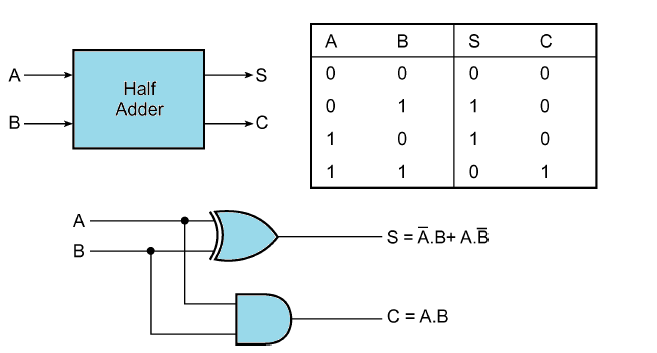
**COA**

**DCSE, UET Peshawar**

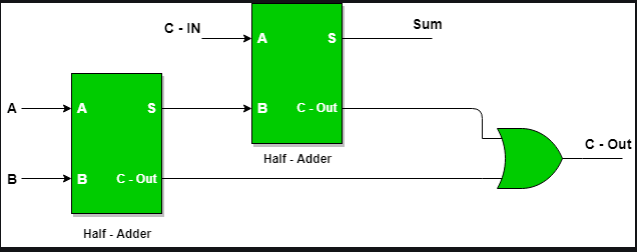
**LAB 6**

**INTRODUCTION TO VERILOG:**

Q NO 1: implement half adder in Verilog using gate level modeling.

Block and circuit diagram of half adder

Q NO 2: implement full adder using two half adder. *(use the above half adder to create full adder)*



Q NO 3: Write a Verilog code for 4 bit ripple carry adder.

